**TQFP, BGA**
**Commercial Temp**
**Industrial Temp**

# 256K x 18, 128K x 32, 128K x 36 4Mb Sync Burst SRAMs

**180 MHz–100 MHz**
**3.3 V $V_{DD}$**
**3.3 V and 2.5 V I/O**

## Features

- $\overline{FT}$ pin for user-configurable flow through or pipelined operation
- Single Cycle Deselect (SCD) operation
- 3.3 V +10%/–5% core power supply
- 2.5 V or 3.3 V I/O supply
- $\overline{LBO}$ pin for Linear or Interleaved Burst mode
- Internal input resistors on mode pins allow floating mode pins
- Default to Interleaved Pipelined mode
- Byte Write ($\overline{BW}$) and/or Global Write ($\overline{GW}$) operation
- Common data inputs and data outputs
- Clock control, registered, address, data, and control
- Internal self-timed write cycle
- Automatic power-down for portable applications
- JEDEC standard 100-lead TQFP or 119-Bump BGA package

| | | –180 | –166 | –150 | –100 |
|---|---|---|---|---|---|
| Pipeline 3-1-1-1 | tCycle | 5.5 ns | 6.0 ns | 6.6 ns | 10 ns |
| | $t_{KQ}$ | 3.0 ns | 3.5 ns | 3.8 ns | 4.5 ns |
| | $I_{DD}$ | 185 mA | 170 mA | 155 mA | 105 mA |
| Flow Through 2-1-1-1 | $t_{KQ}$ | 8 ns | 8.5 ns | 10 ns | 12 ns |
| | tCycle | 9.1 ns | 10 ns | 12 ns | 15 ns |
| | $I_{DD}$ | 115 mA | 105 mA | 100 mA | 80 mA |

## Functional Description

### Applications

The GS84018/32/36A is a 4,718,592-bit (4,194,304-bit for x32 version) high performance synchronous SRAM with a 2-bit burst address counter. Although of a type originally developed for Level 2 Cache applications supporting high performance CPUs, the device now finds application in synchronous SRAM applications ranging from DSP main store to networking chip set support. The GS84018/32/36A is available in a JEDEC standard 100-lead TQFP or 119-Bump BGA package.

### Controls

Addresses, data I/Os, chip enables ($\overline{E}_1$, $E_2$, $\overline{E}_3$), address burst control inputs ($\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$), and write control inputs ($\overline{Bx}$, $\overline{BW}$, $\overline{GW}$) are synchronous and are controlled by a positive-edge-triggered clock input (CK). Output enable ($\overline{G}$) and power down control (ZZ) are asynchronous inputs. Burst cycles can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ inputs. In Burst mode, subsequent burst addresses are generated internally and are controlled by $\overline{ADV}$. The burst address counter may be configured to count in either linear or interleave order with the Linear Burst Order ($\overline{LBO}$) input. The burst function need not be used. New addresses can be loaded on every cycle with no degradation of chip performance.

### Flow Through/Pipeline Reads

The function of the Data Output register can be controlled by the user via the $\overline{FT}$ mode pin/bump (pin 14 in the TQFP and bump 5R in the BGA). Holding the $\overline{FT}$ mode pin/bump low places the RAM in Flow Through mode, causing output data to bypass the Data Output Register. Holding $\overline{FT}$ high places the RAM in Pipelined mode, activating the rising-edge-triggered Data Output Register.

### SCD Pipelined Reads

The GS84018/32/36A is an SCD (Single Cycle Deselect) pipelined synchronous SRAM. DCD (Dual Cycle Deselect) versions are also available. SCD SRAMs pipeline deselect commands one stage less than read commands. SCD RAMs begin turning off their outputs immediately after the deselect command has been captured in the input registers.

### Byte Write and Global Write

Byte write operation is performed by using byte write enable ($\overline{BW}$) input combined with one or more individual byte write signals ($\overline{Bx}$). In addition, Global Write ($\overline{GW}$) is available for writing all bytes at one time, regardless of the Byte Write control inputs.

### Sleep Mode

Low power (Sleep mode) is attained through the assertion (High) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Sleep mode.

### Core and Interface Voltages

The GS84018/32/36A operates on a 3.3 V power supply and all inputs/outputs are 3.3 V- and 2.5 V-compatible. Separate output power ($V_{DDQ}$) pins are used to de-couple output noise from the internal circuit.

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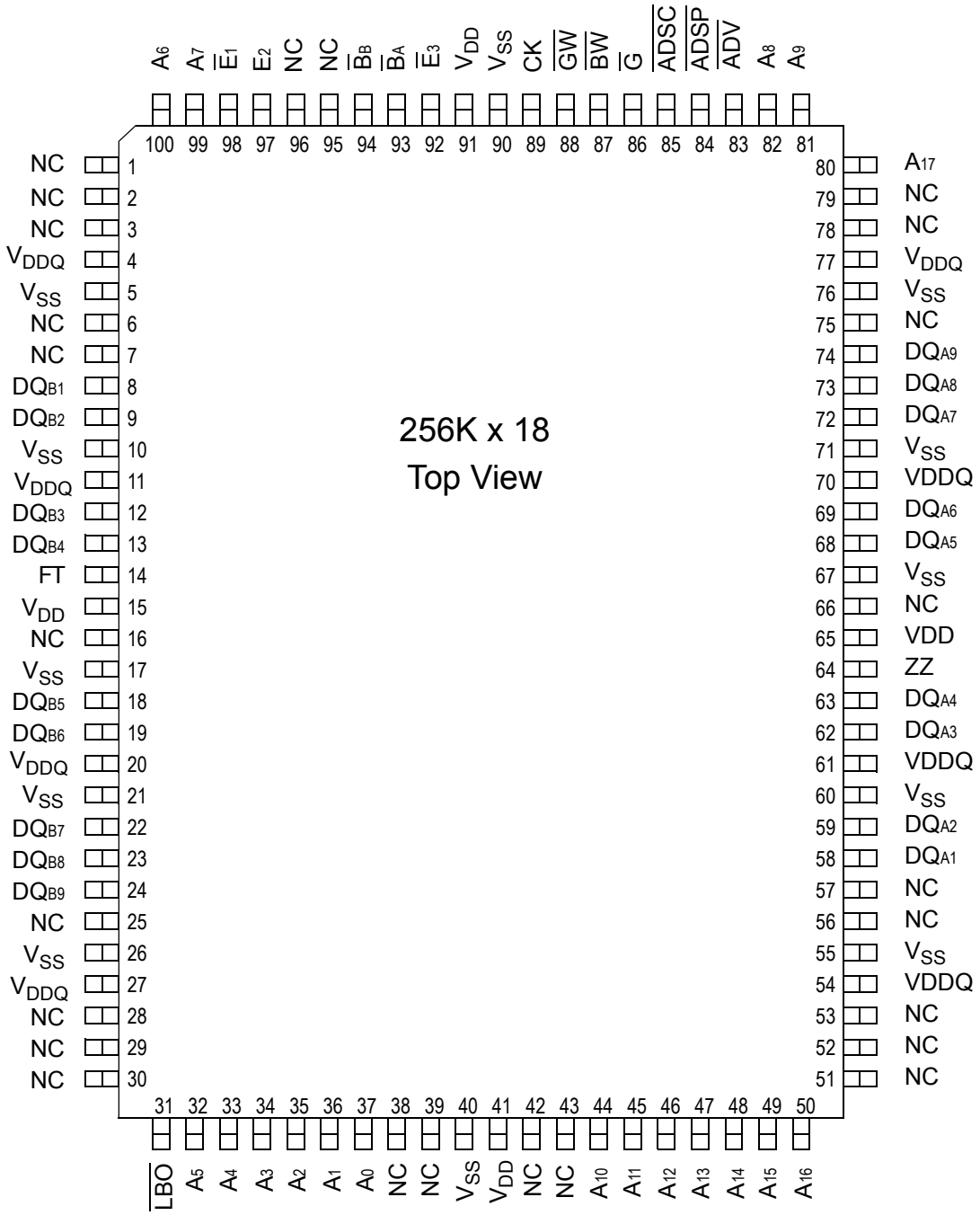
## GS84018A 100-Pin TQFP Pinout

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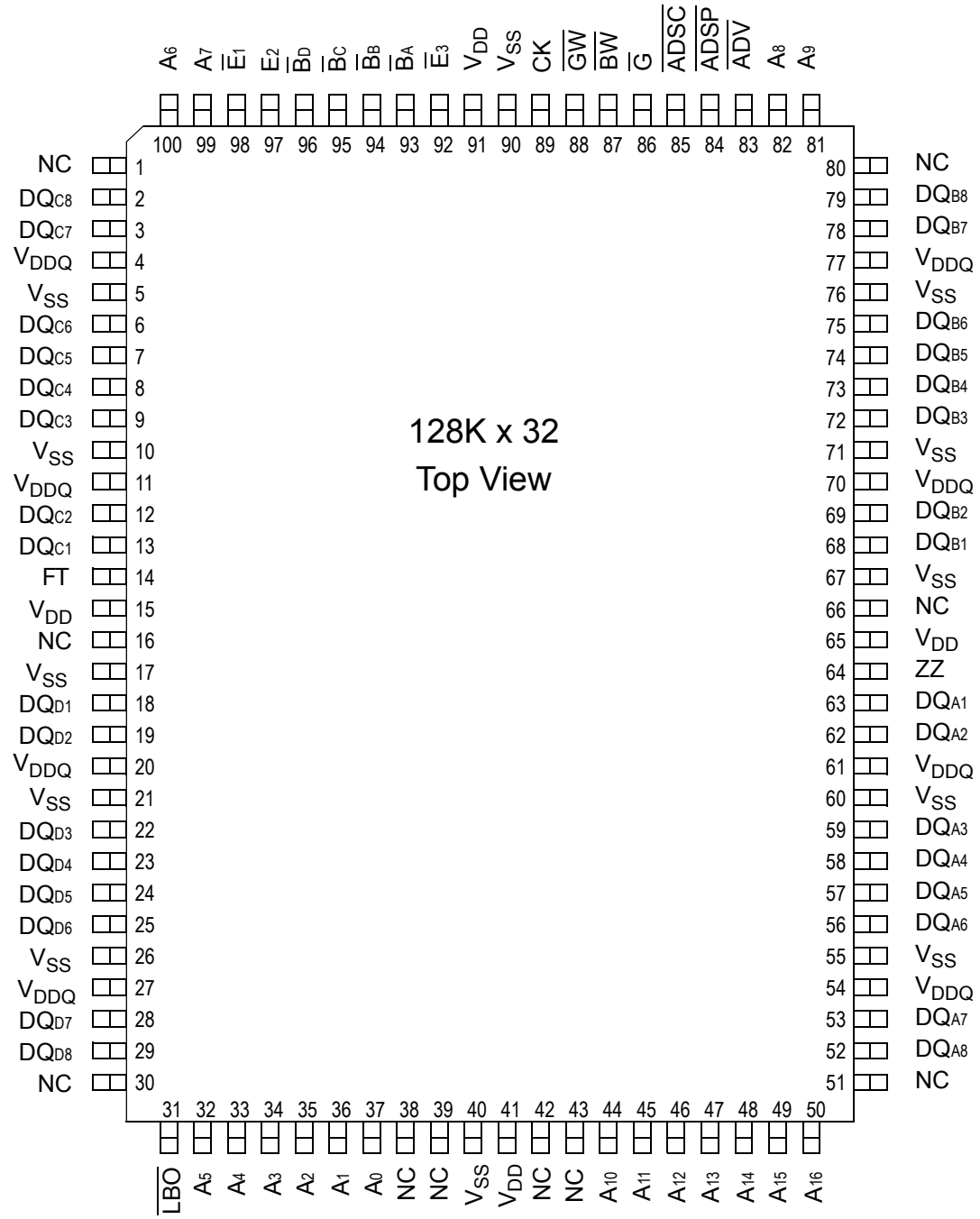
## GS84032A 100-Pin TQFP Pinout

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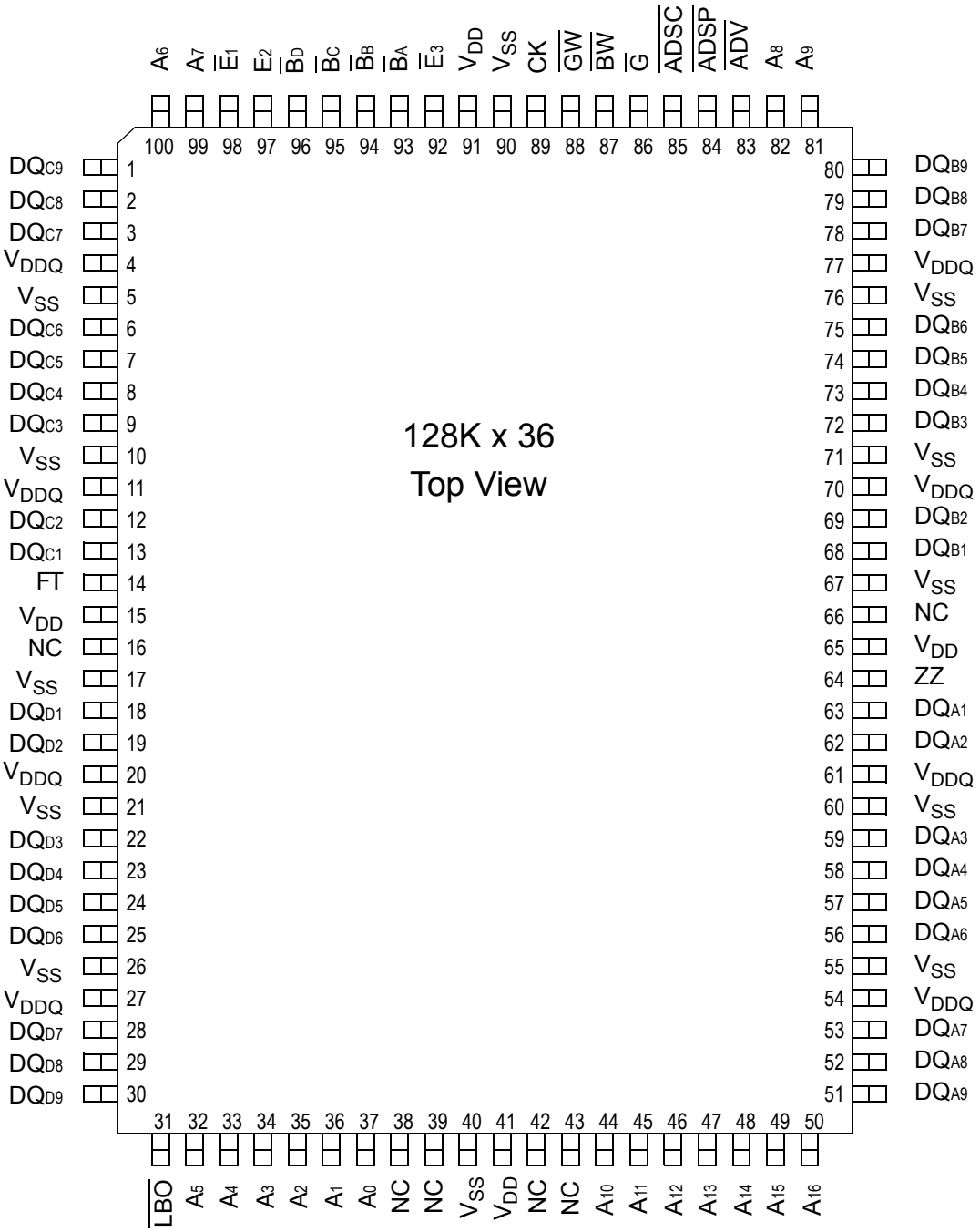
## GS84036A 100-Pin TQFP Pinout

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## TQFP Pin Description

| Pin Location | Symbol | Type | Description |
|---|---|---|---|
| 37, 36 | $A_0$, $A_1$ | I | Address field LSBs and Address Counter preset Inputs |
| 35, 34, 33, 32, 100, 99, 82, 81,44, 45, 46, 47, 48, 49, 50 | $A_2$–$A_{16}$ | I | Address Inputs |
| 80 | $A_{17}$ | I | Address Inputs (x18 versions) |
| 52, 53, 56, 57, 58, 59, 62, 63<br>68, 69, 72, 73, 74, 75, 78, 79<br>2, 3, 6, 7, 8, 9, 12, 13<br>18, 19, 22, 23, 24, 25, 28, 29 | $DQ_{A1}$–$DQ_{A8}$<br>$DQ_{B1}$–$DQ_{B8}$<br>$DQ_{C1}$–$DQ_{C8}$<br>$DQ_{D1}$–$DQ_{D8}$ | I/O | Data Input and Output pins. (x32, x36 Version) |
| 51, 80, 1, 30 | $DQ_{A9}$, $DQ_{B9}$,<br>$DQ_{C9}$, $DQ_{D9}$ | I/O | Data Input and Output pins (x36 Version) |
| 51, 80, 1, 30 | NC | | No Connect (x32 Version) |
| 58, 59, 62, 63, 68, 69, 72, 73, 74<br>8, 9, 12, 13, 18, 19, 22, 23, 24 | $DQ_{A1}$–$DQ_{A9}$<br>$DQ_{B1}$–$DQ_{B9}$ | I/O | Data Input and Output pins (x18 Version) |
| 51, 52, 53, 56, 57<br>75, 78, 79<br>1, 2, 3, 6, 7<br>25, 28, 29, 30 | NC | - | No Connect (x18 Version) |
| 87 | $\overline{BW}$ | I | Byte Write—Writes all enabled bytes; active low |
| 93, 94 | $\overline{B}_A$, $\overline{B}_B$ | I | Byte Write Enable for $DQ_A$, $DQ_B$ Data I/'s; active low |
| 95, 96 | $\overline{B}_C$, $\overline{B}_D$ | I | Byte Write Enable for $DQ_C$, $DQ_D$ Data I/Os; active low (x32, x36 Version) |
| 95, 96 | NC | - | No Connect (x18 Version) |
| 89 | CK | I | Clock Input Signal; active high |
| 88 | $\overline{GW}$ | I | Global Write Enable—Writes all bytes; active low |
| 98, 92 | $\overline{E}_1$, $\overline{E}_3$ | I | Chip Enable; active low |
| 97 | $E_2$ | I | Chip Enable; active high |
| 86 | $\overline{G}$ | I | Output Enable; active low |
| 83 | $\overline{ADV}$ | I | Burst address counter advance enable; active low |
| 84, 85 | $\overline{ADSP}$, $\overline{ADSC}$ | I | Address Strobe (Processor, Cache Controller); active low |
| 64 | ZZ | I | Sleep Mode control; active high |
| 14 | $\overline{FT}$ | I | Flow Through or Pipeline mode; active low |
| 31 | $\overline{LBO}$ | I | Linear Burst Order mode; active low |
| 15, 41, 65, 91 | $V_{DD}$ | I | Core power supply |
| 5,10,17, 21, 26, 40, 55, 60, 67, 71, 76, 90 | $V_{SS}$ | I | I/O and Core Ground |
| 4, 11, 20, 27, 54, 61, 70, 77 | $V_{DDQ}$ | I | Output driver power supply |
| 16, 38, 39, 42, 43, 66 | NC | - | No Connect |

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## GS84018A Pad Out

### 119-Bump BGA—Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| **A** | $V_{DDQ}$ | $A_6$ | $A_7$ | $\overline{ADSP}$ | $A_8$ | $A_9$ | $V_{DDQ}$ |
| **B** | NC | $E_2$ | $A_4$ | $\overline{ADSC}$ | $A_{15}$ | $\overline{E}_3$ | NC |
| **C** | NC | $A_5$ | $A_3$ | $V_{DD}$ | $A_{14}$ | $A_{16}$ | NC |
| **D** | $DQ_{B1}$ | NC | $V_{SS}$ | NC | $V_{SS}$ | $DQ_{A9}$ | NC |
| **E** | NC | $DQ_{B2}$ | $V_{SS}$ | $\overline{E}_1$ | $V_{SS}$ | NC | $DQ_{A8}$ |
| **F** | $V_{DDQ}$ | NC | $V_{SS}$ | $\overline{G}$ | $V_{SS}$ | $DQ_{A7}$ | $V_{DDQ}$ |
| **G** | NC | $DQ_{B3}$ | $\overline{B}_B$ | $\overline{ADV}$ | NC | NC | $DQ_{A6}$ |
| **H** | $DQ_{B4}$ | NC | $V_{SS}$ | $\overline{GW}$ | $V_{SS}$ | $DQ_{A5}$ | NC |
| **J** | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ |
| **K** | NC | $DQ_{B5}$ | $V_{SS}$ | CK | $V_{SS}$ | NC | $DQ_{A4}$ |
| **L** | $DQ_{B6}$ | NC | NC | NC | $\overline{B}_A$ | $DQ_{A3}$ | NC |
| **M** | $V_{DDQ}$ | $DQ_{B7}$ | $V_{SS}$ | $\overline{BW}$ | $V_{SS}$ | NC | $V_{DDQ}$ |
| **N** | $DQ_{B8}$ | NC | $V_{SS}$ | $A_1$ | $V_{SS}$ | $DQ_{A2}$ | NC |
| **P** | NC | $DQ_{B9}$ | $V_{SS}$ | $A_0$ | $V_{SS}$ | NC | $DQ_{A1}$ |
| **R** | NC | $A_2$ | $\overline{LBO}$ | $V_{DD}$ | $\overline{FT}$ | $A_{13}$ | NC |
| **T** | NC | $A_{10}$ | $A_{11}$ | NC | $A_{12}$ | $A_{17}$ | ZZ |
| **U** | $V_{DDQ}$ | NC | NC | NC | NC | NC | $V_{DDQ}$ |

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## GS84032A Pad Out

### 119-Bump BGA—Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| **A** | $V_{DDQ}$ | $A_6$ | $A_7$ | $\overline{ADSP}$ | $A_8$ | $A_9$ | $V_{DDQ}$ |
| **B** | NC | $E_2$ | $A_4$ | $\overline{ADSC}$ | $A_{15}$ | $\overline{E}_3$ | NC |
| **C** | NC | $A_5$ | $A_3$ | $V_{DD}$ | $A_{14}$ | $A_{16}$ | NC |
| **D** | $DQ_{C4}$ | NC | $V_{SS}$ | NC | $V_{SS}$ | NC | $DQ_{B4}$ |
| **E** | $DQ_{C3}$ | $DQ_{C8}$ | $V_{SS}$ | $\overline{E}_1$ | $V_{SS}$ | $DQ_{B8}$ | $DQ_{B3}$ |
| **F** | $V_{DDQ}$ | $DQ_{C7}$ | $V_{SS}$ | $\overline{G}$ | $V_{SS}$ | $DQ_{B7}$ | $V_{DDQ}$ |
| **G** | $DQ_{C2}$ | $DQ_{C6}$ | $\overline{B}_C$ | $\overline{ADV}$ | $\overline{B}_B$ | $DQ_{B6}$ | $DQ_{B2}$ |
| **H** | $DQ_{C1}$ | $DQ_{C5}$ | $V_{SS}$ | $\overline{GW}$ | $V_{SS}$ | $DQ_{B5}$ | $DQ_{B1}$ |
| **J** | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ |
| **K** | $DQ_{D1}$ | $DQ_{D5}$ | $V_{SS}$ | CK | $V_{SS}$ | $DQ_{A5}$ | $DQ_{A1}$ |
| **L** | $DQ_{D2}$ | $DQ_{D6}$ | $\overline{B}_D$ | NC | $\overline{B}_A$ | $DQ_{A6}$ | $DQ_{A2}$ |
| **M** | $V_{DDQ}$ | $DQ_{D78}$ | $V_{SS}$ | $\overline{BW}$ | $V_{SS}$ | $DQ_{A7}$ | $V_{DDQ}$ |
| **N** | $DQ_{D3}$ | $DQ_{D8}$ | $V_{SS}$ | $A_1$ | $V_{SS}$ | $DQ_{A8}$ | $DQ_{A3}$ |
| **P** | $DQ_{D4}$ | NC | $V_{SS}$ | $A_0$ | $V_{SS}$ | NC | $DQ_{A4}$ |
| **R** | NC | $A_2$ | $\overline{LBO}$ | $V_{DD}$ | $\overline{FT}$ | $A_{13}$ | NC |
| **T** | NC | NC | $A_{10}$ | $A_{11}$ | $A_{12}$ | NC | ZZ |
| **U** | $V_{DDQ}$ | NC | NC | NC | NC | NC | $V_{DDQ}$ |

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## GS84036A Pad Out

### 119-Bump BGA—Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| **A** | $V_{DDQ}$ | $A_6$ | $A_7$ | $\overline{ADSP}$ | $A_8$ | $A_9$ | $V_{DDQ}$ |
| **B** | NC | $E_2$ | $A_4$ | $\overline{ADSC}$ | $A_{15}$ | $\overline{E}_3$ | NC |
| **C** | NC | $A_5$ | $A_3$ | $V_{DD}$ | $A_{14}$ | $A_{16}$ | NC |
| **D** | $DQ_{C4}$ | $DQ_{C9}$ | $V_{SS}$ | NC | $V_{SS}$ | $DQ_{B9}$ | $DQ_{B4}$ |
| **E** | $DQ_{C3}$ | $DQ_{C8}$ | $V_{SS}$ | $\overline{E}_1$ | $V_{SS}$ | $DQ_{B8}$ | $DQ_{B3}$ |
| **F** | $V_{DDQ}$ | $DQ_{C7}$ | $V_{SS}$ | $\overline{G}$ | $V_{SS}$ | $DQ_{B7}$ | $V_{DDQ}$ |
| **G** | $DQ_{C2}$ | $DQ_{C6}$ | $\overline{B}_C$ | $\overline{ADV}$ | $\overline{B}_B$ | $DQ_{B6}$ | $DQ_{B2}$ |
| **H** | $DQ_{C1}$ | $DQ_{C5}$ | $V_{SS}$ | $\overline{GW}$ | $V_{SS}$ | $DQ_{B5}$ | $DQ_{B1}$ |
| **J** | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ |
| **K** | $DQ_{D1}$ | $DQ_{D5}$ | $V_{SS}$ | CK | $V_{SS}$ | $DQ_{A5}$ | $DQ_{A1}$ |
| **L** | $DQ_{D2}$ | $DQ_{D6}$ | $\overline{B}_D$ | NC | $\overline{B}_A$ | $DQ_{A6}$ | $DQ_{A2}$ |
| **M** | $V_{DDQ}$ | $DQ_{D78}$ | $V_{SS}$ | $\overline{BW}$ | $V_{SS}$ | $DQ_{A7}$ | $V_{DDQ}$ |
| **N** | $DQ_{D3}$ | $DQ_{D8}$ | $V_{SS}$ | $A_1$ | $V_{SS}$ | $DQ_{A8}$ | $DQ_{A3}$ |
| **P** | $DQ_{D4}$ | $DQ_{D9}$ | $V_{SS}$ | $A_0$ | $V_{SS}$ | $DQ_{A9}$ | $DQ_{A4}$ |
| **R** | NC | $A_2$ | $\overline{LBO}$ | $V_{DD}$ | $\overline{FT}$ | $A_{13}$ | NC |
| **T** | NC | NC | $A_{10}$ | $A_{11}$ | $A_{12}$ | NC | ZZ |
| **U** | $V_{DDQ}$ | NC | NC | NC | NC | NC | $V_{DDQ}$ |

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## BGA Pin Description

| Pin Location | Symbol | Type | Description |
|---|---|---|---|
| N4, P4 | $A_0$, $A_1$ | I | Address field LSBs and Address Counter Preset Inputs |
| A2, A3, A5, A6, B3, B5, C2, C3, C5, C6, R2, R6, T3, T5 | An | I | Address Inputs |
| T4 | An | | Address Input (x32/36 Versions) |
| T2, T6 | NC | - | No Connect (x32/36 Versions) |
| T2, T6 | An | I | Address Input (x18 Version) |
| K7, K6, L7, L6, M6, N7, N6, P7<br>H7, H6, G7, G6, F6, E7, E6, D7<br>H1, H2, G1, G2, F2, E1, E2, D1<br>K1, K2, L1, L2, M2, N1, N2, P1 | $DQ_{A1}$-$DQ_{A8}$<br>$DQ_{B1}$-$DQ_{B8}$<br>$DQ_{C1}$-$DQ_{C8}$<br>$DQ_{D1}$-$DQ_{D8}$ | I/O | Data Input and Output pins (x32/36 Versions) |
| P6, D6, D2, P2 | $DQ_{A9}$, $DQ_{B9}$, $DQ_{C9}$, $DQ_{D9}$ | I/O | Data Input and Output pins (x36 Version) |
| P6, D6, D2, P2 | NC | - | No Connect (x32 Version) |
| L5, G5, G3, L3 | $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$ | I | Byte Write Enable for $DQ_A$, $DQ_B$, $DQ_C$, $DQ_D$ I/O's; active low ( x36 Version) |
| P7, N6, L6, K7, H6, G7, F6, E7, D6<br>D1, E2, G2, H1, K2, L1, M2, N1, P2 | $DQ_{A1}$-$DQ_{A9}$<br>$DQ_{B1}$-$DQ_{B9}$ | I/O | Data Input and Output pins (x18 Version) |
| L5, G3 | $\overline{B}_A$, $\overline{B}_B$ | I | Byte Write Enable for $DQ_A$, $DQ_B$ I/O's; active low ( x18 Version) |
| B1, C1, R1, T1, U2, J3, U3, D4, L4, U4, J5, U5, U6, B7, C7, R7 | NC | - | No Connect |
| P6, N7, M6, L7, K6, H7, G6, E6, D7, D2, B1, E1, F2, G1, H2, K1, L2, N2, P1, G5, L3, T4 | NC | - | No Connect (x18 Version) |
| K4 | CK | I | Clock Input Signal; active high |
| M4 | $\overline{BW}$ | I | Byte Write—Writes all enabled bytes; active low |
| H4 | $\overline{GW}$ | I | Global Write Enable—Writes all bytes; active low |
| E4, B6 | $\overline{E}_1$, $\overline{E}_3$ | I | Chip Enable; active low |
| B2 | $E_2$ | I | Chip Enable; active high |
| F4 | $\overline{G}$ | I | Output Enable; active low |
| G4 | $\overline{ADV}$ | I | Burst address counter advance enable; active low |
| A4, B4 | $\overline{ADSP}$, $\overline{ADSC}$ | I | Address Strobe (Processor, Cache Controller); active low |
| T7 | ZZ | I | Sleep Mode control; active high |
| R5 | $\overline{FT}$ | I | Flow Through or Pipeline mode; active low |
| R3 | $\overline{LBO}$ | I | Linear Burst Order mode; active low |
| J2, C4, J4, R4, J6 | $V_{DD}$ | I | Core power supply |
| D3, E3, F3, H3, K3, M3, N3, P3, D5, E5, F5, H5, K5, M5, N5, P5 | $V_{SS}$ | I | I/O and Core Ground |
| A1, F1, J1, M1, U1, A7, F7, J7, M7, U7 | $V_{DDQ}$ | I | Output driver power supply |

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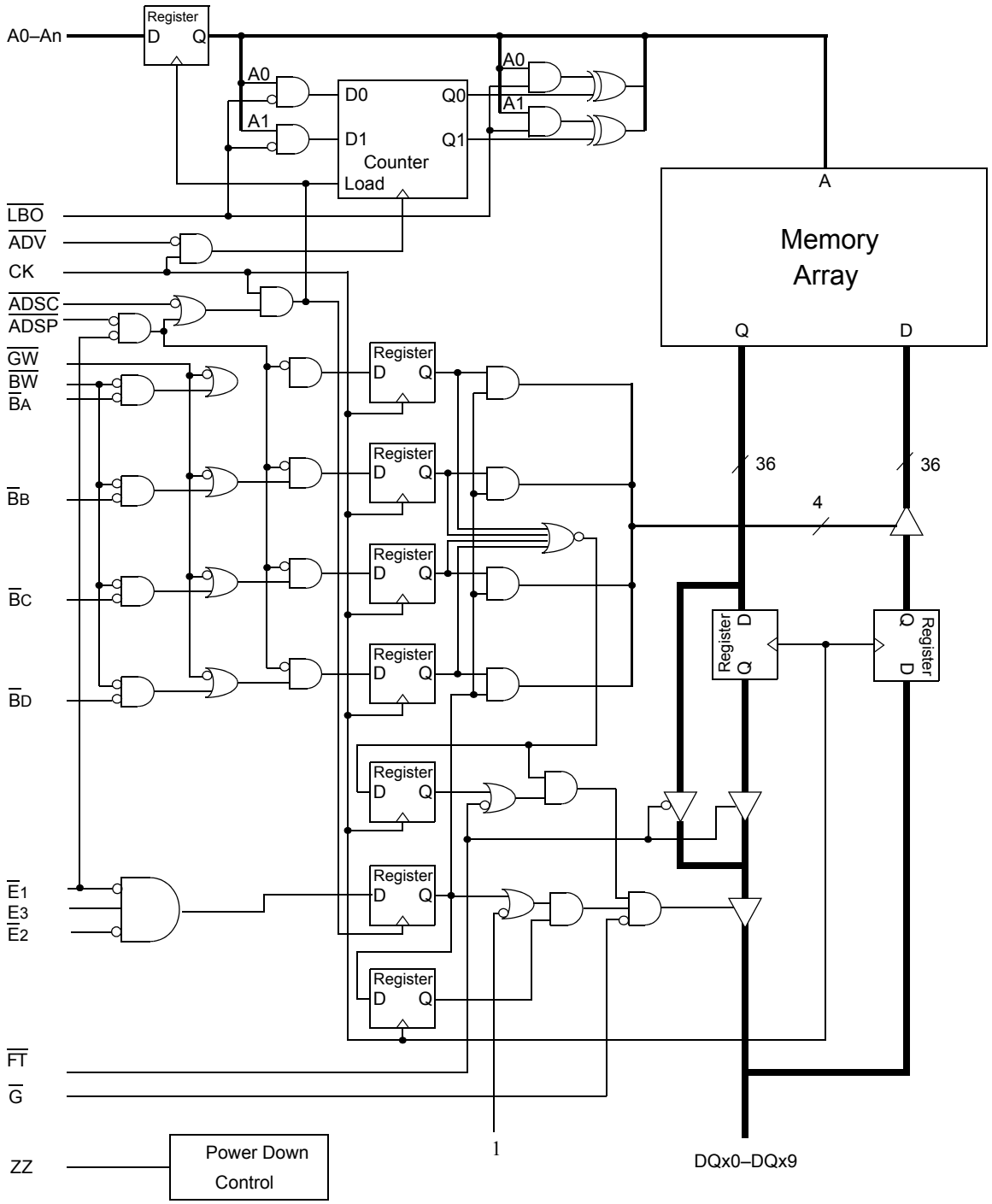
## GS84018/32/36A Block Diagram




Note: Only x36 version shown for simplicity.

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## Mode Pin Functions

| Mode Name | Pin Name | State | Function |
|---|---|---|---|
| Burst Order Control | $\overline{LBO}$ | L | Linear Burst |
| | | H or NC | Interleaved Burst |
| Output Register Control | $\overline{FT}$ | L | Flow Through |
| | | H or NC | Pipeline |
| Power Down Control | ZZ | L or NC | Active |
| | | H | Standby, $I_{DD} = I_{SB}$ |

Note:
There are pull-up devices on $\overline{LBO}$ and $\overline{FT}$ pins and a pull down device on the ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above tables.

## Burst Counter Sequences

### Linear Burst Sequence

| | A[1:0] | A[1:0] | A[1:0] | A[1:0] |
|---|---|---|---|---|
| 1st address | 00 | 01 | 10 | 11 |
| 2nd address | 01 | 10 | 11 | 00 |
| 3rd address | 10 | 11 | 00 | 01 |
| 4th address | 11 | 00 | 01 | 10 |

Note: The burst counter wraps to initial state on the 5th clock.

### Interleaved Burst Sequence

| | A[1:0] | A[1:0] | A[1:0] | A[1:0] |
|---|---|---|---|---|
| 1st address | 00 | 01 | 10 | 11 |
| 2nd address | 01 | 00 | 11 | 10 |
| 3rd address | 10 | 11 | 00 | 01 |
| 4th address | 11 | 10 | 01 | 00 |

Note: The burst counter wraps to initial state on the 5th clock.

## Byte Write Truth Table

| Function | $\overline{GW}$ | $\overline{BW}$ | $\overline{B}_A$ | $\overline{B}_B$ | $\overline{B}_C$ | $\overline{B}_D$ | Notes |
|---|---|---|---|---|---|---|---|
| Read | H | H | X | X | X | X | 1 |
| Read | H | L | H | H | H | H | 1 |
| Write byte A | H | L | L | H | H | H | 2, 3 |
| Write byte B | H | L | H | L | H | H | 2, 3 |
| Write byte C | H | L | H | H | L | H | 2, 3, 4 |
| Write byte D | H | L | H | H | H | L | 2, 3, 4 |
| Write all bytes | H | L | L | L | L | L | 2, 3, 4 |
| Write all bytes | L | X | X | X | X | X | |

Notes:
1. All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs.
2. Byte Write Enable inputs $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$ and/or $\overline{B}_D$ may be used in any combination with $\overline{BW}$ to write single or multiple bytes.
3. All byte I/Os remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.
4. Bytes "C" and "D" are only available on the x32 and x36 versions.

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## Synchronous Truth Table

| Operation | Address Used | State Diagram Key[5] | $\overline{E}_1$ | $E^2$ | $\overline{ADSP}$ | $\overline{ADSC}$ | $\overline{ADV}$ | $W^3$ | $DQ^4$ |
|---|---|---|---|---|---|---|---|---|---|
| **Deselect Cycle, Power Down** | **None** | **X** | **H** | **X** | **X** | **L** | **X** | **X** | **High-Z** |
| Deselect Cycle, Power Down | None | X | L | F | L | X | X | X | High-Z |
| **Deselect Cycle, Power Down** | **None** | **X** | **L** | **F** | **H** | **L** | **X** | **X** | **High-Z** |
| Read Cycle, Begin Burst | External | R | L | T | L | X | X | X | Q |
| **Read Cycle, Begin Burst** | **External** | **R** | **L** | **T** | **H** | **L** | **X** | **F** | **Q** |
| **Write Cycle, Begin Burst** | **External** | **W** | **L** | **T** | **H** | **L** | **X** | **T** | **D** |
| *Read Cycle, Continue Burst* | *Next* | *CR* | *X* | *X* | *H* | *H* | *L* | *F* | *Q* |
| Read Cycle, Continue Burst | Next | CR | H | X | X | H | L | F | Q |
| *Write Cycle, Continue Burst* | *Next* | *CW* | *X* | *X* | *H* | *H* | *L* | *T* | *D* |
| Write Cycle, Continue Burst | Next | CW | H | X | X | H | L | T | D |
| Read Cycle, Suspend Burst | Current | | X | X | H | H | H | F | Q |
| Read Cycle, Suspend Burst | Current | | H | X | X | H | H | F | Q |
| Write Cycle, Suspend Burst | Current | | X | X | H | H | H | T | D |
| Write Cycle, Suspend Burst | Current | | H | X | X | H | H | T | D |

Notes:
1. X = Don't Care, H = High, L = Low.
2. E = T (True) if $E_2$ = 1 and $\overline{E}_3$ = 0; E = F (False) if $E_2$ = 0 or $\overline{E}_3$ = 1.
3. W = T (True) and F (False) is defined in the Byte Write Truth Table preceding.
4. $\overline{G}$ is an asynchronous input. $\overline{G}$ can be driven high at any time to disable active output drivers. $\overline{G}$ low can only enable active drivers (shown as "Q" in the Truth Table above).
5. All input combinations shown above are tested and supported. Input combinations shown in gray boxes need not be used to accomplish basic synchronous or synchronous burst operations and may be avoided for simplicity.
6. Tying $\overline{ADSP}$ high and $\overline{ADSC}$ low allows simple non-burst synchronous operations. See **BOLD** items above.
7. Tying $\overline{ADSP}$ high and $\overline{ADV}$ low while using $\overline{ADSC}$ to load new addresses allows simple burst operations. See *ITALIC* items above.

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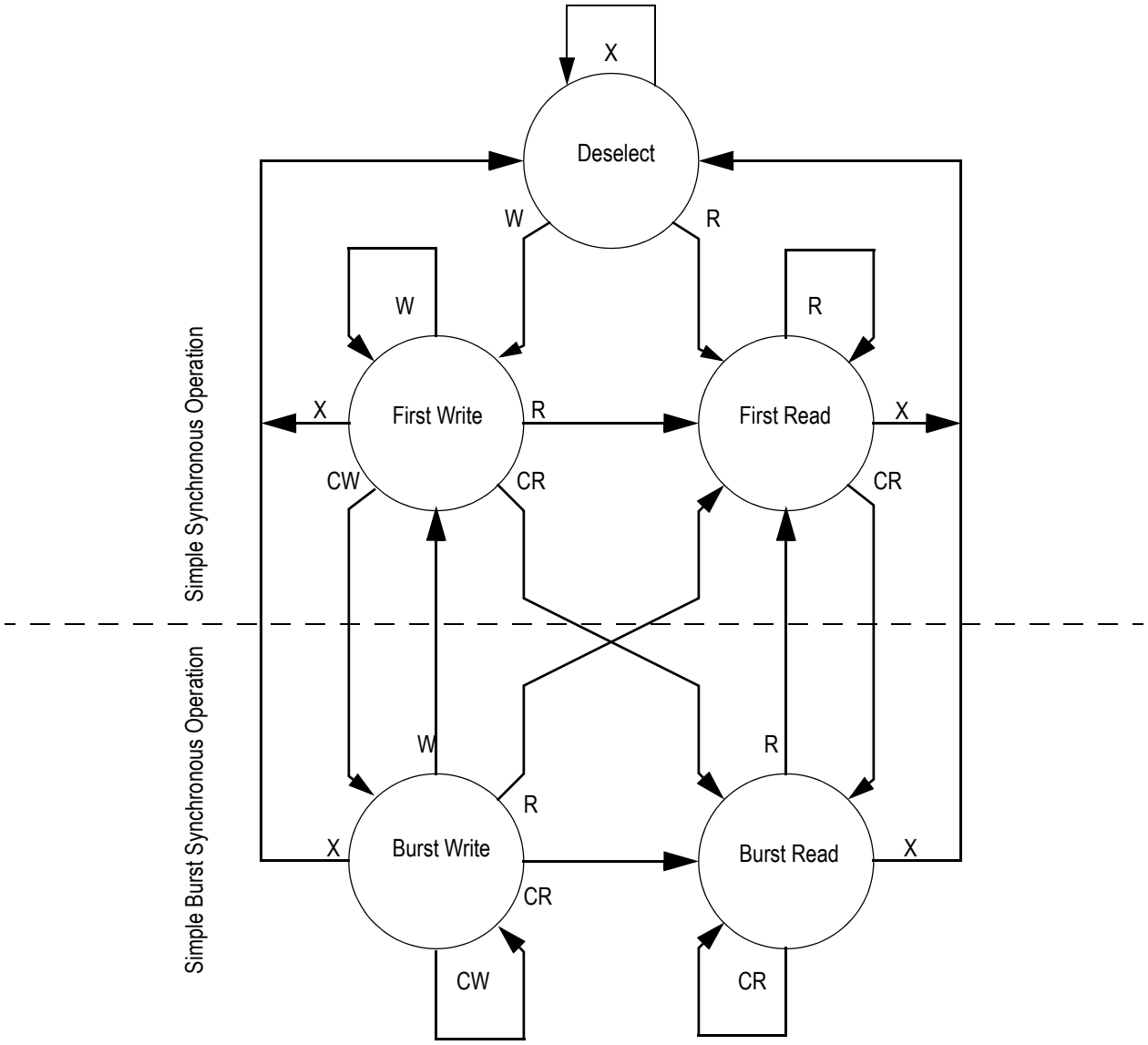
## Simplified State Diagram




Notes:

1. The diagram shows only supported (tested) synchronous state transitions. The diagram presumes $\overline{G}$ is tied Low.
2. The upper portion of the diagram assumes active use of only the Enable ($\overline{E}_1$, $E_2$, $\overline{E}_3$) and Write ($\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$, $\overline{BW}$ and $\overline{GW}$) control inputs and that $\overline{ADSP}$ is tied high and $\overline{ADSC}$ is tied low.
3. The upper and lower portions of the diagram together assume active use of only the Enable, Write and $\overline{ADSC}$ control inputs and assumes $\overline{ADSP}$ is tied high and $\overline{ADV}$ is tied low.

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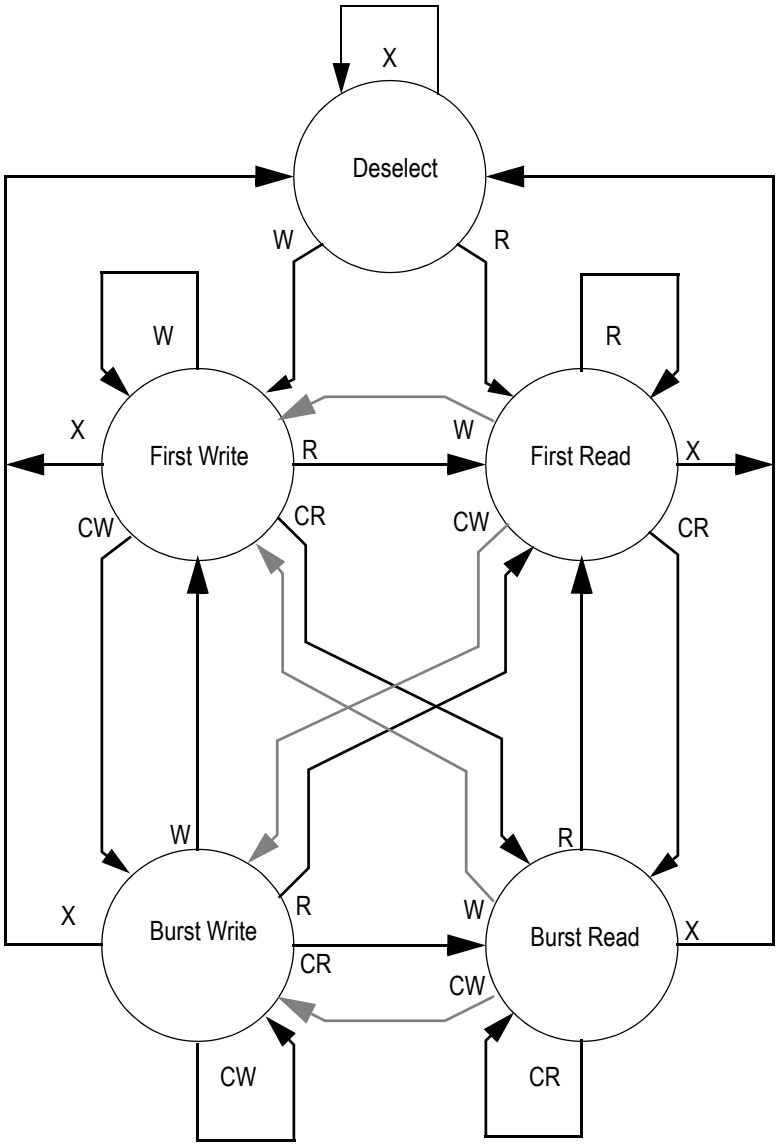
## Simplified State Diagram with $\overline{G}$




Notes:
1. The diagram shows supported (tested) synchronous state transitions plus supported transitions that depend upon the use of $\overline{G}$.
2. Use of "Dummy Reads" (Read Cycles with $\overline{G}$ High) may be used to make the transition from Read cycles to Write cycles without passing through a Deselect cycle. Dummy Read cycles increment the address counter just like normal Read cycles.
3. Transitions shown in grey tone assume $\overline{G}$ has been pulsed high long enough to turn the RAM's drivers off and for incoming data to meet Data Input Set Up Time.

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## Absolute Maximum Ratings

(All voltages reference to $V_{SS}$)

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Voltage on $V_{DD}$ Pins | –0.5 to 4.6 | V |
| $V_{DDQ}$ | Voltage in $V_{DDQ}$ Pins | –0.5 to $V_{DD}$ | V |
| $V_{CK}$ | Voltage on Clock Input Pin | –0.5 to 6 | V |
| $V_{I/O}$ | Voltage on I/O Pins | –0.5 to $V_{DDQ}$ +0.5 (≤ 4.6 V max.) | V |
| $V_{IN}$ | Voltage on Other Input Pins | –0.5 to $V_{DD}$ +0.5 (≤ 4.6 V max.) | V |
| $I_{IN}$ | Input Current on Any Pin | +/–20 | mA |
| $I_{OUT}$ | Output Current on Any I/O Pin | +/–20 | mA |
| $P_D$ | Package Power Dissipation | 1.5 | W |
| $T_{STG}$ | Storage Temperature | –55 to 125 | °C |
| $T_{BIAS}$ | Temperature Under Bias | –55 to 125 | °C |

Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

## Recommended Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 3.135 | 3.3 | 3.6 | V | |
| I/O Supply Voltage | $V_{DDQ}$ | 2.375 | 2.5 | $V_{DD}$ | V | 1 |
| Input High Voltage | $V_{IH}$ | 1.7 | — | $V_{DD}$ +0.3 | V | 2 |
| Input Low Voltage | $V_{IL}$ | –0.3 | — | 0.8 | V | 2 |
| Ambient Temperature (Commercial Range Versions) | $T_A$ | 0 | 25 | 70 | °C | 3 |
| Ambient Temperature (Industrial Range Versions) | $T_A$ | –40 | 25 | 85 | °C | 3 |

Note:
1. Unless otherwise noted, all performance specifications quoted are evaluated for worst case at both 2.75 V ≤ $V_{DDQ}$ ≤ 2.375 V (i.e., 2.5 V I/O) and 3.6 V ≤ $V_{DDQ}$ ≤ 3.135 V (i.e., 3.3 V I/O) and quoted at whichever condition is worst case.
2. This device features input buffers compatible with both 3.3 V and 2.5 V I/O drivers.
3. Most speed grades and configurations of this device are offered in both Commercial and Industrial Temperature ranges. The part number of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
4. Input Under/overshoot voltage must be –2 V > Vi < $V_{DD}$+2 V with a pulse width not to exceed 20% tKC.

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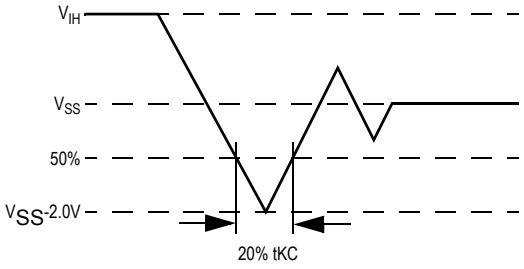
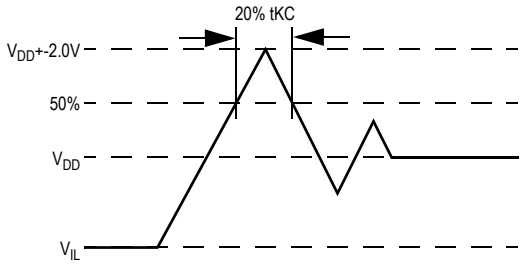
**Undershoot Measurement and Timing**




**Overshoot Measurement and Timing**




## Capacitance

($T_A$ = 25°C, f = 1 MHz, $V_{DD}$ = 3.3 V)

| Parameter | Symbol | Test conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Control Input Capacitance | $C_I$ | $V_{DD}$ = 3.3 V | 3 | 4 | pF |
| Input Capacitance | $C_{IN}$ | $V_{IN}$ = 0 V | 4 | 5 | pF |
| Output Capacitance | $C_{OUT}$ | $V_{OUT}$ = 0 V | 6 | 7 | pF |

Note: This parameter is sample tested.

## Package Thermal Characteristics

| Rating | Layer Board | Symbol | TQFP Max | BGA Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Junction to Ambient (at 200 lfm) | single | $R_{\Theta JA}$ | 40 | 38 | °C/W | 1,2,4 |
| Junction to Ambient (at 200 lfm) | four | $R_{\Theta JA}$ | 24 | 21 | °C/W | 1,2,4 |
| Junction to Case (TOP) | | $R_{\Theta JC}$ | 9 | 5 | °C/W | 3,4 |

Notes:
1. Junction temperature is a function of SRAM power dissipation, package thermal resistance, mounting board temperature, ambient. Temperature air flow, board density, and PCB thermal resistance.
2. SCMI G-38-87.
3. Average thermal resistance between die and top surface, MIL SPEC-883, Method 1012.1.
4. For x18 configuration, consult factory.

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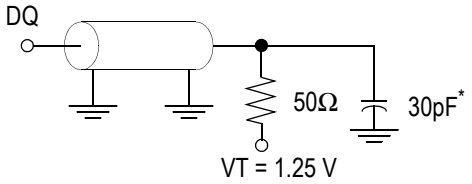
## AC Test Conditions

| Parameter | Conditions |
|---|---|
| Input high level | 2.3 V |
| Input low level | 0.2 V |
| Input slew rate | 1 V/ns |
| Input reference level | 1.25 V |
| Output reference level | 1.25 V |
| Output load | **Fig. 1& 2** |

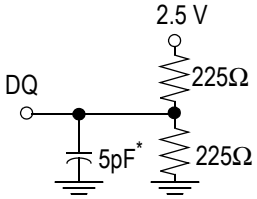
Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Output Load 2 for $t_{LZ}$, $t_{HZ}$, $t_{OLZ}$ and $t_{OHZ}$.
4. Device is deselected as defined by the Truth Table.

Output Load 1




* Distributed Test Jig Capacitance

Output Load 2




## DC Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Max |
|---|---|---|---|---|
| Input Leakage Current (except mode pins) | $I_{IL}$ | $V_{IN}$ = 0 to $V_{DD}$ | –1 uA | 1uA |
| ZZ Input Current | $I_{INZZ}$ | $V_{DD} \geq V_{IN} \geq V_{IH}$<br>$0V \leq V_{IN} \leq V_{IH}$ | –1 uA<br>–1 uA | 1 uA<br>300 uA |
| Mode Pin Input Current | $I_{INM}$ | $V_{DD} \geq V_{IN} \geq V_{IL}$<br>$0V \leq V_{IN} \leq V_{IL}$ | –300 uA<br>–1uA | 1 uA<br>1 uA |
| Output Leakage Current | $I_{OL}$ | Output Disable, $V_{OUT}$ = 0 to $V_{DD}$ | –1 uA | 1 uA |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = –4 mA, $V_{DDQ}$ = 2.375 V | 1.7 V | |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = –4 mA, $V_{DDQ}$ = 3.135 V | 2.4 V | |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 4 mA | | 0.4 V |

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## Operating Currents

| Parameter | Test Conditions | Symbol | -180 | | -166 | | -150 | | -100 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 to 70°C | –40 to 85°C | 0 to 70°C | –40 to 85°C | 0 to 70°C | –40 to 85°C | 0 to 70°C | –40 to 85°C | |
| Operating Current | Device Selected; All other inputs ≥$V_{IH}$ or ≤ $V_{IL}$ Output open | $I_{DD}$ Pipeline | 185 | 195 | 170 | 180 | 155 | 165 | 105 | 115 | mA |
| | | $I_{DD}$ Flow Through | 115 | 125 | 105 | 115 | 100 | 110 | 80 | 90 | mA |
| Standby Current | ZZ ≥ $V_{DD}$ – 0.2 V | $I_{SB}$ Pipeline | 20 | 30 | 20 | 30 | 20 | 30 | 20 | 30 | mA |
| | | $I_{SB}$ Flow Through | 20 | 30 | 20 | 30 | 20 | 30 | 20 | 30 | mA |
| Deselect Current | Device Deselected; All other inputs ≥ $V_{IH}$ or ≤ $V_{IL}$ | $I_{DD}$ Pipeline | 35 | 45 | 30 | 40 | 30 | 40 | 20 | 30 | mA |
| | | $I_{DD}$ Flow Through | 20 | 30 | 20 | 30 | 15 | 25 | 15 | 25 | mA |

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## AC Electrical Characteristics

| | Parameter | Symbol | -180 | | -166 | | -150 | | -100 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Pipeline | Clock Cycle Time | tKC | 5.5 | — | 6.0 | — | 6.7 | — | 10 | — | ns |
| | Clock to Output Valid | tKQ | — | 3.0 | — | 3.5 | — | 3.8 | — | 4.5 | ns |
| | Clock to Output Invalid | tKQX | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| | Clock to Output in Low-Z | tLZ[1] | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| Flow Through | Clock Cycle Time | tKC | 9.1 | — | 10.0 | — | 12.0 | — | 15.0 | — | ns |
| | Clock to Output Valid | tKQ | — | 8.0 | — | 8.5 | — | 10.0 | — | 12.0 | ns |
| | Clock to Output Invalid | tKQX | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | — | ns |
| | Clock to Output in Low-Z | tLZ[1] | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | — | ns |
| | Clock HIGH Time | tKH | 1.3 | — | 1.3 | — | 1.3 | — | 1.3 | — | ns |
| | Clock LOW Time | tKL | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| | Clock to Output in High-Z | tHZ[1] | 1.5 | 3.2 | 1.5 | 3.5 | 1.5 | 3.8 | 1.5 | 5 | ns |
| | $\overline{G}$ to Output Valid | tOE | — | 3.2 | — | 3.5 | — | 3.8 | — | 5 | ns |
| | $\overline{G}$ to output in Low-Z | tOLZ[1] | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| | $\overline{G}$ to output in High-Z | tOHZ[1] | — | 3.2 | — | 3.5 | — | 3.8 | — | 5 | ns |
| | Setup time | tS | 1.5 | — | 1.5 | — | 1.5 | — | 2.0 | — | ns |
| | Hold time | tH | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| | ZZ setup time | tZZS[2] | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| | ZZ hold time | tZZH[2] | 1 | — | 1 | — | 1 | — | 1 | — | ns |
| | ZZ recovery | tZZR | 20 | — | 20 | — | 20 | — | 20 | — | ns |

Notes:
1. These parameters are sampled and are not 100% tested
2. ZZ is an asynchronous signal. However, In order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

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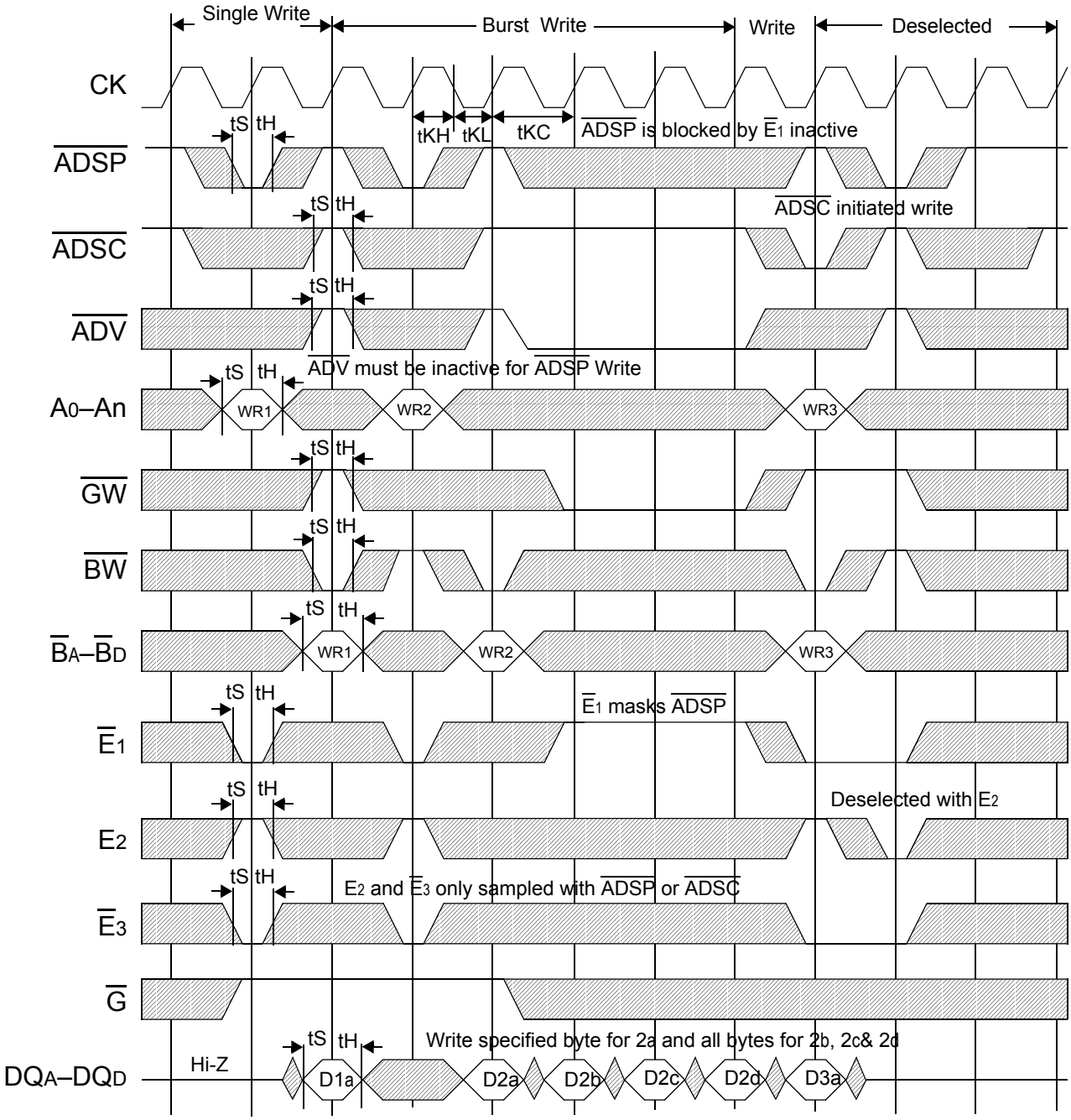
## Write Cycle Timing

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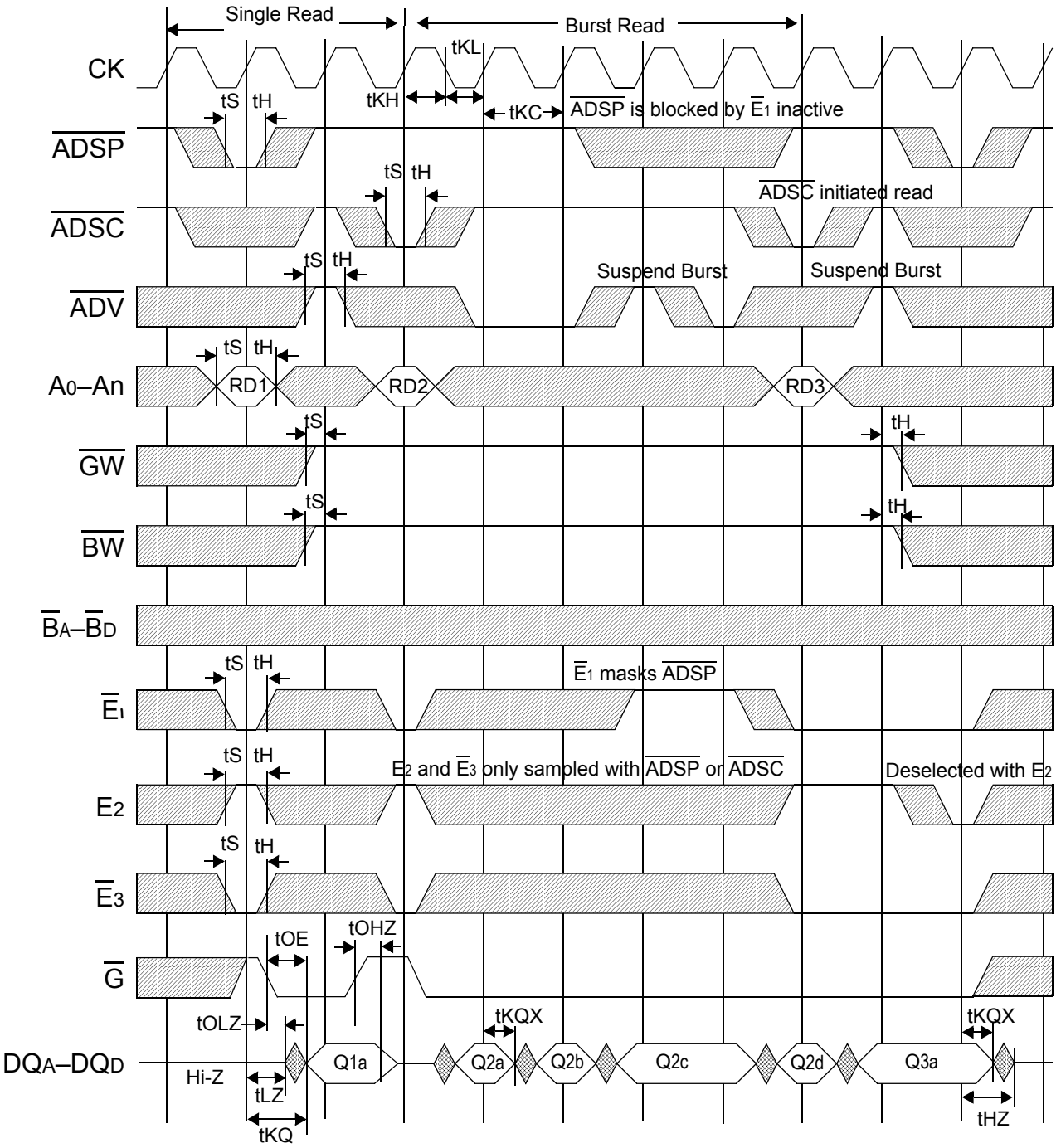
## Flow Through Read Cycle Timing

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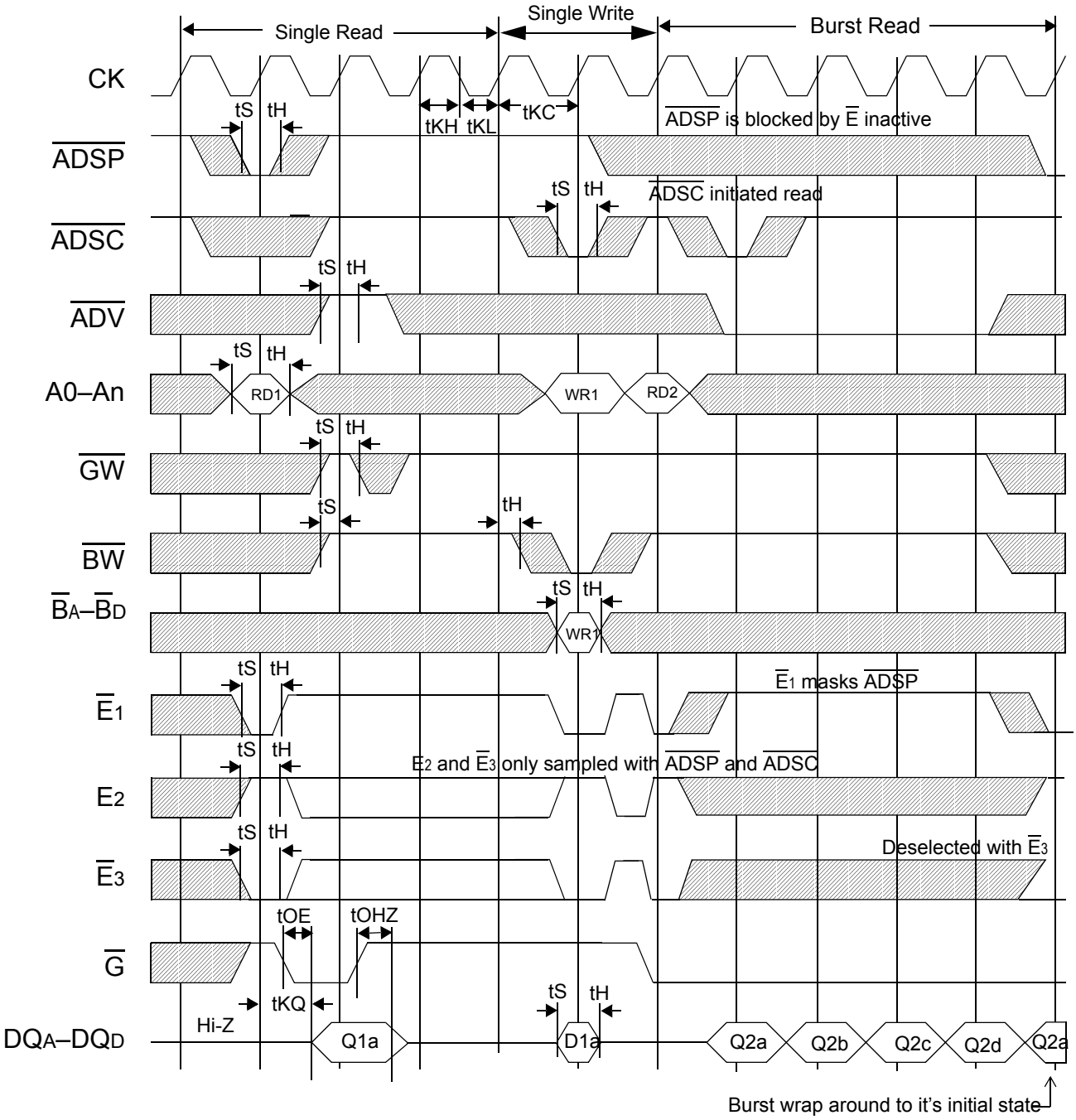
## Flow Through Read-Write Cycle Timing

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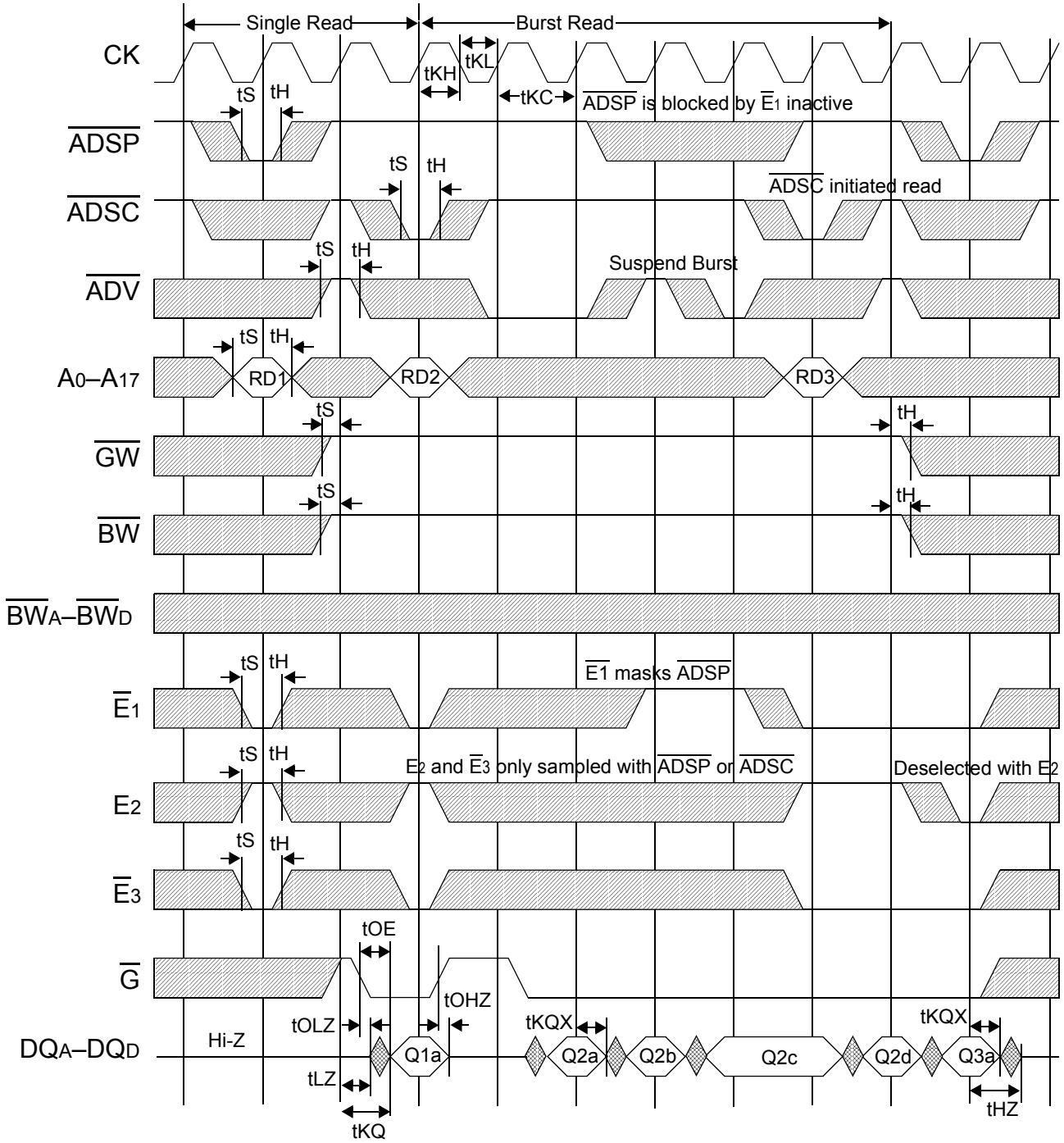
## Pipelined SCD Read Cycle Timing

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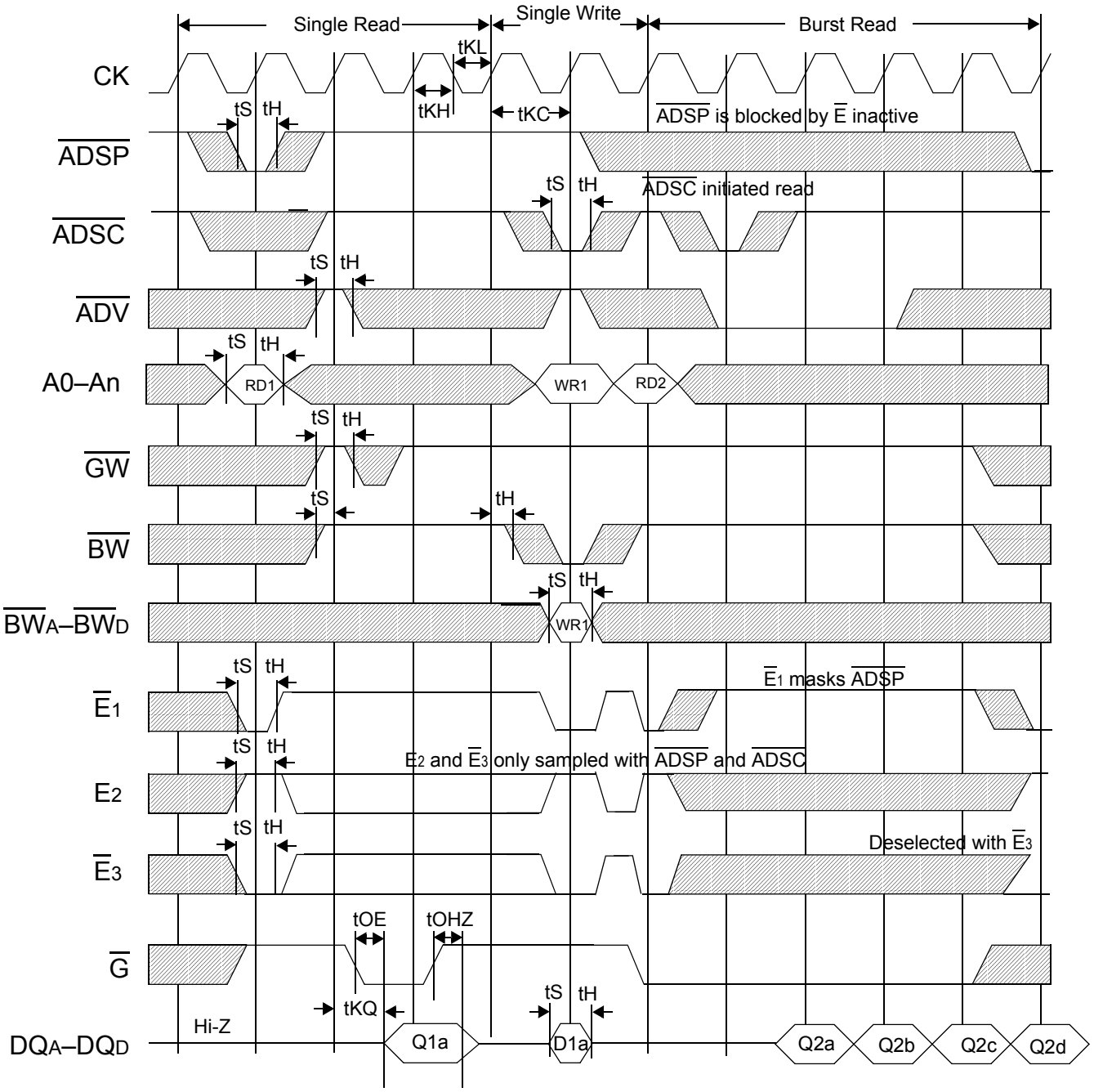
## Pipelined SCD Read-Write Cycle Timing

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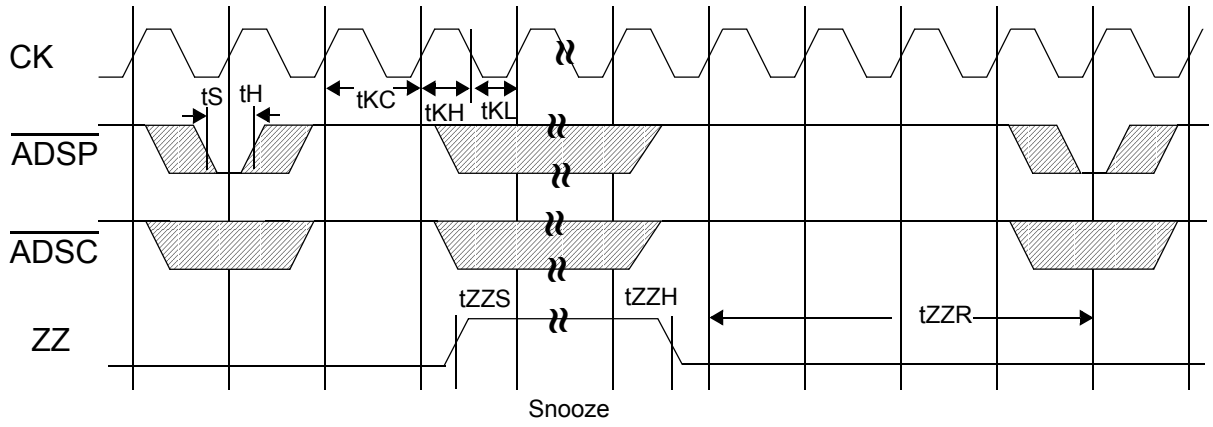
## Sleep Mode Timing Diagram




## Application Tips

### Single and Dual Cycle Deselect

SCD devices force the use of “dummy read cycles” (read cycles that are launched normally but that are ended with the output drivers inactive) in a fully synchronous environment. Dummy read cycles waste performance but their use usually assures there will be no bus contention in transitions from reads to writes or between banks of RAMs. DCD SRAMs do not waste bandwidth on dummy cycles and are logically simpler to manage in a multiple bank application (wait states need not be inserted at bank address boundary crossings), but greater care must be exercised to avoid excessive bus contention.

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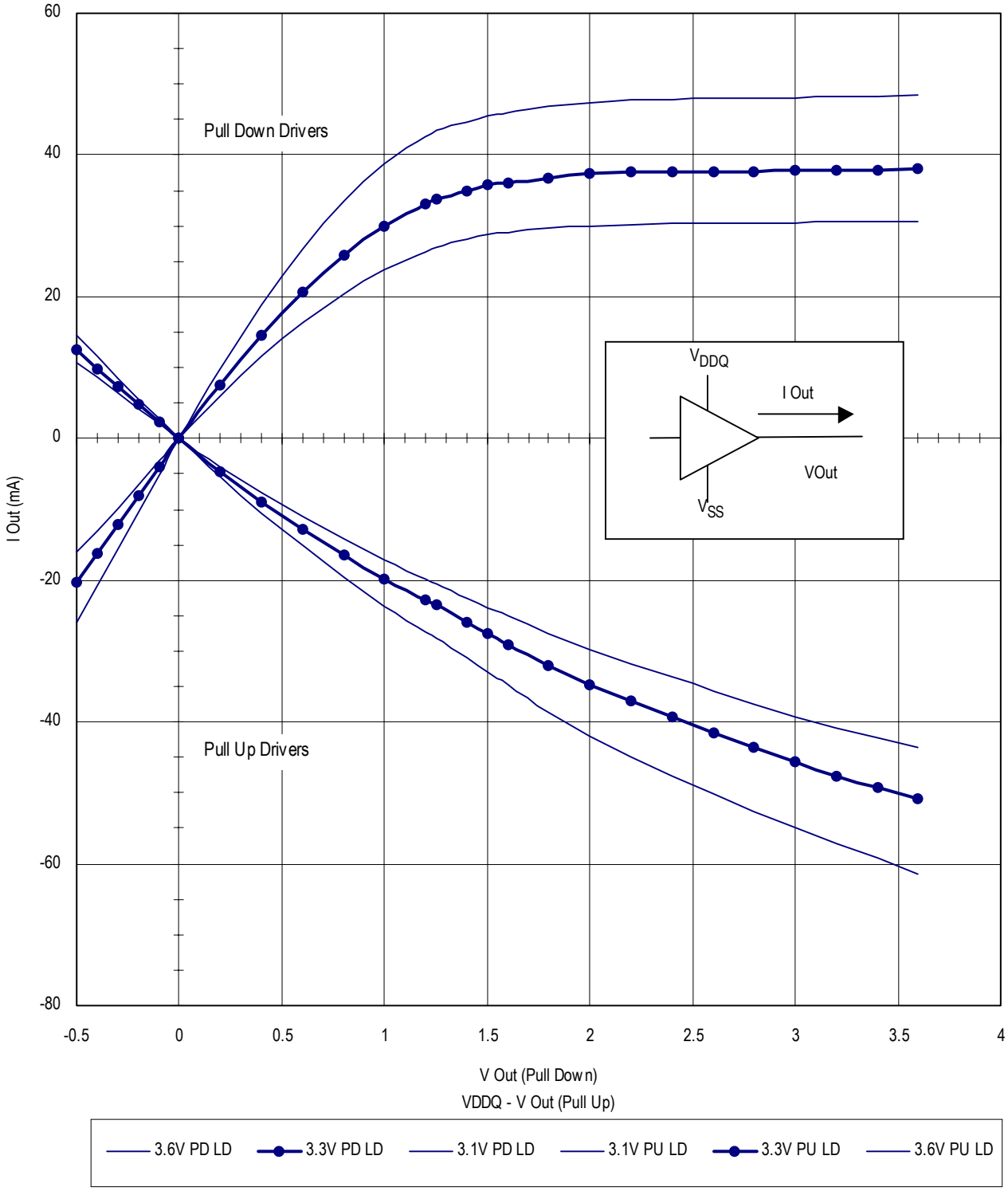
## GS84018/32/36A Output Driver Characteristics

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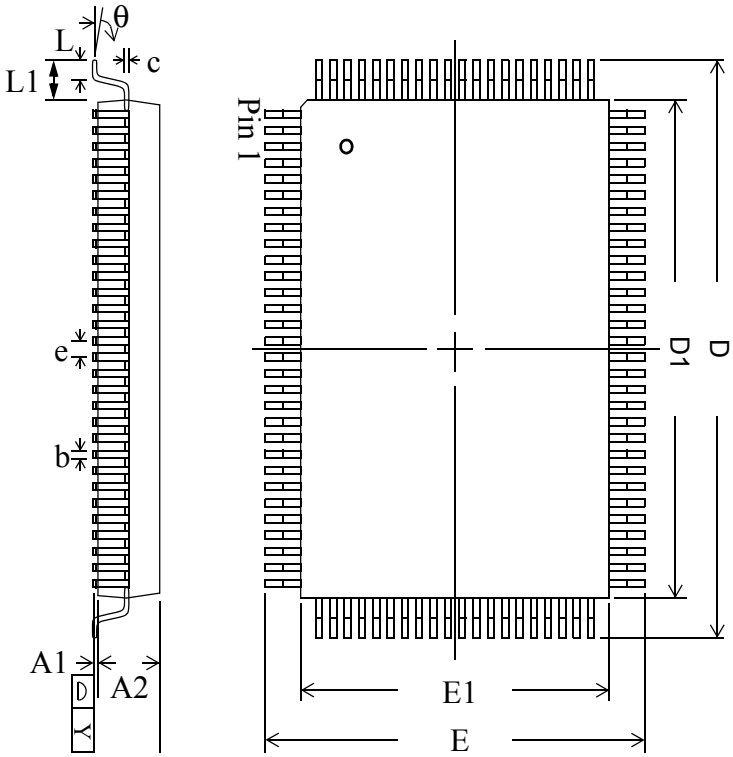
## TQFP Package Drawing

| Symbol | Description | Min. | Nom. | Max |
|---|---|---|---|---|
| A1 | Standoff | 0.05 | 0.10 | 0.15 |
| A2 | Body Thickness | 1.35 | 1.40 | 1.45 |
| b | Lead Width | 0.20 | 0.30 | 0.40 |
| c | Lead Thickness | 0.09 | | 0.20 |
| D | Terminal Dimension | 21.9 | 22.0 | 22.1 |
| D1 | Package Body | 19.9 | 20.0 | 20.1 |
| E | Terminal Dimension | 15.9 | 16.0 | 16.1 |
| E1 | Package Body | 13.9 | 14.0 | 14.1 |
| e | Lead Pitch | | 0.65 | |
| L | Foot Length | 0.45 | 0.60 | 0.75 |
| L1 | Lead Length | | 1.00 | |
| Y | Coplanarity | | | 0.10 |
| θ | Lead Angle | 0° | | 7° |




Notes:
1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.

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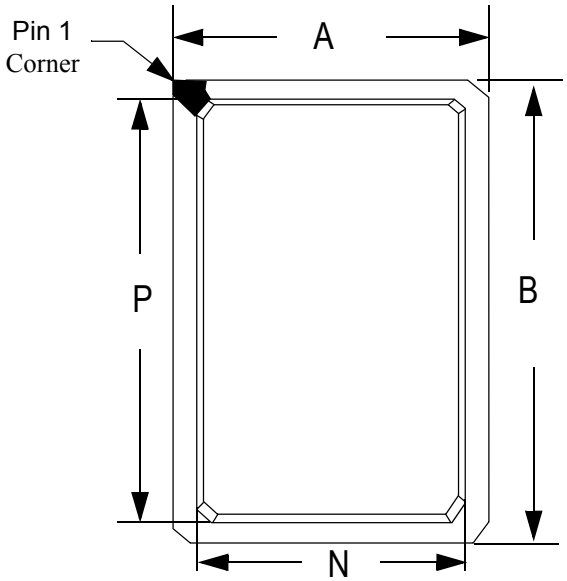
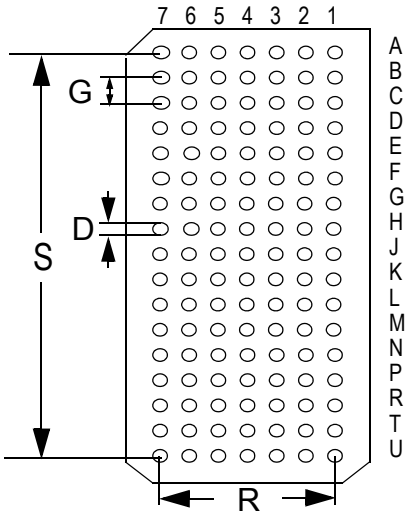
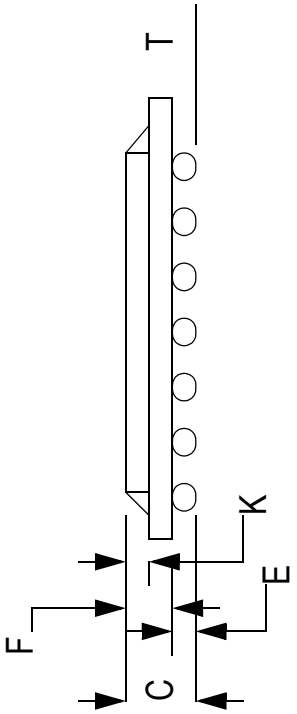
## Package Dimensions—119-Pin BGA




Top View




Bottom View




Side View

### Package Dimensions—119-Pin BGA

| Symbol | Description | Min. | Nom. | Max |
|---|---|---|---|---|
| A | Width | 13.8 | 14.0 | 14.2 |
| B | Length | 21.8 | 22.0 | 22.2 |
| C | Package Height (including ball) | - | | 2.40 |
| D | Ball Size | 0.60 | 0.75 | 0.90 |
| E | Ball Height | 0.50 | 0.60 | 0.70 |
| F | Package Height (excluding balls) | | 1.46 | 1.70 |
| G | Width between Balls | | 1.27 | |
| K | Package Height above board | 0.80 | 0.90 | 1.00 |
| N | Cut-out Package Width | | 12.00 | |
| P | Foot Length | | 19.50 | |
| R | Width of package between balls | | 7.62 | |
| S | Length of package between balls | | 20.32 | |
| T | Variance of Ball Height | | 0.15 | |

Unit: mm

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## Ordering Information for GSI Synchronous Burst RAMS

| Org | Part Number[1] | Type | Package | Speed[2] (MHz/ns) | $T_A$[3] | Status |
|---|---|---|---|---|---|---|
| 256K x 18 | GS84018AT-180 | Pipeline/Flow Through | TQFP | 180/8 | C | |
| 256K x 18 | GS84018AT-166 | Pipeline/Flow Through | TQFP | 166/8.5 | C | |
| 256K x 18 | GS84018AT-150 | Pipeline/Flow Through | TQFP | 150/10 | C | |
| 256K x 18 | GS84018AT-100 | Pipeline/Flow Through | TQFP | 100/12 | C | |
| 128K x 32 | GS84032AT-180 | Pipeline/Flow Through | TQFP | 180/8 | C | |
| 128K x 32 | GS84032AT-166 | Pipeline/Flow Through | TQFP | 166/8.5 | C | |
| 128K x 32 | GS84032AT-150 | Pipeline/Flow Through | TQFP | 150/10 | C | |
| 128K x 32 | GS84032AT-100 | Pipeline/Flow Through | TQFP | 100/12 | C | |
| 128K x 36 | GS84036AT-180 | Pipeline/Flow Through | TQFP | 180/8 | C | |
| 128K x 36 | GS84036AT-166 | Pipeline/Flow Through | TQFP | 166/8.5 | C | |
| 128K x 36 | GS84036AT-150 | Pipeline/Flow Through | TQFP | 150/10 | C | |
| 128K x 36 | GS84036AT-100 | Pipeline/Flow Through | TQFP | 100/12 | C | |
| 256K x 18 | GS84018AT-180I | Pipeline/Flow Through | TQFP | 180/8 | I | |
| 256K x 18 | GS84018AT-166I | Pipeline/Flow Through | TQFP | 166/8.5 | I | |
| 256K x 18 | GS84018AT-150I | Pipeline/Flow Through | TQFP | 150/10 | C | |
| 256K x 18 | GS84018AT-100I | Pipeline/Flow Through | TQFP | 100/12 | C | |
| 128K x 32 | GS84032AT-180I | Pipeline/Flow Through | TQFP | 180/8 | I | |
| 128K x 32 | GS84032AT-166I | Pipeline/Flow Through | TQFP | 166/8.5 | I | |
| 128K x 32 | GS84032AT-150I | Pipeline/Flow Through | TQFP | 150/10 | C | |
| 128K x 32 | GS84032AT-100I | Pipeline/Flow Through | TQFP | 100/12 | C | |
| 128K x 36 | GS84036AT-180I | Pipeline/Flow Through | TQFP | 180/8 | I | |
| 128K x 36 | GS84036AT-166I | Pipeline/Flow Through | TQFP | 166/8.5 | I | |
| 128K x 36 | GS84036AT-150I | Pipeline/Flow Through | TQFP | 150/10 | C | |
| 128K x 36 | GS84036AT-100I | Pipeline/Flow Through | TQFP | 100/12 | C | |
| 256K x 18 | GS84018AB-180 | Pipeline/Flow Through | BGA | 180/8 | C | |
| 256K x 18 | GS84018AB-166 | Pipeline/Flow Through | BGA | 166/8.5 | C | |
| 256K x 18 | GS84018AB-150 | Pipeline/Flow Through | BGA | 150/10 | C | |
| 256K x 18 | GS84018AB-100 | Pipeline/Flow Through | BGA | 100/12 | C | |
| 128K x 32 | GS84032AB-180 | Pipeline/Flow Through | BGA | 180/8 | C | |
| 128K x 32 | GS84032AB-166 | Pipeline/Flow Through | BGA | 166/8.5 | C | |

Notes:

1. Customers requiring delivery in Tape and Reel should add the character “T” to the end of the part number. Example: GS84032AT-8T.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipelined mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow through mode-selectable by the user.
3. $T_A$ = C = Commercial Temperature Range. $T_A$ = I = Industrial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings.

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| Org | Part Number[1] | Type | Package | Speed[2] (MHz/ns) | $T_A$[3] | Status |
|---|---|---|---|---|---|---|
| 128K x 32 | GS84032AB-150 | Pipeline/Flow Through | BGA | 150/10 | C | |
| 128K x 32 | GS84032AB-100 | Pipeline/Flow Through | BGA | 100/12 | C | |
| 128K x 36 | GS84036AB-180 | Pipeline/Flow Through | BGA | 180/8 | C | |
| 128K x 36 | GS84036AB-166 | Pipeline/Flow Through | BGA | 166/8.5 | C | |
| 128K x 36 | GS84036AB-150 | Pipeline/Flow Through | BGA | 150/10 | C | |
| 128K x 36 | GS84036AB-100 | Pipeline/Flow Through | BGA | 100/12 | C | |
| 256K x 18 | GS84018AB-180I | Pipeline/Flow Through | BGA | 180/8 | I | |
| 256K x 18 | GS84018AB-166I | Pipeline/Flow Through | BGA | 166/8.5 | I | |
| 256K x 18 | GS84018AB-150I | Pipeline/Flow Through | BGA | 150/10 | C | |
| 256K x 18 | GS84018AB-100I | Pipeline/Flow Through | BGA | 100/12 | C | |
| 128K x 32 | GS84032AB-180I | Pipeline/Flow Through | BGA | 180/8 | I | |
| 128K x 32 | GS84032AB-166I | Pipeline/Flow Through | BGA | 166/8.5 | I | |
| 128K x 32 | GS84032AB-150I | Pipeline/Flow Through | BGA | 150/10 | C | |
| 128K x 32 | GS84032AB-100I | Pipeline/Flow Through | BGA | 100/12 | C | |
| 128K x 36 | GS84036AB-180I | Pipeline/Flow Through | BGA | 180/8 | I | |
| 128K x 36 | GS84036AB-166I | Pipeline/Flow Through | BGA | 166/8.5 | I | |
| 128K x 36 | GS84036AB-150I | Pipeline/Flow Through | BGA | 150/10 | C | |
| 128K x 36 | GS84036AB-100I | Pipeline/Flow Through | BGA | 100/12 | C | |

Notes:

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4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings.

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## Revision History

| Rev. Code: Old; New | Types of Changes Format or Content | Page /Revisions;Reason |
|---|---|---|
| GS84018/32/36 Rev 1.02c 5/1999; GS84018/32/36A 1.00First Release 8/1999D | Format/Typos | • Document/Continued changing to new format. |
| | Content | • First Datasheet for this part. |
| GS84018/32/36A1.00 8/ 1999;GS84018/32/36A1.01 9/ 1999E | Format/Typos | • Took “E” out of 840HE...in Core and Interface Voltages.<br>• Pin outs/New small caps format.<br>• Timing Diagrams/New format.<br>• Block Diagrams/New small caps format. |
| | Content | • Pin outs/x32 & x36 TQFP/Changed pin 72 from DQA3 to DQB3.<br>• Pin Description/Rearranged Address Inputs to match order on TQFP Pinout.<br>• TQFP Package Diagram/Corrected Dimension D Max from 20.1 to 22.1. |
| GS84018/32/36A1.01 9/ 1999E;GS84018/32/36A1.02 | | • Fixed Ordering information and speed bins.<br>• Took out Fine Pitch BGA Package. Package change in progress. |
| GS84018/32/36A1.0210-11/ 1999;GS84018/32/36A1.032/ 2000G | Format | • New GSI Logo<br>• Took “Pin” out of heading for consistency. |
| GS84018/32/36A1.032/2000G; 84018A_r1_04 | Content | • Corrected all part order numbers |
| 84018A_r1_04; 84018A_r1_05 | Content | • Updated pin descriptions table |
| 84018A_r1_05; 84018A_r1_06 | Content | • Updated BGA pin description table to meet JEDEC standard |
| 84018A_r1_06; 84018A_r1_07 | Content/Format | • Added “non-A” speed bins to Operating Currents table, AC Electrical Characteristics table, and Ordering Information table<br>• Updated format to fit Technical Documentation standards |
| 84018A_r1_07; 84018A_r1_08 | Content/Format | • Updated font<br>• Corrected $I_{DD}$ for 150 MHz and 100 MHz on page 1 and page 18 |
| 84018A_r1_08; 84018A_r1_09 | Content | • Updated table on page 1<br>• Updated Operating Currents table on page 18<br>• Updated Electrical Characteristics table on page 19 |
| 84018A_r1_09, 84018A_r1_10 | Content | • Reduced $I_{DD}$ by 20 mA in table on page 1 and Operating Currents table |
| 84018A_r1_10; 84018A_r1_11 | Content | • Corrected incorrect package type in ordering information table |
| 84018A_r1_11; 84018A_r1_12 | Content | • Removed 200 MHz references from entire datasheet |

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