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October 2014

FDMS7578

N-Channel Power Trench[®] MOSFET 25 V,60 A, 5.8 m Ω

Features

- Max $r_{DS(on)} = 5.8 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 17 \text{ A}$
- Max $r_{DS(on)} = 8 \text{ m}\Omega$ at $V_{GS} = 4.5 \text{ V}$, $I_D = 14 \text{ A}$
- Advanced Package and Silicon combination for low r_{DS(on)} and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

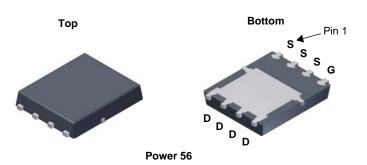


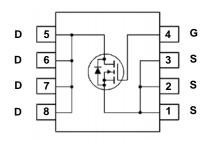
General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$, fast switching speed and body diode reverse recovery performance.

Applications

- Control MOSFET for Synchronous Buck Converters
- Notebook
- Server
- Telecomm
- High Efficiency DC-DC Switch Mode Power Supplies





MOSFET Maximum Ratings TA = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V _{DS}	Drain to Source Voltage			25	V
V _{GS}	Gate to Source Voltage		(Note 4)	±20	V
I _D	Drain Current -Continuous	T _C = 25 °C		60	
	-Continuous	T _A = 25 °C	(Note 1a)	17	Α
	-Pulsed		(Note5)	90	
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	40	mJ
D	Power Dissipation	T _C = 25 °C		33	W
P_{D}	Power Dissipation	T _A = 25 °C	(Note 1a)	2.5	VV
T _J , T _{STG}	Operating and Storage Junction Tempera	ature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		3.7	°C/W
$R_{\theta,JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS7578	FDMS7578	Power 56	13 "	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	25			V
$\Delta BV_{DSS} = \Delta T_J$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25 °C		20		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 20 V, V _{GS} = 0 V			1	μΑ
I _{GSS}	Gate to Source Leakage Current, Forward	V _{GS} = 20 V, V _{DS} = 0 V			100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	1.0	1.6	3.0	V
$\Delta V_{GS(th)} = \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		-6		mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 17 \text{ A}$		4.6	5.8	
		$V_{GS} = 4.5 \text{ V}, I_D = 14 \text{ A}$		6.3	8	mΩ
		$V_{GS} = 10 \text{ V}, I_D = 17 \text{ A}, T_J = 125 ^{\circ}\text{C}$		6.7	8.5	
g _{FS}	Forward Transconductance	V _{DD} = 5 V, I _D = 17 A		77		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 40.V V 0.V	1221	1625	pF
C _{oss}	Output Capacitance	$V_{DS} = 13 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$	371	495	pF
C _{rss}	Reverse Transfer Capacitance	1 = 1 1011 12	54	85	pF
R_g	Gate Resistance		1.2	2.4	Ω

Switching Characteristics

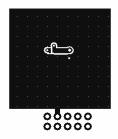
t _{d(on)}	Turn-On Delay Time		8	17	ns
t _r	Rise Time	V _{DD} = 13 V, I _D = 17 A,	2.6	10	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	20	33	ns
t _f	Fall Time		2.2	10	ns
0	Total Gate Charge	V _{GS} = 0 V to 10 V	18	25	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to } 4.5 \text{ V}$ $V_{DD} = 13 \text{ V}$	8	11	nC
Q_{gs}	Total Gate Charge	I _D = 17 A	3.7		nC
Q_{gd}	Gate to Drain "Miller" Charge		1.7		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 2 \text{ A}$	(Note 2)	0.72	1.1	V
		$V_{GS} = 0 \text{ V}, I_{S} = 17 \text{ A}$	(Note 2)	0.83	1.2	V
t _{rr}	Reverse Recovery Time	$I_F = 17 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s}$		20	32	ns
Q _{rr}	Reverse Recovery Charge			6	12	nC
t _{rr}	Reverse Recovery Time	$I_F = 17 \text{ A}, \text{ di/dt} = 300 \text{ A/}\mu\text{s}$		19	34	ns
Q _{rr}	Reverse Recovery Charge			13	24	nC

NOTES

^{1.} $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50 °C/W when mounted on a 1 in² pad of 2 oz copper



b.125 °C/W when mounted on a minimum pad of 2 oz copper

- 2. Pulse Test: Pulse Width < 300 $\mu\text{s},$ Duty cycle < 2.0 %.
- 3. E_{AS} of 40 mJ is based on starting T_J = 25 °C, L = 1 mH, I_{AS} = 9 A, V_{DD} = 23 V, V_{GS} = 10 V. 100% test at L = 0.3 mH, I_{AS} = 14 A.
- 4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.
- 5. Pulse Id refers to Figure.11 Forward Bias Safe Operation Area.

Typical Characteristics T_J = 25 °C unless otherwise noted

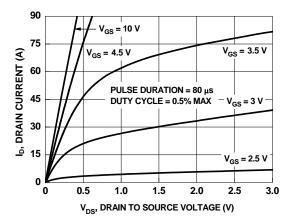


Figure 1. On-Region Characteristics

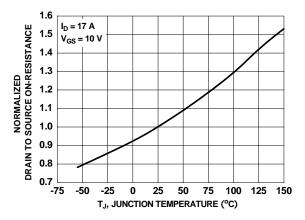


Figure 3. Normalized On-Resistance vs Junction Temperature

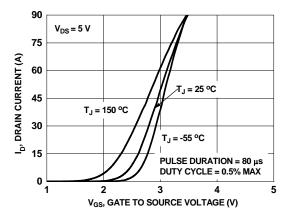


Figure 5. Transfer Characteristics

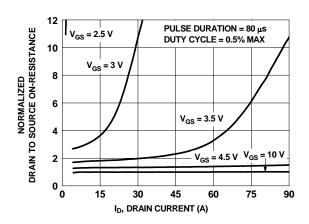


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

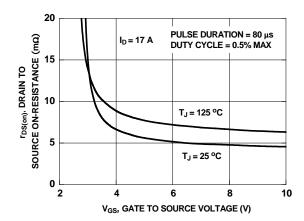


Figure 4. On-Resistance vs Gate to Source Voltage

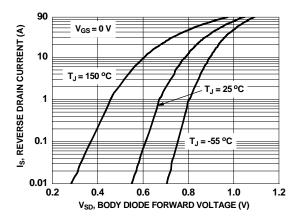


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

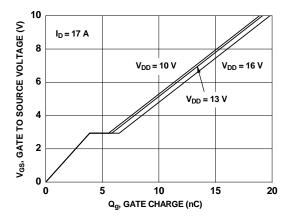


Figure 7. Gate Charge Characteristics

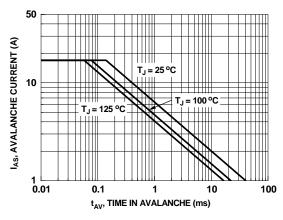


Figure 9. Unclamped Inductive Switching Capability

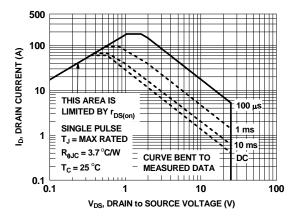


Figure 11. Forward Bias Safe Operating Area

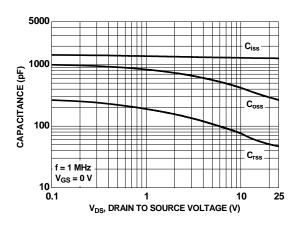


Figure 8. Capacitance vs Drain to Source Voltage

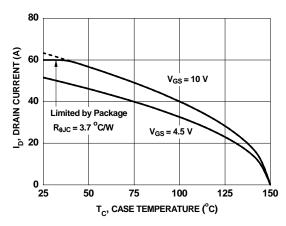


Figure 10. Maximum Continuous Drain Current vs Case Temperature

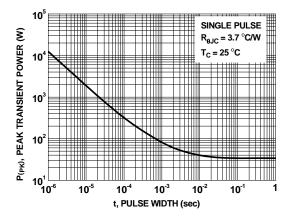


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25$ °C unless otherwise noted

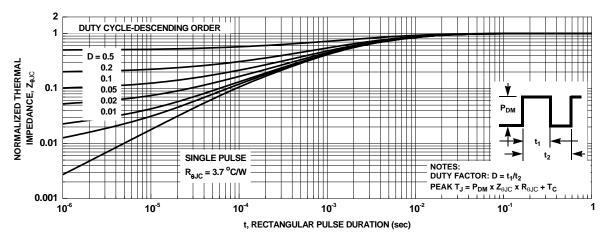


Figure 13. Transient Thermal Response Curve



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