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# FDMT1D3N08B

# N-Channel Dual Cool<sup>TM</sup> 88 PowerTrench<sup>®</sup> MOSFET 80 V, 164 A, 1.35 m $\Omega$

#### **Features**

- Max  $r_{DS(on)}$  = 1.35 m $\Omega$  at  $V_{GS}$  = 10 V,  $I_D$  = 36 A
- Max  $r_{DS(on)}$  = 1.8 m $\Omega$  at  $V_{GS}$  = 8 V,  $I_D$  = 31 A
- Advanced Package and Silicon Combination for Low r<sub>DS(on)</sub> and High Efficiency
- Next Generation Enhanced Body Diode Technology, Engineered for Soft Recovery
- Low Profile 8x8 mm MLP Package
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant

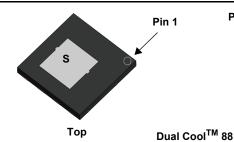
# **General Description**

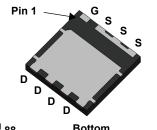
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process. Advancements in both silicon and Dual Cool  $^{TM}$  package technologies have been combined to offer the lowest  $r_{DS(on)}$  while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

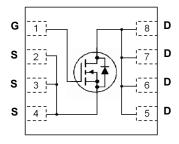
#### **Applications**

- OringFET / Load Switching
- Synchronous Rectification
- DC-DC Conversion









### **MOSFET Maximum Ratings** T<sub>A</sub> = 25 °C unless otherwise noted.

Symbol	Param	eter		Ratings	Units
$V_{DS}$	Drain to Source Voltage			80	V
$V_{GS}$	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T <sub>C</sub> = 25 °C	(Note 5)	164	
	-Continuous	T <sub>C</sub> = 100 °C	(Note 5)	103	^
'D	-Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	36	Α
	-Pulsed		(Note 4)	864	
E <sub>AS</sub>	Single Pulse Avalanche Energy		(Note 3)	1734	mJ
В	Power Dissipation	T <sub>C</sub> = 25 °C		178	w
$P_{D}$	Power Dissipation	T <sub>A</sub> = 25 °C	(Note 1a)	3.3	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Tempera	ature Range		-55 to +150	°C

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Top Source)	1.9	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Bottom Drain)	0.7	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	81	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1i)	15	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1j)	21	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1k)	9	

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
1D3N08B	FDMT1D3N08B	Dual Cool <sup>TM</sup> 88	13"	13.3 mm	3000 units

# **Electrical Characteristics** $T_J$ = 25 °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Chara	cteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		50		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 64 V, V <sub>GS</sub> = 0 V			1	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			100	nA

#### **On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2.0	3.2	4.0	V
$\Delta V_{GS(th)} \over \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25 °C		-11		mV/°C
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 36 A		1.1	1.35	
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 8 V, I <sub>D</sub> = 31 A		1.3	1.8	mΩ
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 36 A, T <sub>J</sub> = 125 °C		1.8	2.2	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 36 A		116		S

# **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V = 40 V V = 0 V		14000	19600	pF
Coss	Output Capacitance	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, f = 1 MHz		2050	2870	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 1011 12		50	150	pF
$R_g$	Gate Resistance		0.1	1.4	2.1	Ω

## **Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time		63	101	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 40 V, I <sub>D</sub> = 36 A,	56	90	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS}$ = 10 V, $R_{GEN}$ = 6 $\Omega$	68	109	ns
t <sub>f</sub>	Fall Time		20	32	ns
$Q_{g(TOT)}$	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V	186	260	nC
$Q_{g(TOT)}$	Total Gate Charge	V <sub>GS</sub> = 0 V to 8 V V <sub>DD</sub> = 40 V,	152	213	nC
$Q_{gs}$	Gate to Source Charge	I <sub>D</sub> = 36 A	67		nC
$Q_{gd}$	Gate to Drain "Miller" Charge		37		nC
Q <sub>oss</sub>	Output Charge	V <sub>DD</sub> = 40 V, V <sub>GS</sub> = 0 V	185		nC

#### **Drain-Source Diode Characteristics**

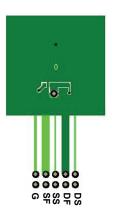
V <sub>SD</sub> Source to Drain Diode Fo	Source to Drain Diode, Fenyard Voltage	$V_{GS} = 0 \text{ V}, I_S = 2.6 \text{ A}$ (Note 2)	0.7	1.1	\/
	Source to Drain Diode Torward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 36 A (Note 2)	0.8	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>E</sub> = 36 A, di/dt = 100 A/μs	83	132	ns
Q <sub>rr</sub>	Reverse Recovery Charge	1F - 30 A, αι/αι - 100 A/μs	90	143	nC

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Top Source)	1.9	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Bottom Drain)	0.7	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1c)	26	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1d)	34	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1e)	14	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1f)	16	C/VV
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1g)	26	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1h)	60	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1i)	15	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1j)	21	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1k)	9	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1I)	11	

#### NOTES:

1. R<sub>0.JA</sub> is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below. R<sub>0.CA</sub> is determined by the user's board design.



a. 38 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 81 °C/W when mounted on a minimum pad of 2 oz copper

- c. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in  $^{\!2}\,\mathrm{pad}$  of 2 oz copper
- d. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- e. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- $f. \ Still \ air, \ 45.2x41.4x11.7mm \ Aavid \ Thermalloy \ Part \# \ 10-L41B-11 \ Heat \ Sink, \ minimum \ pad \ of \ 2 \ oz \ copper \ and \ Copper \ air \ Aavid \ Thermalloy \ Part \# \ 10-L41B-11 \ Heat \ Sink, \ minimum \ pad \ of \ 2 \ oz \ copper \ Aavid \ Thermalloy \ Part \# \ 10-L41B-11 \ Heat \ Sink, \ minimum \ pad \ of \ 2 \ oz \ copper \ Aavid \ Part \ Aavid \ Part \ Part$
- g. 200FPM Airflow, No Heat Sink,1 in  $^{\!2}$  pad of 2 oz copper
- h. 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
- i. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- j. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- k. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- I. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- 2. Pulse Test: Pulse Width < 300  $\mu s,$  Duty cycle < 2.0%.
- 3.  $E_{AS}$  of 1734 mJ is based on starting  $T_J$  = 25 °C; N-ch: L = 3 mH,  $I_{AS}$  = 34 A,  $V_{DD}$  = 80 V,  $V_{GS}$  =10 V. 100% test at L = 0.3 mH,  $I_{AS}$  = 77 A.
- 4. Pulsed Id please refer to Fig 11 SOA graph for more details.
- 5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

#### Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted.

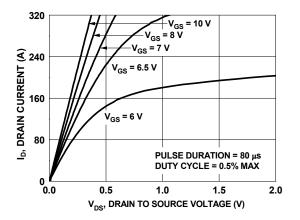


Figure 1. On Region Characteristics

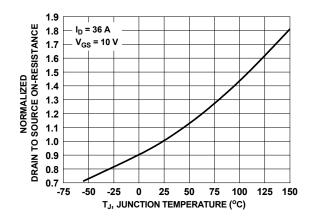


Figure 3. Normalized On Resistance vs. Junction Temperature

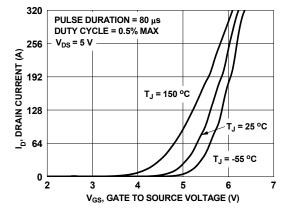


Figure 5. Transfer Characteristics

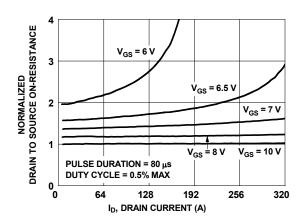


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

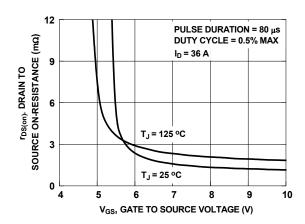


Figure 4. On-Resistance vs. Gate to Source Voltage

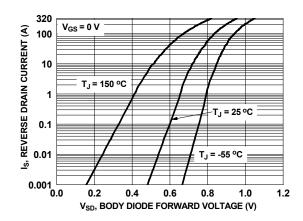


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

## **Typical Characteristics** $T_J = 25$ °C unless otherwise noted.

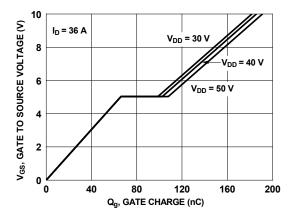


Figure 7. Gate Charge Characteristics

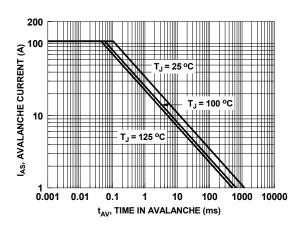


Figure 9. Unclamped Inductive Switching Capability

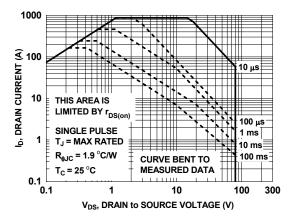


Figure 11. Forward Bias Safe Operating Area

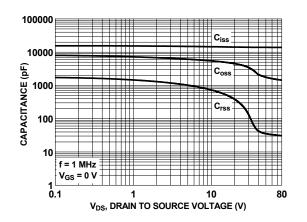


Figure 8. Capacitance vs. Drain to Source Voltage

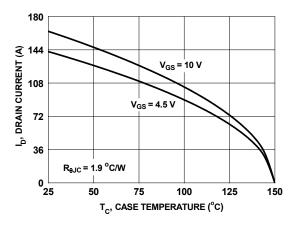


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

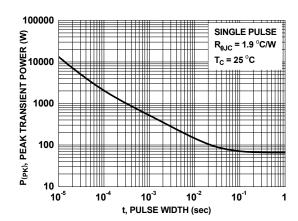


Figure 12. Single Pulse Maximum Power Dissipation



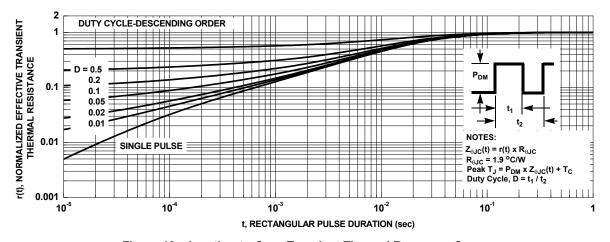
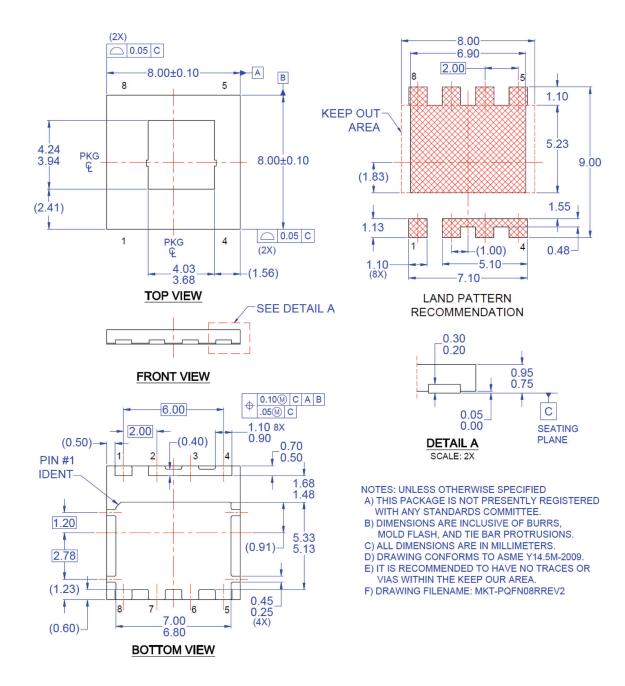


Figure 13. Junction-to-Case Transient Thermal Response Curve

#### **Dimensional Outline and Pad Layout**

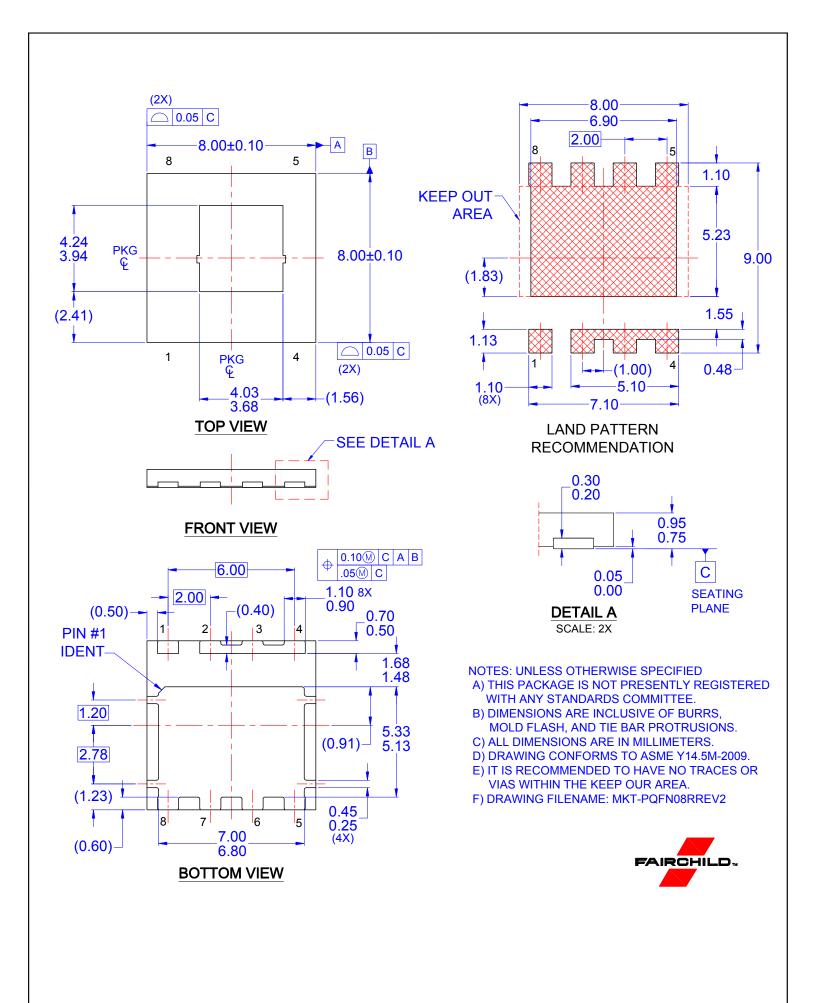


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