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March 2015

FDD6637

35V P-Channel PowerTrench^O MOSFET

General Description

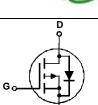
This P-Channel MOSFET has been produced using Fairchild Semiconductor's proprietary PowerTrench technology to deliver low Rdson and optimized Bvdss capability to offer superior performance benefit in the applications.

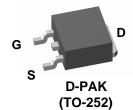
Applications

- Inverter
- Power Supplies

Features

- -55 A, -35 V $R_{DS(ON)}$ = 11.6 m Ω @ V_{GS} = -10 V $R_{DS(ON)}$ = 18 m Ω @ V_{GS} = -4.5 V
- High performance trench technology for extremely low $R_{\text{DS(ON)}}$
- RoHS Compliant





Absolute Maximum Ratings T_A=25'

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units	
V _{DSS}	Drain-Source Voltage			- 35	V
V _{DS(Avalanche)}	Drain-Source Avalanche Voltage (maximum) (Note 4)			-40	V
V _{GSS}	Gate-Source Voltage			±25	V
I _D	Continuous Drain Current	@T _C =25°C	(Note 3)	– 55	A
		@T _A =25°C	(Note 1a)	-13	
		Pulsed	(Note 1a)	-100	
P _D	Power Dissipation	@T _C =25°C	(Note 3)	57	W
		@ T _A =25°C	(Note 1a)	3.1	
		@ T _A =25°C	(Note 1b)	1.3	
T _J , T _{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C	

Thermal Characteristics

R _{eJC}	Thermal Resistance, Junction-to-Case	(Note 1)	2.2	°C/W
R _{eJA}	Thermal Resistance, Junction-to-Ambient	(Note 1a)	40	
R _{e,IA}	Thermal Resistance, Junction-to-Ambient	(Note 1b)	96	

Package Marking and Ordering Information

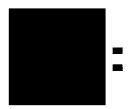
Device Marking	Device	Package	Reel Size	Tape width	Quantity	
FDD6637	FDD6637	D-PAK (TO-252)	13"	16mm	2500 units	

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Drain-So	urce Avalanche Ratings					ı
E _{AS}	Drain-Source Avalanche Energy (Single Pulse)	V _{DD} = -35 V, I _D = -11 A, L=1mH		61		mJ
I _{AS}	Drain-Source Avalanche Current			-14		Α
Off Chara	acteristics(Note 2)					
BV _{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \qquad I_{D} = -250 \mu\text{A}$	-35			V
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -28 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μΑ
I _{GSS}	Gate-Body Leakage	$V_{GS} = \pm 25 \text{ V}, \qquad V_{DS} = 0 \text{ V}$			±100	nA
On Chara	acteristics (Note 2)					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-1	-1.6	-3	V
R _{DS(on)}	Static Drain-Source On-Resistance	$V_{GS} = -10 \text{ V}, I_D = -14 \text{ A}$ $V_{GS} = -4.5 \text{ V}, I_D = -11 \text{ A}$ $V_{GS} = -10 \text{ V}, I_D = -14 \text{ A}, T_J = 125^{\circ}\text{C}$		9.7 14.4 14.7	11.6 18 19	mΩ
g _{FS}	Forward Transconductance	$V_{DS} = -5 \text{ V}, \qquad I_{D} = -14 \text{ A}$		35		S
Dvnamic	Characteristics		•			
C _{iss}	Input Capacitance			2370		pF
Coss	Output Capacitance	$V_{DS} = -20 \text{ V}, \qquad V_{GS} = 0 \text{ V},$		470		pF
C _{rss}	Reverse Transfer Capacitance	f = 1.0 MHz		250		pF
R _G	Gate Resistance	f = 1.0 MHz		3.6		Ω
Switchin	g Characteristics (Note 2)	1				
t _{d(on)}	Turn-On Delay Time			18	32	ns
t _r	Turn-On Rise Time	$V_{DD} = -20 \text{ V}, \qquad I_{D} = -1 \text{ A},$		10	20	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = -10 \text{ V}, \qquad R_{GEN} = 6 \Omega$		62	100	ns
t _f	Turn-Off Fall Time	1		36	58	ns
Q _g	Total Gate Charge, V _{GS} = −10V			45	63	nC
Q _g	Total Gate Charge, V _{GS} = −5V	$V_{DS} = -20 \text{ V}, I_{D} = -14 \text{ A}$		25	35	nC
Q _{gs}	Gate-Source Charge	7		7		nC
Q_{gd}	Gate-Drain Charge			10		nC

Electrical Characteristics T _A = 25°C unless otherwise noted								
Symbol	Parameter	Test Conditions	Min	Тур	Max	Units		
Drain-Source Diode Characteristics								
V _{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -14 \text{ A}$ (Note 2)		-0.8	-1.2	V		
trr	Diode Reverse Recovery Time	IF = -14 A, $diF/dt = 100 A/µs$		28		ns		
Qrr	Diode Reverse Recovery Charge			15		nC		

Notes

1. R_{BJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{BJC} is guaranteed by design while R_{BCA} is determined by the user's board design.



a) $R_{\theta JA} = 40^{\circ} C/W$ when mounted on a $1in^2$ pad of 2 oz copper



b) $R_{\theta JA} = 96$ °C/W when mounted on a minimum pad.

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width < 300μ s, Duty Cycle < 2.0%

3. Maximum current is calculated as: $\sqrt{\frac{P_D}{R_{DS(ON)}}}$

where P_D is maximum power dissipation at $T_C = 25^{\circ}C$ and $R_{DS(on)}$ is at $T_{J(max)}$ and $V_{GS} = 10V$. Package current limitation is 21A

4. BV(avalanche) Single-Pulse rating is guaranteed if device is operated within the UIS SOA boundary of the device.

Typical Characteristics

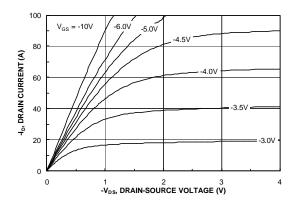


Figure 1. On-Region Characteristics

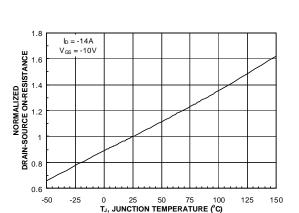


Figure 3. On-Resistance Variation with Temperature

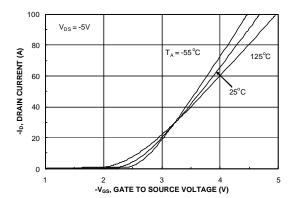


Figure 5. Transfer Characteristics

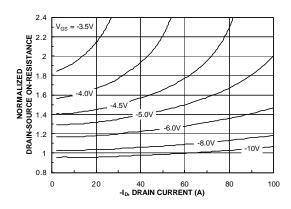


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

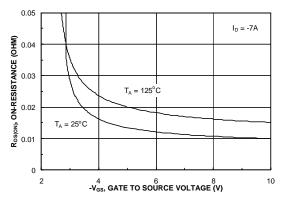


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

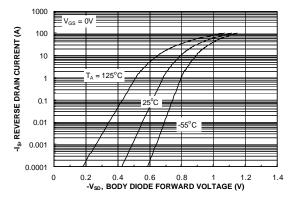


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

Typical Characteristics

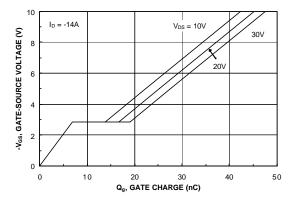


Figure 7. Gate Charge Characteristics

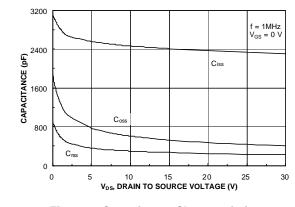


Figure 8. Capacitance Characteristics

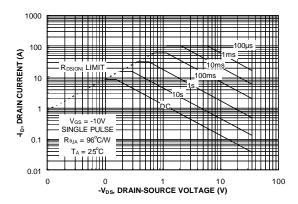


Figure 9. Maximum Safe Operating Area

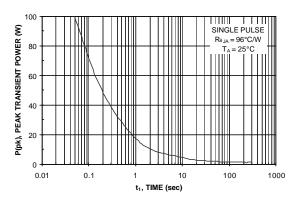


Figure 10. Single Pulse Maximum Power Dissipation

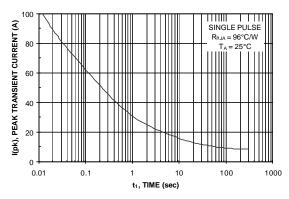


Figure 11. Single Pulse Maximum Peak Current

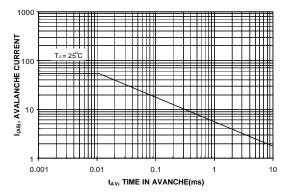


Figure 12. Unclamped Inductive Switching Capability

Typical Characteristics

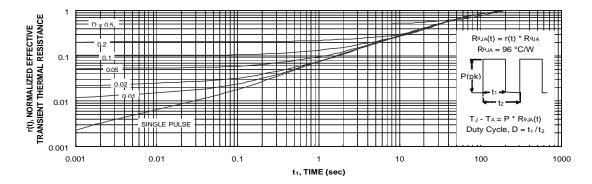


Figure 13. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

Test Circuits and Waveforms

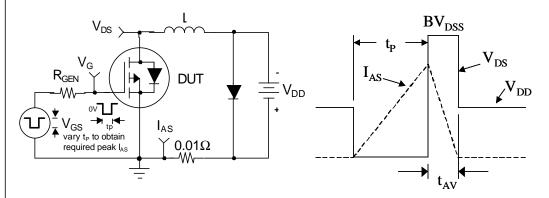


Figure 14. Unclamped Inductive Load Test Circuit

Figure 15. Unclamped Inductive Waveforms

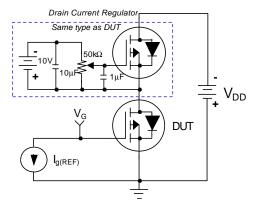


Figure 16. Gate Charge Test Circuit

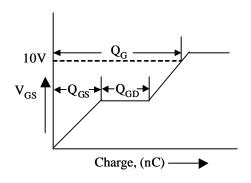


Figure 17. Gate Charge Waveform

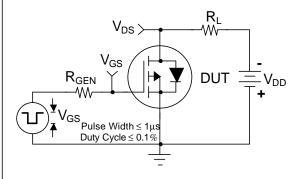


Figure 18. Switching Time Test Circuit

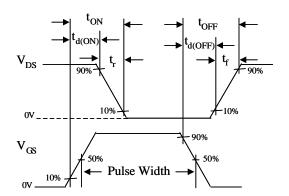
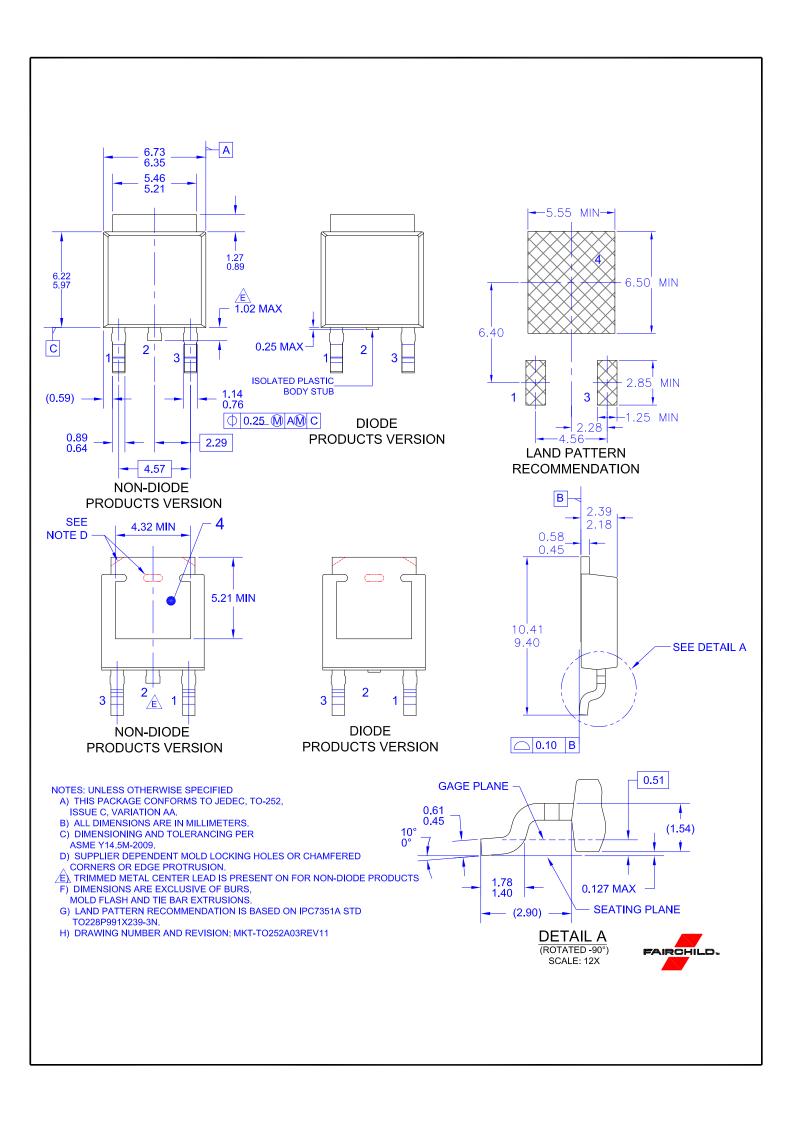


Figure 19. Switching Time Waveforms



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