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March 2015

FDMS86550

N-Channel PowerTrench[®] MOSFET 60 V, 234 A, 1.65 m Ω

Features

- Max $r_{DS(on)}$ = 1.65 m Ω at V_{GS} = 10 V, I_D = 32 A
- Max $r_{DS(on)} = 2.2 \text{ m}\Omega$ at $V_{GS} = 8 \text{ V}$, $I_D = 27 \text{ A}$
- Advanced Package and Silicon combination for low r_{DS(on)} and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

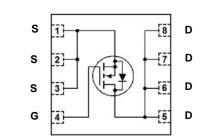


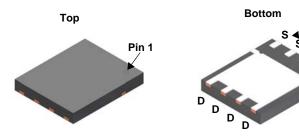
General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Applications

- Primary DC-DC MOSFET
- Secondary Synchronous Rectifier
- Load Switch





Power 56

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units	
V_{DS}	Drain to Source Voltage			60	V	
V_{GS}	Gate to Source Voltage			±20	V	
	Drain Current -Continuous	T _C = 25 °C	(Note 5)	234		
	-Continuous	T _C = 100 °C	(Note 5)	148		
ID	-Continuous	T _A = 25 °C	(Note 1a)	32	Α	
	-Pulsed		(Note 4)	1021		
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	937	mJ	
D	Power Dissipation	T _C = 25 °C		156	W	
P_{D}	Power Dissipation	T _A = 25 °C	(Note 1a)	2.7	VV	
T_J , T_{STG}	Operating and Storage Junction Temperature F	Range		-55 to +150	°C	

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	45	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86550	FDMS86550	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	60			V
ΔBV_{DSS} ΔT_{J}	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		31		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 48 V, V _{GS} = 0 V			1	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	2.5	3.3	4.5	V
$\Delta V_{GS(th)} \over \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		-12		mV/°C
		$V_{GS} = 10 \text{ V}, I_D = 32 \text{ A}$		1.4	1.65	
r _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 8 \text{ V}, I_D = 27 \text{ A}$		1.7	2.2	mΩ
, ,		$V_{GS} = 10 \text{ V}, I_D = 32 \text{ A}, T_J = 125 ^{\circ}\text{C}$		2.2	2.6	
g _{FS}	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_{D} = 32 \text{ A}$		96		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 20 V V 0 V		8235	11530	рF
C _{oss}	Output Capacitance	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz		2140	3000	pF
C _{rss}	Reverse Transfer Capacitance	1 = 1 1011 12		70	120	pF
R_g	Gate Resistance		0.1	0.9	2.7	Ω

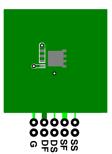
Switching Characteristics

t _{d(on)}	Turn-On Delay Time		43	69	ns
t _r	Rise Time	V _{DD} = 30 V, I _D = 32 A,	27	43	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	42	67	ns
t _f	Fall Time		11	20	ns
Qg	Total Gate Charge	V _{GS} = 0 V to 10 V	110	154	nC
Qg	Total Gate Charge	$V_{GS} = 0 \text{ V to 8 V} V_{DD} = 30 \text{ V},$	90	126	nC
Q_{gs}	Gate to Source Charge	I _D = 32 A	40		nC
Q_{gd}	Gate to Drain "Miller" Charge		20		nC

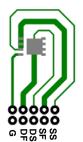
Drain-Source Diode Characteristics

V _{SD} Source to Drain Diode Forward Voltage	Source to Drain Diade Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2.1 \text{ A}$ (Note 2)	0.7	1.2	\/
	$V_{GS} = 0 \text{ V}, I_S = 32 \text{ A}$ (Note 2)	8.0	1.3	v	
t _{rr}	Reverse Recovery Time	I _E = 32 A. di/dt = 100 A/μs	68	109	ns
Q _{rr}	Reverse Recovery Charge	1F = 32 A, αι/αι = 100 A/μs	62	99	nC

^{1.} R_{0JA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0CA} is determined by the user's board design.



a. 45 °C/W when mounted on a 1 in² pad of 2 oz copper.



b. 115 °C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%.
- 3. E_{AS} of 937 mJ is based on starting $T_{J} = 25$ °C, L = 3 mH, $I_{AS} = 25$ A, $V_{DD} = 60$ V, $V_{GS} = 10$ V. 100% test at L = 0.1 mH, $I_{AS} = 79$ A.
- 4. Pulsed Id please refer to Fig 11 SOA graph for more details.
- 5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics T_J = 25 °C unless otherwise noted

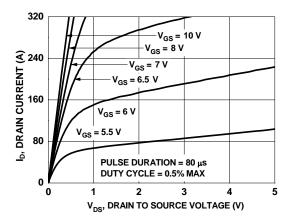


Figure 1. On-Region Characteristics

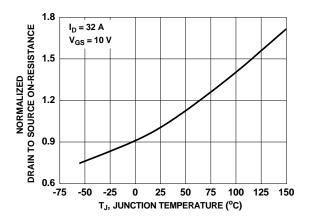


Figure 3. Normalized On-Resistance vs Junction Temperature

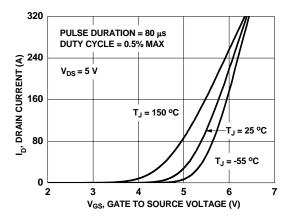


Figure 5. Transfer Characteristics

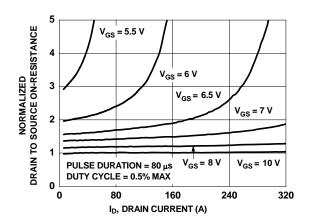


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

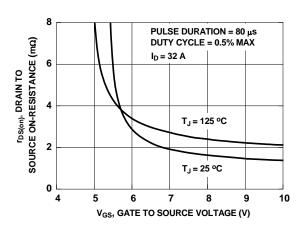


Figure 4. On-Resistance vs Gate to Source Voltage

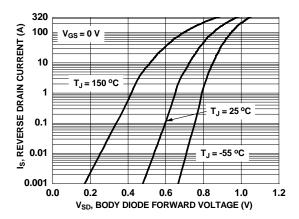


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

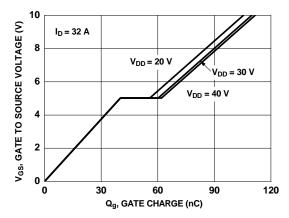


Figure 7. Gate Charge Characteristics

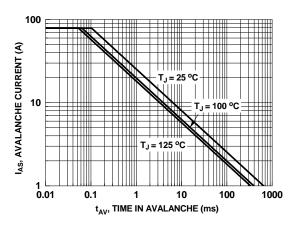


Figure 9. Unclamped Inductive Switching Capability

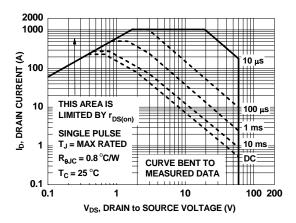


Figure 11. Forward Bias Safe Operating Area

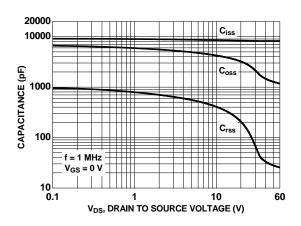


Figure 8. Capacitance vs Drain to Source Voltage

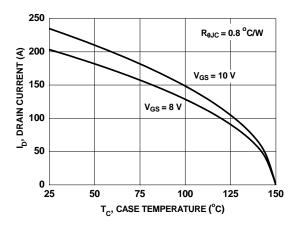


Figure 10. Maximum Continuous Drain Current vs Case Temperature

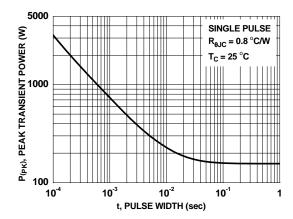


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

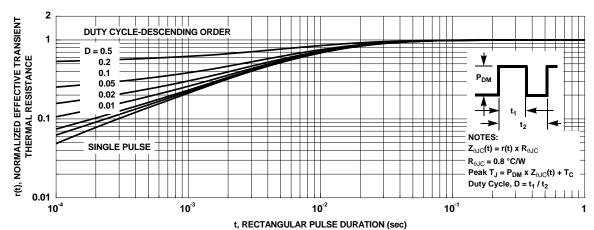
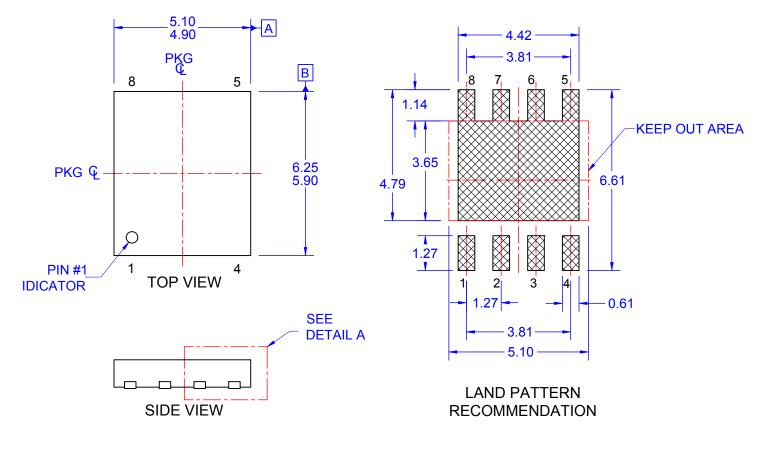
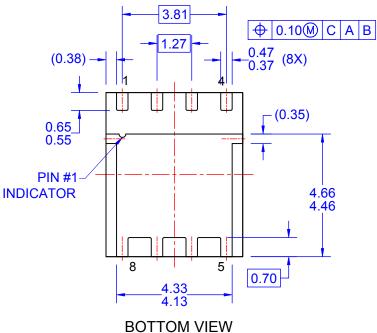
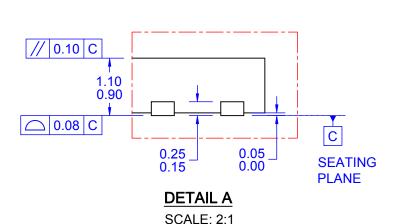


Figure 13. Transient Thermal Response Curve







NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
- F) DRAWING FILE NAME: PQFN08JREV3.



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