

74AHC00; 74AHCT00

Quad 2-input NAND gate

Rev. 5 — 26 May 2020

Product data sheet

1. General description

The 74AHC00; 74AHCT00 are quad 2-input NAND gates. Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

2. Features

- Wide supply voltage range from 2.0 V to 5.5 V
- Input levels:
 - For 74AHC00: CMOS level
 - For 74AHCT00: TTL level
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- ESD protection:
 - HBM EIA/JESD22-A114E exceeds 2000 V
 - MM EIA/JESD22-A115-A exceeds 200 V
 - CDM EIA/JESD22-C101C exceeds 1000 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | Version |
| 74AHC00D | -40 °C to +125 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74AHCT00D | | | | |
| 74AHC00PW | -40 °C to +125 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |
| 74AHCT00PW | | | | |
| 74AHC00BQ | -40 °C to +125 °C | DHVQFN14 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm | SOT762-1 |
| 74AHCT00BQ | | | | |

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|--------------|----------------|
| 1A, 2A, 3A, 4A | 1, 4, 9, 12 | data inputs |
| 1B, 2B, 3B, 4B | 2, 5, 10, 13 | data inputs |
| 1Y, 2Y, 3Y, 4Y | 3, 6, 8, 11 | data outputs |
| GND | 7 | ground (0 V) |
| V _{CC} | 14 | supply voltage |

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; X = don't care.

| Input | | Output |
|-------|----|--------|
| nA | nB | nY |
| L | X | H |
| X | L | H |
| H | H | L |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|------|------|------|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V |
| V_I | input voltage | | -0.5 | +7.0 | V |
| I_{IK} | input clamping current | $V_I < -0.5$ V [1] | -20 | - | mA |
| I_{OK} | output clamping current | $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1] | -20 | +20 | mA |
| I_O | output current | $V_O = -0.5$ V to $(V_{CC} + 0.5)$ V | -25 | +25 | mA |
| I_{CC} | supply current | | - | +75 | mA |
| I_{GND} | ground current | | -75 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40$ °C to +125 °C [2] | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 74AHC00 | | | 74AHCT00 | | | Unit |
|---------------------|-------------------------------------|------------------------------|---------|-----|----------|----------|-----|----------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V_{CC} | supply voltage | | 2.0 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | V |
| V_I | input voltage | | 0 | - | 5.5 | 0 | - | 5.5 | V |
| V_O | output voltage | | 0 | - | V_{CC} | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | +25 | +125 | -40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 3.3$ V \pm 0.3 V | - | - | 100 | - | - | - | ns/V |
| | | $V_{CC} = 5.0$ V \pm 0.5 V | - | - | 20 | - | - | 20 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|---------------------------|---|----------------|---|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74AHC00 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 3.0 V | 2.1 | - | - | 2.1 | - | 2.1 | - | V |
| | | V _{CC} = 5.5 V | 3.85 | - | - | 3.85 | - | 3.85 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 3.0 V | - | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | V _{CC} = 5.5 V | - | - | 1.65 | - | 1.65 | - | 1.65 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = -50 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = -50 μA; V _{CC} = 3.0 V | 2.9 | 3.0 | - | 2.9 | - | 2.9 | - | V |
| | | I _O = -50 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -4.0 mA; V _{CC} = 3.0 V | 2.58 | - | - | 2.48 | - | 2.40 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 50 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 50 μA; V _{CC} = 3.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 50 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 3.0 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| | | I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 2.0 | - | 20 | - |
| C _I | input capacitance | V _I = V _{CC} or GND | - | 3.0 | 10 | - | 10 | - | 10 | pF |
| 74AHCT00 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = -50 μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| V _{OL} | LOW-level output voltage | I _O = -8.0 mA | 3.94 | - | - | 3.80 | - | 3.70 | - | V |
| | | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| I _I | input leakage current | I _O = 50 μA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 8.0 mA | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 2.0 | - | 20 | - | 40 | μA |

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|---------------------------|--|-------|-----|------|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| ΔI_{CC} | additional supply current | per input pin; $V_I = V_{CC} - 2.1 \text{ V}$; $I_O = 0 \text{ A}$; other pins at V_{CC} or GND; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | - | - | 1.35 | - | 1.5 | - | 1.5 | mA |
| C_I | input capacitance | $V_I = V_{CC}$ or GND | - | 3.0 | 10 | - | 10 | - | 10 | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|-------------------------------|--|-------|--------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| 74AHC00 | | | | | | | | | | |
| t_{pd} | propagation delay | nA, nB to nY; see Fig. 6 [2] | | | | | | | | |
| | | $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ | | | | | | | | |
| | | $C_L = 15 \text{ pF}$ | - | 4.5 | 7.9 | 1.0 | 9.5 | 1.0 | 10.0 | ns |
| | | $C_L = 50 \text{ pF}$ | - | 6.0 | 11.4 | 1.0 | 13.0 | 1.0 | 14.5 | ns |
| | | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | | | | | | | | |
| | | $C_L = 15 \text{ pF}$ | - | 3.2 | 5.5 | 1.0 | 6.5 | 1.0 | 7.0 | ns |
| | | $C_L = 50 \text{ pF}$ | - | 4.5 | 7.5 | 1.0 | 8.5 | 1.0 | 9.5 | ns |
| C_{PD} | power dissipation capacitance | $C_L = 50 \text{ pF}$; $f_i = 1 \text{ MHz}$; $V_I = \text{GND to } V_{CC}$ [3] | - | 7.0 | - | - | - | - | - | pF |
| 74AHCT00 | | | | | | | | | | |
| t_{pd} | propagation delay | nA, nB to nY; see Fig. 6 [2] | | | | | | | | |
| | | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | | | | | | | | |
| | | $C_L = 15 \text{ pF}$ | - | 3.3 | 6.9 | 1.0 | 8.0 | 1.0 | 9.0 | ns |
| | | $C_L = 50 \text{ pF}$ | - | 4.5 | 7.9 | 1.0 | 9.0 | 1.0 | 10.0 | ns |
| C_{PD} | power dissipation capacitance | $C_L = 50 \text{ pF}$; $f_i = 1 \text{ MHz}$; $V_I = \text{GND to } V_{CC}$ [3] | - | 7.0 | - | - | - | - | - | pF |

[1] Typical values are measured at nominal supply voltage ($V_{CC} = 3.3 \text{ V}$ and $V_{CC} = 5.0 \text{ V}$).

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

10.1. Waveforms

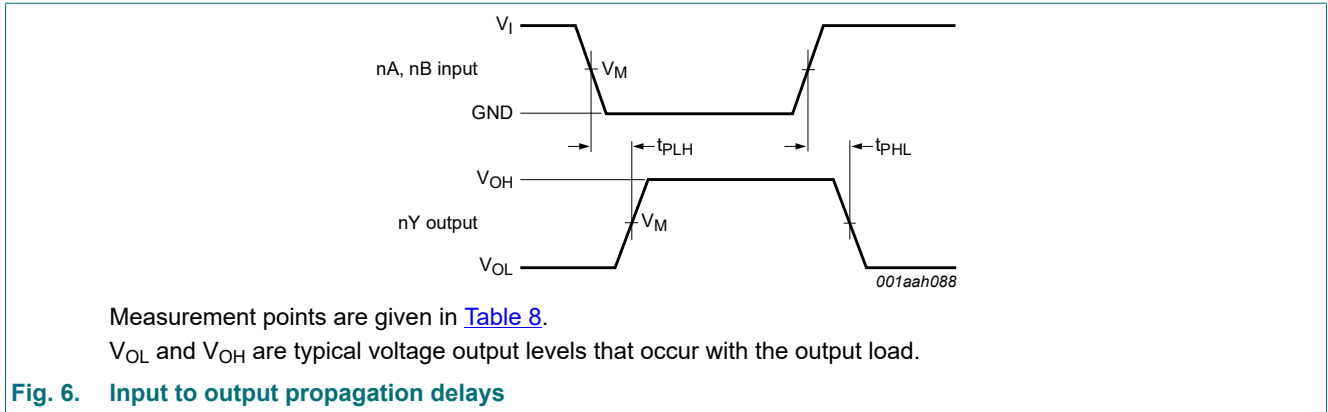


Table 8. Measurement points

| Type | Input | Output |
|----------|---------------------|---------------------|
| | V_M | V_M |
| 74AHC00 | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |
| 74AHCT00 | 1.5 V | $0.5 \times V_{CC}$ |

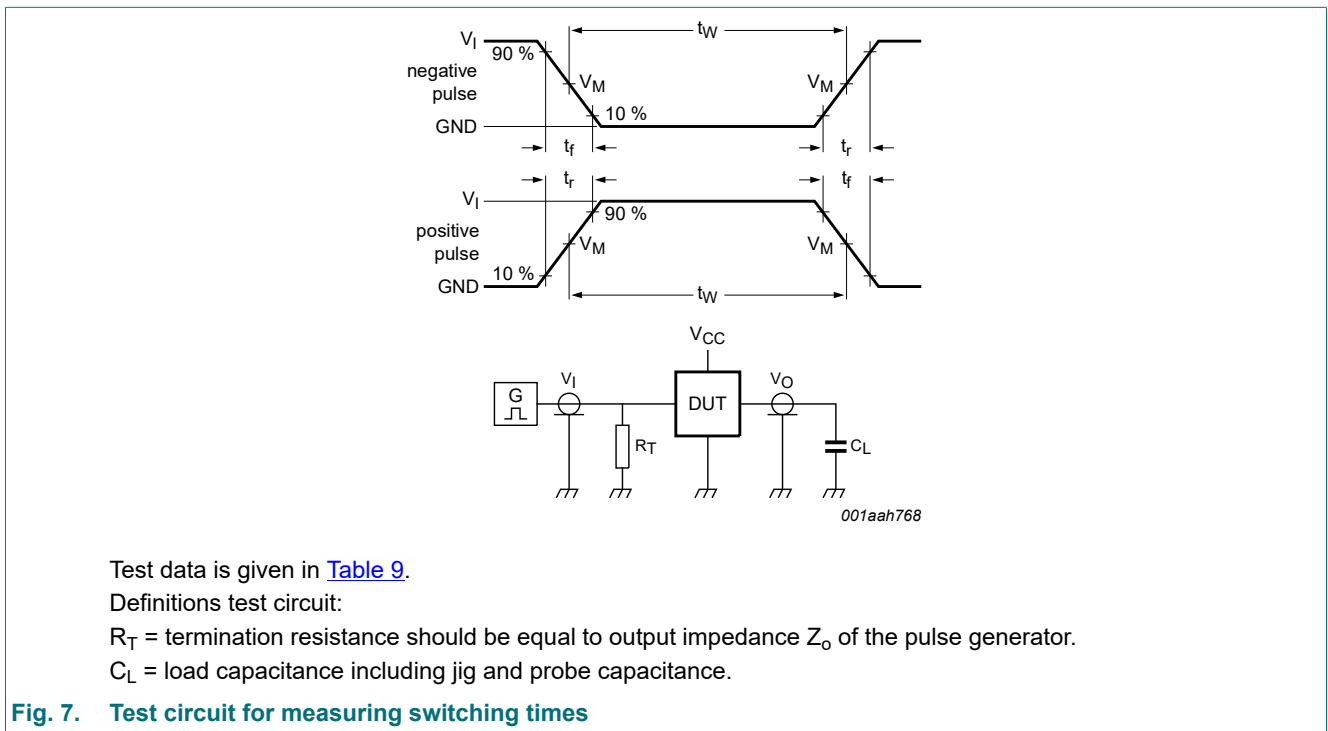


Table 9. Test data

| Type | Input | | Load | Test |
|----------|----------|---------------|--------------|--------------------|
| | V_I | t_r, t_f | C_L | |
| 74AHC00 | V_{CC} | ≤ 3.0 ns | 15 pF, 50 pF | t_{PLH}, t_{PHL} |
| 74AHCT00 | 3.0 V | ≤ 3.0 ns | 15 pF, 50 pF | t_{PLH}, t_{PHL} |

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Fig. 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



Fig. 9. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Fig. 10. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charge Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|------------------|---|-----------------------|---------------|------------------|
| 74AHC_AHCT00 v.5 | 20200526 | Product data sheet | - | 74AHC_AHCT00 v.4 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 1 and Section 2 updated. Table 4: Derating values for P_{tot} total power dissipation have been updated. Package outline drawing of SOT762-1 (Fig. 10) updated. | | | |
| 74AHC_AHCT00 v.4 | 20080428 | Product data sheet | - | 74AHC_AHCT00 v.3 |
| Modifications: | <ul style="list-style-type: none"> Table 6: the conditions for input leakage current have been changed. | | | |
| 74AHC_AHCT00 v.3 | 20080108 | Product data sheet | - | 74AHC_AHCT00 v.2 |
| 74AHC_AHCT00 v.2 | 19990923 | Product specification | - | 74AHC_AHCT00 v.1 |
| 74AHC_AHCT00 v.1 | 19981209 | Product specification | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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