

## Features

- Temperature ranges
  - Industrial: -40 °C to 85 °C
- Pin and function compatible with CY7C1041BV33
- High speed
  - $t_{AA} = 8 \text{ ns}$
- Low active power
  - 360 mW (max)
- 2.0 V data retention
- Automatic power down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Available in Pb-free 44-pin TSOP II package

## Functional Description

The CY7C1041CV33 is a high performance CMOS static RAM organized as 262,144 words by 16 bits.

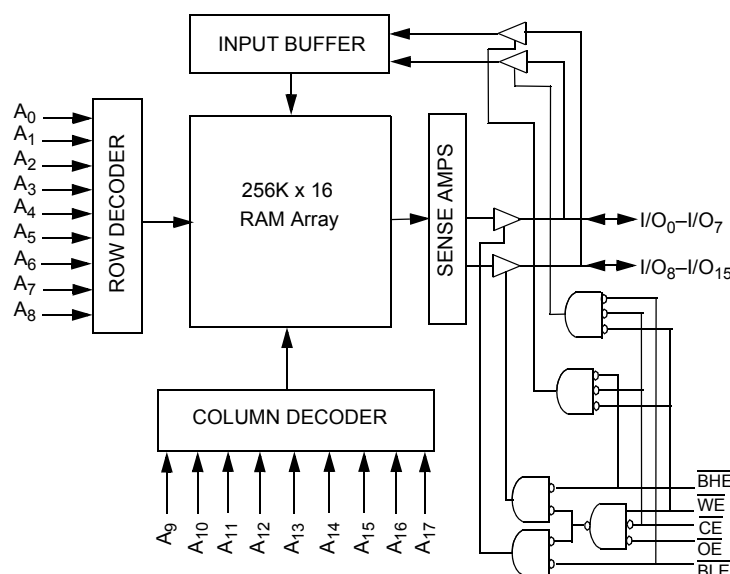
To write to the device, take Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{17}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from IO pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{17}$ ).

To read from the device, take Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on  $I/O_8$  to  $I/O_{15}$ . For more information, see the [Truth Table on page 10](#) for a complete description of Read and Write modes.

The input and output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

For a complete list of related documentation, click [here](#).

## Logic Block Diagram



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## Selection Guide

| Description                  | -8  | Unit |
|------------------------------|-----|------|
| Maximum Access Time          | 8   | ns   |
| Maximum Operating Current    | 100 | mA   |
| Maximum CMOS Standby Current | 10  | mA   |

## Pin Configurations

Figure 1. 44-pin TSOP II pinout (Top View) <sup>[1]</sup>

|                  |    |    |                   |
|------------------|----|----|-------------------|
| A <sub>0</sub>   | 1  | 44 | A <sub>17</sub>   |
| A <sub>1</sub>   | 2  | 43 | A <sub>16</sub>   |
| A <sub>2</sub>   | 3  | 42 | A <sub>15</sub>   |
| A <sub>3</sub>   | 4  | 41 | OE                |
| A <sub>4</sub>   | 5  | 40 | BHE               |
| CE               | 6  | 39 | BLE               |
| I/O <sub>0</sub> | 7  | 38 | I/O <sub>15</sub> |
| I/O <sub>1</sub> | 8  | 37 | I/O <sub>14</sub> |
| I/O <sub>2</sub> | 9  | 36 | I/O <sub>13</sub> |
| I/O <sub>3</sub> | 10 | 35 | I/O <sub>12</sub> |
| V <sub>CC</sub>  | 11 | 34 | V <sub>SS</sub>   |
| V <sub>SS</sub>  | 12 | 33 | V <sub>CC</sub>   |
| I/O <sub>4</sub> | 13 | 32 | I/O <sub>11</sub> |
| I/O <sub>5</sub> | 14 | 31 | I/O <sub>10</sub> |
| I/O <sub>6</sub> | 15 | 30 | I/O <sub>9</sub>  |
| I/O <sub>7</sub> | 16 | 29 | I/O <sub>8</sub>  |
| WE               | 17 | 28 | NC                |
| A <sub>5</sub>   | 18 | 27 | A <sub>14</sub>   |
| A <sub>6</sub>   | 19 | 26 | A <sub>13</sub>   |
| A <sub>7</sub>   | 20 | 25 | A <sub>12</sub>   |
| A <sub>8</sub>   | 21 | 24 | A <sub>11</sub>   |
| A <sub>9</sub>   | 22 | 23 | A <sub>10</sub>   |

### Note

1. NC pins are not connected on the die.

## Pin Definitions

| Pin Name                                       | TSOP Pin Number           | I/O Type         | Description   |
|--|---------------------------|------------------|---|
| A <sub>0</sub> –A <sub>17</sub>                | 1–5, 18–27, 42–44         | Input            | <b>Address Inputs.</b> Used to select one of the address locations.   |
| I/O <sub>0</sub> –I/O <sub>15</sub>            | 7–10, 13–16, 29–32, 35–38 | Input or Output  | <b>Bidirectional Data IO lines.</b> Used as input or output lines depending on operation.   |
| NC   | 28                        | No Connect       | <b>No Connects.</b> Not connected to the die.   |
| $\overline{\text{WE}}$                         | 17                        | Input or Control | <b>Write Enable Input, Active LOW.</b> When selected LOW, a write is conducted. When deselected HIGH, a read is conducted.  |
| $\overline{\text{CE}}$                         | 6                         | Input or Control | <b>Chip Enable Input, Active LOW.</b> When LOW, selects the chip. When HIGH, deselects the chip.  |
| $\overline{\text{BHE}}, \overline{\text{BLE}}$ | 40, 39                    | Input or Control | <b>Byte Write Select Inputs, Active LOW.</b> $\overline{\text{BHE}}$ controls I/O <sub>15</sub> –I/O <sub>8</sub> , $\overline{\text{BLE}}$ controls I/O <sub>7</sub> –I/O <sub>0</sub> .                       |
| $\overline{\text{OE}}$                         | 41                        | Input or Control | <b>Output Enable, Active LOW.</b> Controls the direction of the I/O pins. When LOW, the IO pins are allowed to behave as outputs. When deasserted HIGH, the I/O pins are tri-stated and act as input data pins. |
| V <sub>SS</sub>                                | 12, 34                    | Ground           | <b>Ground for the Device.</b> Connected to ground of the system.  |
| V <sub>CC</sub>                                | 11, 33                    | Power Supply     | <b>Power Supply Inputs to the Device.</b>   |

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65 °C to +150 °C

Ambient Temperature with  
Power Applied ..... -55 °C to +125 °C

Supply Voltage  
on  $V_{CC}$  Relative to GND <sup>[2]</sup> ..... -0.5 V to +4.6 V

DC Voltage Applied to Outputs  
in High Z State <sup>[2]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC Input Voltage <sup>[2]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage  
(MIL-STD-883, Method 3015) ..... > 2001 V

Latch Up Current ..... > 200 mA

## Operating Range

| Range      | Ambient Temperature ( $T_A$ ) | $V_{CC}$        |
|------------|-------------------------------|-----------------|
| Industrial | -40 °C to +85 °C              | 3.3 V $\pm$ 10% |

## Electrical Characteristics

Over the Operating Range

| Parameter               | Description                                      | Test Conditions   | -8   |                | Unit          |
|-------------------------|--|---|------|----------------|---------------|
|                         |  |   | Min  | Max            |               |
| $V_{OH}$                | Output HIGH Voltage                              | $V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$   | 2.4  | –              | V             |
| $V_{OL}$                | Output LOW Voltage                               | $V_{CC} = \text{Min}, I_{OL} = 8.0 \text{ mA}$  | –    | 0.4            | V             |
| $V_{IH}$                | Input HIGH Voltage                               |   | 2.0  | $V_{CC} + 0.3$ | V             |
| $V_{IL}$ <sup>[2]</sup> | Input LOW Voltage                                |   | -0.3 | 0.8            | V             |
| $I_{IX}$                | Input Leakage Current                            | $GND \leq V_I \leq V_{CC}$  | -1   | +1             | $\mu\text{A}$ |
| $I_{OZ}$                | Output Leakage Current                           | $GND \leq V_{OUT} \leq V_{CC}$ , Output disabled  | -1   | +1             | $\mu\text{A}$ |
| $I_{CC}$                | $V_{CC}$ Operating Supply Current                | $V_{CC} = \text{Max}, f = f_{MAX} = 1/t_{RC}$   | –    | 100            | mA            |
| $I_{SB1}$               | Automatic CE Power Down<br>Current – TTL Inputs  | Max $V_{CC}$ , $\overline{CE} \geq V_{IH}$ ,<br>$V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$                                    | –    | 40             | mA            |
| $I_{SB2}$               | Automatic CE Power Down<br>Current – CMOS Inputs | Max $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3 \text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.3 \text{ V}$ , or $V_{IN} \leq 0.3 \text{ V}$ , $f = 0$ | –    | 10             | mA            |

### Note

2.  $V_{IL}(\text{min}) = -2.0 \text{ V}$  and  $V_{IH}(\text{max}) = V_{CC} + 0.5 \text{ V}$  for pulse durations of less than 20 ns.

## Capacitance

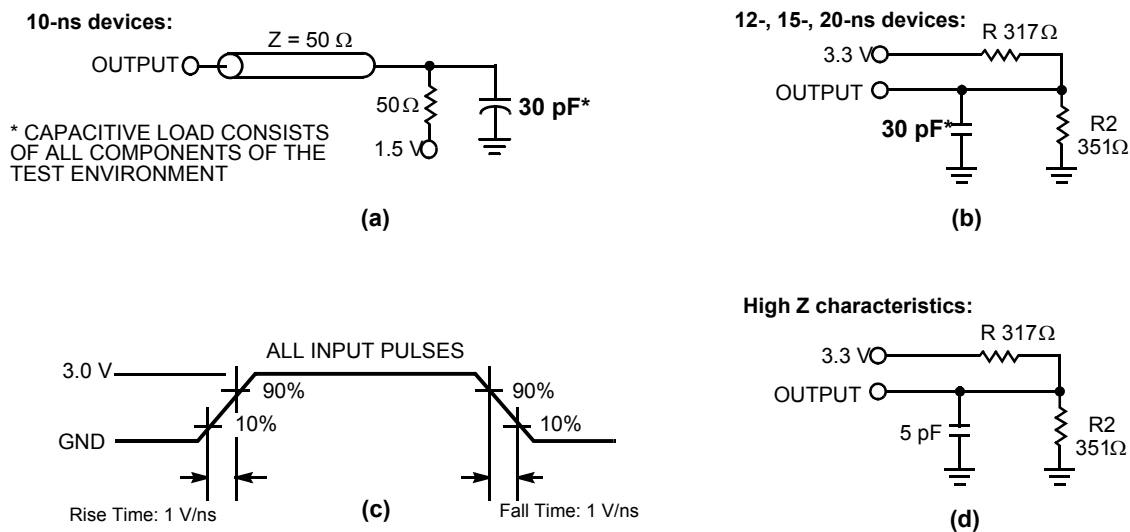
| Parameter <sup>[3]</sup> | Description        | Test Conditions   | Max | Unit |
|--------------------------|--------------------|---|-----|------|
| $C_{IN}$                 | Input Capacitance  | $T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 3.3\text{ V}$ | 8   | pF   |
| $C_{OUT}$                | Output Capacitance |   | 8   | pF   |

## Thermal Resistance

| Parameter <sup>[3]</sup> | Description                              | Test Conditions   | TSOP II | Unit               |
|--------------------------|--|---|---------|--------------------|
| $\Theta_{JA}$            | Thermal Resistance (Junction to Ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51 | 42.96   | $^\circ\text{C/W}$ |
| $\Theta_{JC}$            | Thermal Resistance (Junction to Case)    |   | 10.75   | $^\circ\text{C/W}$ |

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms <sup>[4]</sup>



### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High Z) for 10-ns parts are tested using the load conditions shown in Figure 2 (a). All other speeds are tested using the Thevenin load shown in Figure 2 (b). High Z characteristics are tested for all speeds using the test load shown in Figure 2 (d).

## Switching Characteristics

Over the Operating Range

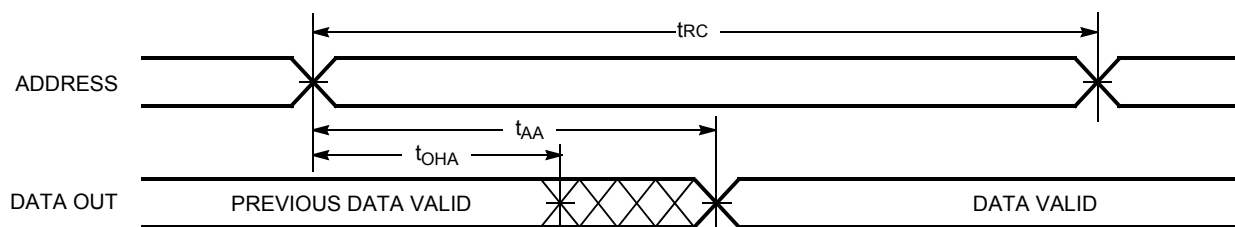
| Parameter <sup>[5]</sup>          | Description   | -8  |     | Unit |
|-----------------------------------|---|-----|-----|------|
|                                   |   | Min | Max |      |
| Read Cycle                        |   |     |     |      |
| t <sub>power</sub> <sup>[6]</sup> | V <sub>CC</sub> (Typical) to the First Access           | 100 | —   | μs   |
| t <sub>RC</sub>                   | Read Cycle Time   | 8   | —   | ns   |
| t <sub>AA</sub>                   | Address to Data Valid                                   | —   | 8   | ns   |
| t <sub>OHA</sub>                  | Data Hold from Address Change                           | 3   | —   | ns   |
| t <sub>ACE</sub>                  | $\overline{\text{CE}}$ LOW to Data Valid                | —   | 8   | ns   |
| t <sub>DOE</sub>                  | $\overline{\text{OE}}$ LOW to Data Valid                | —   | 5   | ns   |
| t <sub>LZOE</sub>                 | $\overline{\text{OE}}$ LOW to Low Z <sup>[7]</sup>      | 0   | —   | ns   |
| t <sub>HZOE</sub>                 | $\overline{\text{OE}}$ HIGH to High Z <sup>[7, 8]</sup> | —   | 4   | ns   |
| t <sub>LZCE</sub>                 | $\overline{\text{CE}}$ LOW to Low Z <sup>[7]</sup>      | 3   | —   | ns   |
| t <sub>HZCE</sub>                 | $\overline{\text{CE}}$ HIGH to High Z <sup>[7, 8]</sup> | —   | 4   | ns   |
| t <sub>PU</sub>                   | $\overline{\text{CE}}$ LOW to Power Up                  | 0   | —   | ns   |
| t <sub>PD</sub>                   | $\overline{\text{CE}}$ HIGH to Power Down               | —   | 8   | ns   |
| t <sub>DBE</sub>                  | Byte Enable to Data Valid                               | —   | 5   | ns   |
| t <sub>LZBE</sub>                 | Byte Enable to Low Z                                    | 0   | —   | ns   |
| t <sub>HZBE</sub>                 | Byte Disable to High Z                                  | —   | 5   | ns   |
| Write Cycle <sup>[9, 10]</sup>    |   |     |     |      |
| t <sub>WC</sub>                   | Write Cycle Time  | 8   | —   | ns   |
| t <sub>SCE</sub>                  | $\overline{\text{CE}}$ LOW to Write End                 | 6   | —   | ns   |
| t <sub>AW</sub>                   | Address Setup to Write End                              | 6   | —   | ns   |
| t <sub>HA</sub>                   | Address Hold from Write End                             | 0   | —   | ns   |
| t <sub>SA</sub>                   | Address Setup to Write Start                            | 0   | —   | ns   |
| t <sub>PWE</sub>                  | $\overline{\text{WE}}$ Pulse Width                      | 6   | —   | ns   |
| t <sub>SD</sub>                   | Data Setup to Write End                                 | 4   | —   | ns   |
| t <sub>HD</sub>                   | Data Hold from Write End                                | 0   | —   | ns   |
| t <sub>LZWE</sub>                 | $\overline{\text{WE}}$ HIGH to Low Z <sup>[7]</sup>     | 3   | —   | ns   |
| t <sub>HZWE</sub>                 | $\overline{\text{WE}}$ LOW to High Z <sup>[7, 8]</sup>  | —   | 4   | ns   |
| t <sub>BW</sub>                   | Byte Enable to End of Write                             | 6   | —   | ns   |

### Notes

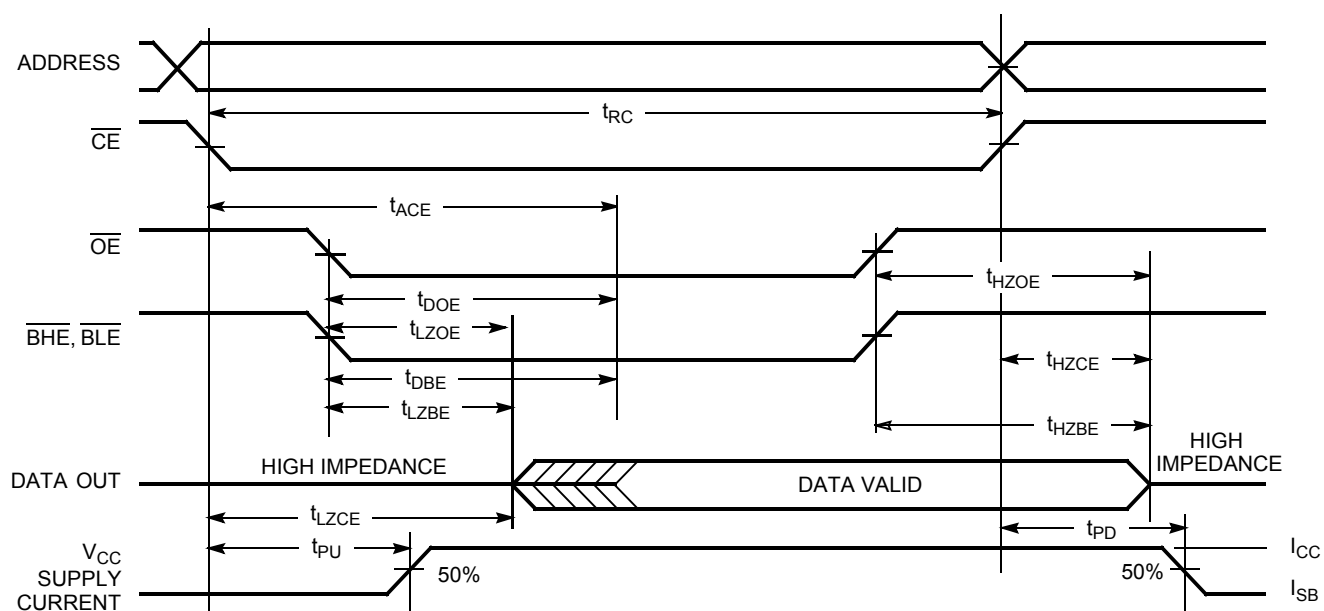
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.
- $t_{\text{POWER}}$  gives the minimum amount of time that the power supply is at typical  $V_{\text{CC}}$  values until the first memory access is performed.
- At any temperature and voltage condition,  $t_{\text{HZCE}}$  is less than  $t_{\text{LZCE}}$ ,  $t_{\text{HZBE}}$  is less than  $t_{\text{LZBE}}$ ,  $t_{\text{HZOE}}$  is less than  $t_{\text{LZOE}}$ , and  $t_{\text{HZWE}}$  is less than  $t_{\text{LZWE}}$  for any device.
- $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ ,  $t_{\text{HZBE}}$ , and  $t_{\text{HZWE}}$  are specified with a load capacitance of 5 pF as in part (d) of [Figure 2 on page 6](#). Transition is measured  $\pm 500$  mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW,  $\overline{\text{WE}}$  LOW, and  $\overline{\text{BHE/BL}}\overline{\text{E}}$  LOW.  $\overline{\text{CE}}$ ,  $\overline{\text{WE}}$ , and  $\overline{\text{BHE/BL}}\overline{\text{E}}$  must be LOW to initiate a write. The transition of these signals terminate the write. The input data setup and hold timing is referenced to the leading edge of the signal that terminates the write.
- The minimum Write cycle time for Write Cycle No. 3 (WE Controlled, OE LOW) is the sum of  $t_{\text{SD}}$  and  $t_{\text{HZWE}}$ .

## Switching Waveforms

**Figure 3. Read Cycle No. 1 (Address Transition Controlled)** [11, 12]



**Figure 4. Read Cycle No. 2 ( $\overline{OE}$  Controlled)** [12, 13]

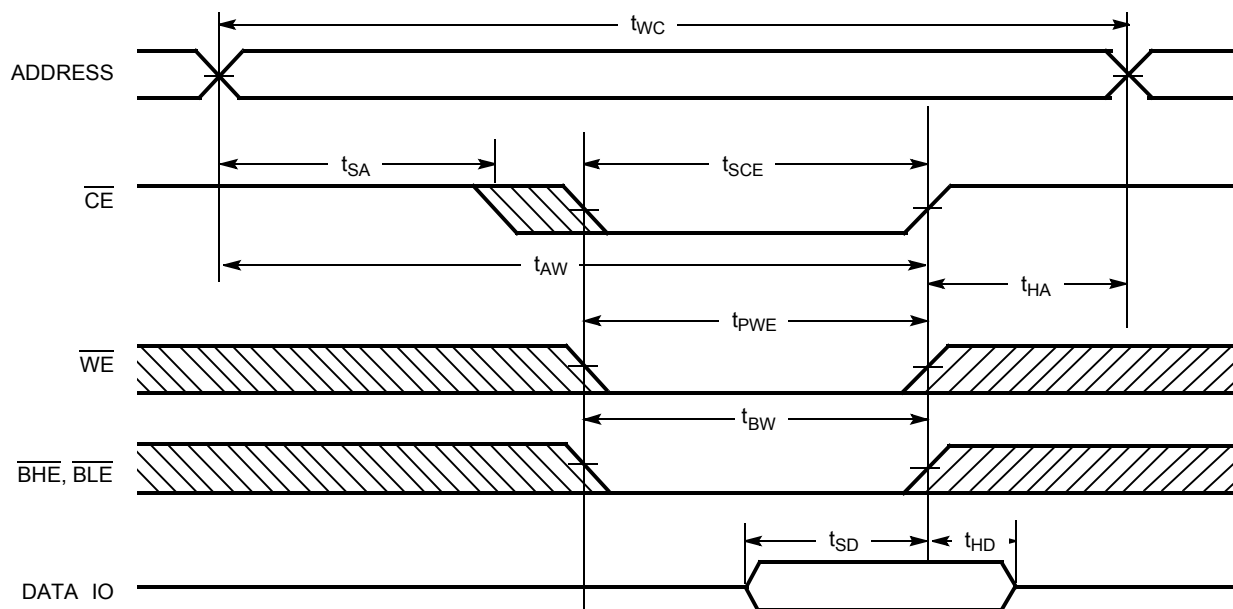
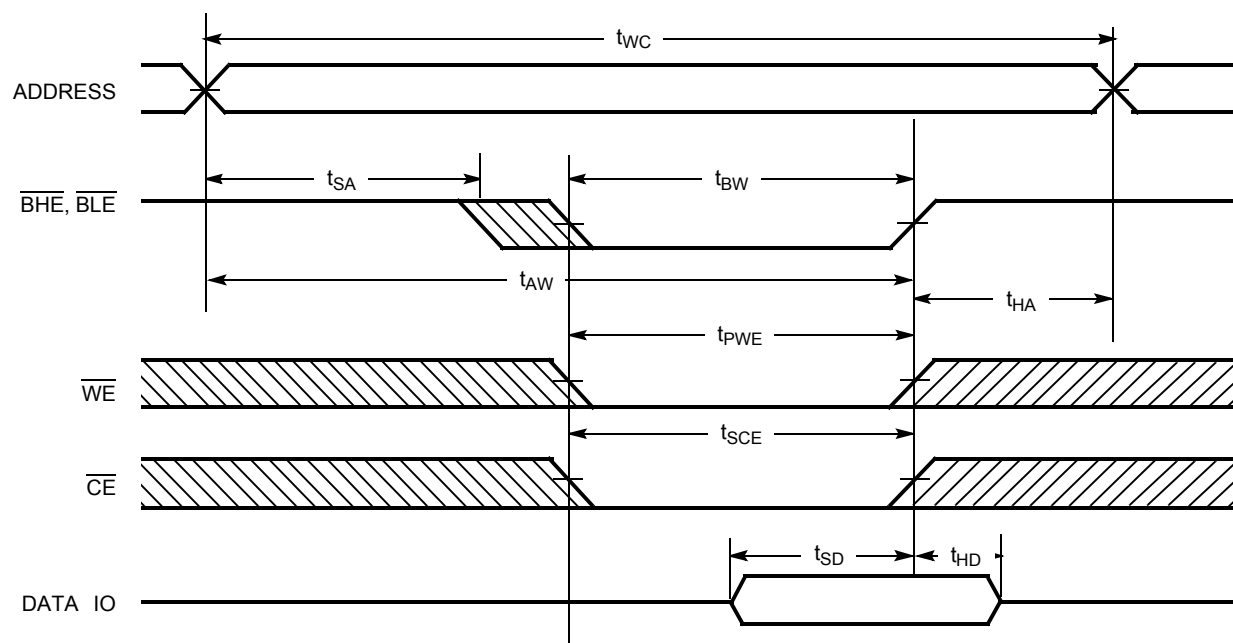


### Notes

11. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$ , and/or  $\overline{BLE}$  =  $V_{IL}$ .
12.  $\overline{WE}$  is HIGH for read cycle.
13. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

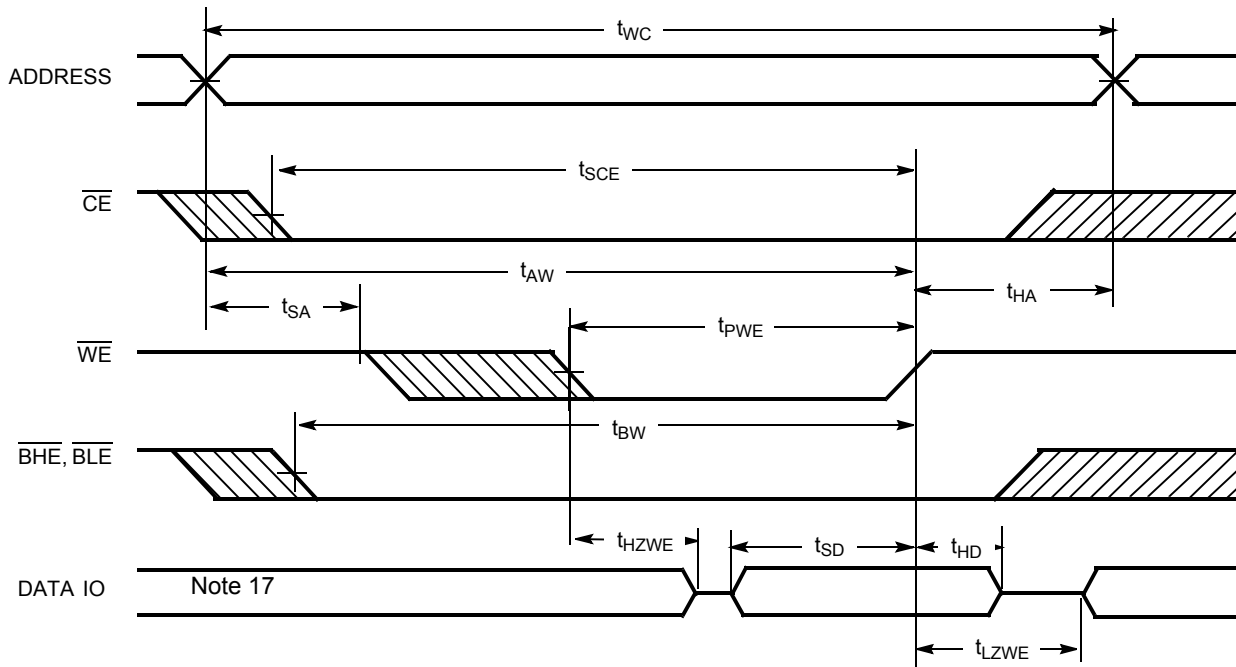


**Switching Waveforms** (continued)

**Figure 5. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)** [14, 15]

**Figure 6. Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**

**Notes**

 14. Data IO is high impedance if  $\overline{\text{OE}}$ ,  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{IH}$ .

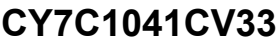
 15. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high impedance state.

**Switching Waveforms** *(continued)*
**Figure 7. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) <sup>[16]</sup>**

**Notes**

16. The minimum write cycle pulse width should be equal to the sum of  $t_{SD}$  and  $t_{HZWE}$ .
17. During this time I/Os are in output state. Do not apply input signal.

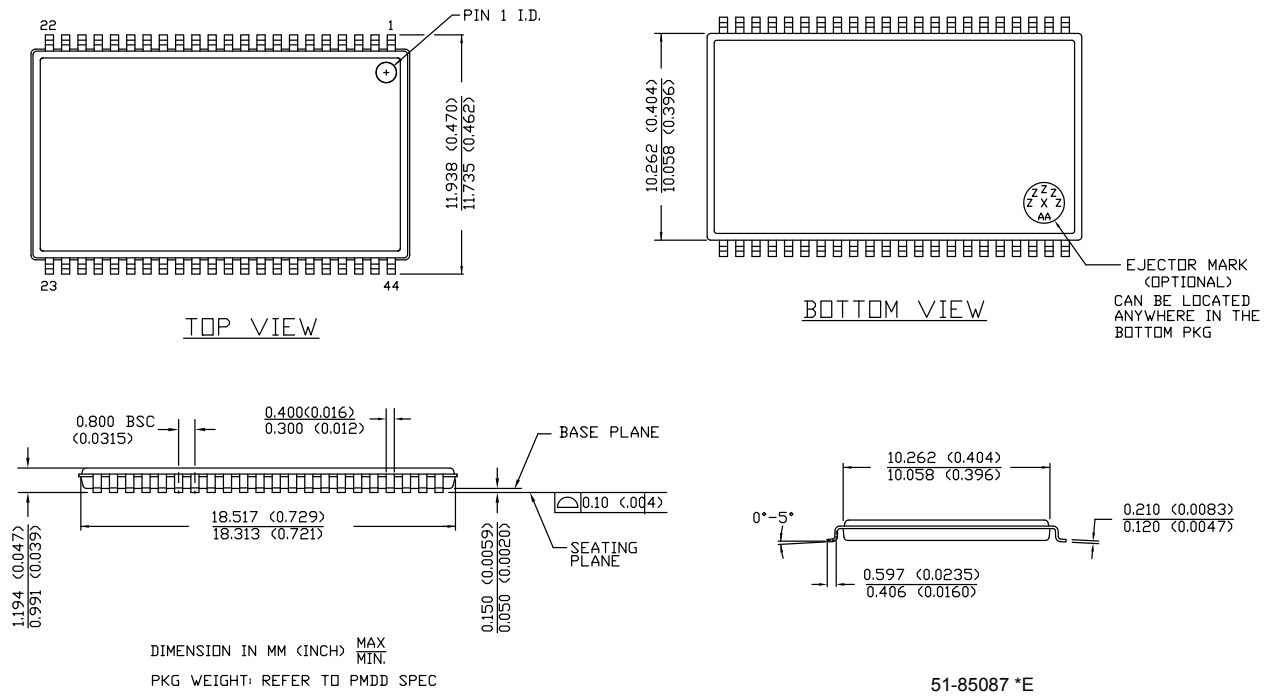
## Truth Table

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{BLE}$ | $\overline{BHE}$ | I/O <sub>0</sub> –I/O <sub>7</sub> | I/O <sub>8</sub> –I/O <sub>15</sub> | Mode                       | Power                      |
|-----------------|-----------------|-----------------|------------------|------------------|------------------------------------|-------------------------------------|----------------------------|----------------------------|
| H               | X               | X               | X                | X                | High Z                             | High Z                              | Power Down                 | Standby (I <sub>SB</sub> ) |
| L               | L               | H               | L                | L                | Data Out                           | Data Out                            | Read – All Bits            | Active (I <sub>CC</sub> )  |
|                 |                 |                 | L                | H                | Data Out                           | High Z                              | Read – Lower Bits Only     | Active (I <sub>CC</sub> )  |
|                 |                 |                 | H                | L                | High Z                             | Data Out                            | Read – Upper Bits Only     | Active (I <sub>CC</sub> )  |
| L               | X               | L               | L                | L                | Data In                            | Data In                             | Write – All Bits           | Active (I <sub>CC</sub> )  |
|                 |                 |                 | L                | H                | Data In                            | High Z                              | Write – Lower Bits Only    | Active (I <sub>CC</sub> )  |
|                 |                 |                 | H                | L                | High Z                             | Data In                             | Write – Upper Bits Only    | Active (I <sub>CC</sub> )  |
| L               | H               | H               | X                | X                | High Z                             | High Z                              | Selected, Outputs Disabled | Active (I <sub>CC</sub> )  |
| L               | X               | X               | H                | H                | High Z                             | High Z                              | Selected, Outputs Disabled | Active (I <sub>CC</sub> )  |



## Package Diagram

Figure 8. 44-pin TSOP Z44-II Package Outline, 51-85087



## Acronyms

| Acronym                | Description                             |
|------------------------|---|
| $\overline{\text{CE}}$ | Chip Enable                             |
| CMOS                   | Complementary Metal Oxide Semiconductor |
| I/O                    | Input/Output                            |
| $\overline{\text{OE}}$ | Output Enable                           |
| SRAM                   | Static Random Access Memory             |
| TSOP                   | Thin Small Outline Package              |
| TTL                    | Transistor-Transistor Logic             |
| $\overline{\text{WE}}$ | Write Enable                            |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celsius  |
| MHz    | megahertz       |
| μA     | microampere     |
| μs     | microsecond     |
| mA     | milliampere     |
| mm     | millimeter      |
| ms     | millisecond     |
| mW     | milliwatt       |
| ns     | nanosecond      |
| Ω      | ohm             |
| %      | percent         |
| pF     | picofarad       |
| V      | volt            |
| W      | watt            |

## Document History Page

| Document Title: CY7C1041CV33, 4-Mbit (256 K × 16) Static RAM<br>Document Number: 38-05134 |         |            |                 |  |
|---|---------|------------|-----------------|--|
| Rev.  | ECN No. | Issue Date | Orig. of Change | Description of Change  |
| **  | 109513  | 12/13/01   | HGK             | New data sheet   |
| *A  | 112440  | 12/20/01   | BSS             | Updated 51-85106 from revision *A to *C  |
| *B  | 112859  | 03/25/02   | DFP             | Added CY7C1042CV33 in BGA package<br>Removed 1042 BGA option pin ACC Final Data Sheet  |
| *C  | 116477  | 09/16/02   | CEA             | Add applications foot note to data sheet   |
| *D  | 119797  | 10/21/02   | DFP             | Added 20-ns speed bin  |
| *E  | 262949  | See ECN    | RKF             | 1) Added Lead (Pb)-Free parts in the Ordering info (Page #9)<br>2) Added Automotive Specs to Datasheet   |
| *F  | 361795  | See ECN    | SYT             | Added Pb-Free offerings in the Ordering Information  |
| *G  | 435387  | See ECN    | NXR             | Removed -8 Speed bin from Product offering.<br>Corrected typo in description for BHE/BLE in pin definitions table on Page# 3 corrected their Pin name from OE2 to OE.<br>Included the Maximum Ratings for Static Discharge Voltage and Latch up Current.<br>Changed the description of I <sub>IX</sub> current from Input Load Current to Input Leakage Current<br>Added note# 4 on page# 4<br>Updated the Ordering Information table  |
| *H  | 499153  | See ECN    | NXR             | Added Automotive-A Operating Range<br>Changed t <sub>power</sub> value from 1 μs to 100 μs<br>Updated Ordering Information table   |
| *I  | 2104110 | See ECN    | VKN/AESA        | Added Automotive-E specs for 12 ns speed<br>Updated Ordering Information table   |
| *J  | 2897141 | 03/22/10   | AJU/VIVG        | Updated <a href="#">Ordering Information</a> (Removed inactive parts).<br>Updated <a href="#">Package Diagram</a> .  |
| *K  | 3072834 | 11/12/2010 | PRAS            | Updated <a href="#">Ordering Information</a> :<br>Removed inactive parts.<br>Added <a href="#">Ordering Code Definitions</a> .   |
| *L  | 3186840 | 03/03/2011 | PRAS            | Updated <a href="#">Features</a> .<br>Updated <a href="#">Selection Guide</a> (Added -8 ns speed grade devices and removed -10 ns, -12 ns, -15 ns and -20 ns speed grade devices).<br>Removed Figure "48-Ball FBGA Pinout (Top View)" and renamed Figure "44-Pin SOJ/TSOP II (Top View)" as "44-pin TSOP II (Top View)" in <a href="#">Pin Configurations</a> .<br>Updated <a href="#">Pin Definitions</a> (Deleted the column "BGA Pin Number" and renamed the column "SOJ, TSOP Pin Number" as "TSOP Pin Number".<br>Updated <a href="#">Operating Range</a><br>Updated <a href="#">Electrical Characteristics</a> (Added -8 ns speed grade devices and removed -10 ns, -12 ns, -15 ns and -20 ns speed grade devices).<br>Updated <a href="#">Thermal Resistance</a> (Deleted the columns SOJ and FBGA).<br>Updated <a href="#">Switching Characteristics</a> (Added -8 ns speed grade devices and removed -10 ns, -12 ns, -15 ns and -20 ns speed grade devices).<br>Updated <a href="#">Ordering Information</a> (Added new speed bin (-8 ns speed grade devices) and removed -10 ns, -12 ns, -15 ns and -20 ns speed grade devices).<br>Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> .<br>Dislodged Automotive information to new datasheet (001-67307)<br>Removed SOJ and FBGA package related information in all instances in the document.<br>Updated to new template. |

**Document History Page** *(continued)*

| Document Title: CY7C1041CV33, 4-Mbit (256 K × 16) Static RAM<br>Document Number: 38-05134 |         |            |                 |  |
|---|---------|------------|-----------------|--|
| Rev.  | ECN No. | Issue Date | Orig. of Change | Description of Change  |
| *M  | 3199948 | 03/18/2011 | PRAS            | Updated <a href="#">Features</a> (Updated Operating Temperature Range from Commercial to Industrial).<br>Updated <a href="#">Operating Range</a> (Updated Operating Temperature Range from Commercial to Industrial).<br>Updated <a href="#">Ordering Information</a> (Updated Operating Temperature Range from Commercial to Industrial). |
| *N  | 3266084 | 05/28/2011 | PRAS            | Updated <a href="#">Functional Description</a> (Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.").   |
| *O  | 4315741 | 03/20/2014 | VINI            | Updated <a href="#">Package Diagram</a> :<br>spec 51-85087 – Changed revision from *C to *E.<br>Updated to new template.<br>Completing Sunset Review.  |
| *P  | 4578447 | 01/16/2015 | VINI            | Added related documentation hyperlink in page 1.<br>Updated <a href="#">Switching Waveforms</a> :<br>Added Note <a href="#">16</a> and referred the same note in <a href="#">Figure 7</a> .  |
| *Q  | 4702949 | 03/27/2015 | VINI            | Updated <a href="#">Switching Waveforms</a> :<br>Added Note <a href="#">17</a> and referred the same note in DATA IO in <a href="#">Figure 7</a> .<br>Completing Sunset Review.  |
| *R  | 5962455 | 11/09/2017 | AESATMP8        | Updated logo and Copyright.  |



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