

FEATURES

Amplitude settling time: 200 ns
Wideband rejection: ≥ 35 dB
Single-chip replacement for mechanically tuned designs
RoHS compliant, 32-lead, 5 mm \times 5 mm LFCSP package

APPLICATIONS

Testing and measurement equipment
**Military radar and electronic warfare/electronic counter
measures (ECMs)**
Satellite communication and space
Industrial and medical equipment

GENERAL DESCRIPTION

The HMC882A is a monolithic microwave integrated circuit (MMIC) low-pass filter that features a user-selectable cutoff frequency (f_{3dB}). The cutoff frequency can be varied from 3.95 GHz to 6.9 GHz by applying a single analog tuning voltage between 0 V and 14 V. This low-pass filter provides a low 3 dB insertion loss, 13 dB return loss, and >20 dB stopband attenuation at $1.28 \times f_{3dB}$ GHz. This tunable filter can be used as a much

smaller alternative to physically large switched filter banks and cavity tuned filters. The HMC882A has excellent microphonics due to the monolithic design and low residual phase noise of -165 dBc/Hz, and provides a dynamically adjustable solution in advanced communications applications. The low-pass tunable filter is packaged in a RoHS compliant, 5 mm \times 5mm LFCSP package.

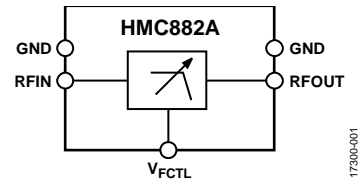
FUNCTIONAL BLOCKDIAGRAM

Figure 1.

TABLE OF CONTENTS

Features	1	Typical Performance Characteristics	6
Applications.....	1	Theory of Operation	9
Functional BlockDiagram	1	Applications Information	10
General Description	1	Typical Application Circuit.....	10
Revision History	2	Evaluation Printed Circuit Board (PCB).....	10
Specifications.....	3	Outline Dimensions	11
Absolute Maximum Ratings.....	4	Ordering Guide	11
ESD Caution.....	4		
Pin Configuration and Function Descriptions.....	5		

REVISION HISTORY

2/2019—Revision 0: Initial Version

SPECIFICATIONS

$T_A = 25^\circ\text{C}$, with cutoff frequency control voltage (V_{FCTL}) varying from 0 V to 14 V, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE					
Passband	0		6.9	GHz	
Cutoff Frequency ($f_{3\text{dB}}$)	3.95		6.9	GHz	
REJECTION					
Stopband Frequency		$1.28 \times f_{3\text{dB}}$		GHz	≥ 20 dB
Re-Entry Frequency		≥ 30		GHz	≥ 35 dB wideband rejection
LOSS					
Insertion Loss		3		dB	
Return Loss		13		dB	
DYNAMIC PERFORMANCE					
Maximum Input Power for Linear Operation			10	dBm	
Input Third-Order Intercept		41		dBm	Input power (P_{IN}) = 20 dBm, two-tone
Group Delay		0.4		ns	
Amplitude Settling		200		ns	Time to settle to minimum insertion loss, within ≤ 0.5 dB of static insertion loss
Drift Rate		0.3		MHz/ $^\circ\text{C}$	
RESIDUAL PHASE NOISE					
1 MHz Offset		-165		dBc/Hz	
TUNING					
Voltage (V_{FCTL})	0		14	V	
Cutoff Frequency Control Current (I_{FCTL})			± 1	μA	Rated current for pin

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Tuning	
Voltage (V_{FCTL})	-0.5 V to +15 V
Current (I_{FCTL})	± 1 mA
RF Input Power	27 dBm
Temperature	
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature for 1 Million Mean Time to Failure (MTTF)	175°C
Nominal Junction Temperature (Exposed Pad Temperature, $T_{EPAD} = 85^\circ\text{C}$, $P_{IN} = 10$ dBm)	90
Electrostatic Discharge (ESD) Rating	
Human Body Model (HBM)	1000 V
Field Induced Charge Device Model (FICDM)	1250 V
Moisture Sensitivity Level (MSL) Rating	MSL3

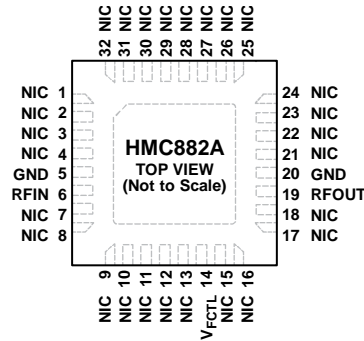
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES**
1. NIC = NOT INTERNALLY CONNECTED. ALL DATA SHOWN HEREIN WAS MEASURED WITH THESE PINS CONNECTED TO RF AND DC GROUND EXTERNALLY.
 2. EXPOSED PAD. THE PACKAGE BOTTOM HAS AN EXPOSED PAD THAT MUST BE CONNECTED TO RF AND DC GROUND.

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4, 7 to 13, 15 to 18, 21 to 32	NIC	Not Internally Connected. These pins are not connected internally. All data shown herein was measured with these pins connected to RF and dc ground externally.
5, 20	GND	Ground. Connect these pins to RF and dc ground.
6	RFIN	Radio Frequency Input. This pin is dc-coupled and matched to 50 Ω. Do not apply an external voltage to this pin.
14	V _{FCTL}	Cutoff Frequency Control Voltage. This pin controls the cutoff frequency of the device.
19	RFOUT	Radio Frequency Output. This pin is dc-coupled and matched at 50 Ω. Do not apply an external voltage to this pin.
	EPAD	Exposed Pad. The package bottom has an exposed metal pad that must be connected to RF and dc ground.



Figure 3. GND Interface Schematic

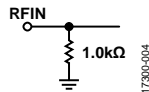


Figure 4. RFIN Interface Schematic

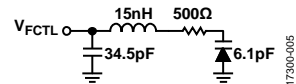


Figure 5. V_{FCTL} Interface Schematic

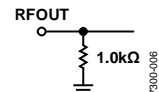


Figure 6. RFOUT Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS



Figure 7. Insertion Loss vs. Broadband Frequency at Various V_{FCTL} Voltages



Figure 10. Return Loss vs. Broadband Frequency at Various V_{FCTL} Voltages



Figure 8. Insertion Loss vs. RF Frequency at Various V_{FCTL} Voltages



Figure 11. Return Loss vs. RF Frequency at Various V_{FCTL} Voltages



Figure 9. Insertion Loss vs. RF Frequency at Various Temperatures, $V_{FCTL} = 7V$



Figure 12. Return Loss vs. RF Frequency at Various Temperatures, $V_{FCTL} = 7V$



Figure 13. Cutoff Frequency (f_{3dB}) vs. V_{FCTL} at Various Temperatures



Figure 16. Return Loss vs. V_{FCTL} at Various Temperatures, 2 dB Bandwidth



Figure 14. Rejection Ratio vs. V_{FCTL} at Various Temperatures; Rejection Ratio Is the Ratio of the Frequency of Which the Relative Insertion Loss Is 20 dB to f_{3dB}



Figure 17. Tuning Sensitivity vs. V_{FCTL} at Various Temperatures



Figure 15. Insertion Loss vs. V_{FCTL} at Various Temperatures



Figure 18. Residual Phase Noise vs. Offset Frequency at Various V_{FCTL} Voltages

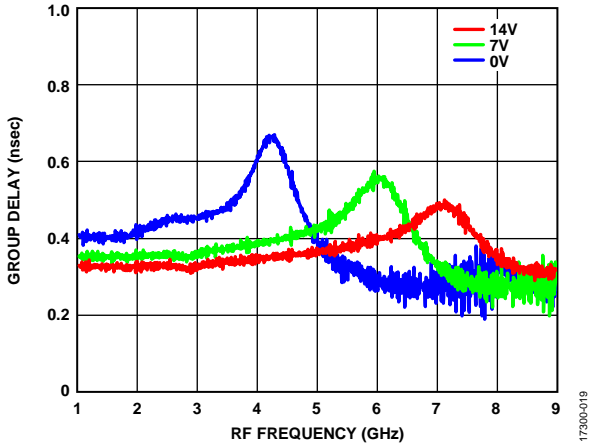


Figure 19. Group Delay vs. RF Frequency at Various V_{FCTL} Voltages



Figure 21. Phase Shift vs. Input Power (P_{IN}) at Various V_{FCTL} Voltages

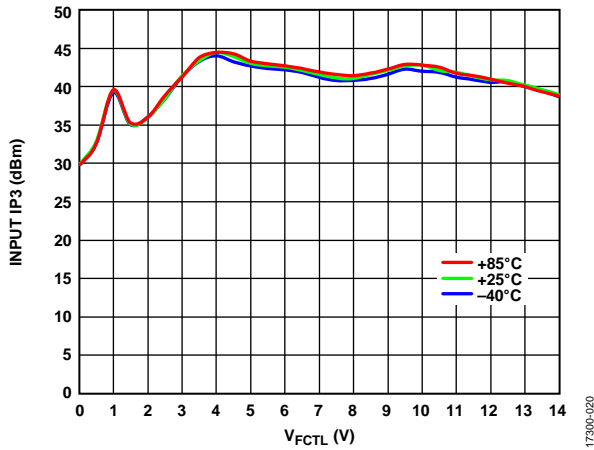


Figure 20. Input $IP3$ vs. V_{FCTL} at Various Temperatures, $P_{IN} = 20$ dBm

THEORY OF OPERATION

The HMC882A is a MMIC low-pass filter that features a user-selectable pass band frequency. Varying the applied analog tuning voltage between 0 V and 14 V at V_{FCTL} varies the f_{3dB} frequency between 3.95 GHz and 6.9 GHz.

APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUIT

Figure 22 shows the typical application circuit for the HMC882A. The RFIN and RFOUT pins are dc-coupled and require external, 100 pF series capacitors (C1 and C2).



Figure 22. Typical Application Circuit

EVALUATION PRINTED CIRCUIT BOARD (PCB)

All RF traces are routed on Layer 1 (primary side) and the remaining three layers are ground planes that provide a solid ground for RF transmission lines, as shown in Figure 23. The top dielectric material is Rogers 4350, which offers low loss performance. The prepreg material in Layer 2 attaches the Isola 370HR core layer with copper traces layers above and below the core layer. Both the prepreg material and the Isola 370HR core layer are used to achieve the required board finish thickness.



Figure 23. Cross Sectional View of the EV1HMC882ALP5 PCB Layers

The PCB in this application uses RF circuit design techniques. Signal lines must have 50 Ω impedance and the package ground leads and exposed pad must be connected directly to the ground plane (see Figure 23). Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation PCB shown in Figure 24 is available from Analog Devices, Inc., upon request.

Table 4. Bill of Materials for the EV1HMC882ALP5

Item	Description
J1 to J2	PCB mount SRI Subminiature Version A (SMA) connector
J3 to J4	PCB mount Johnson SMA connector
C1, C2	Capacitor, 100 pF, 0402
U1	HMC882A
PCB ¹	08-049598 ² evaluation PCB

¹ Circuit board material is Arlon 25FR or Rogers 25FR.

² 08-049598 is the raw, bare PCB identifier. Reference the EV1HMC882ALP5 when ordering the complete evaluation PCB.



Figure 24. Evaluation PCB Top Layer Outline Dimensions

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