

## Power Amplifier, 4 W 28.5 - 31 GHz

Rev. V1

### Features

- High Gain: 22 dB @ 30 GHz
- P1dB: 34.5 dBm
- P<sub>SAT</sub>: 36 dBm
- IM3 Level: -27 dBc @ P<sub>OUT</sub> 29 dBm/tone
- Power Added Efficiency: 23% @ P<sub>SAT</sub>
- Lead-Free 5 mm 32-lead AQFN Plastic Package
- RoHS\* Compliant

### Description

The MAAP-011139 is a 4-stage, 4 W power amplifier assembled in a lead-free 5 mm 32-lead AQFN plastic package. This power amplifier operates from 28.5 to 31 GHz and provides 22 dB of linear gain, 4 W saturated output power, and 23% efficiency while biased at 6 V.

The MAAP-011139 is a power amplifier ideally suited for VSAT communications.

This product is fabricated using a GaAs pHEMT process which features full passivation for enhanced reliability.

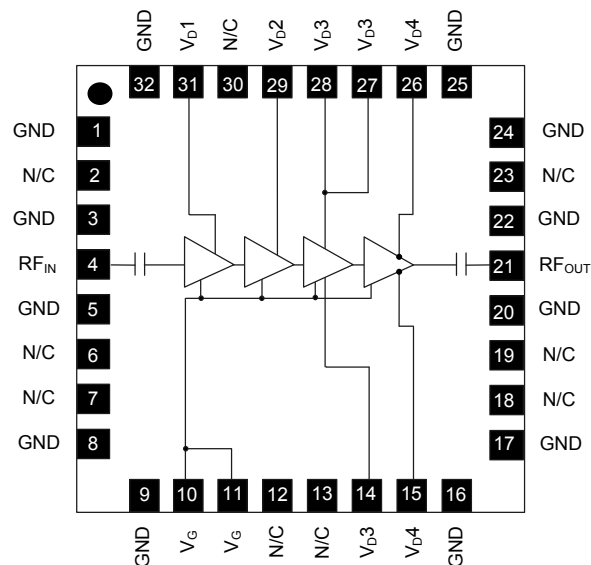
### Ordering Information<sup>1,2</sup>

Part Number	Package
MAAP-011139-TR0500	500 piece reel
MAAP-011139-SMB	Sample Board

1. Reference Application Note M513 for reel size information.
2. All sample boards include 3 loose parts.

\*Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

### Functional Schematic



### Pin Configuration<sup>3</sup>

Pin No.	Function	Pin No.	Function
1	Ground	18, 19	No Connection
2	No Connection	20	Ground
3	Ground	21	RF Output
4	RF Input	22	Ground
5	Ground	23	No Connection
6, 7	No Connection	24, 25	Ground
8, 9	Ground	26	Drain Voltage 4
10	Gate Voltage	27	Drain Voltage 3
11	Gate Voltage	28	Drain Voltage 3
12, 13	No Connection	29	Drain Voltage 2
14	Drain Voltage 3	30	No Connection
15	Drain Voltage 4	31	Drain Voltage 1
16, 17	Ground	32	Ground
		Paddle <sup>4</sup>	Ground

3. MACOM recommends connecting unused package pins to ground.
4. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

**Electrical Specifications: Freq. = 30 GHz, T<sub>A</sub> = +25°C, V<sub>D</sub> = 6 V, Z<sub>0</sub> = 50 Ω**

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	P <sub>IN</sub> = 0 dBm	dB	19	22	—
P <sub>OUT</sub>	P <sub>IN</sub> = +17 dBm	dBm	34.5	36.0	—
IM3 Level	P <sub>OUT</sub> = +29 dBm / tone	dBc	—	-27	—
Power Added Efficiency	P <sub>SAT</sub> (P <sub>IN</sub> = +17 dBm)	%	—	23	—
Input Return Loss	P <sub>IN</sub> = -20 dBm	dB	—	10	—
Output Return Loss	P <sub>IN</sub> = -20 dBm	dB	—	10	—
Quiescent Current	I <sub>DQ</sub> (see bias conditions, page 5 )	mA	—	2000	—
Current	P <sub>SAT</sub> (P <sub>IN</sub> = +17 dBm)	mA	—	2700	—

### Maximum Operating Conditions

Parameter	Maximum
Input Power	+17 dBm
Junction Temperature <sup>5,6</sup>	+160°C
Operating Temperature	-40°C to +85°C

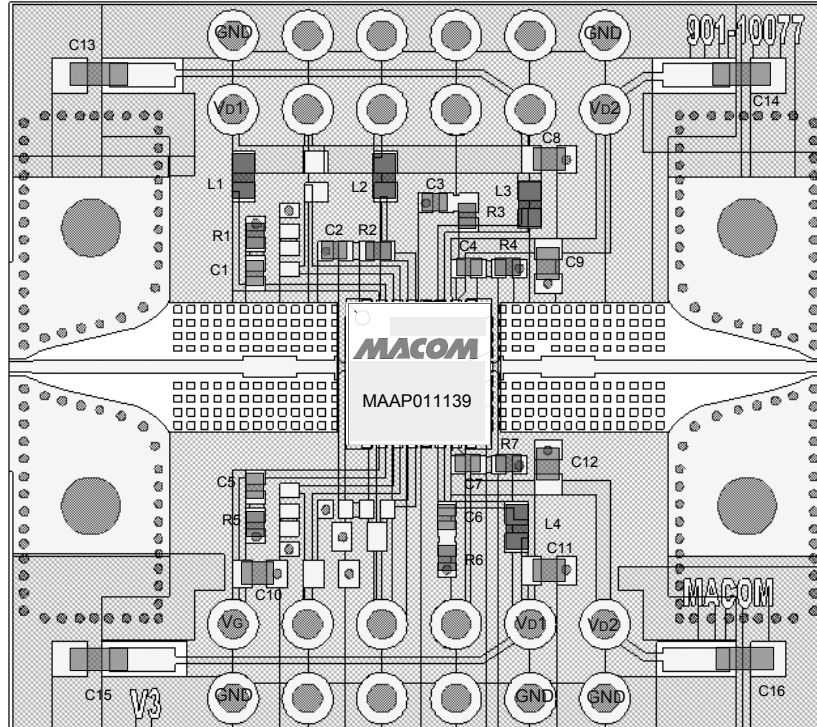
5. Operating at nominal conditions with junction temperature ≤ +160°C will ensure MTTF > 1 x 10<sup>6</sup> hours.
6. Junction Temperature (T<sub>J</sub>) = T<sub>C</sub> + Θ<sub>JC</sub> \* [(V \* I) - (P<sub>OUT</sub> - P<sub>IN</sub>)].  
Typical thermal resistance (Θ<sub>JC</sub>) = 4.4 °C/W.
  - a) For T<sub>C</sub> = +25°C,  
T<sub>J</sub> = +79°C @ 6 V, 2.7 A, P<sub>OUT</sub> = 36 dBm, P<sub>IN</sub> = 17 dBm
  - b) For T<sub>C</sub> = +85°C,  
T<sub>J</sub> = +143°C @ 6 V, 2.7 A, P<sub>OUT</sub> = 35.1 dBm, P<sub>IN</sub> = 17 dBm

### Absolute Maximum Ratings<sup>7,8</sup>

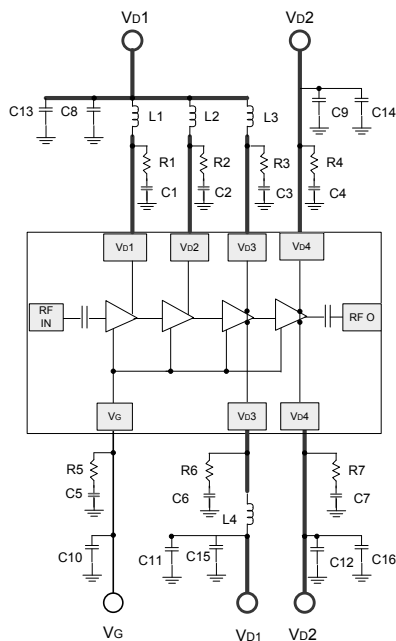
Parameter	Absolute Maximum
Input Power	+23 dBm
Drain Voltage	+6.5 V
Gate Voltage	-3 to 0 V
Junction Temperature <sup>9</sup>	+175°C
Storage Temperature	-65°C to +125°C

7. Exceeding any one or combination of these limits may cause permanent damage to this device.
8. MACOM does not recommend sustained operation near these survivability limits.
9. Junction Temperature directly effects device MTTF. Junction temperature should be kept as low as possible to maximize lifetime.

## Sample Board Layout



## Application Schematic



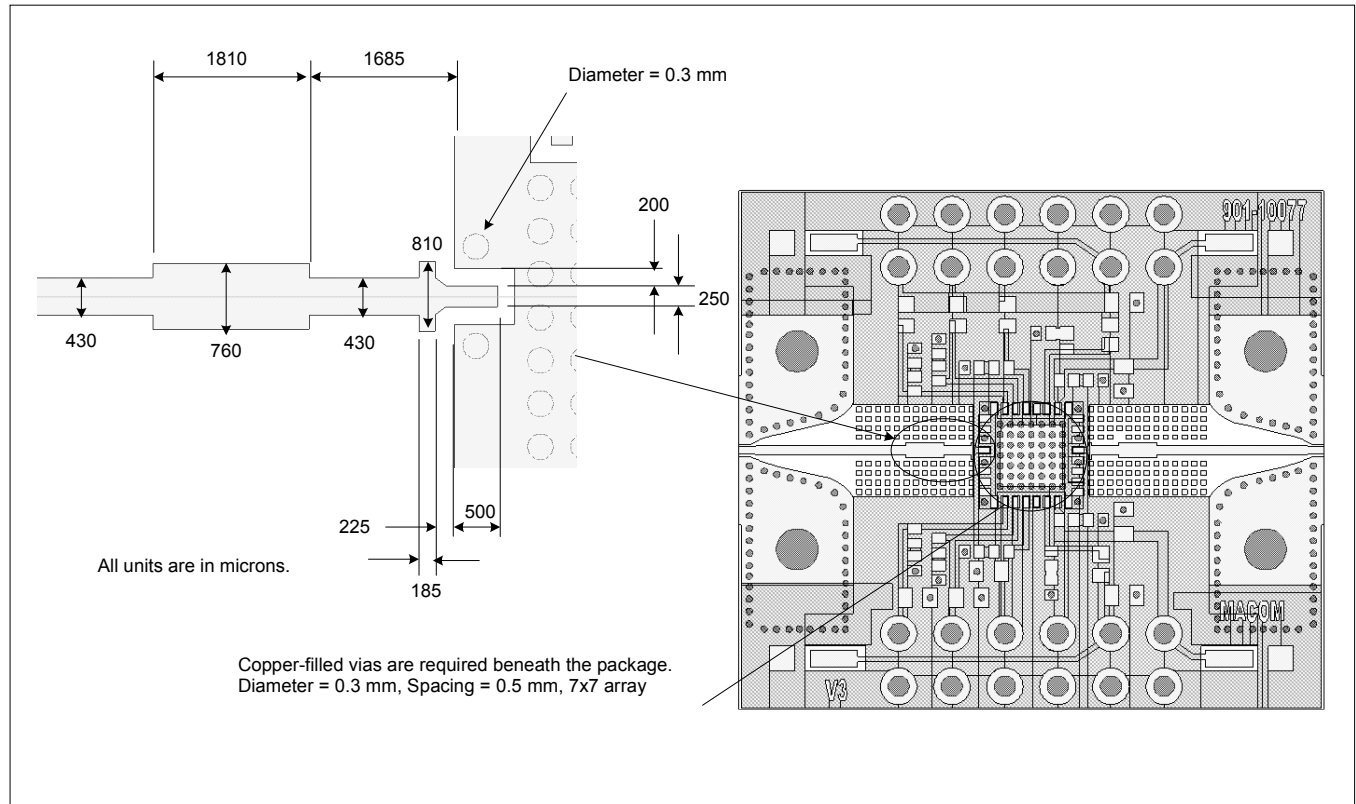
## Parts List

Part	Value	Case Style
C1 - C7	0.01 $\mu$ F	0402
C8 - C12	1 $\mu$ F	0603
C13 - C16	10 $\mu$ F	0805
R1 - R7	10 $\Omega$	0402
L1 - L4 (Chip Ferrite Bead)	BLM18HE601SN1D	0603

## Sample Board Material Specifications

Top Layer: 1/2 oz Copper Cladding, 0.017 mm thickness  
 Dielectric Layer: Rogers RO4003C 0.203 mm thickness  
 Bottom Layer: 1/2 oz Copper Cladding, 0.017 mm thickness  
 Finished overall thickness: 0.238 mm

Sample Board Layout: RF input and output port pre-matching circuit patterns are designed to compensate for packaging effects. Input and output match patterns are identical.



## Application Information

The MAAP-011139 is designed to be easy to use yet high performance. The ultra small size and simple bias allow easy placement on system board. RF input and output ports are DC de-coupled internally.

## Biasing conditions

Recommended biasing conditions are  $V_D = 6\text{ V}$ ,  $I_{DQ} = 2000\text{ mA}$  (controlled with  $V_G$ ). The drain bias voltage range is 3 to 6 V, and the quiescent drain current biasing range is 1500 to 2500 mA.

$V_G$  pins 10 and 11 are connected internally; choose either pin for layout convenience. Muting can be accomplished by setting the  $V_G$  to the pinched off voltage ( $V_G = -2\text{ V}$ ).

$V_D$  bias must be applied to  $V_{D1}$ ,  $V_{D2}$ ,  $V_{D3}$ , and  $V_{D4}$  pins.

$V_{D3}$  pins 14 and either pin 27 or 28 are required for current symmetry. Pins 27 and 28 are connected internally; choose either pin for layout convenience.

Both  $V_{D4}$  pins 15 and 26 are required for current symmetry.

## Operating the MAAP-011139

### Turn-on

1. Apply  $V_G$  (-1.5 V).
2. Apply  $V_D$  (6.0 V typical).
3. Set  $I_{DQ}$  by adjusting  $V_G$  more positive (typically  $V_G \sim -0.9\text{ V}$  for  $I_{DQ} = 2000\text{ mA}$ ).
4. Apply  $RF_{IN}$  signal.

### Turn-off

1. Remove  $RF_{IN}$  signal.
2. Decrease  $V_G$  to -1.5 V.
3. Decrease  $V_D$  to 0 V.

## Handling Procedures

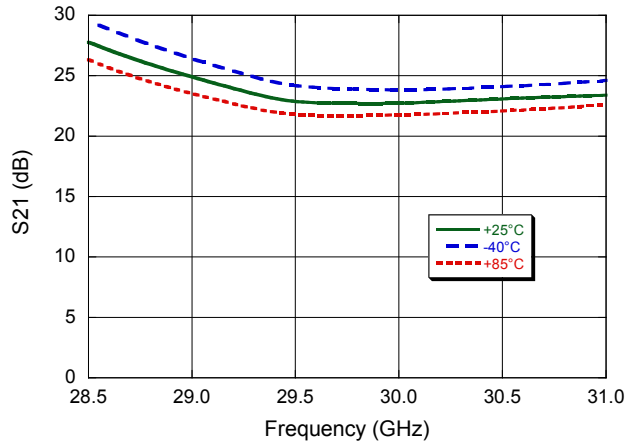
Please observe the following precautions to avoid damage:

## Static Sensitivity

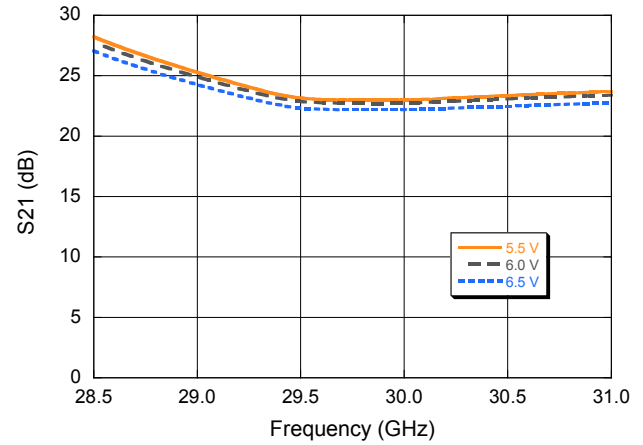
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.

## Typical Performance Curves

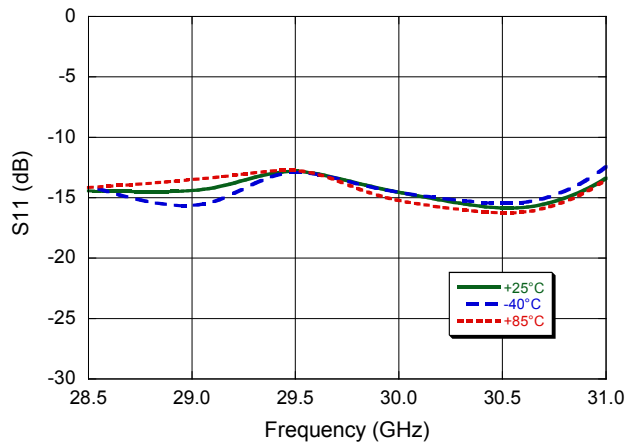
**Small Signal Gain vs. Frequency over Temperature**



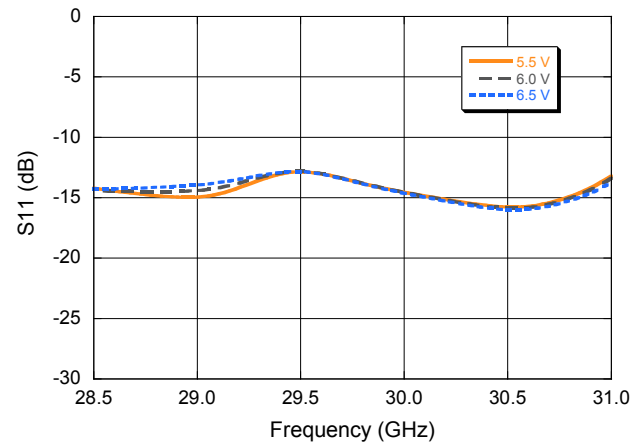
**Small Signal Gain vs. Frequency over Bias Voltage**



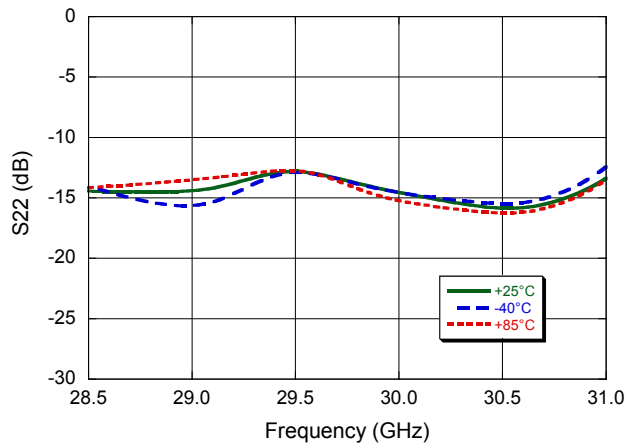
**Input Return Loss vs. Frequency over Temperature**



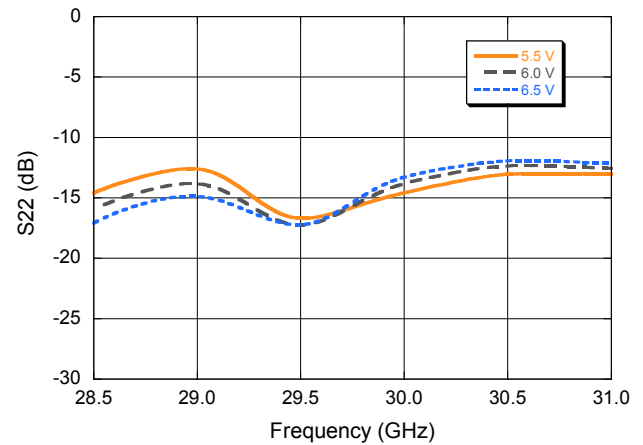
**Input Return Loss vs. Frequency over Bias Voltage**



**Output Return Loss vs. Frequency over Temperature**

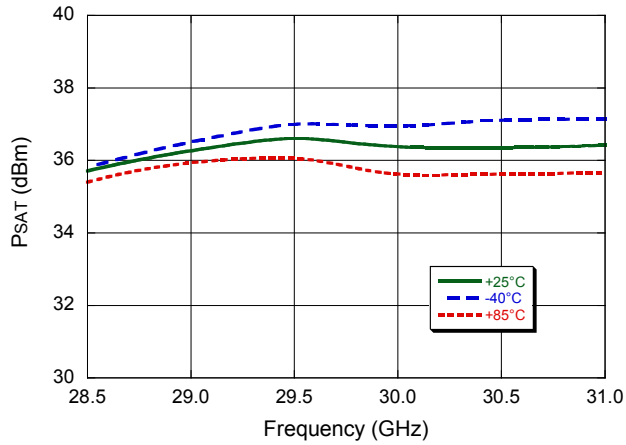


**Output Return Loss vs. Frequency over Bias Voltage**

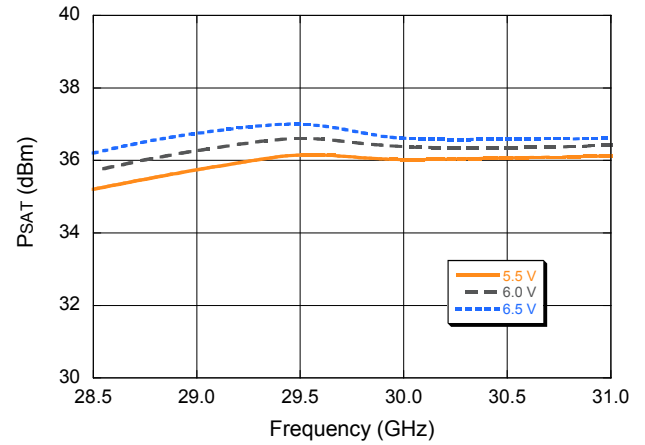


## Typical Performance Curves

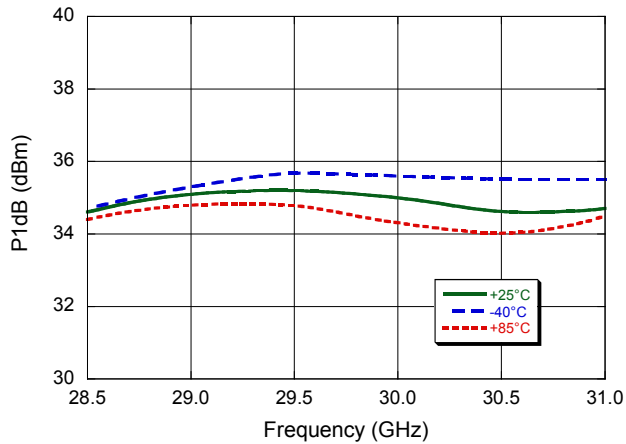
*P<sub>SAT</sub> vs. Frequency over Temperature*



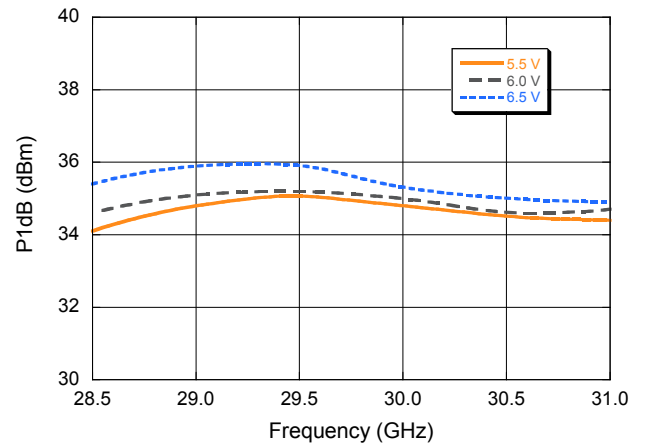
*P<sub>SAT</sub> vs. Frequency over Bias Voltage*



*P1dB vs. Frequency over Temperature*

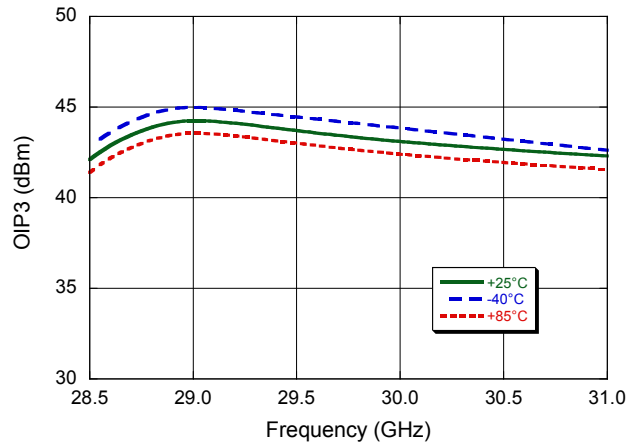


*P1dB vs. Frequency over Bias Voltage*

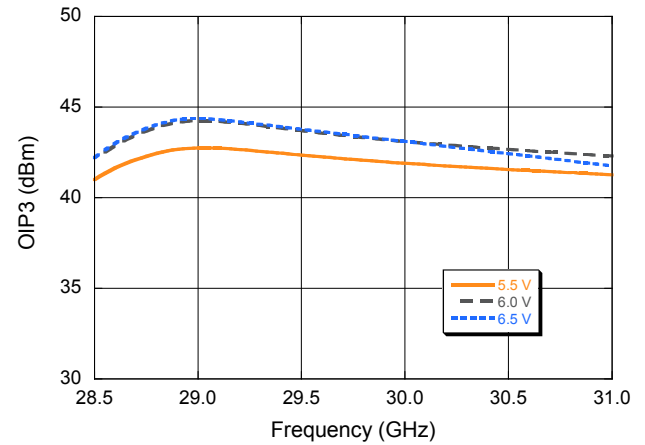


## Typical Performance Curves

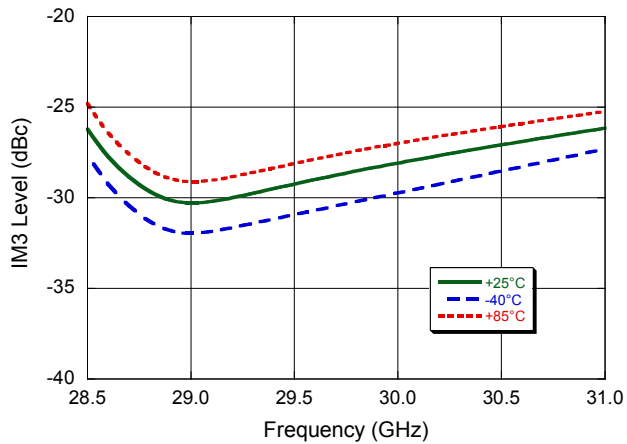
**Output IP3 over Temperature ( $P_{out}=29$  dBm/tone)**



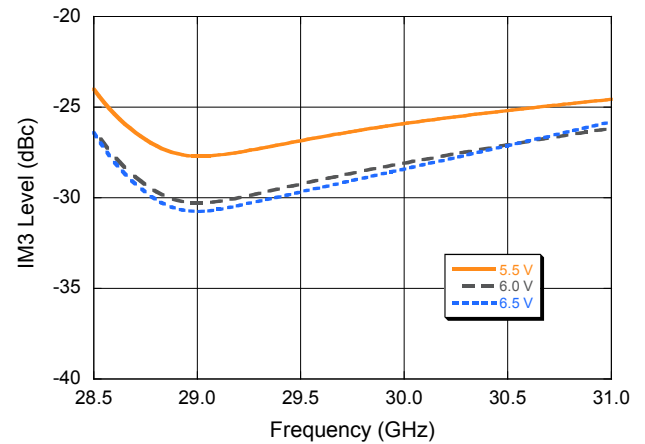
**Output IP3 over Bias Voltage ( $P_{out}=29$  dBm/Tone)**



**IM3 over Temperature ( $P_{out}=29$  dBm/tone)**



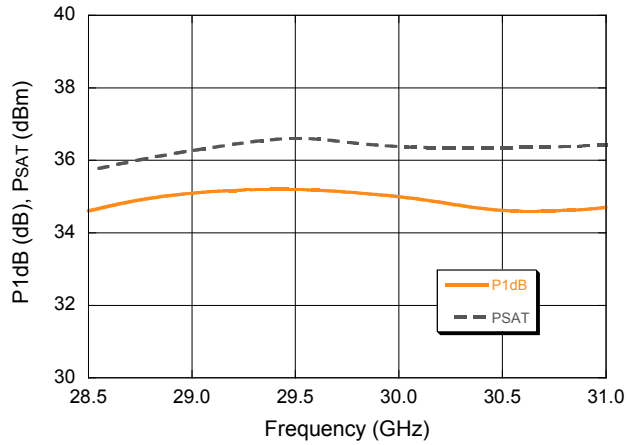
**IM3 over Bias Voltage ( $P_{out}=29$  dBm/tone)**



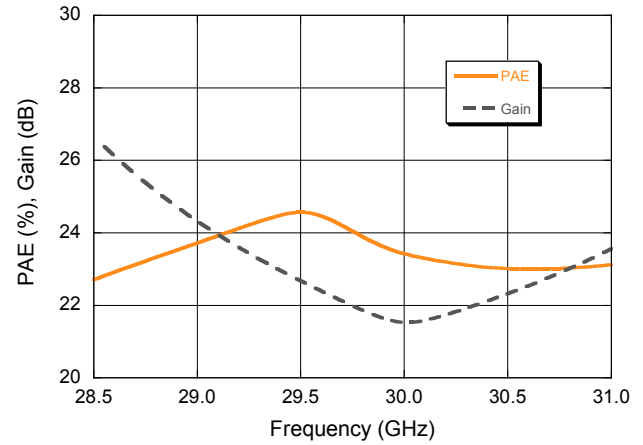


## Typical Performance Curves

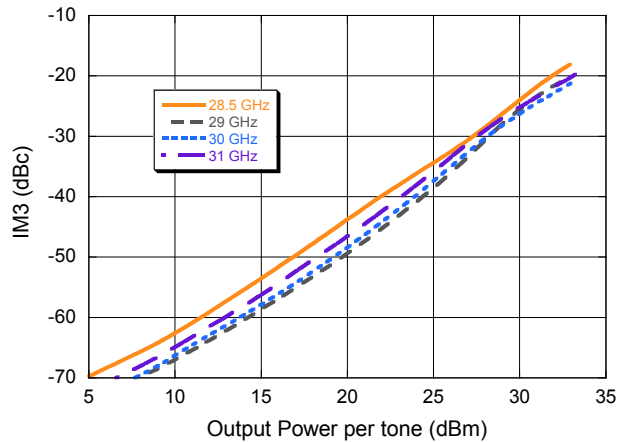
***P<sub>1dB</sub>, P<sub>SAT</sub> vs. Frequency***



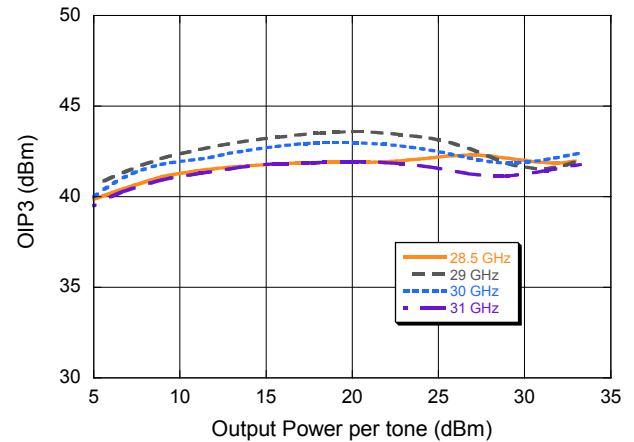
***PAE, Gain vs. Frequency***



***IM3 vs. Output Power (per tone)***

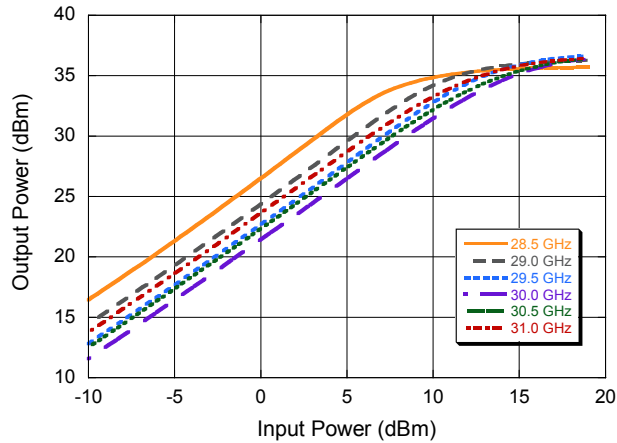


***Output IP3 vs. Output Power (per tone)***

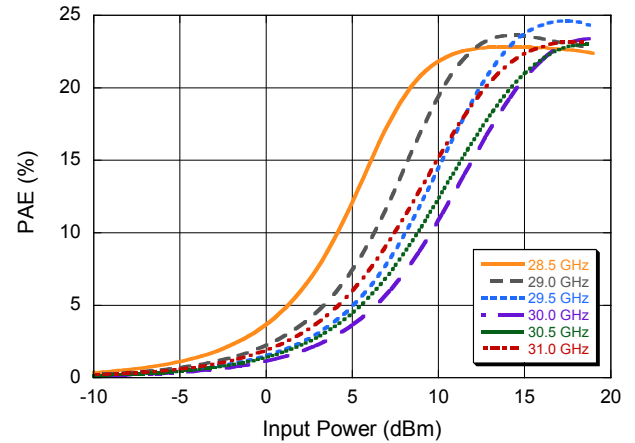


## Typical Performance Curves

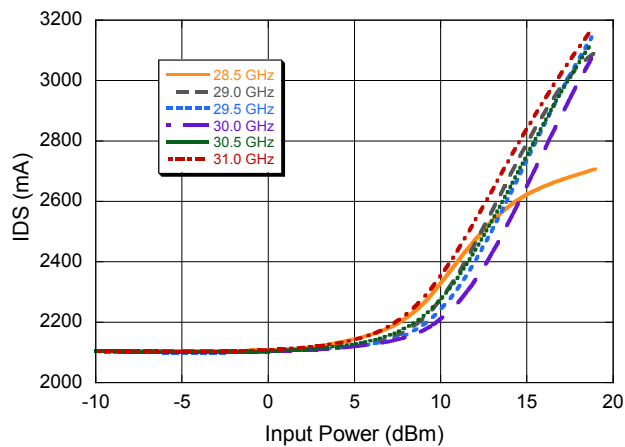
**Output Power vs. Input Power**



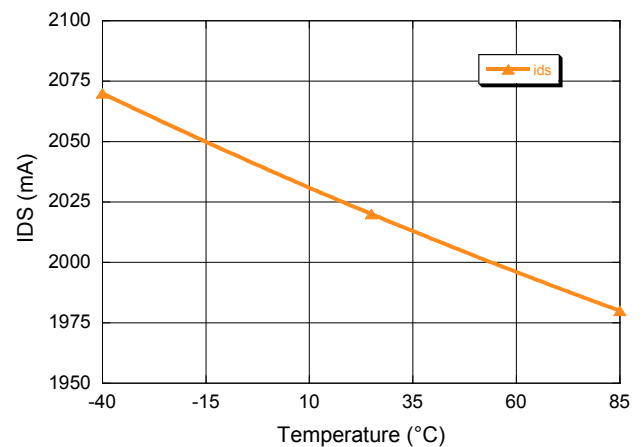
**PAE vs. Input Power**



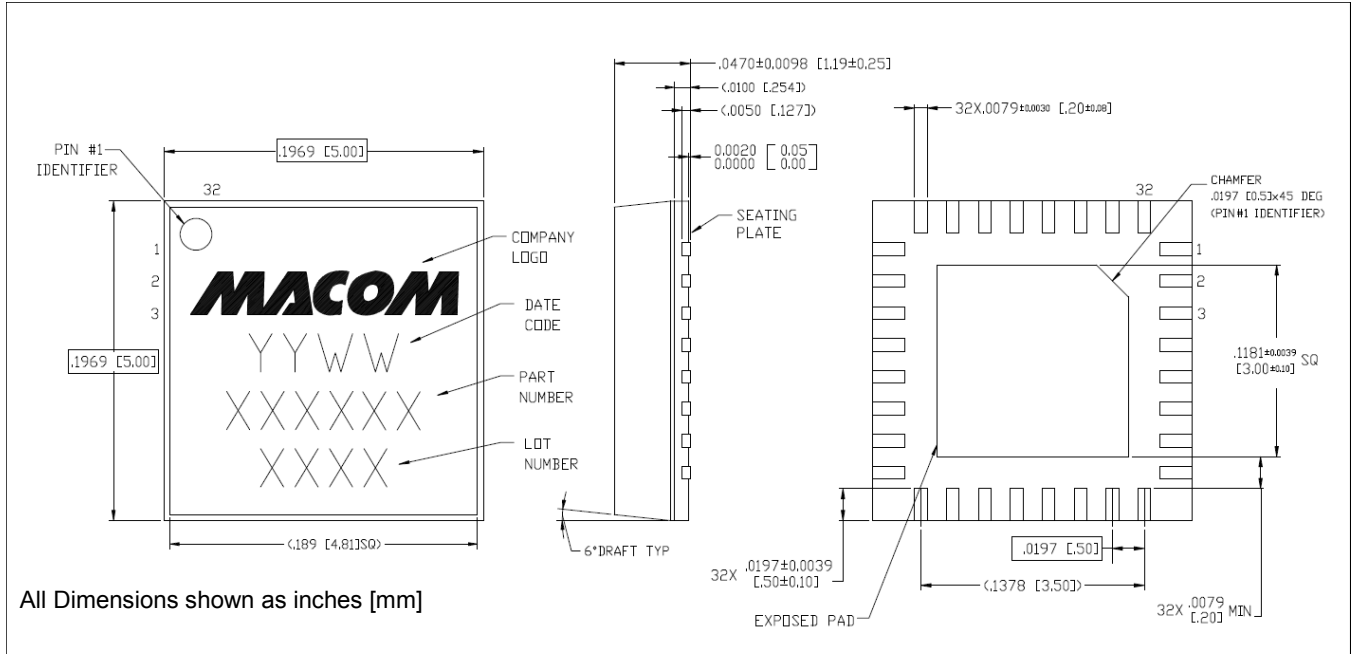
**Bias Current vs. Input Power**



**Quiescent Drain Current vs. Temperature**



**Lead-Free 5 mm QFN 32-Lead<sup>†</sup>**



<sup>†</sup> Reference Application Note S2083 for lead-free solder reflow recommendations.  
Meets JEDEC moisture sensitivity level 3 requirements.  
Plating is NiPdAu.

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