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June 2014

FDMC8554

N-Channel Power Trench® MOSFET

20V, **16.5A**, **5m** Ω

Features

- Max $r_{DS(on)} = 5m\Omega$ at $V_{GS} = 10V$, $I_D = 16.5A$
- Max $r_{DS(on)} = 6.4 \text{m}\Omega$ at $V_{GS} = 4.5 \text{V}$, $I_D = 14 \text{A}$
- Low Profile 1mm max in Power 33
- RoHS Compliant

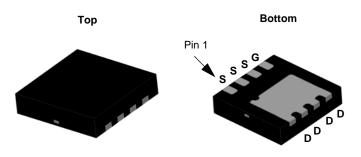


General Description

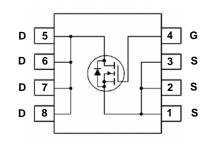
This N-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced Power Trench process. It has been optimized for power management applications.

Application

■ DC - DC Conversion







MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			20	V
V_{GS}	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T _C = 25°C		16.5	
I _D	-Continuous	T _A = 25°C	(Note 1a)	16.5	Α
	-Pulsed			36	
D	Power Dissipation	T _C = 25°C		41	W
P_{D}	Power Dissipation	T _A = 25°C	(Note 1a)	2.0	VV
T _J , T _{STG}	Operating and Storage Junction Temperature R	ange		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8554	FDMC8554	Power 33	7"	8mm	3000 units

Electrical Characteristics $T_J = 25^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		15.7		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16V,$ $V_{GS} = 0V$ $T_{J} = 125^{\circ}C$			1 100	μА
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20V$, $V_{DS} = 0V$			±100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	1.0	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		-6.1		mV/°C
		$V_{GS} = 10V, I_D = 16.5A$		3.6	5.0	
r _{DS(on)}	Drain to Source On Resistance	$V_{GS} = 4.5V, I_D = 14A$		4.6	6.4	mΩ
, ,		$V_{GS} = 10V$, $I_D = 16.5A$, $T_J = 125$ °C		5.4	7.1	
9 _{FS}	Forward Transconductance	$V_{DS} = 5V, I_{D} = 16.5A$		62		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 40V V 0V	2540	3380	pF
C _{oss}	Output Capacitance	$V_{DS} = 10V, V_{GS} = 0V,$ f = 1MHz	795	1060	pF
C _{rss}	Reverse Transfer Capacitance	1 - 11/11/12	510	765	pF
R _a	Gate Resistance	f = 1MHz	1.2		Ω

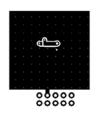
Switching Characteristics

t _{d(on)}	Turn-On Delay Time	.,		13	24	ns
t _r	Rise Time	$V_{DD} = 10V, I_{D} = 16.5A$ $V_{GS} = 10V, R_{GEN} = 6\Omega$		10	20	ns
t _{d(off)}	Turn-Off Delay Time			32	51	ns
t _f	Fall Time			7	14	ns
Q _{g(TOT)}	Total Gate Charge at 10V			44	62	nC
$Q_{g(TOT)}$	Total Gate Charge at 4.5V	$V_{DD} = 10V, I_D = 16.5A$		24	34	nC
Q _{gs}	Gate to Source Gate Charge			8.5		nC
Q _{ad}	Gate to Drain "Miller" Charge			10		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0V, I_S = 16.5A$ (Note 2)		0.8	1.3	V
t _{rr}	Reverse Recovery Time	L - 16.54 di/dt - 1004/		31	47	ns
Q _{rr}	Reverse Recovery Charge	I _F = 16.5A, di/dt = 100A/μs		22	33	nC

Notes:
 1: R_{BJA} is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{BJC} is guaranteed by design while R_{BCA} is determined by the user's board design.



a. 60°C/W when mounted on a 1 in² pad of 2 oz copper

b. 135°C/W when mounted on a minimum pad of 2 oz copper



2: Pulse Test: Pulse Width < $300\mu s$, Duty cycle < 2.0%.

Typical Characteristics T_J = 25°C unless otherwise noted

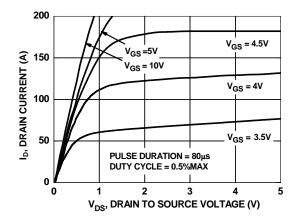


Figure 1. On-Region Characteristics

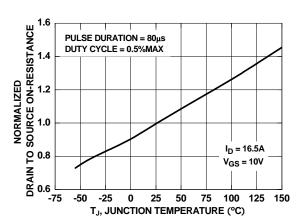


Figure 3. Normalized On-Resistance vs Junction Temperature

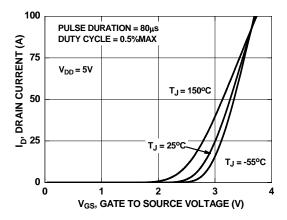


Figure 5. Transfer Characteristics

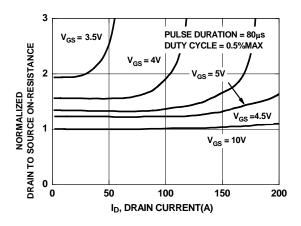


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

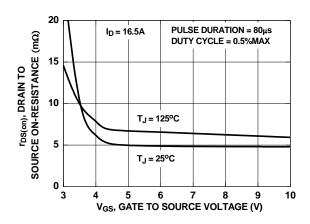


Figure 4. On-Resistance vs Gate to Source Voltage

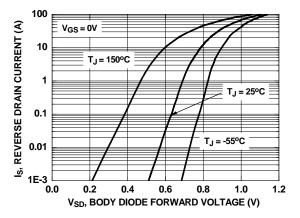


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

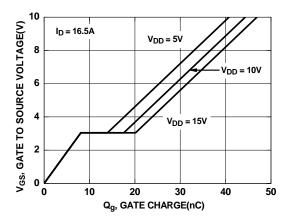


Figure 7. Gate Charge Characteristics

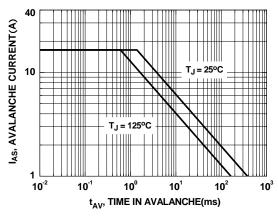


Figure 9. Unclamped Inductive Switching Capability

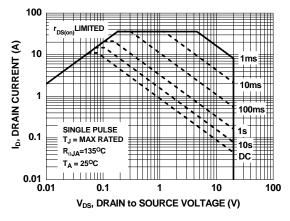


Figure 11. Forward Bias Safe Operating Area

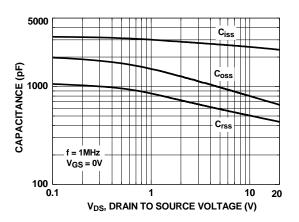


Figure 8. Capacitance vs Drain to Source Voltage

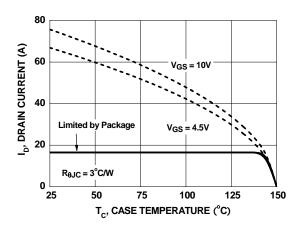


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

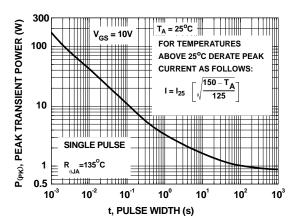


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

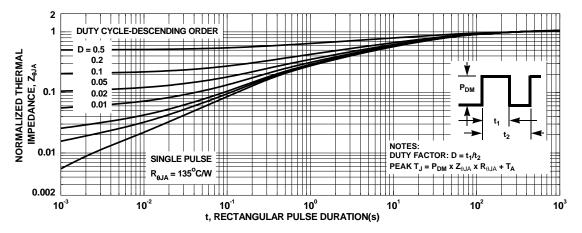
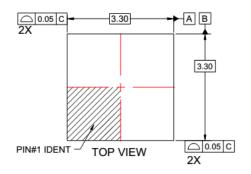
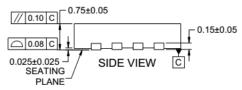
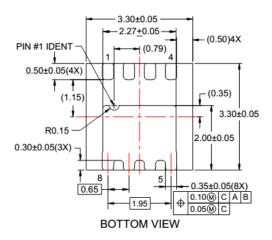


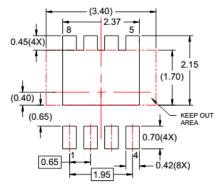
Figure 13. Transient Thermal Response Curve

Dimensional Outline and Pad Layout









RECOMMENDED LAND PATTERN

NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP08Srev3.



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