S-25C010A/020A/040A

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SPI SERIAL E^{2}PROM

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Rev.4.3_02_C

The S-25C010A/020A/040A is a SPI serial E^{2}PROM which operate at high speed, with low current consumption and the wide range operation. The S-25C010A/020A/040A has the capacity of 1 K-bit, 2 K-bit, 4 K-bit and the organization of 128 words × 8-bit, 256 words × 8-bit, 512 words × 8-bit. Page write and sequential read are available.

■ Features

- Operating voltage range: Read 1.6 V to 5.5 V
  Write 1.7 V to 5.5 V
- Operation frequency: 5.0 MHz (V_{CC} = 2.5 V to 5.5 V)
- Write time: 4.0 ms max.
- SPI mode (0, 0) and (1, 1)
- Page write: 16 bytes / page
- Sequential read
- Write protect: Software, Hardware
  Protect area: 25%, 50%, 100%
- Monitors write to the memory by a status register
- Function to prevent malfunction by monitoring clock pulse
- Write protect function during the low power supply
- CMOS schmitt input ($\overline{\text{CS}}$, SCK, SI, $\overline{\text{WP}}$, $\overline{\text{HOLD}}$)
- Endurance: 10^6 cycles / word[*1] (Ta = +25°C)
- Data retention: 100 years (Ta = +25°C)
- Memory capacity: S-25C010A 1 K-bit
  S-25C020A 2 K-bit
  S-25C040A 4 K-bit
- Initial delivery state: FFh, BP1 = 0, BP0 = 0
- Operation temperature range: Ta = −40°C to +85°C
- Lead-free, Sn 100%, halogen-free[*2]

***1.** For each address (Word: 8-bit)
***2.** Refer to "**■ Product Name Structure**" for details.

■ Packages

- 8-Pin SOP (JEDEC)
- 8-Pin TSSOP
- TMSOP-8
- SNT-8A

Caution This product is intended to use in general electronic devices such as consumer electronics, office equipment, and communications devices. Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, contact to ABLIC Inc. is indispensable.

■ Pin Configurations

1. 8-Pin SOP (JEDEC)

8-Pin SOP (JEDEC)
Top view

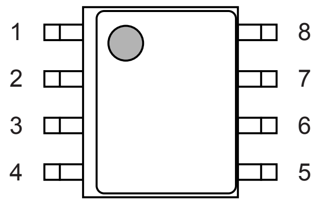


Figure 1

S-25C010A0I-J8T1x
S-25C020A0I-J8T1x
S-25C040A0I-J8T1x

Table 1

Pin No.	Symbol	Description
1	$\overline{\text{CS}}$ [*1]	Chip select input
2	SO	Serial data output
3	$\overline{\text{WP}}$ [*1]	Write protect input
4	GND	Ground
5	SI [*1]	Serial data input
6	SCK [*1]	Serial clock input
7	$\overline{\text{HOLD}}$ [*1]	Hold input
8	VCC	Power supply

***1.** Do not use it in high impedance.

2. 8-Pin TSSOP

8-Pin TSSOP
Top view

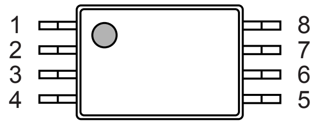


Figure 2

S-25C010A0I-T8T1x
S-25C020A0I-T8T1x
S-25C040A0I-T8T1x

Table 2

Pin No.	Symbol	Description
1	$\overline{\text{CS}}$ [*1]	Chip select input
2	SO	Serial data output
3	$\overline{\text{WP}}$ [*1]	Write protect input
4	GND	Ground
5	SI [*1]	Serial data input
6	SCK [*1]	Serial clock input
7	$\overline{\text{HOLD}}$ [*1]	Hold input
8	VCC	Power supply

***1.** Do not use it in high impedance.

Remark **1.** Refer to the “**Package drawings**” for the details
2. x: G or U
3. Please select products of environmental code = U for Sn 100%, halogen-free products.

3. TMSOP-8

TMSOP-8
Top view

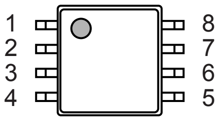


Figure 3

S-25C010A0I-K8T3U
S-25C020A0I-K8T3U
S-25C040A0I-K8T3U

Table 3

Pin No.	Symbol	Description
1	$\overline{\text{CS}}$ [*1]	Chip select input
2	SO	Serial data output
3	$\overline{\text{WP}}$ [*1]	Write protect input
4	GND	Ground
5	SI [*1]	Serial data input
6	SCK [*1]	Serial clock input
7	$\overline{\text{HOLD}}$ [*1]	Hold input
8	VCC	Power supply

[*1] Do not use it in high impedance.

4. SNT-8A

SNT-8A
Top view

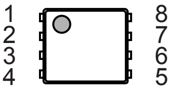


Figure 4

S-25C010A0I-I8T1U
S-25C020A0I-I8T1U
S-25C040A0I-I8T1U

Table 4

Pin No.	Symbol	Description
1	$\overline{\text{CS}}$ [*1]	Chip select input
2	SO	Serial data output
3	$\overline{\text{WP}}$ [*1]	Write protect input
4	GND	Ground
5	SI [*1]	Serial data input
6	SCK [*1]	Serial clock input
7	$\overline{\text{HOLD}}$ [*1]	Hold input
8	VCC	Power supply

[*1] Do not use it in high impedance.

Remark Refer to the “**Package drawings**” for the details

■ Block Diagram

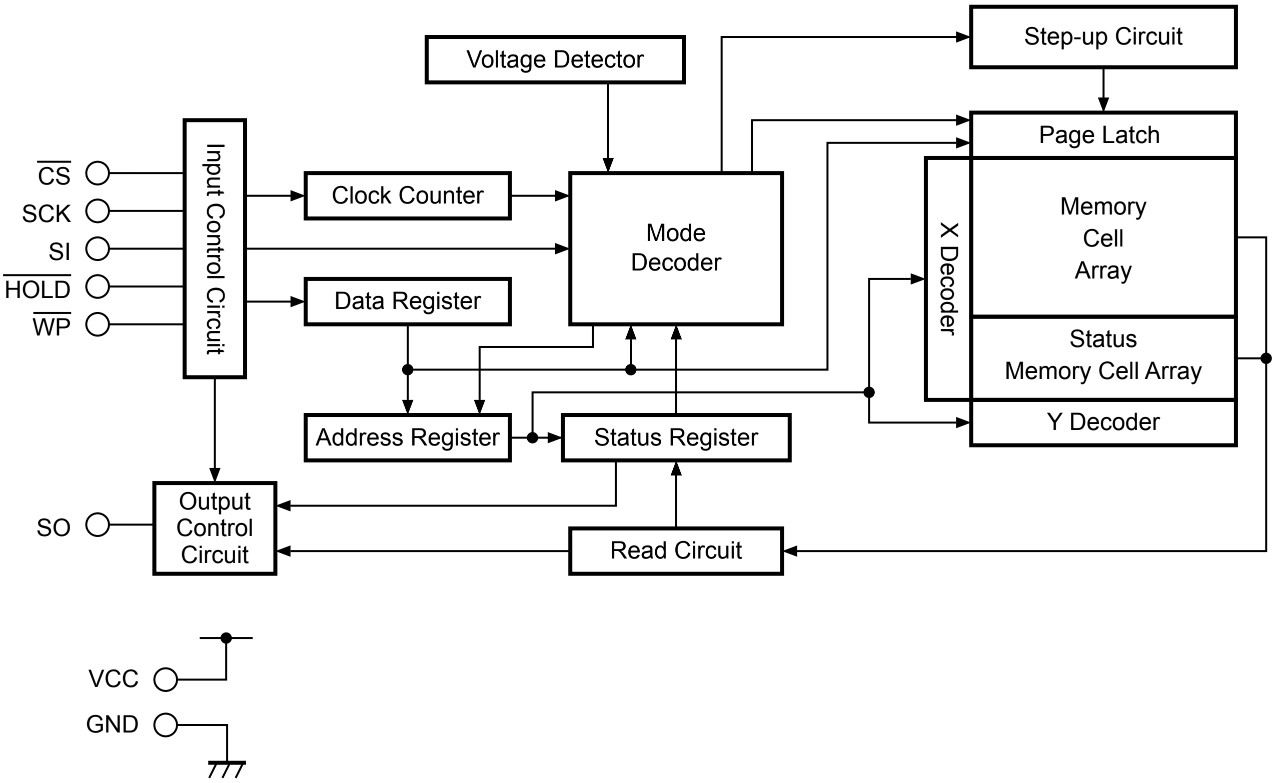

Step-up Circuit
Voltage Detector
Page Latch
CS
SCK
SI
HOLD
WP
Input Control Circuit
Clock Counter
Mode Decoder
Data Register
X Decoder
Memory Cell Array
Status Memory Cell Array
Address Register
Status Register
Y Decoder
SO
Output Control Circuit
Read Circuit
VCC
GND

Figure 5

■ Absolute Maximum Ratings

Table 5

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	V_{CC}	-0.3 to $+7.0$	V
Input voltage	V_{IN}	-0.3 to $+7.0$	V
Output voltage	V_{OUT}	-0.3 to $V_{CC} + 0.3$	V
Operation ambient temperature	T_{opr}	-40 to $+85$	°C
Storage temperature	T_{stg}	-65 to $+150$	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operating Conditions

Table 6

Item	Symbol	Condition	Ta = −40°C to +85°C		Unit
			Min.	Max.	
Power supply voltage	V_{CC}	Read operation	1.6	5.5	V
		Write operation	1.7	5.5	V
High level input voltage	V_{IH}	V_{CC} = 1.6 V to 5.5 V	$0.7 \times V_{CC}$	$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}	V_{CC} = 1.6 V to 5.5 V	-0.3	$0.3 \times V_{CC}$	V

■ Pin Capacitance

Table 7

(Ta = +25°C, f = 1.0 MHz, V_{CC} = 5.0 V)

Item	Symbol	Condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	−	8	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V (SO)	−	10	pF

■ Endurance

Table 8

Item	Symbol	Operation Ambient Temperature	Min.	Max.	Unit
Endurance	N_W	Ta = +25°C	10^6	−	cycles / word*1

***1.** For each address (Word: 8-bit)

■ Data Retention

Table 9

Item	Symbol	Operation Ambient Temperature	Min.	Max.	Unit
Data retention	−	Ta = +25°C	100	−	year

■ DC Electrical Characteristics

Table 10

Item	Symbol	Condition	Ta = −40°C to +85°C						Unit
			V_{CC} = 1.6 V to 2.5 V f_{SCK} = 2.0 MHz		V_{CC} = 2.5 V to 4.5 V f_{SCK} = 5.0 MHz		V_{CC} = 4.5 V to 5.5 V f_{SCK} = 5.0 MHz		
			Min.	Max.	Min.	Max.	Min.	Max.	
Current consumption (READ)	I_{CC1}	No load at SO pin	−	1.5	−	2.0	−	2.5	mA

Table 11

Item	Symbol	Condition	Ta = −40°C to +85°C						Unit
			V_{CC} = 1.7 V to 2.5 V f_{SCK} = 2.0 MHz		V_{CC} = 2.5 V to 4.5 V f_{SCK} = 5.0 MHz		V_{CC} = 4.5 V to 5.5 V f_{SCK} = 5.0 MHz		
			Min.	Max.	Min.	Max.	Min.	Max.	
Current consumption (WRITE)	I_{CC2}	No load at SO pin	−	2.0	−	2.5	−	3.0	mA

Table 12

Item	Symbol	Condition	Ta = −40°C to +85°C						Unit
			V_{CC}=1.6 V to 2.5 V		V_{CC}=2.5 V to 4.5 V		V_{CC}=4.5 V to 5.5 V		
			Min.	Max.	Min.	Max.	Min.	Max.	
Standby current consumption	I_{SB}	$\overline{CS}$ = V_{CC}, SO = Open Other inputs are V_{CC} or GND	−	1.5	−	1.5	−	1.5	μA
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	−	1.0	−	1.0	−	1.0	μA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}	−	1.0	−	1.0	−	1.0	μA
Low level output voltage	V_{OL1}	I_{OL} = 2.0 mA	−	−	−	0.4	−	0.4	V
	V_{OL2}	I_{OL} = 1.5 mA	−	0.4	−	0.4	−	0.4	V
High level output voltage	V_{OH1}	I_{OH} = −2.0 mA	−	−	0.8 × V_{CC}	−	0.8 × V_{CC}	−	V
	V_{OH2}	I_{OH} = −0.4 mA	0.8 × V_{CC}	−	0.8 × V_{CC}	−	0.8 × V_{CC}	−	V

■ AC Electrical Characteristics

Table 13 Measurement Conditions

Input pulse voltage	0.2 × V_{CC} to 0.8 × V_{CC}
Output reference voltage	0.5 × V_{CC}
Output load	100 pF

Table 14

Item	Symbol	Ta = −40°C to +85°C						Unit
		V_{CC} = 1.6 V to 2.5 V		V_{CC} = 2.5 V to 4.5 V		V_{CC} = 4.5 V to 5.5 V		
		Min.	Max.	Min.	Max.	Min.	Max.	
SCK clock frequency	f_{SCK}	−	2.0	−	5.0	−	5.0	MHz
$\overline{\text{CS}}$ setup time during $\overline{\text{CS}}$ falling	$t_{\text{CSS.CL}}$	150	−	90	−	90	−	ns
$\overline{\text{CS}}$ setup time during $\overline{\text{CS}}$ rising	$t_{\text{CSS.CH}}$	150	−	90	−	90	−	ns
$\overline{\text{CS}}$ deselect time	t_{CDS}	200	−	90	−	90	−	ns
$\overline{\text{CS}}$ hold time during $\overline{\text{CS}}$ falling	$t_{\text{CSH.CL}}$	200	−	90	−	90	−	ns
$\overline{\text{CS}}$ hold time during $\overline{\text{CS}}$ rising	$t_{\text{CSH.CH}}$	150	−	90	−	90	−	ns
SCK clock time “H” *1	t_{HIGH}	200	−	90	−	90	−	ns
SCK clock time “L” *1	t_{LOW}	200	−	90	−	90	−	ns
Rising time of SCK clock *2	t_{RSK}	−	1	−	1	−	1	µs
Falling time of SCK clock *2	t_{FSK}	−	1	−	1	−	1	µs
SI data input setup time	t_{DS}	50	−	20	−	20	−	ns
SI data input hold time	t_{DH}	60	−	30	−	30	−	ns
SCK “L” hold time during $\overline{\text{HOLD}}$ rising	$t_{\text{SKH.HH}}$	150	−	70	−	70	−	ns
SCK “L” hold time during $\overline{\text{HOLD}}$ falling	$t_{\text{SKH.HL}}$	100	−	40	−	40	−	ns
SCK “L” setup time during $\overline{\text{HOLD}}$ falling	$t_{\text{SKS.HL}}$	150	−	60	−	60	−	ns
SCK “L” setup time during $\overline{\text{HOLD}}$ rising	$t_{\text{SKS.HH}}$	150	−	60	−	60	−	ns
Disable time of SO output *2	t_{OZ}	−	200	−	100	−	100	ns
Delay time of SO output	t_{OD}	−	150	−	70	−	70	ns
Hold time of SO output	t_{OH}	0	−	0	−	0	−	ns
Rising time of SO output *2	t_{RO}	−	100	−	40	−	40	ns
Falling time of SO output *2	t_{FO}	−	100	−	40	−	40	ns
Disable time of SO output during $\overline{\text{HOLD}}$ falling *2	$t_{\text{OZ.HL}}$	−	200	−	100	−	100	ns
Delay time of SO output during $\overline{\text{HOLD}}$ rising *2	$t_{\text{OD.HH}}$	−	150	−	50	−	50	ns
$\overline{\text{WP}}$ setup time	t_{WS1}	0	−	0	−	0	−	ns
$\overline{\text{WP}}$ hold time	t_{WH1}	0	−	0	−	0	−	ns
$\overline{\text{WP}}$ release / setup time	t_{WS2}	0	−	0	−	0	−	ns
$\overline{\text{WP}}$ release / hold time	t_{WH2}	60	−	30	−	30	−	ns

***1.** The clock cycle of the SCK clock (frequency f_{SCK}) is 1 / f_{SCK} µs. This clock cycle is determined by a combination of several AC characteristics. Note that the clock cycle cannot be set as (1 / f_{SCK}) = t_{LOW} (min.) + t_{HIGH} (min.) by minimizing the SCK clock cycle time.

***2.** These are values of sample and not 100% tested.

Table 15

Item	Symbol	Ta = −40°C to +85°C		Unit
		V_{CC} = 1.7 V to 5.5 V		
		Min.	Max.	
Write time	t_{PR}	−	4.0	ms

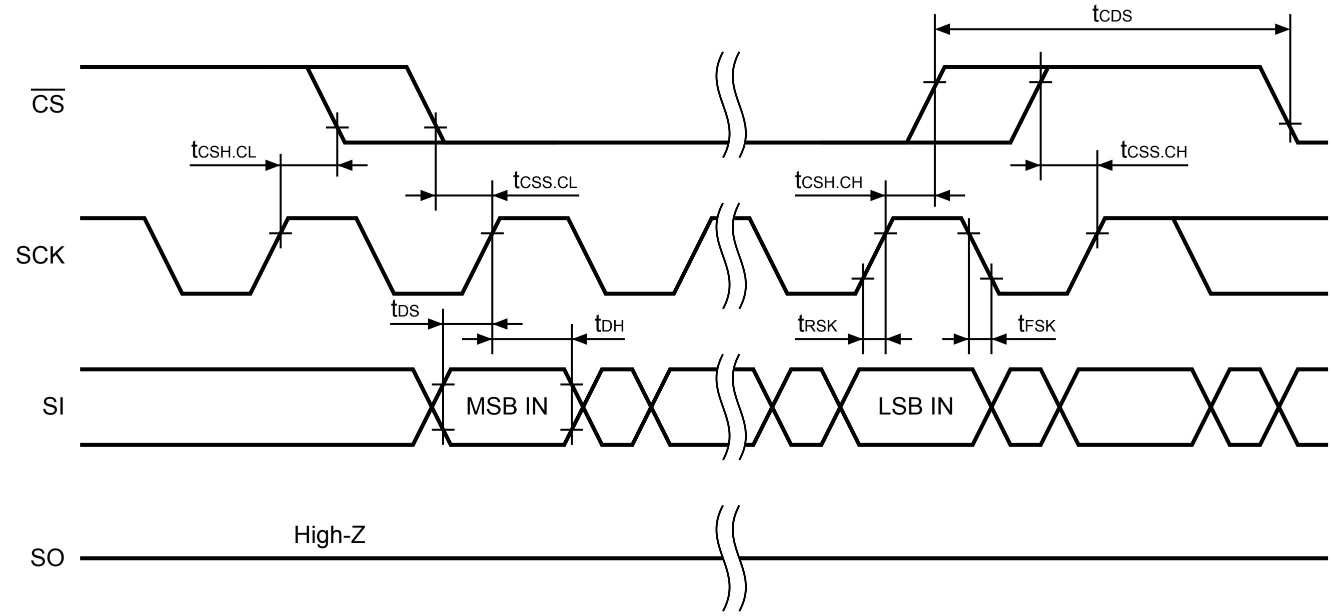

t_{CDS}
$\overline{CS}$
$t_{CSH.CL}$
$t_{CSS.CL}$
$t_{CSH.CH}$
$t_{CSS.CH}$
SCK
t_{DS}
t_{DH}
t_{RSK}
t_{FSK}
SI
MSB IN
LSB IN
High-Z
SO

Figure 6 Serial Input Timing

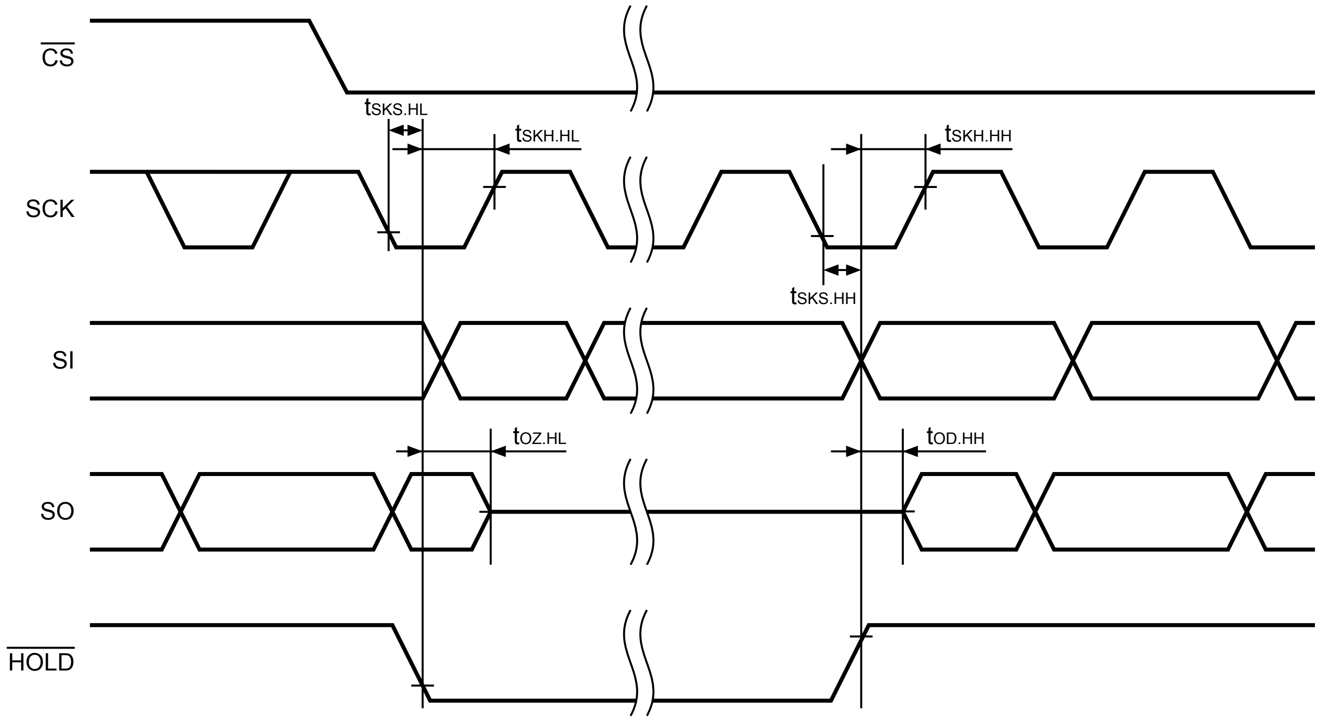

$\overline{CS}$
$t_{SKS.HL}$
$t_{SKH.HL}$
$t_{SKH.HH}$
SCK
$t_{SKS.HH}$
SI
$t_{OZ.HL}$
$t_{OD.HH}$
SO
$\overline{HOLD}$

Figure 7 Hold Timing

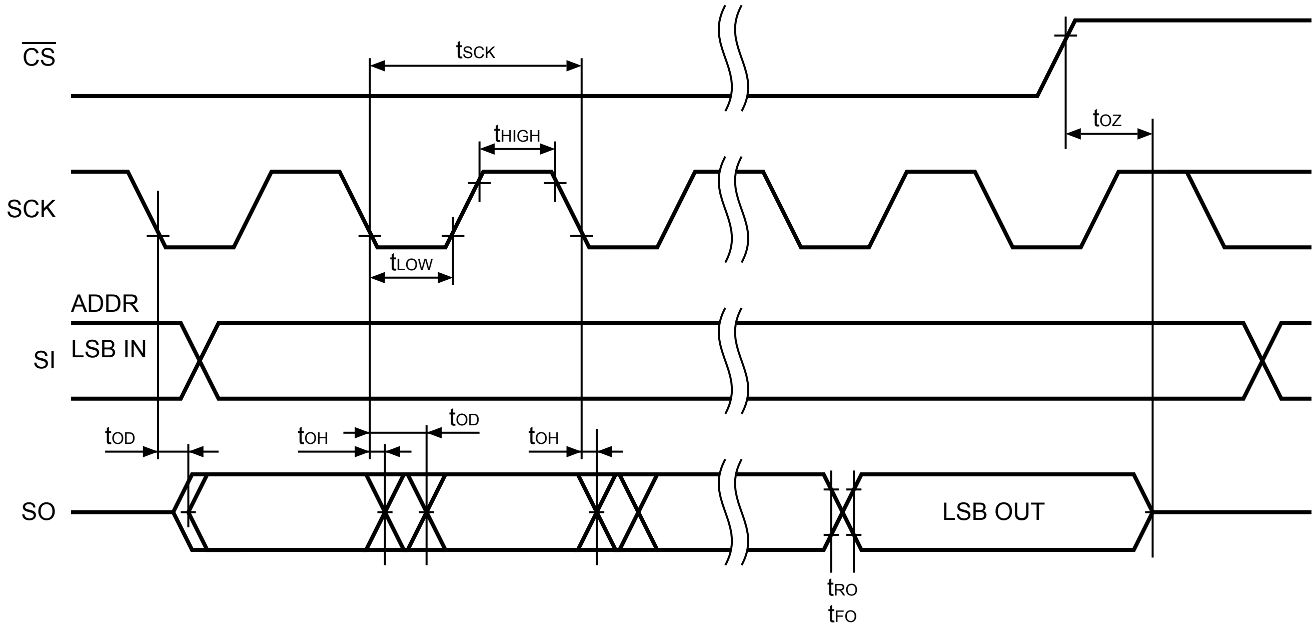

CS
SCK
ADDR
SI
LSB IN
SO
tSCK
tHIGH
tLOW
tOD
tOH
tOD
tOH
tOZ
LSB OUT
tRO
tFO

Figure 8 Serial Output Timing

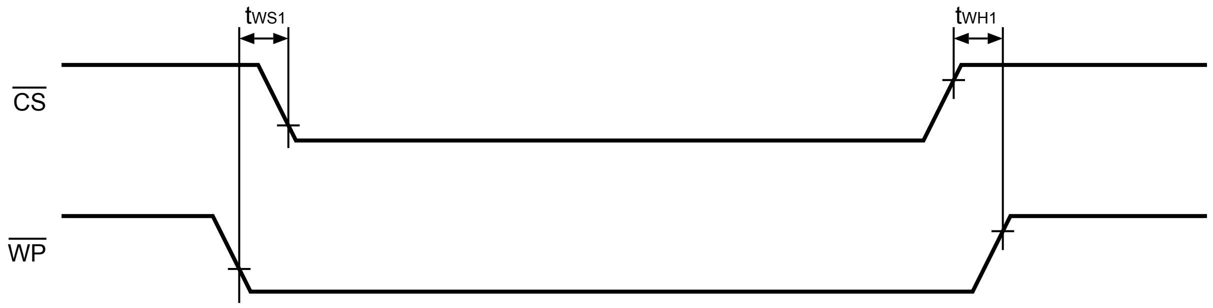

tWS1
tWH1
CS
WP

Figure 9 Valid Timing in Write Protect

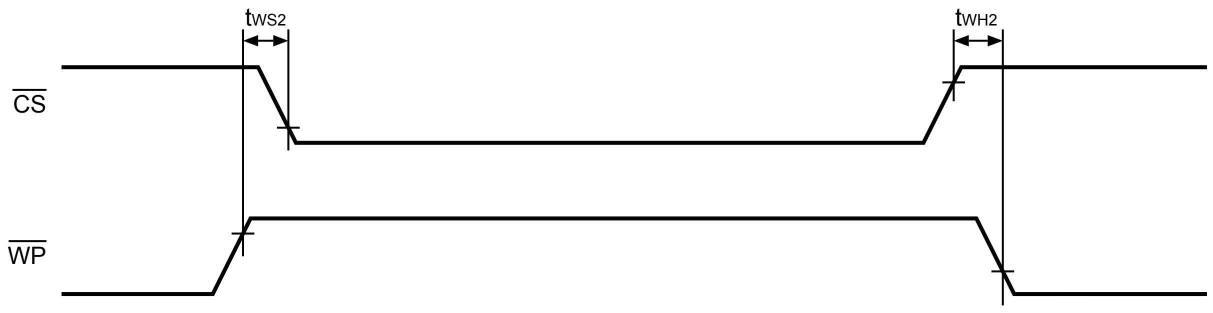

tWS2
tWH2
CS
WP

Figure 10 Invalid Timing in Write Protect

■ Pin Functions

1. $\overline{\text{CS}}$ (Chip select input) pin

This is an input pin to set a chip in the select status. In the “H” input level, the device is in the non-select status and its output is high impedance. The device is in standby as long as it is not in Write inside. The device goes in active by setting the chip select to “L”. Input any instruction code after power-on and a falling of chip select.

2. SI (Serial data input) pin

This pin is to input serial data. This pin receives an instruction code, an address and Write data. This pin latches data at rising edge of serial clock.

3. SO (Serial data output) pin

This pin is to output serial data. The data output changes at falling edge of serial clock.

4. SCK (Serial clock input) pin

This is a clock input pin to set the timing of serial data. An instruction code, an address and Write data are received at a rising edge of clock. Data is output at falling edge of clock.

5. $\overline{\text{WP}}$ (Write protect input) pin

This is an input pin to protect memory data when Write instruction (WRITE, WRSR) is being input. By setting this pin to “L”, the WEL bit in the status register is set to “L”. Therefore S-25C010A/020A/040A does not Write to the E^{2}PROM, however, it accepts other instructions. Fix this pin “H” or “L” not to set it in the floating state.
Refer to “■ **Protect Operation**” for details.

6. $\overline{\text{HOLD}}$ (HOLD input) pin

This pin is used to pause serial communications without setting the device in the non-select status.
In the hold status, the serial output goes in high impedance, the serial input and the serial clock go in “Don’t care”.
During the hold operation, be sure to set the device in active by setting the chip select ($\overline{\text{CS}}$ pin) to “L”.
Refer to “■ **Hold Operation**” for details.

■ Initial Delivery State

Initial delivery state of all addresses is “FFh”.
Moreover, initial delivery state of the status register nonvolatile memory is as follows.

- BP1 = 0
- BP0 = 0

■ Instruction Sets

Table 16 and 17 are the lists of instruction for the S-25C010A/020A/040A. The instruction is able to be input by changing the $\overline{\text{CS}}$ pin "H" to "L". Input the instruction in the MSB first. Each instruction code is organized with 1-byte as shown below.
If the S-25C010A/020A/040A receives any invalid instruction code, the device goes in the non-select status.

1. S-25C010A/020A

Table 16 Instruction Set

Instruction	Operation	Instruction Code	Address	Data
		SCK Input Clock 1 to 8	SCK Input Clock 9 to 16	SCK Input Clock 17 to 24
WREN	Write enable	0000 X110	–	–
WRDI	Write disable	0000 X100	–	–
RDSR	Read the status register	0000 X101	b7 to b0 output *1	–
WRSR	Write in the status register	0000 X001	b7 to b0 input	–
READ	Read memory data	0000 X011	A7*2 to A0	D7 to D0 output *3
WRITE	Write memory data	0000 X010	A7*2 to A0	D7 to D0 input

***1.** Sequential data reading is possible.
***2.** In the S-25C010A, A7 = Don't care because the address range is A6 to A0.
***3.** After outputting data in the specified address, data in the following address is output.

Remark X = Don't care.

2. S-25C040A

Table 17 Instruction Set

Instruction	Operation	Instruction Code	Address	Data
		SCK Input Clock 1 to 8	SCK Input Clock 9 to 16	SCK Input Clock 17 to 24
WREN	Write enable	0000 X110	–	–
WRDI	Write disable	0000 X100	–	–
RDSR	Read the status register	0000 X101	b7 to b0 output *1	–
WRSR	Write in the status register	0000 X001	b7 to b0 input	–
READ	Read memory data	0000 [A8*2] 011	A7 to A0	D7 to D0 output *3
WRITE	Write memory data	0000 [A8*2] 010	A7 to A0	D7 to D0 input

***1**. Sequential data reading is possible.
***2.** In the S-25C040A, assign bit A8 in the address into the fifth bit in an instruction code.
***3.** After outputting data in the specified address, data in the following address is output.

Remark X = Don't care.

■ Operation

1. Status register

The status register's organization is below. The status register can Write and Read by a specific instruction.

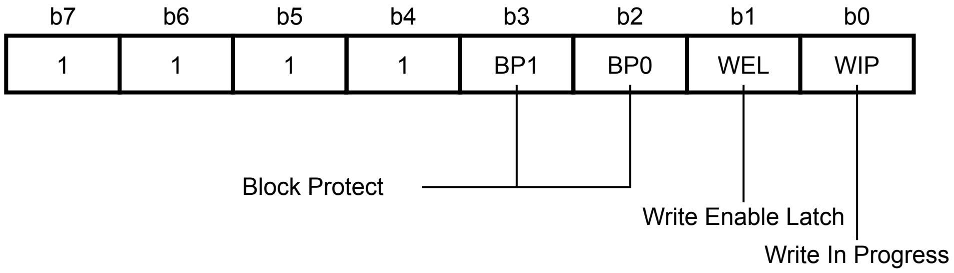


Figure 11 Organization of Status Register

The status/control bits of the status register are as follows.

1. 1 BP1, BP0 (b3, b2) : Block Protect

Bit BP1 and BP0 are composed of the nonvolatile memory. The area size of Software Protect against WRITE instruction is defined by them. Rewriting these bits is possible by the WRSR instruction. To protect the memory area against the WRITE instruction, set either or both of bit BP1 and BP0 to "1". Rewriting bit BP1 and BP0 is possible unless they are in Hardware Protect mode ($\overline{\text{WP}}$ pin is "L"). Refer to "■ **Protect Operation**" for details of "Block Protect".

1. 2 WEL (b1) : Write Enable Latch

Bit WEL shows the status of internal Write Enable Latch. Bit WEL is set by the WREN instruction only. If bit WEL is "1", this is the status that Write Enable Latch is set. If bit WEL is "0", Write Enable Latch is in reset, so that the S-25C010A/020A/040A does not receive the WRITE or WRSR instruction. Bit WEL is reset after these operations;

- The power supply voltage is dropping
- Power-on
- After performing WRDI
- After the Write operation by the WRSR instruction has completed
- After the Write operation by the WRITE instruction has completed
- After setting the $\overline{\text{WP}}$ pin to "L"

1. 3 WIP (b0) : Write In Progress

Bit WIP is Read Only and shows whether the internal memory is in the Write operation or not by the WRITE or WRSR instruction. Bit WIP is "1" during the Write operation but "0" during any other status. **Figure 12** shows the usage example.

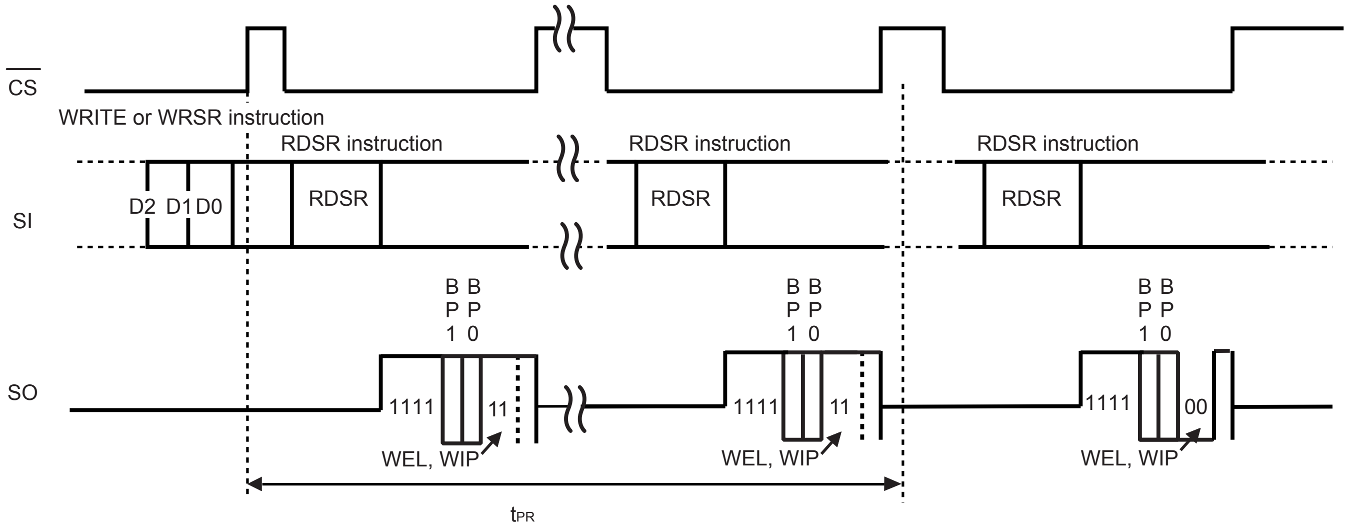
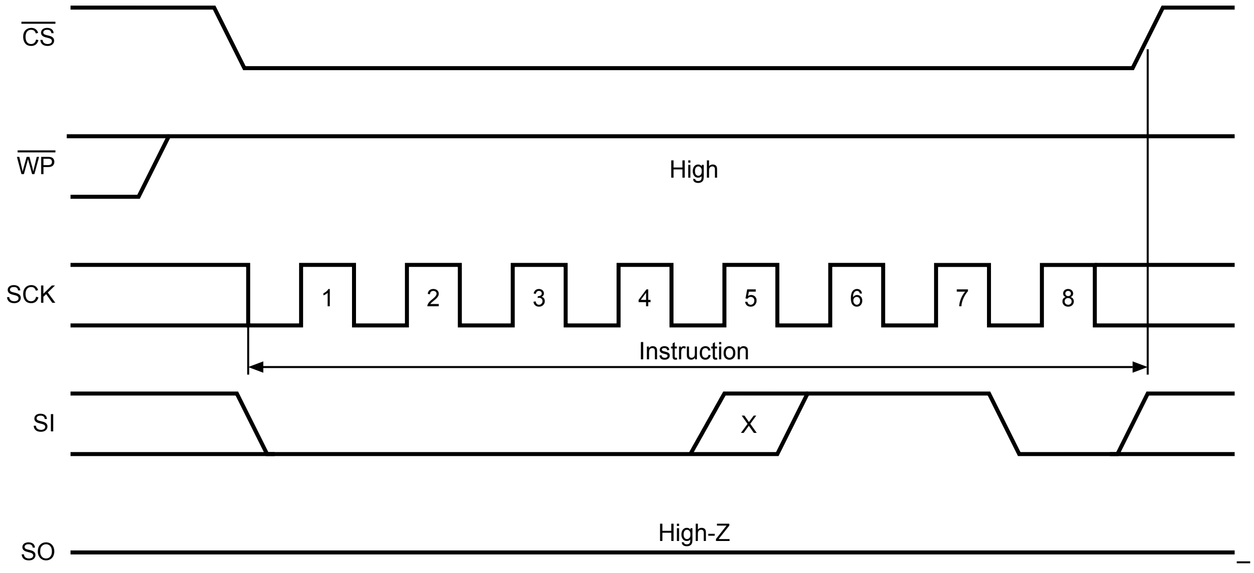

CS
WRITE or WRSR instruction
RDSR instruction
RDSR instruction
RDSR instruction
SI
D2
D1
D0
RDSR
RDSR
RDSR
B P 1
B P 0
B P 1
B P 0
B P 1
B P 0
SO
1111
11
1111
11
1111
00
WEL, WIP
WEL, WIP
WEL, WIP
tPR

Figure 12 Usage Example of WEL, WIP Bits during Write

2. Write enable (WREN)

Before writing data (WRITE and WRSR), be sure to set bit Write Enable Latch (WEL). This instruction is to set bit WEL. Its operation is below.
After selecting the device by the chip select ($\overline{\text{CS}}$), input the instruction code from serial data input (SI). To set bit WEL, set the device in the non-select status by $\overline{\text{CS}}$ at the 8th clock of the serial clock (SCK). To cancel the WREN instruction, input the clock different from a specified value (n = 8 clock) while $\overline{\text{CS}}$ is in "L".



Remark X = Don't care.

Figure 13 WREN Operation

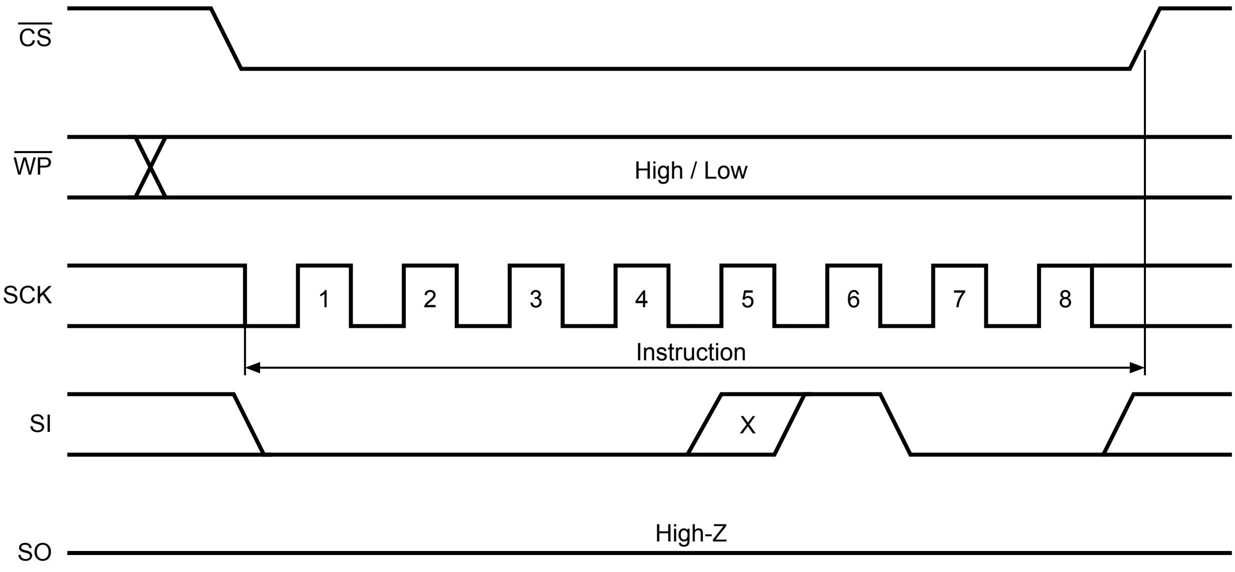
3. Write disable (WRDI)

The WRDI instruction is one of ways to reset bit Write Enable Latch (WEL). After selecting the device by the chip select ($\overline{\text{CS}}$), input the instruction code from serial data input (SI).

To reset bit WEL, set the device in the non-select status by $\overline{\text{CS}}$ at the 8th clock of the serial clock. To cancel the WRDI instruction, input the clock different from a specified value (n = 8 clock) while $\overline{\text{CS}}$ is in “L”.

Bit WEL is reset after the operations shown below.

- The power supply voltage is dropping
- Power on
- After performing WRDI
- After the completion of Write operation by the WRSR instruction
- After the completion of Write operation by the WRITE instruction
- After setting the $\overline{\text{WP}}$ pin to “L”



Remark X = Don’t care.

Figure 14 WRDI Operation

4. Read the status register (RDSR)

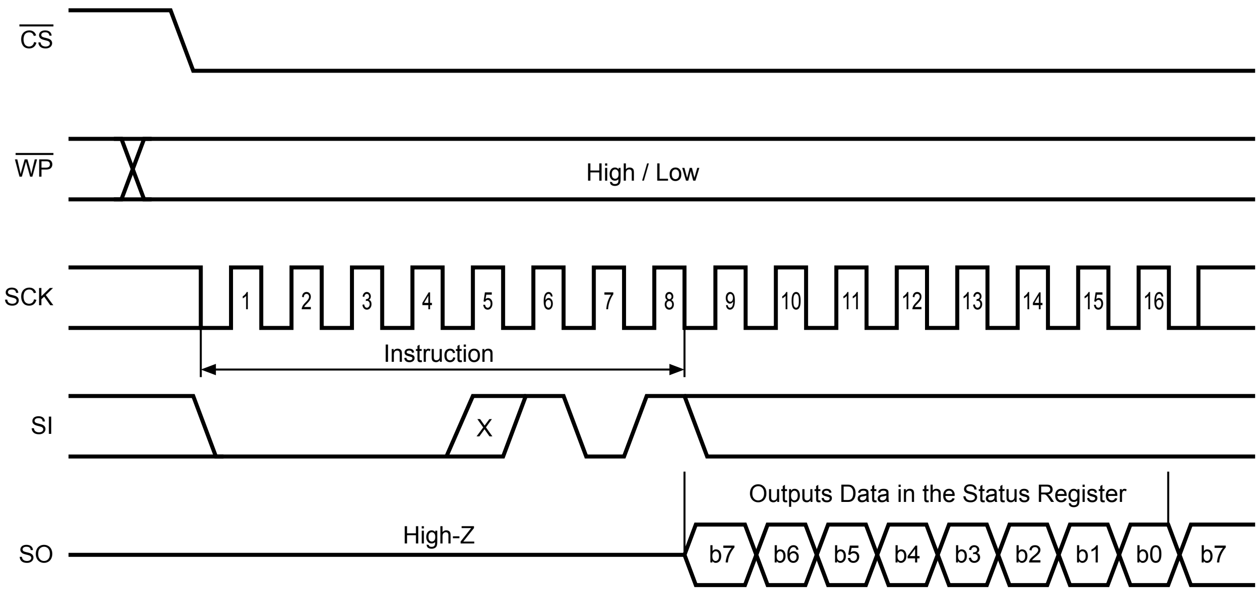
Reading data in the status register is possible by the RDSR instruction. During the Write operation, it is possible to confirm the progress by checking bit WIP.

Set the chip select ($\overline{\text{CS}}$) "L" first. After that, input the instruction code from serial data input (SI). The status of bit in the status register is output from serial data output (SO). Sequential Read is available for the status register. To stop the Read cycle, set $\overline{\text{CS}}$ to "H".

It is possible to read the status register always. The bits in it are valid and can be read by RDSR even in the Write cycle.

The 2 bits WEL and WIP are updated during the write cycle. The updated nonvolatile bits BP1 and BP0 can be acquired by performing a new RDSR instruction after verifying the completion of the write cycle.

b7, b6, b5, b4 are "1" when they are read by the RDSR instruction.

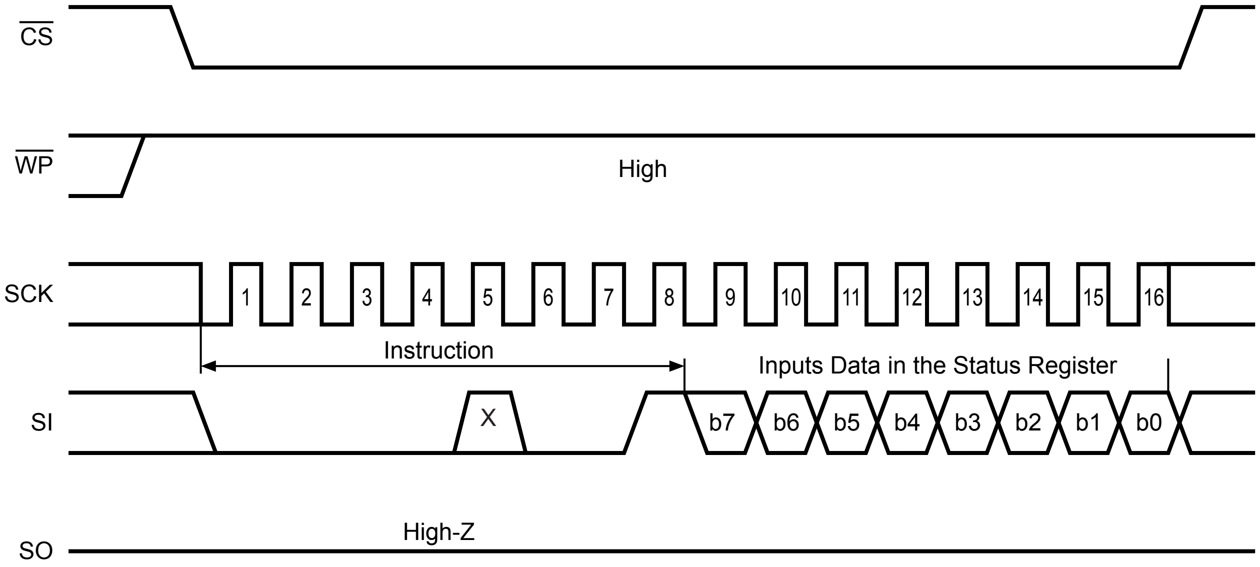

CS
WP
High / Low
SCK
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
Instruction
SI
X
Outputs Data in the Status Register
SO
High-Z
b7
b6
b5
b4
b3
b2
b1
b0
b7

Remark X = Don't care.

Figure 15 RDSR Operation

5. Write in the status register (WRSR)

The values of status register (BP1, BP0) can be rewritten by inputting the WRSR instruction. But b7, b6, b5, b4, b1, b0 of status register cannot be rewritten. b7 to b4 are always “1” when reading the status register.
Before inputting the WRSR instruction, set bit WEL by the WREN instruction. The operation of WRSR is shown below.
Set the chip select ($\overline{\text{CS}}$) “L” first. After that, input the instruction code and data from serial data input (SI). To start WRSR Write (t_{PR}), set the chip select ($\overline{\text{CS}}$) to “H” after inputting data or before inputting a rising of the next serial clock.
It is possible to confirm the operation status by reading the value of bit WIP during WRSR Write. Bit WIP is “1” during Write, “0” during any other status. Bit WEL is reset when Write is completed.
With the WRSR instruction, the values of BP1 and BP0; which determine the area size the users can handle as the Read Only memory; can be changed. But if the signal $\overline{\text{WP}}$ is in “L”, S-25C010A/020A/040A does not send the WRSR instruction (Refer to “■ **Protect Operation**”).
Bit BP1, BP0 keep the value which is the one prior to the WRSR instruction during the WRSR instruction. The newly updated value is changed when the WRSR instruction has completed.
To cancel the WRSR instruction, input the clock different from a specified value (n = 16clock) while $\overline{\text{CS}}$ is in “L”.



Remark X = Don’t care.

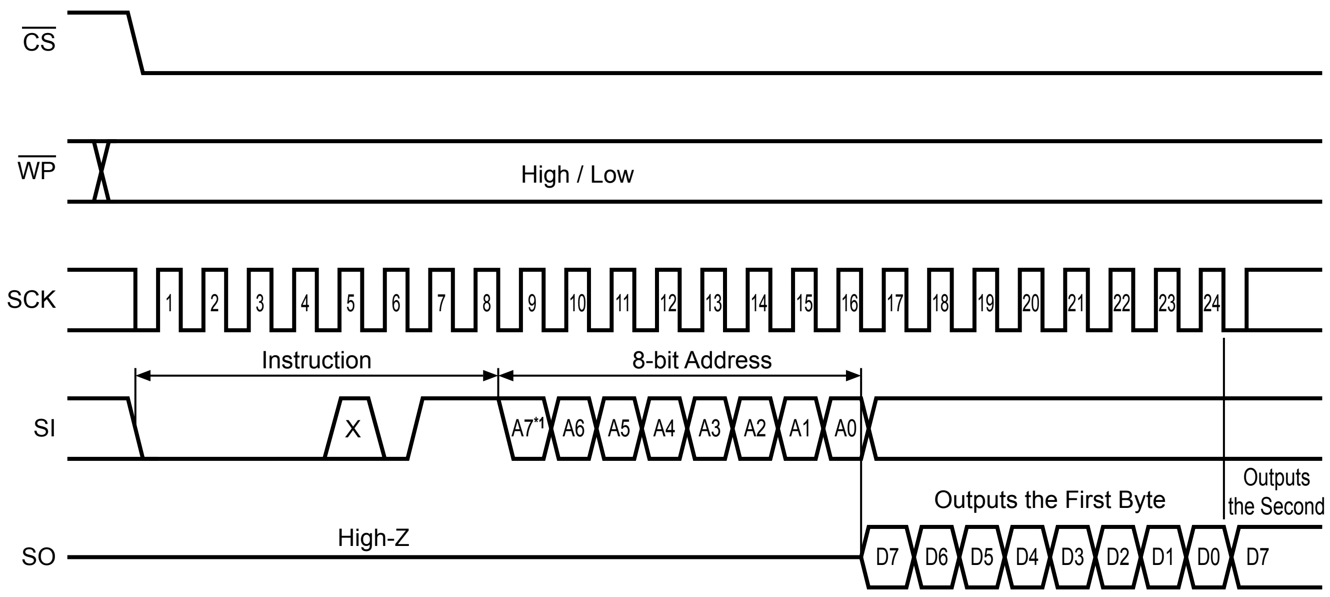
Figure 16 WRSR Operation

6. Read memory data (READ)

The Read operation is shown below. Input the instruction code and the address from serial data input (SI) after inputting "L" to the chip select ($\overline{\text{CS}}$). The input address is loaded to the internal address counter, and data in the address is output from the serial data output (SO).

Next, by inputting the serial clock (SCK) keeping the chip select ($\overline{\text{CS}}$) in "L", the address is automatically incremented so that data in the following address is sequentially output. The address counter rolls over to the first address by increment in the last address.

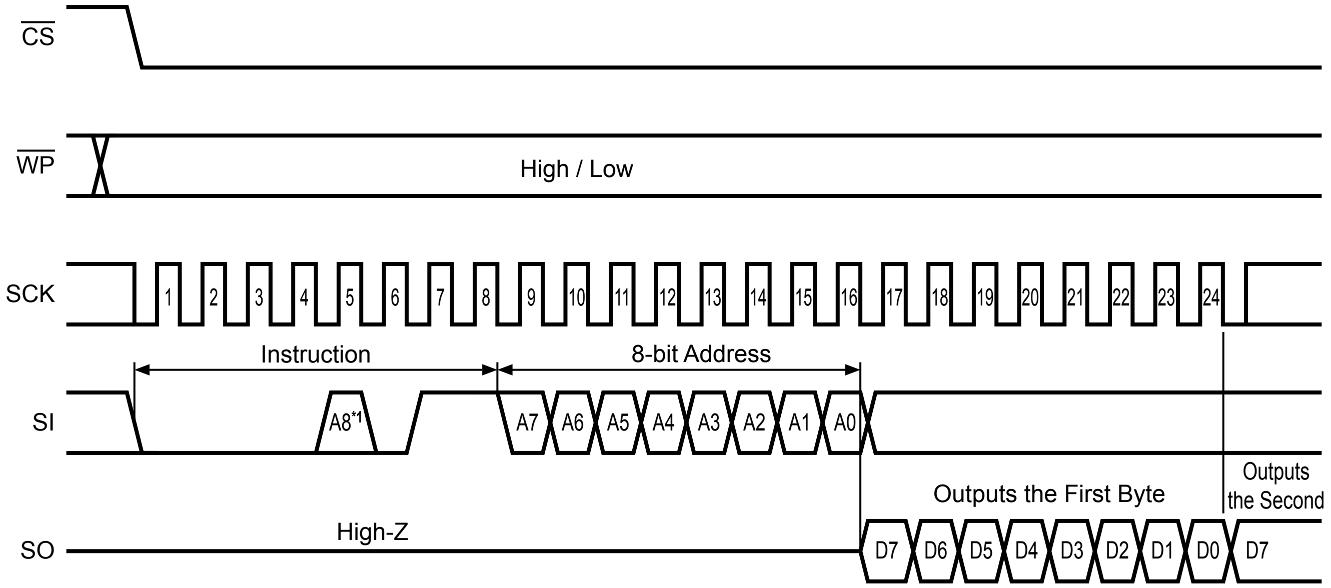
To finish the Read cycle, set $\overline{\text{CS}}$ to "H". It is possible to raise the chip select always during the cycle. During Write, the read instruction code is not be accepted or operated.


CS
WP
High / Low
SCK
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
Instruction
8-bit Address
SI
X
A7*1
A6
A5
A4
A3
A2
A1
A0
Outputs the First Byte
Outputs the Second
SO
High-Z
D7
D6
D5
D4
D3
D2
D1
D0
D7

***1** In the S-25C010A, A7 = Don't care because the address range is A6 to A0.

Remark X = Don't care.

Figure 17 READ Operation (S-25C010A/020A)


CS
WP
High / Low
SCK
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
Instruction
8-bit Address
SI
A8*1
A7
A6
A5
A4
A3
A2
A1
A0
Outputs the First Byte
Outputs the Second
SO
High-Z
D7
D6
D5
D4
D3
D2
D1
D0
D7

***1** In the S-25C040A, assign bit A8 in the address into the fifth bit in an instruction code.

Figure 18 READ Operation (S-25C040A)

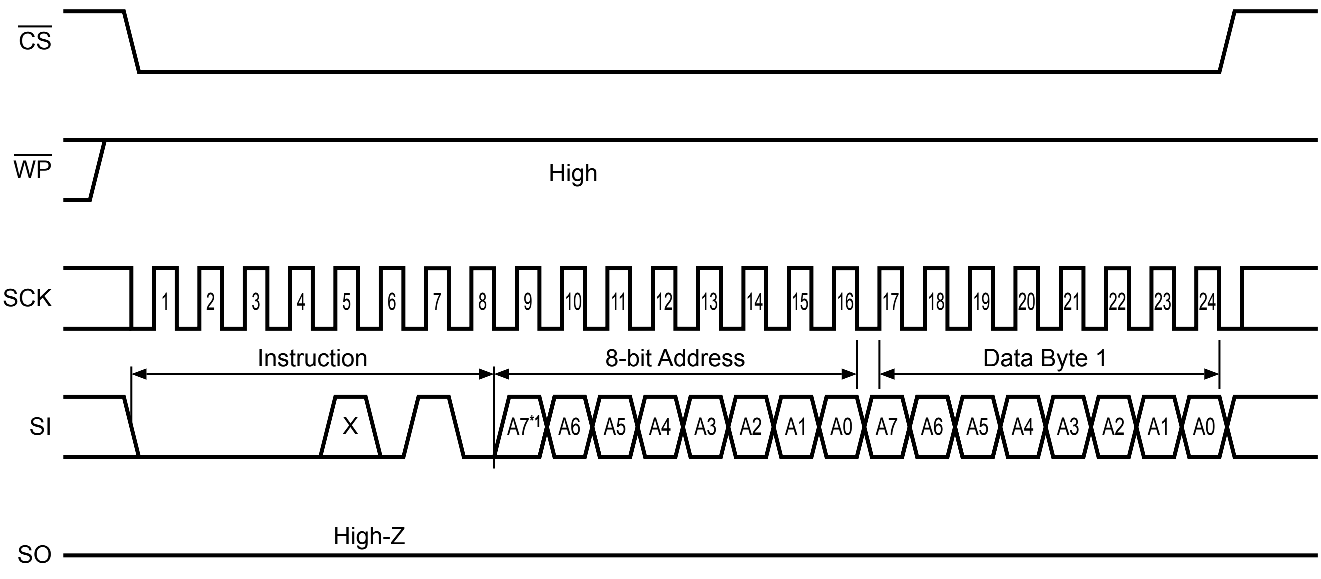
7. Write memory data (WRITE)

Figure 19 and 20 show the timing chart when inputting 1-byte data. Input the instruction code, the address and data from serial data input (SI) after inputting “L” to the chip select ($\overline{\text{CS}}$). To start Write (t_{PR}), set the chip select ($\overline{\text{CS}}$) to “H” after inputting data or before inputting a rising of the next serial clock. Bit WIP is reset to “0” when Write has completed.
The S-25C010A/020A/040A can Page Write of 16 bytes. Its function to transmit data is as same as Byte Write basically, but it operates Page Write by receiving sequential 8-bit Write data as much data as page size has. Input the instruction code, the address and data from serial data input (SI) after inputting “L” in $\overline{\text{CS}}$, as the WRITE operation (page) shown in **Figure 21 and 22**. Input the next data while keeping $\overline{\text{CS}}$ in “L”. After that, repeat inputting data of 8-bit sequentially. At the end, by setting $\overline{\text{CS}}$ to “H”, the WRITE operation starts (t_{PR}).
4 of the lower bits in the address are automatically incremented every time when receiving Write data of 8-bit. Thus, even if Write data exceeds 16 bytes, the higher bits in the address do not change. And 4 of lower bits in the address roll over so that Write data which is previously input is overwritten.

These are cases when the WRITE instruction is not accepted or operated.

- Bit WEL is not set to “1” (not set to “1” beforehand immediately before the WRITE instruction)
- During Write
- The address to be written is in the protect area by BP1 and BP0.
- The signal $\overline{\text{WP}}$ is in “L”.

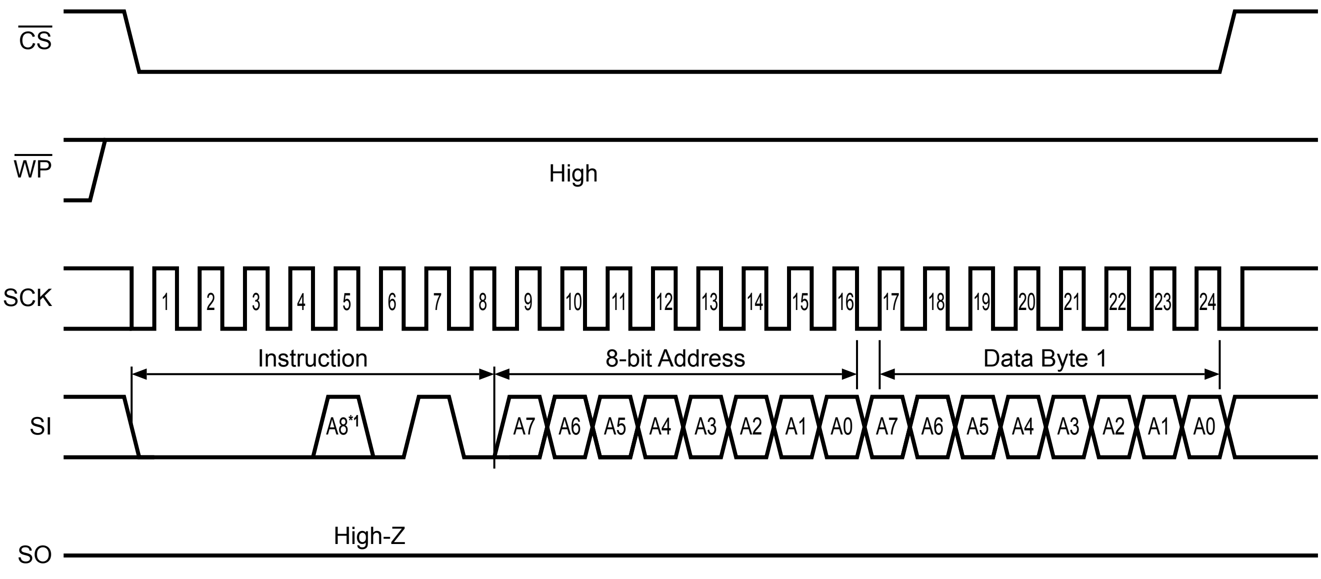
To cancel the WRITE instruction, input the clock different from a specified value (n = 16+m × 8clock) while $\overline{\text{CS}}$ is in “L”.


CS
WP
High
SCK
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
Instruction
8-bit Address
Data Byte 1
SI
X
A7*1
A6
A5
A4
A3
A2
A1
A0
A7
A6
A5
A4
A3
A2
A1
A0
SO
High-Z

***1** In the S-25C010A, A7 = Don’t care because the address range is A6 to A0.

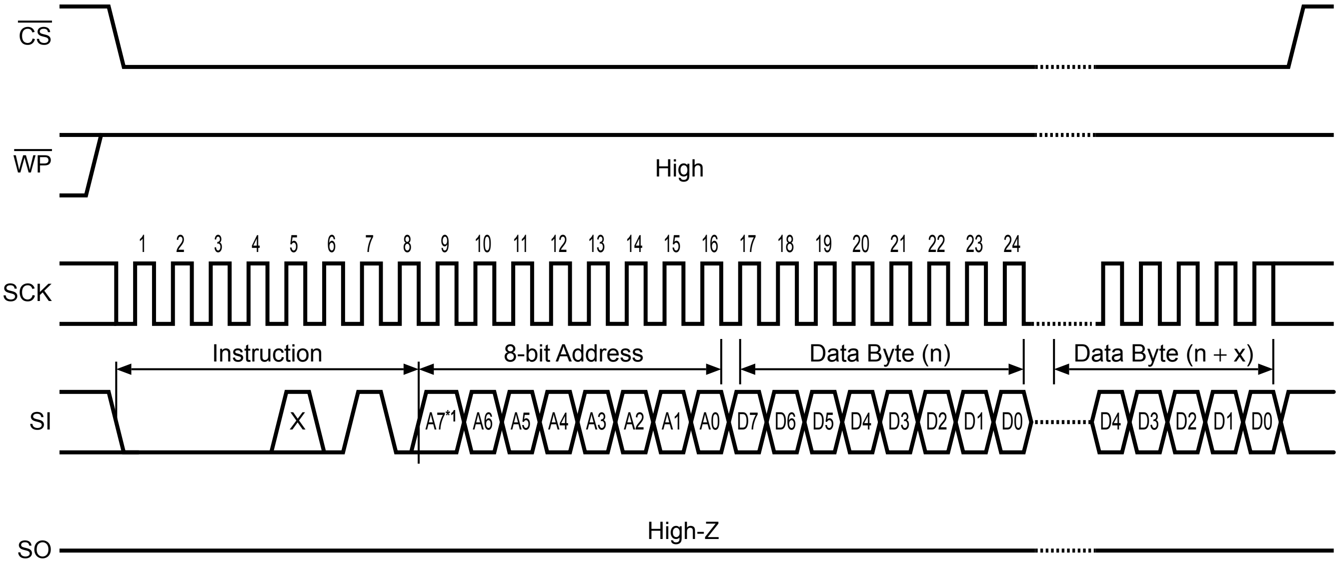
Remark X = Don’t care.

Figure 19 WRITE Operation (1-byte) (S-25C010A/020A)


CS
WP
High
SCK
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
Instruction
8-bit Address
Data Byte 1
SI
A8*1
A7
A6
A5
A4
A3
A2
A1
A0
A7
A6
A5
A4
A3
A2
A1
A0
SO
High-Z

***1** In the S-25C040A, assign bit A8 in the address into the fifth bit in an instruction code.

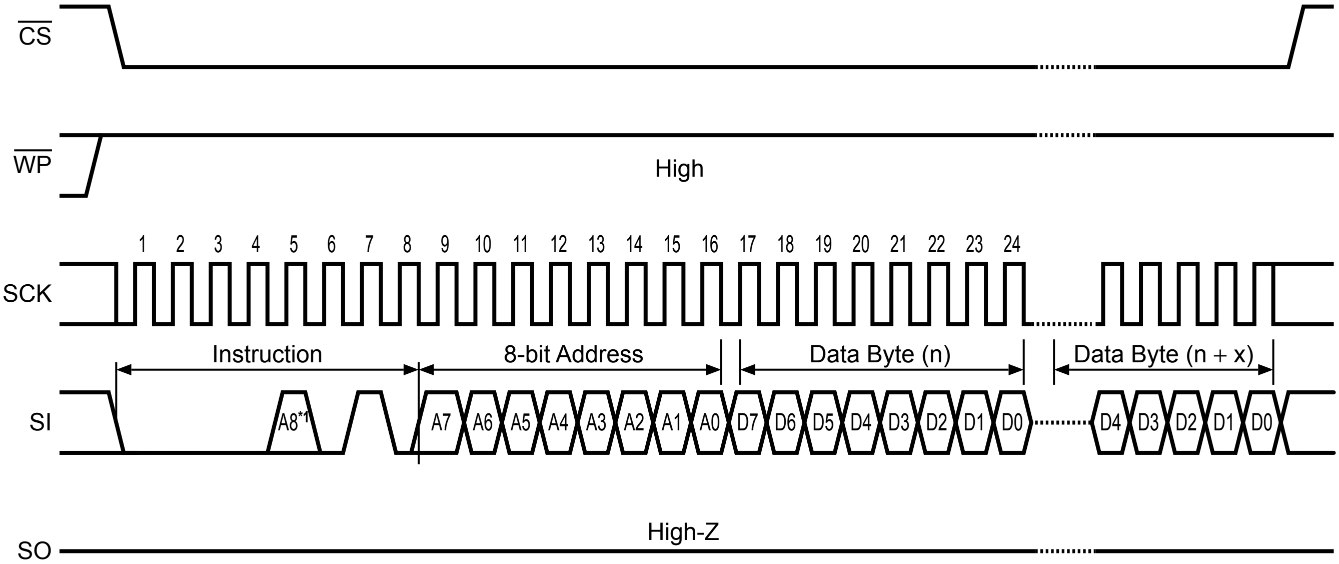
Figure 20 WRITE Operation (1-byte) (S-25C040A)


CS
WP
High
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
SCK
Instruction
8-bit Address
Data Byte (n)
Data Byte (n + x)
SI
X
A7*1 A6 A5 A4 A3 A2 A1 A0 D7 D6 D5 D4 D3 D2 D1 D0
D4 D3 D2 D1 D0
SO
High-Z

***1** In the S-25C010A, A7 = Don’t care because the address range is A6 to A0.

Remark X = Don’t care.

Figure21 WRITE Operation (page) (S-25C010A/020A)


CS
WP
High
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
SCK
Instruction
8-bit Address
Data Byte (n)
Data Byte (n + x)
SI
A8*1
A7 A6 A5 A4 A3 A2 A1 A0 D7 D6 D5 D4 D3 D2 D1 D0
D4 D3 D2 D1 D0
SO
High-Z

***1** In the S-25C040A, assign bit A8 in the address into the fifth bit in an instruction code.

Figure22 WRITE Operation (page) (S-25C040A)

■ Protect Operation

Table 18 shows the block settings of Write protect. Setting value in Protect Bit (BP1, BP0) in the status register protects data in the area of all/50%/25% of the memory address.
Setting signal $\overline{\text{WP}}$ to "L" provides the following settings.

- Write protect for the WRITE, WRSR instructions
- Reset bit WEL

Figure 9 and **10** show the Valid timing in Write protect and Invalid timing in Write protect.

Table 18 Block Settings of Write Protect

Status Register		Area of Write Protect	Address of Write Protect Block		
BP1	BP0		S-25C040A	S-25C020A	S-25C010A
0	0	0 %	None	None	None
0	1	25 %	180h to 1FFh	C0h to FFh	60h to 7Fh
1	0	50 %	100h to 1FFh	80h to FFh	40h to 7Fh
1	1	100 %	000h to 1FFh	00h to FFh	00h to 7Fh

■ Hold Operation

The hold operation is used to pause serial communications without setting the device in the non-select status. In the hold status, the serial data output goes in high impedance, and both of the serial data input and the serial clock go in "Don't care". Be sure to set the chip select ($\overline{\text{CS}}$) to "L" to set the device in the select status during the hold status.

Generally, during the hold status, the device holds the select status. But if setting the device in the non-select status, the users can finish the operation even in progress.

Figure 23 shows the hold operation. Set Hold ($\overline{\text{HOLD}}$) to "L" when the serial clock (SCK) is in "L", Hold ($\overline{\text{HOLD}}$) is switched at the same time the hold status starts. If setting Hold ($\overline{\text{HOLD}}$) to "H", Hold ($\overline{\text{HOLD}}$) is switched at the same time the hold status ends.

Set Hold ($\overline{\text{HOLD}}$) to "L" when the serial clock (SCK) is in "H"; the hold status starts when the serial clock goes in "L" after Hold ($\overline{\text{HOLD}}$) is switched. If setting Hold ($\overline{\text{HOLD}}$) to "H", the hold status ends when the serial clock goes in "L" after Hold ($\overline{\text{HOLD}}$) is switched.

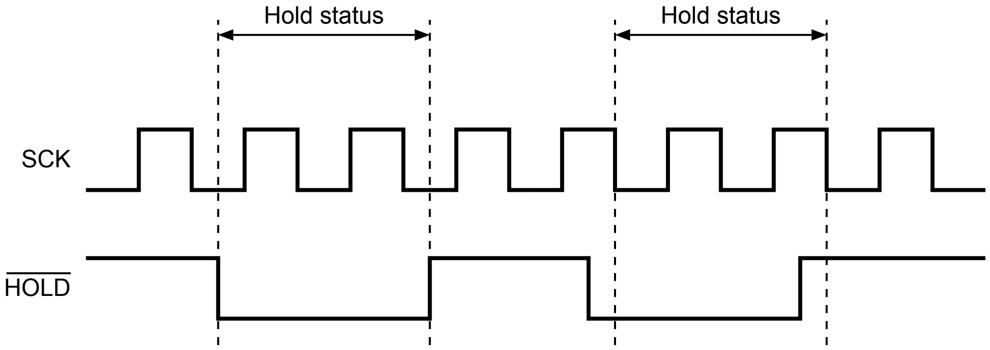


Figure 23 Hold Operation

■ Write Protect Function during the Low Power Supply Voltage

The S-25C010A/020A/040A has a built-in detection circuit which operates with the low power supply voltage. The S-25C010A/020A/040A cancels the Write operation (WRITE, WRSR) when the power supply voltage drops and power-on, at the same time, goes in the Write protect status (WRDI) automatically to reset bit WEL. Its detection and release voltages are 1.20 V typ. (Refer to **Figure 24**).
To operate Write, after the power supply voltage dropped once but rose to the voltage level which allows Write again, be sure to set the Write Enable Latch bit (WEL) before operating Write (WRITE, WRSR).
In the Write operation, data in the address written during the low power supply voltage is not assured.

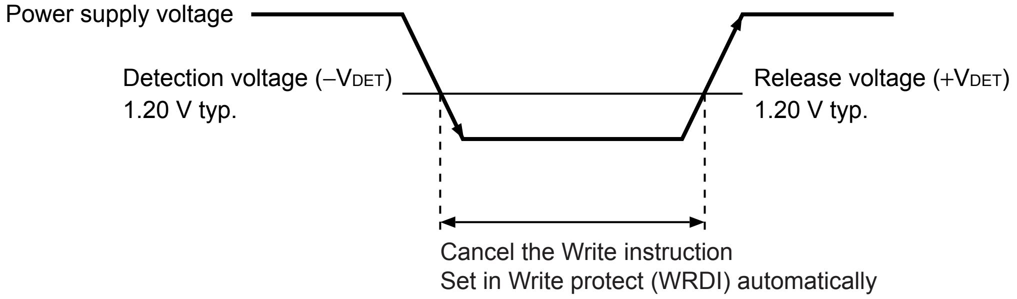

Power supply voltage
Detection voltage (–V_{DET})
1.20 V typ.
Release voltage (+V_{DET})
1.20 V typ.
Cancel the Write instruction
Set in Write protect (WRDI) automatically

Figure 24 Operation during Low Power Supply Voltage

■ Input Pin and Output Pin

1. Connection of input pin

All input pins in the S-25C010A/020A/040A have the CMOS structure. Do not set these pins in high impedance during operation when you design. Especially, set the $\overline{\text{CS}}$ input in the non-select status "H" during power-on/off and standby. The error Write does not occur as long as the $\overline{\text{CS}}$ pin is in the non-select status "H". Set the $\overline{\text{CS}}$ pin to V_{CC} via a resistor (the pull-up resistor of 10 kΩ to 100 kΩ).
If the $\overline{\text{CS}}$ pin and the SCK pin change from "L" to "H" simultaneously, data may be input from the SI pin.
To prevent the error for sure, it is recommended to pull down the SCK pin to GND. In addition, it is recommended to pull up the SI pin, the $\overline{\text{WP}}$ pin and the $\overline{\text{HOLD}}$ pin to V_{CC}, or pull down these pins to GND, respectively. Connecting the $\overline{\text{WP}}$ pin and the $\overline{\text{HOLD}}$ pin to V_{CC} directly is also possible when these pins are not in use.

2. Equivalent circuit of input pin and output

Figure 25 and **26** show the equivalent circuits of input pins in the S-25C010A/020A/040A. A pull-up and pull-down elements are not included in each input pin, pay attention not to set it in the floating state when you design.
Figure 27 shows the equivalent circuit of the output pin. This pin has the tri-state output of "H" level / "L" level / High-Z.

2. 1 Input pin

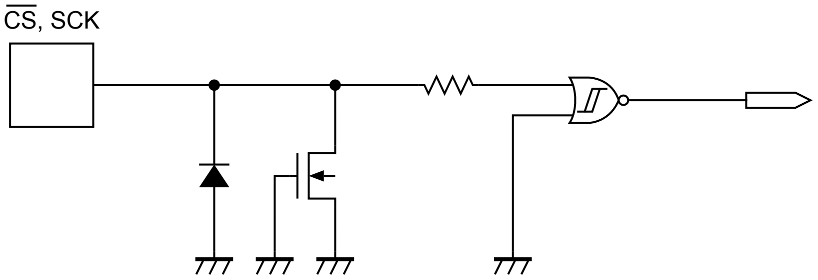


Figure 25 $\overline{\text{CS}}$, SCK Pin

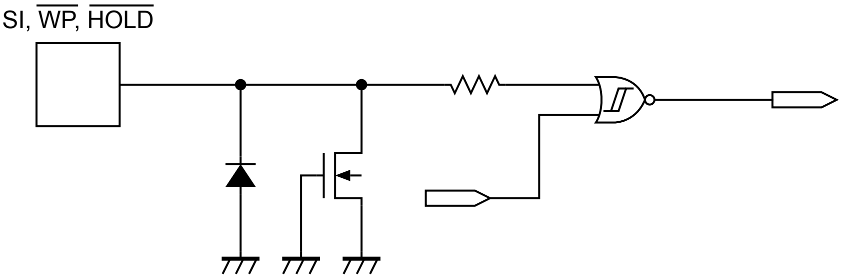


Figure 26 SI, $\overline{\text{WP}}$, $\overline{\text{HOLD}}$ Pin

2. 2 Output pin

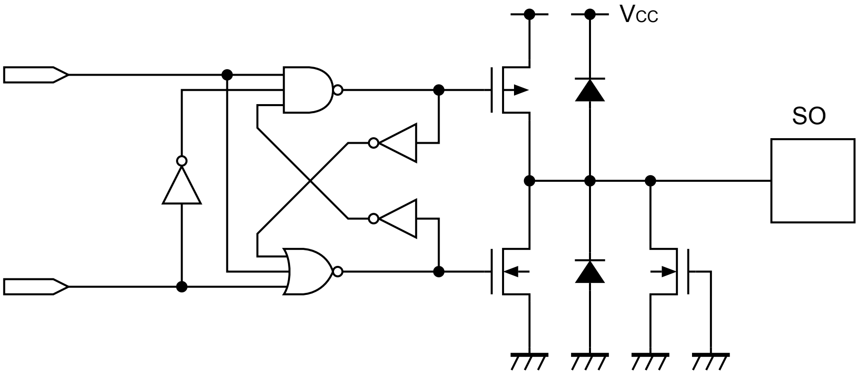


Figure 27 SO Pin

3. Precautions for use

- Absolute maximum ratings: Do not operate these ICs in excess of the absolute maximum ratings (as listed on the data sheet). Exceeding the supply voltage rating can cause latch-up. Perform operations after confirming the detailed operation condition in the data sheet.

- Operations with moisture on the S-25C010A/020A/040A pins may occur malfunction by short-circuit between pins. Especially, in occasions like picking the S-25C010A/020A/040A up from low temperature tank during the evaluation. Be sure that not remain frost on the S-25C010A/020A/040A pin to prevent malfunction by short-circuit.
  Also attention should be paid in using on environment, which is easy to dew for the same reason.

■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

■ Product Name Structure

1. Product name

1. 1 8-Pin SOP (JEDEC), 8-Pin TSSOP

S-25Cxxxx 0I - xxxx x

Environmental code
U: Lead-free (Sn 100%), halogen-free
G: Lead-free (for details, please contact our sales office)

Package name (abbreviation) and IC packing specification
J8T1: 8-Pin SOP (JEDEC) , Tape
T8T1: 8-Pin TSSOP, Tape

Fixed

Product name
S-25C010A: 1 K-bit
S-25C020A: 2 K-bit
S-25C040A: 4 K-bit

1. 2 TMSOP-8, SNT-8A

S-25Cxxxx 0I - xxxx U

Environmental code
U: Lead-free (Sn 100%), halogen-free

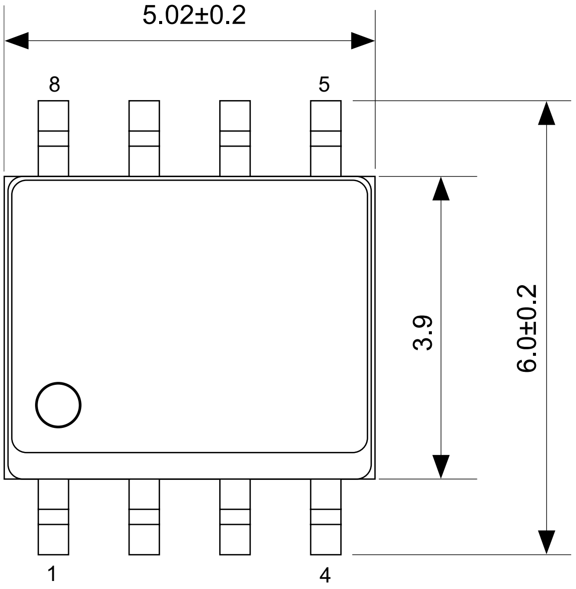
Package name (abbreviation) and IC packing specification
K8T3: TMSOP-8, Tape
I8T1: SNT-8A, Tape

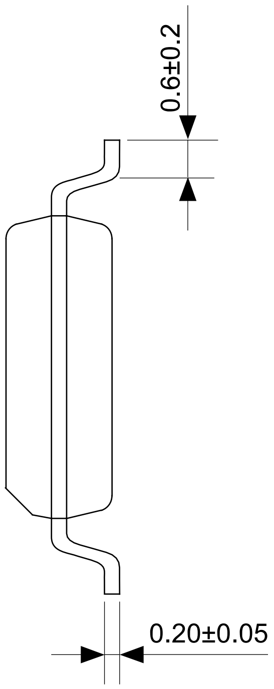
Fixed

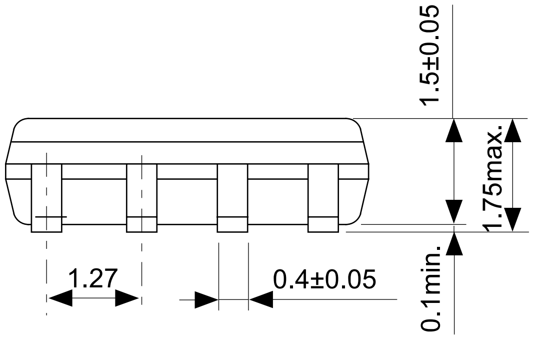
Product name
S-25C010A: 1 K-bit
S-25C020A: 2 K-bit
S-25C040A: 4 K-bit

2. Packages

Package Name		Drawing Code			
		Package	Tape	Reel	Land
8-Pin SOP (JEDEC)	Environmental code = G	FJ008-A-P-SD	FJ008-D-C-SD	FJ008-D-R-SD	−
	Environmental code = U	FJ008-Z-P-SD	FJ008-Z-C-SD	FJ008-Z-R-SD	−
8-Pin TSSOP	Environmental code = G	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-SD	−
	Environmental code = U	FT008-Z-P-SD	FT008-Z-C-SD	FT008-Z-R-SD	−
TMSOP-8		FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD	−
SNT-8A		PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD


5.02±0.2
8
5
3.9
6.0±0.2
1
4

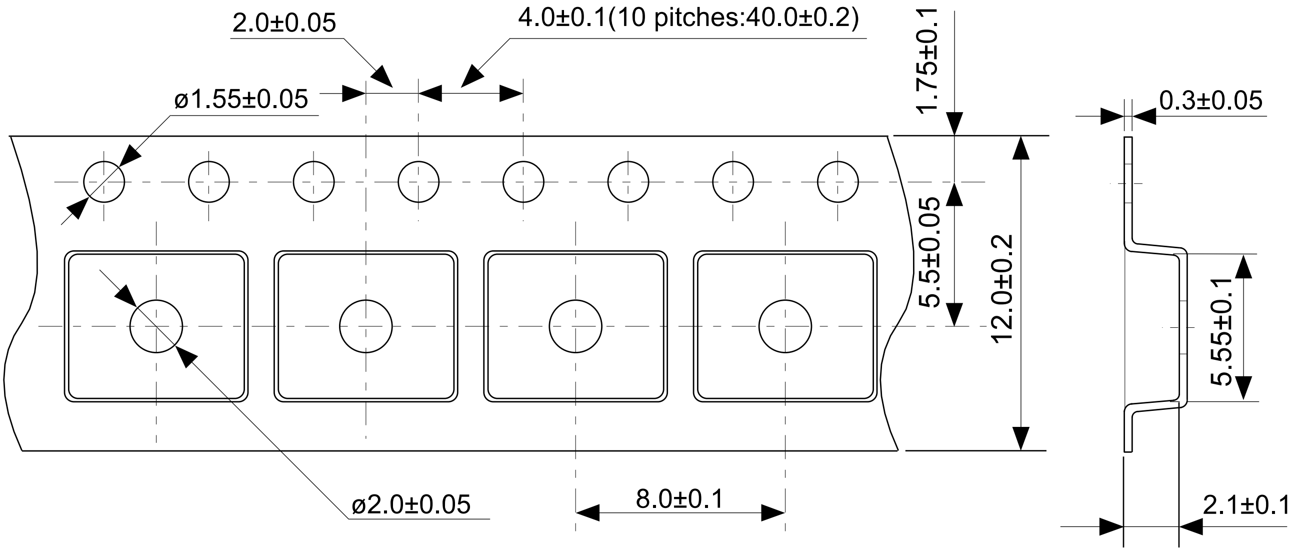

0.6±0.2
0.20±0.05

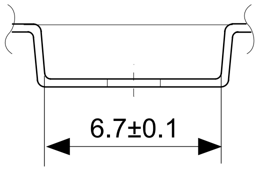

1.5±0.05
1.75max.
1.27
0.4±0.05
0.1min.

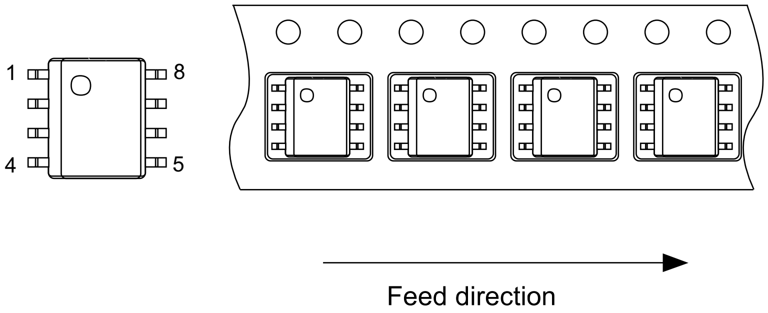
No. FJ008-A-P-SD-2.2

TITLE	SOP8J-D-PKG Dimensions
No.	FJ008-A-P-SD-2.2
ANGLE	
UNIT	mm

ABLIC Inc.

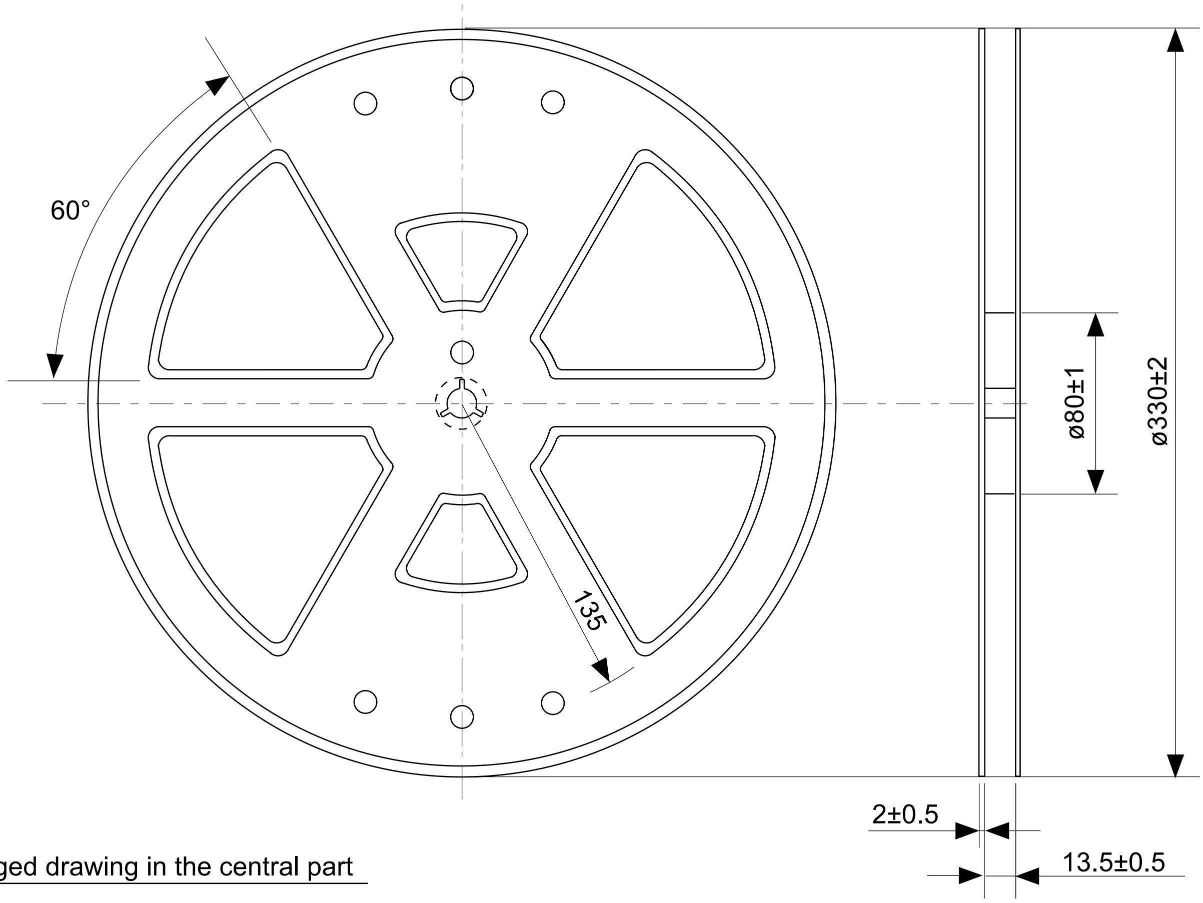

2.0±0.05
4.0±0.1(10 pitches:40.0±0.2)
1.75±0.1
ø1.55±0.05
0.3±0.05
5.5±0.05
12.0±0.2
5.55±0.1
ø2.0±0.05
8.0±0.1
2.1±0.1



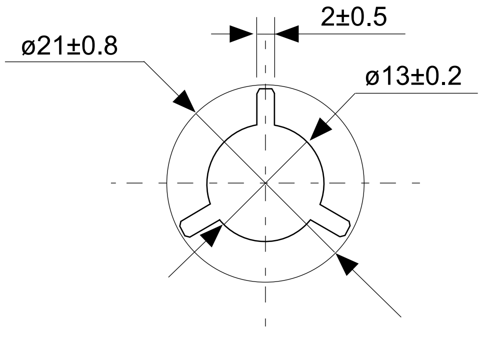

1
8
4
5
Feed direction

No. FJ008-D-C-SD-1.1

TITLE	SOP8J-D-Carrier Tape
No.	FJ008-D-C-SD-1.1
ANGLE	
UNIT	mm
	ABLIC Inc.


60°
135
ø80±1
ø330±2
2±0.5
13.5±0.5

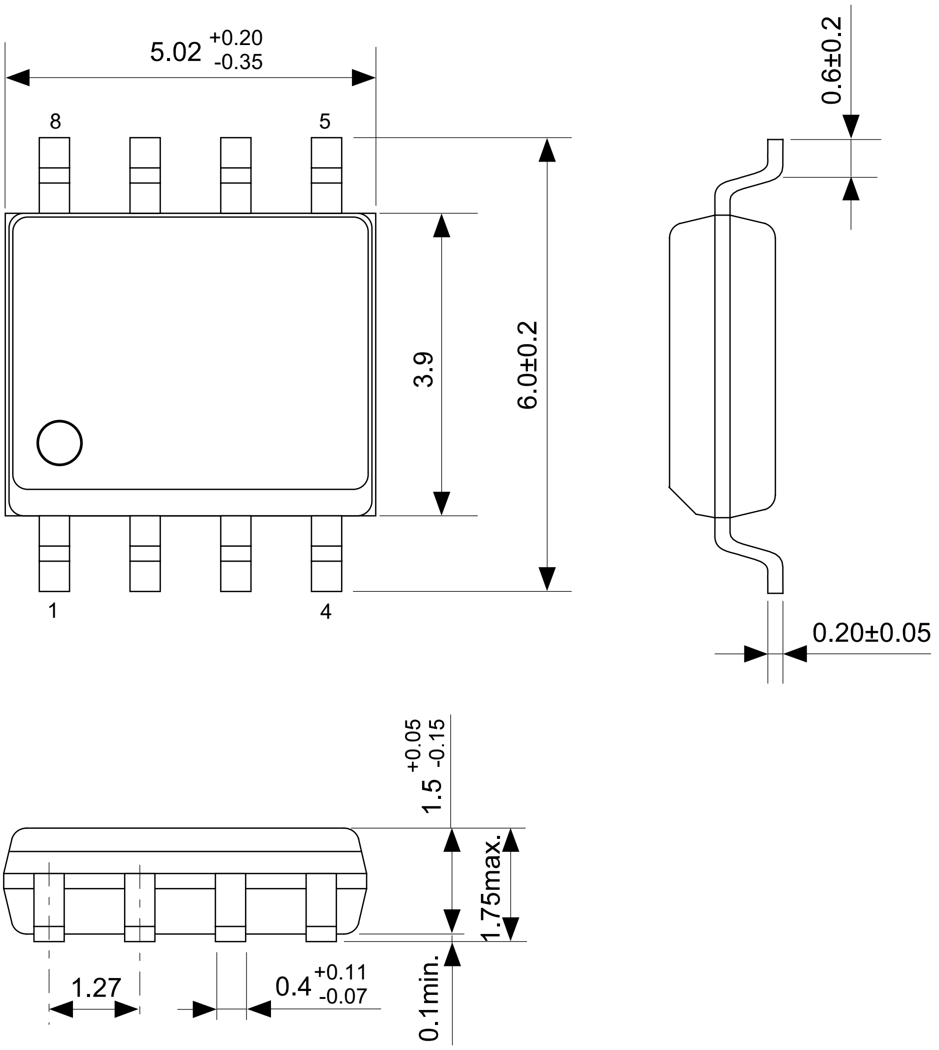
Enlarged drawing in the central part


2±0.5
ø21±0.8
ø13±0.2

No. FJ008-D-R-SD-1.1

TITLE	SOP8J-D-Reel		
No.	FJ008-D-R-SD-1.1		
ANGLE		QTY.	2,000
UNIT	mm		

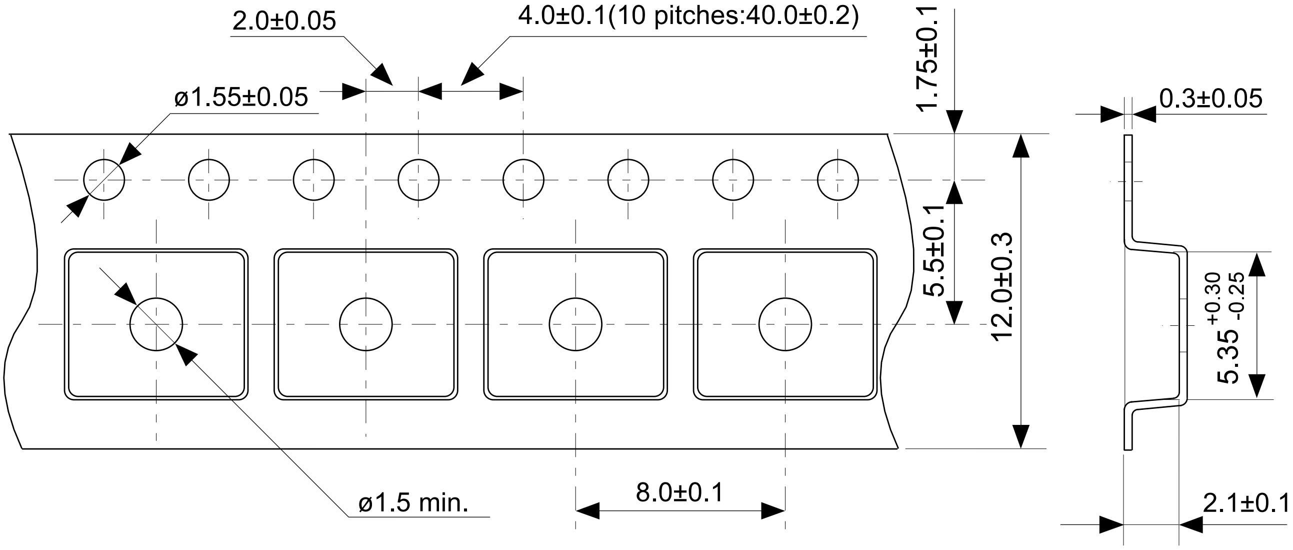
ABLIC Inc.

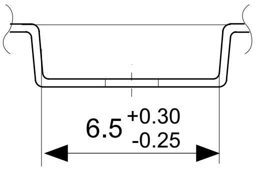

5.02 +0.20 -0.35
8
5
1
4
3.9
6.0±0.2
0.6±0.2
0.20±0.05
1.5 +0.05 -0.15
1.75max.
1.27
0.4 +0.11 -0.07
0.1min.

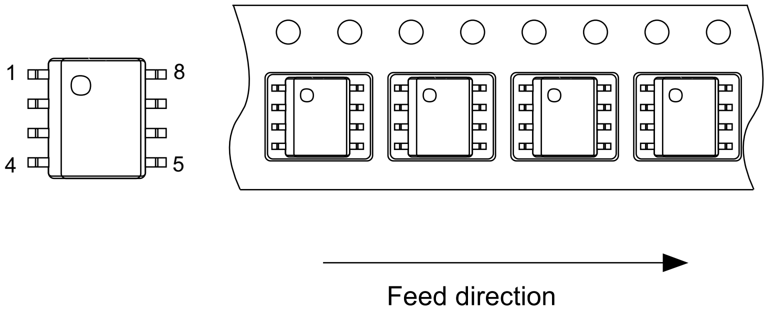
No. FJ008-Z-P-SD-2.1

TITLE	SOP8J-Z-PKG Dimensions
No.	FJ008-Z-P-SD-2.1
ANGLE	
UNIT	mm

ABLIC Inc.

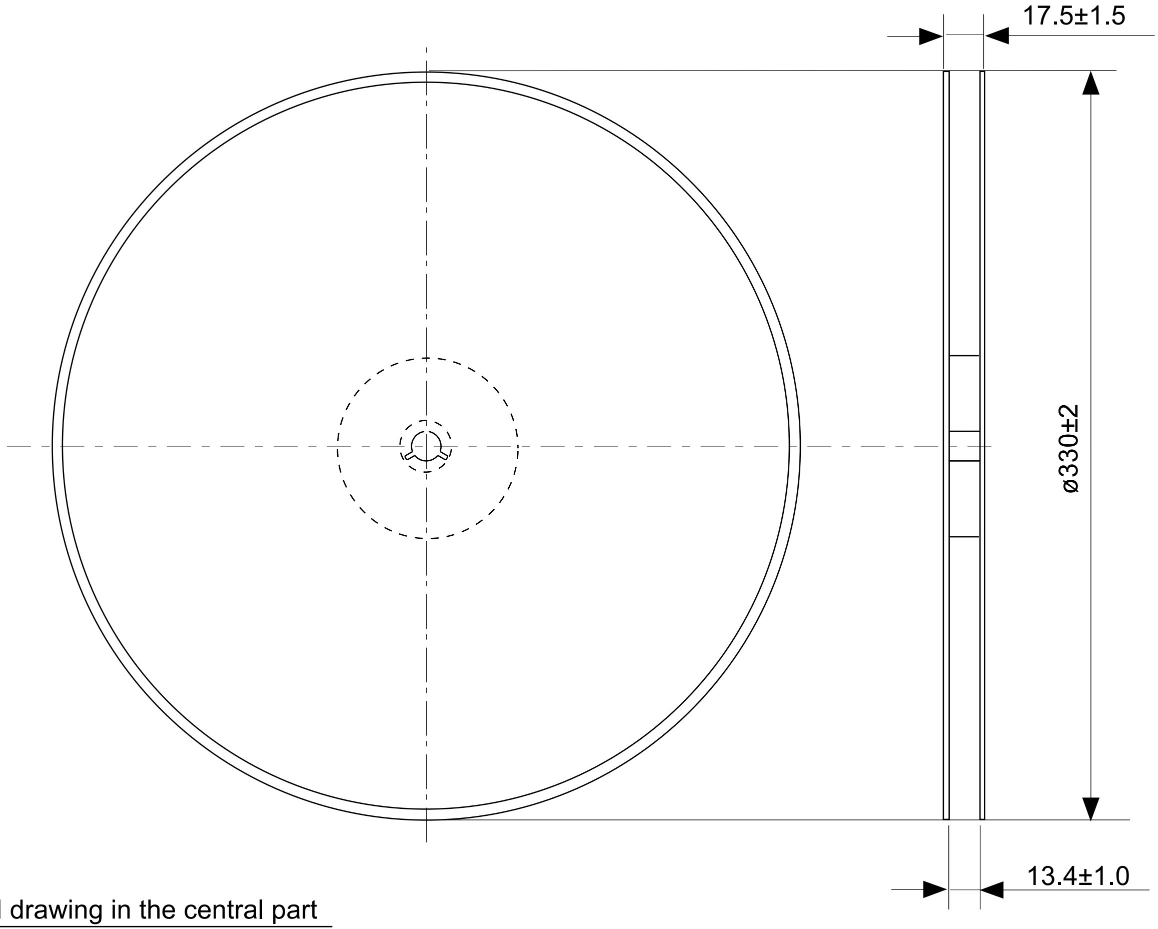

2.0±0.05
4.0±0.1(10 pitches:40.0±0.2)
ø1.55±0.05
1.75±0.1
0.3±0.05
5.5±0.1
12.0±0.3
5.35 +0.30 -0.25
ø1.5 min.
8.0±0.1
2.1±0.1



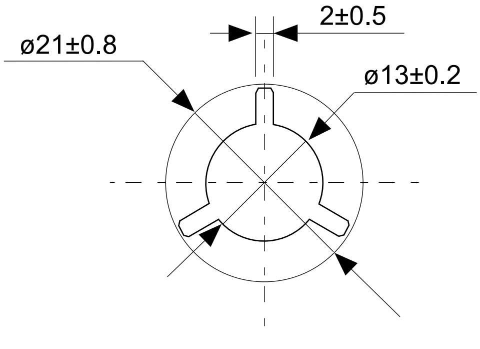

1
8
4
5
Feed direction

No. FJ008-Z-C-SD-1.0

TITLE	SOP8J-Z-Carrier Tape
No.	FJ008-Z-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

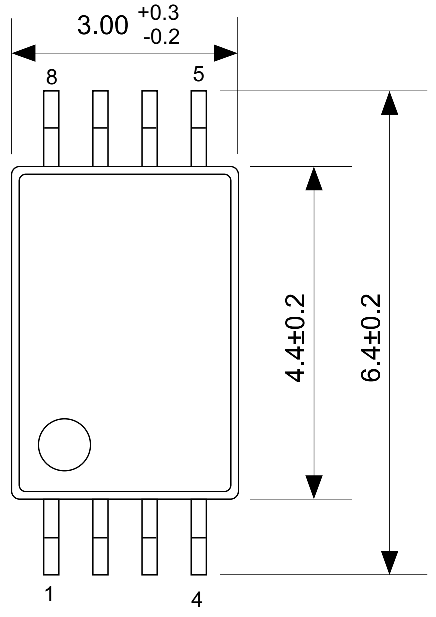

17.5±1.5
ø330±2
13.4±1.0

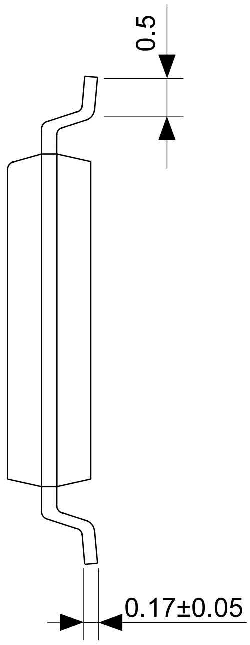
Enlarged drawing in the central part

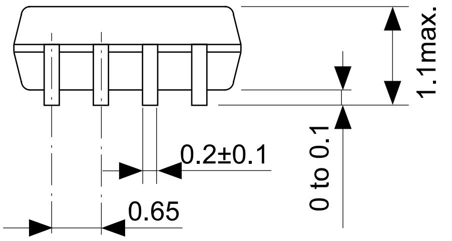

2±0.5
ø21±0.8
ø13±0.2

No. FJ008-Z-R-SD-1.0

TITLE	SOP8J-Z-Reel		
No.	FJ008-Z-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

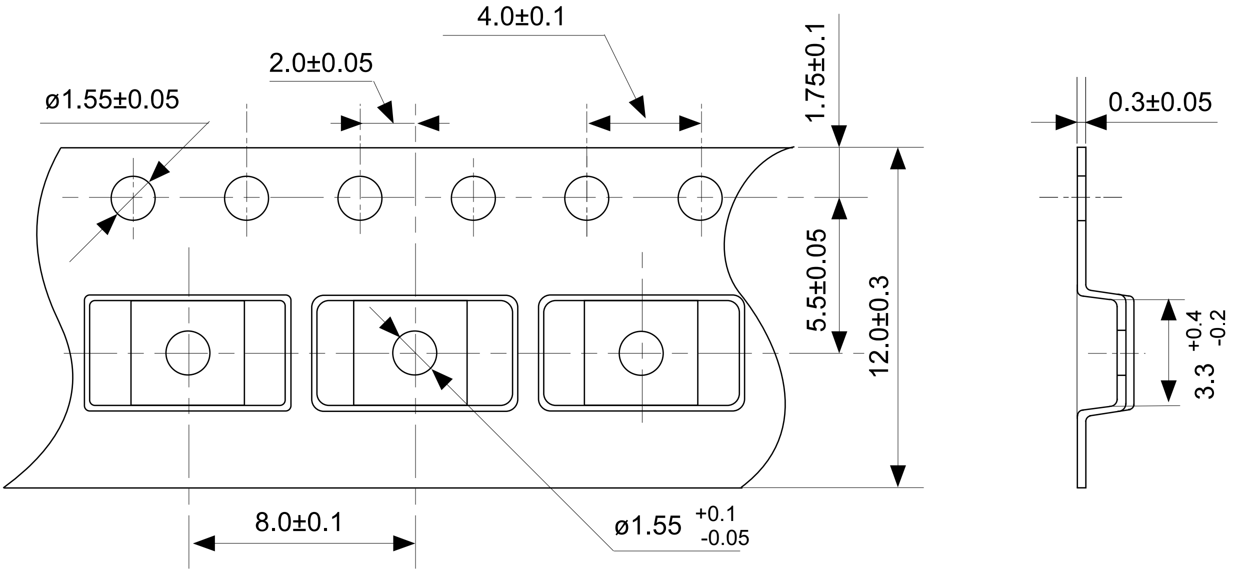

3.00 +0.3 -0.2
8
5
4.4±0.2
6.4±0.2
1
4

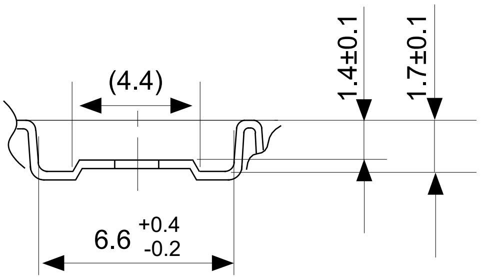


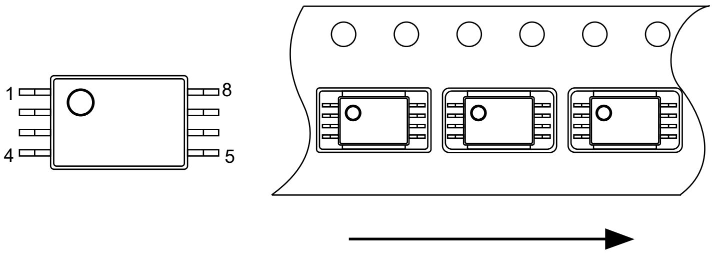

1.1max.
0.2±0.1
0 to 0.1
0.65

No. FT008-A-P-SD-1.2

TITLE	TSSOP8-E-PKG Dimensions
No.	FT008-A-P-SD-1.2
ANGLE	
UNIT	mm
ABLIC Inc.	


4.0±0.1
2.0±0.05
ø1.55±0.05
1.75±0.1
5.5±0.05
12.0±0.3
0.3±0.05
3.3 +0.4 -0.2
8.0±0.1
ø1.55 +0.1 -0.05


(4.4)
1.4±0.1
1.7±0.1
6.6 +0.4 -0.2

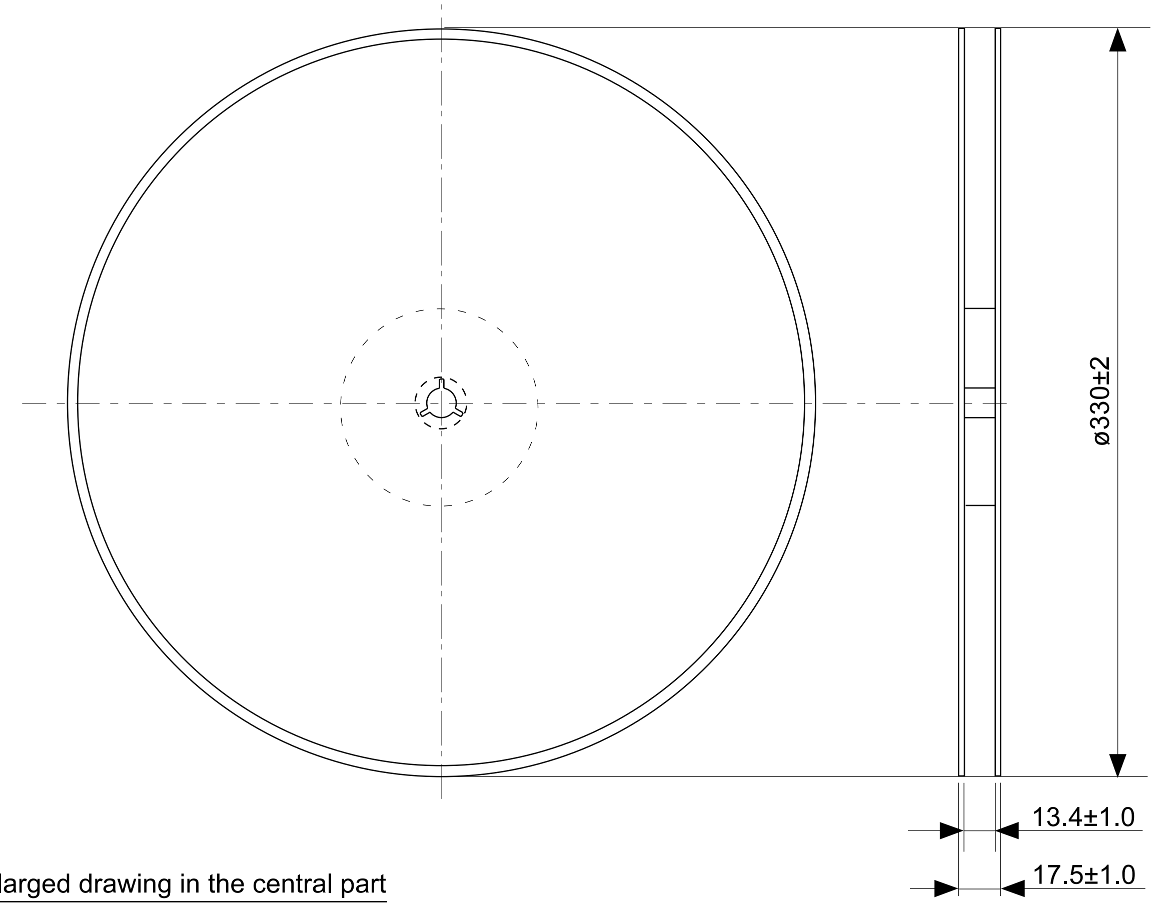


Feed direction

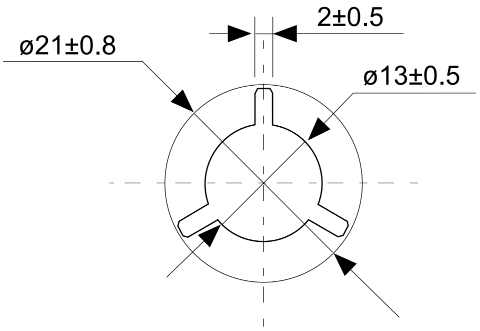
No. FT008-E-C-SD-1.0

TITLE	TSSOP8-E-Carrier Tape
No.	FT008-E-C-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.


ø330±2
13.4±1.0
17.5±1.0

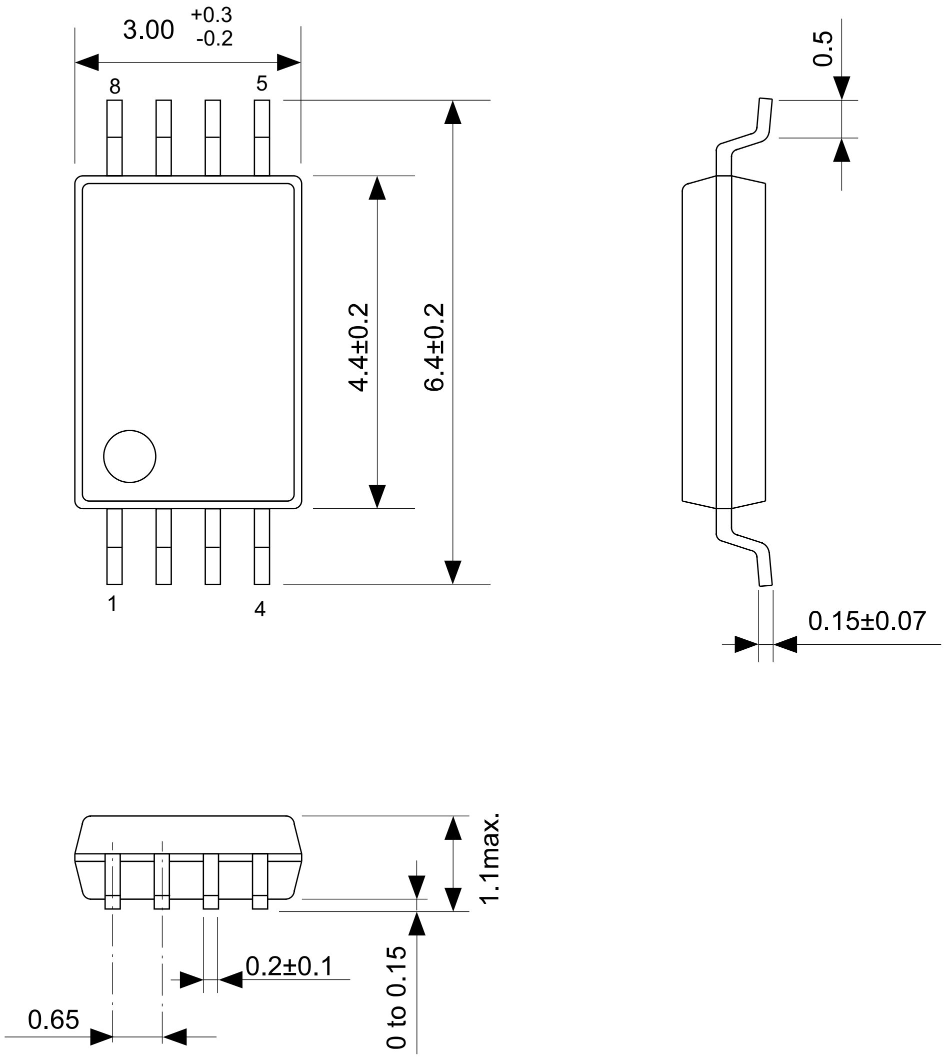
Enlarged drawing in the central part


2±0.5
ø21±0.8
ø13±0.5

No. FT008-E-R-SD-1.0

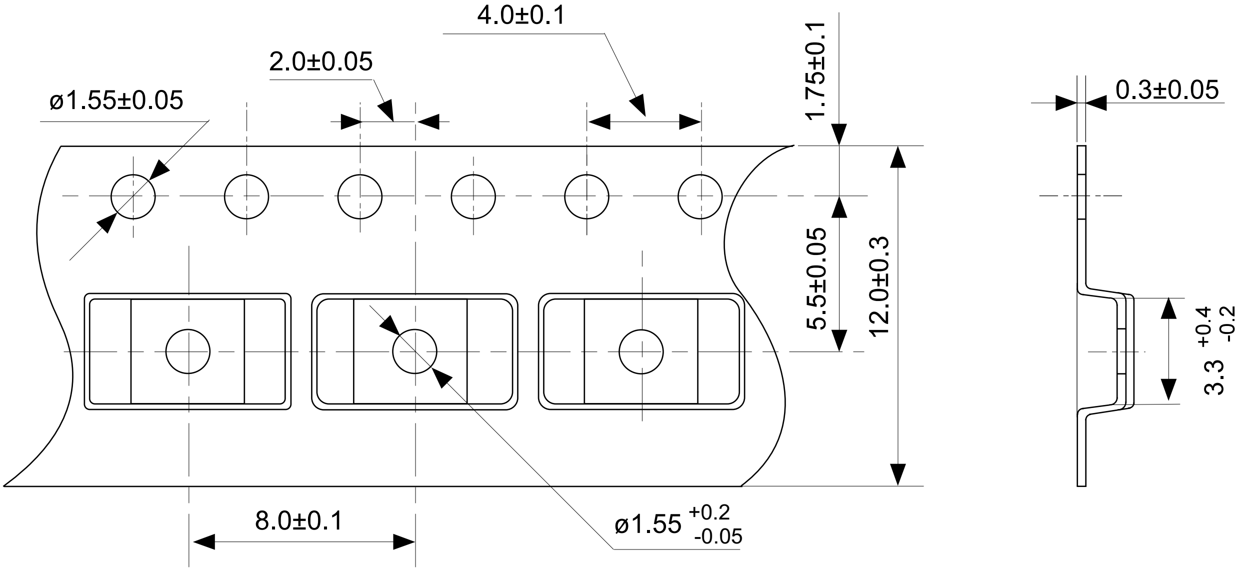
TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-SD-1.0		
ANGLE		QTY.	3,000
UNIT	mm		

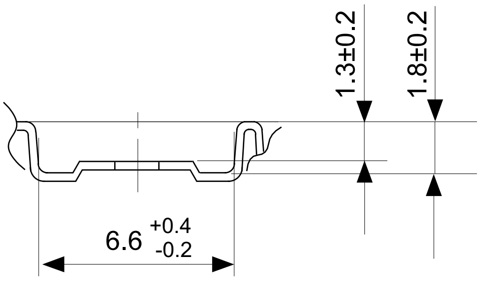
ABLIC Inc.

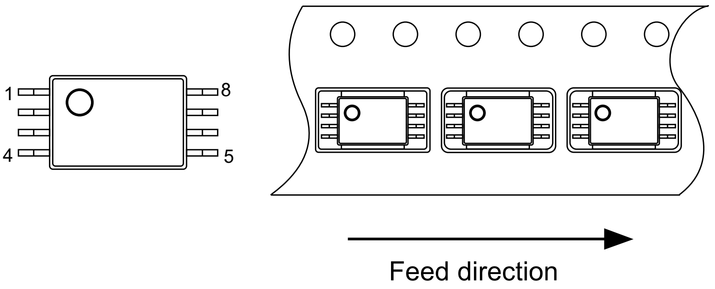

3.00 +0.3 -0.2
8
5
1
4
4.4±0.2
6.4±0.2
0.5
0.15±0.07
1.1max.
0 to 0.15
0.2±0.1
0.65

No. FT008-Z-P-SD-1.2

TITLE	TSSOP8-Z-PKG Dimensions
No.	FT008-Z-P-SD-1.2
ANGLE	
UNIT	mm
ABLIC Inc.	


ø1.55±0.05
2.0±0.05
4.0±0.1
1.75±0.1
5.5±0.05
12.0±0.3
0.3±0.05
3.3 +0.4 -0.2
8.0±0.1
ø1.55 +0.2 -0.05

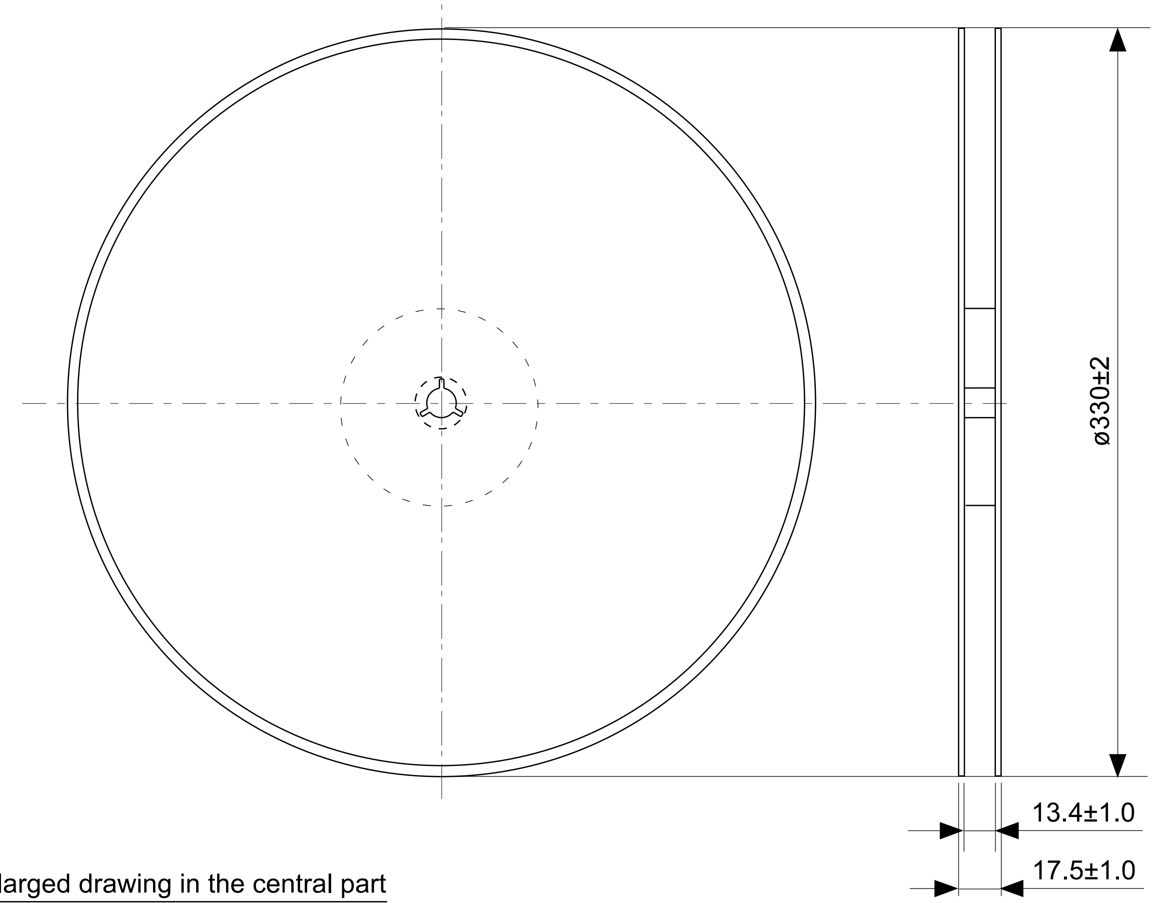

1.3±0.2
1.8±0.2
6.6 +0.4 -0.2


1
8
4
5
Feed direction

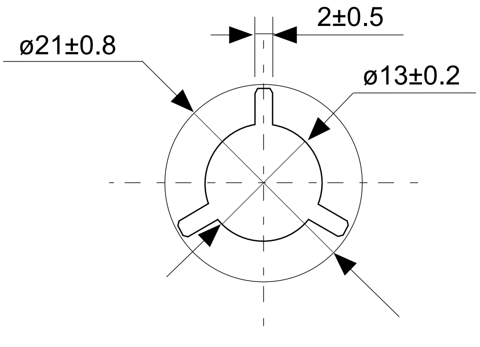
No. FT008-Z-C-SD-1.0

TITLE	TSSOP8-Z-Carrier Tape
No.	FT008-Z-C-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.


ø330±2
13.4±1.0
17.5±1.0

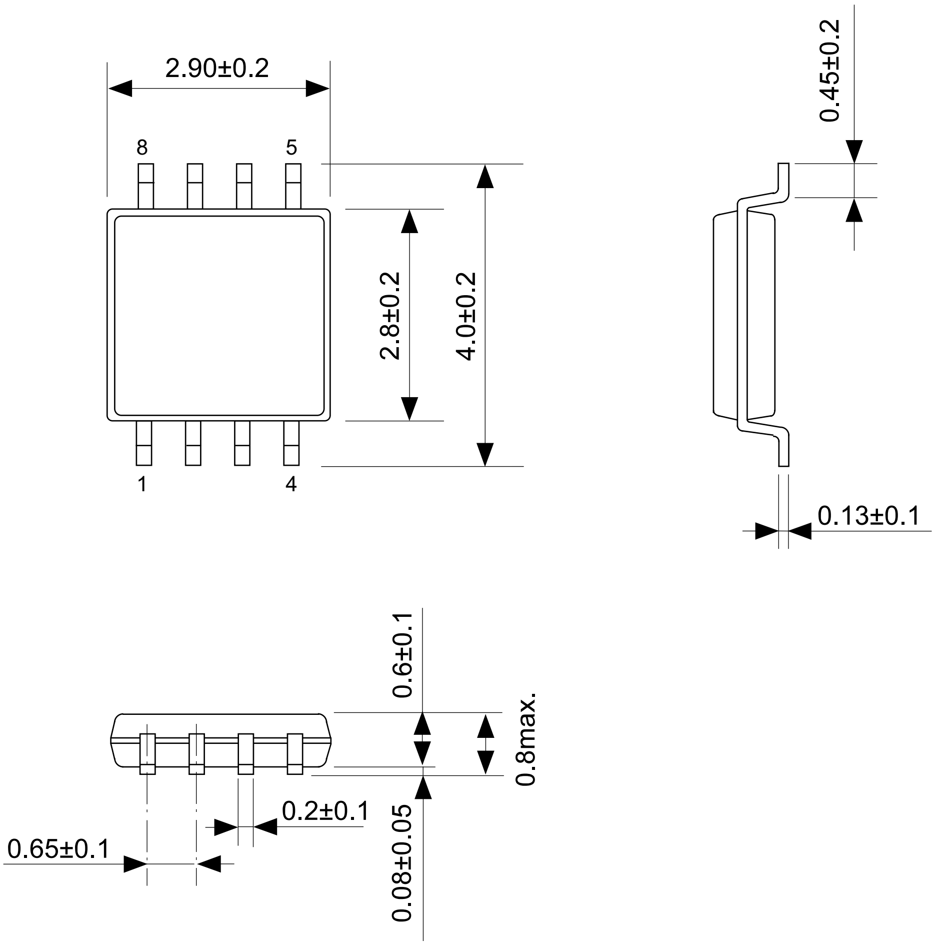
Enlarged drawing in the central part


2±0.5
ø21±0.8
ø13±0.2

No. FT008-Z-R-SD-1.0

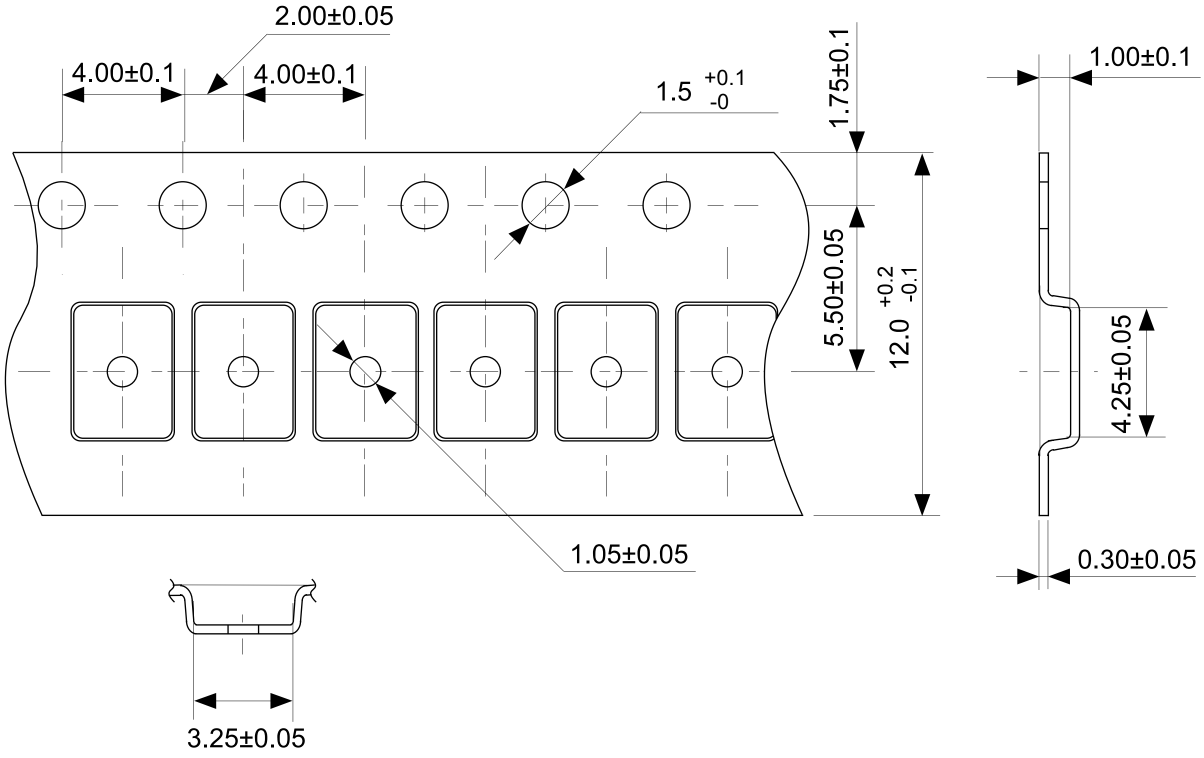
TITLE	TSSOP8-Z-Reel		
No.	FT008-Z-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		

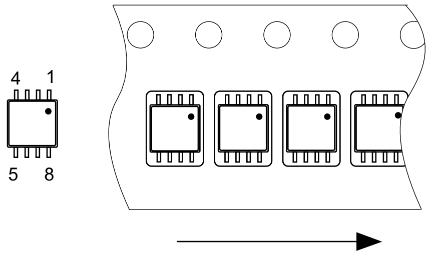
ABLIC Inc.


2.90±0.2
8
5
1
4
2.8±0.2
4.0±0.2
0.45±0.2
0.13±0.1
0.6±0.1
0.8max.
0.2±0.1
0.65±0.1
0.08±0.05

No. FM008-A-P-SD-1.2

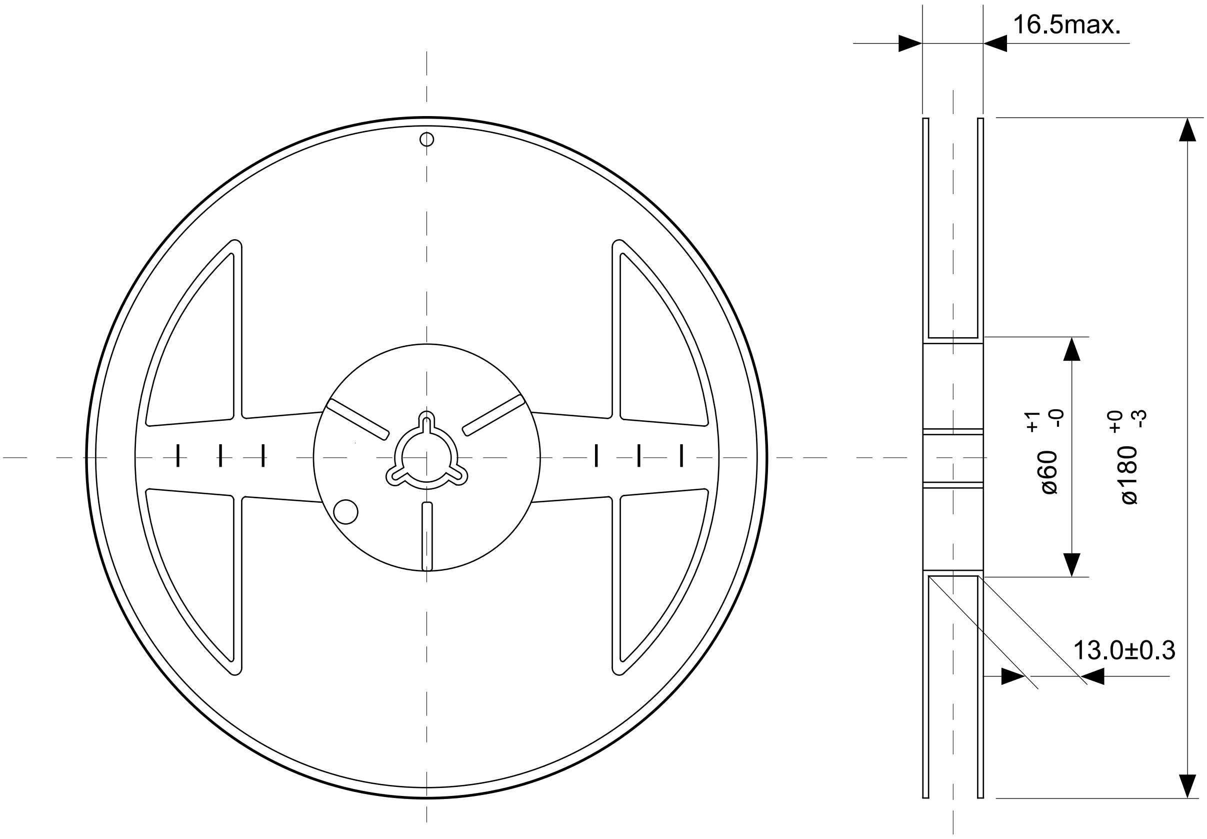
TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm
ABLIC Inc.	


2.00±0.05
4.00±0.1
4.00±0.1
1.5 +0.1 -0
1.75±0.1
1.00±0.1
5.50±0.05
12.0 +0.2 -0.1
4.25±0.05
1.05±0.05
0.30±0.05
3.25±0.05

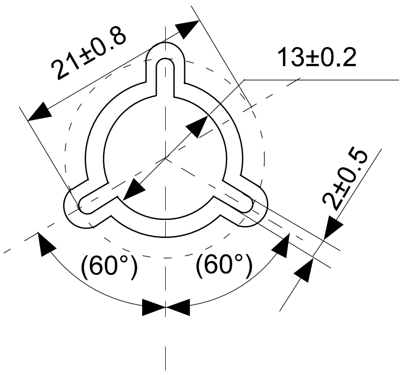

4
1
5
8
Feed direction

No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	


16.5max.
ø60 +1 -0
ø180 +0 -3
13.0±0.3

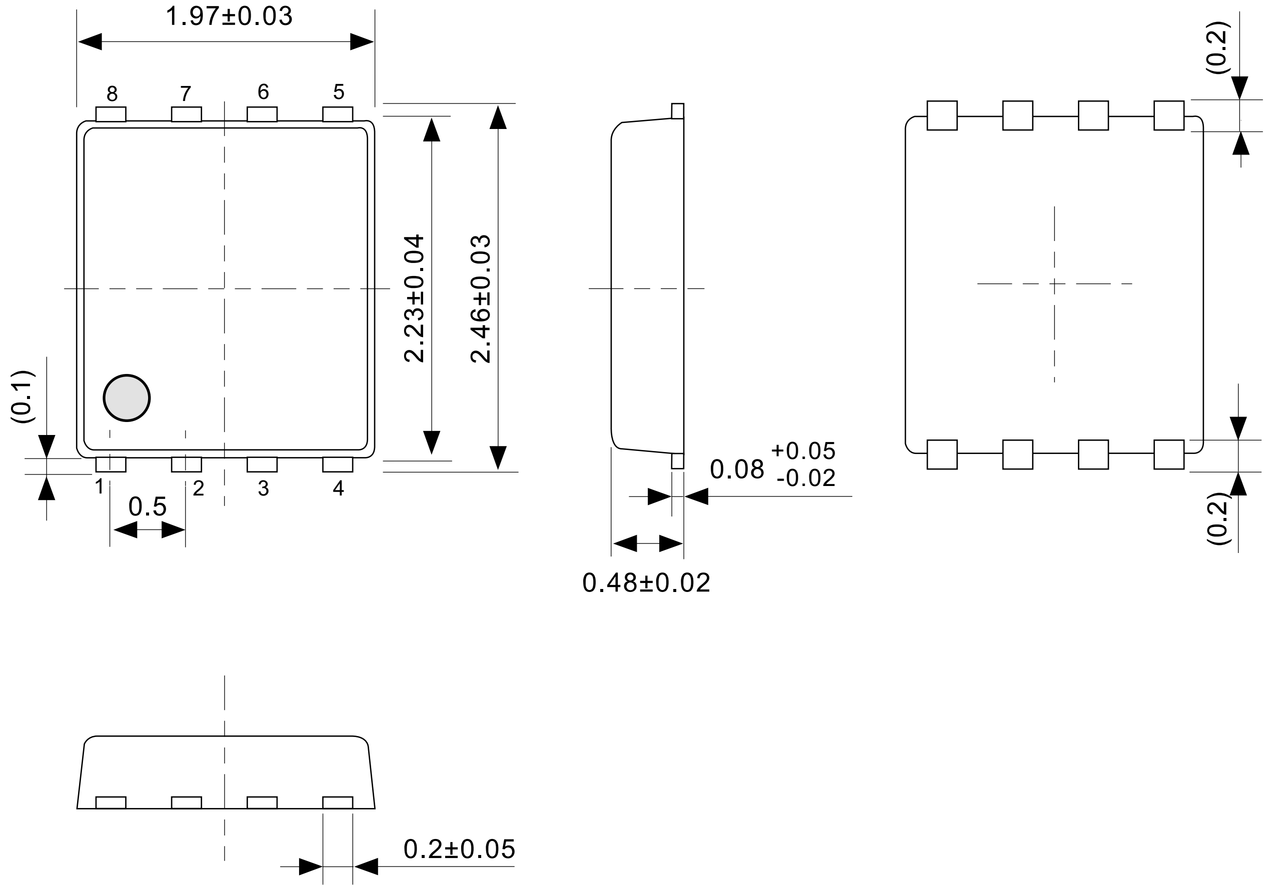
Enlarged drawing in the central part


21±0.8
13±0.2
2±0.5
(60°)
(60°)

No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		

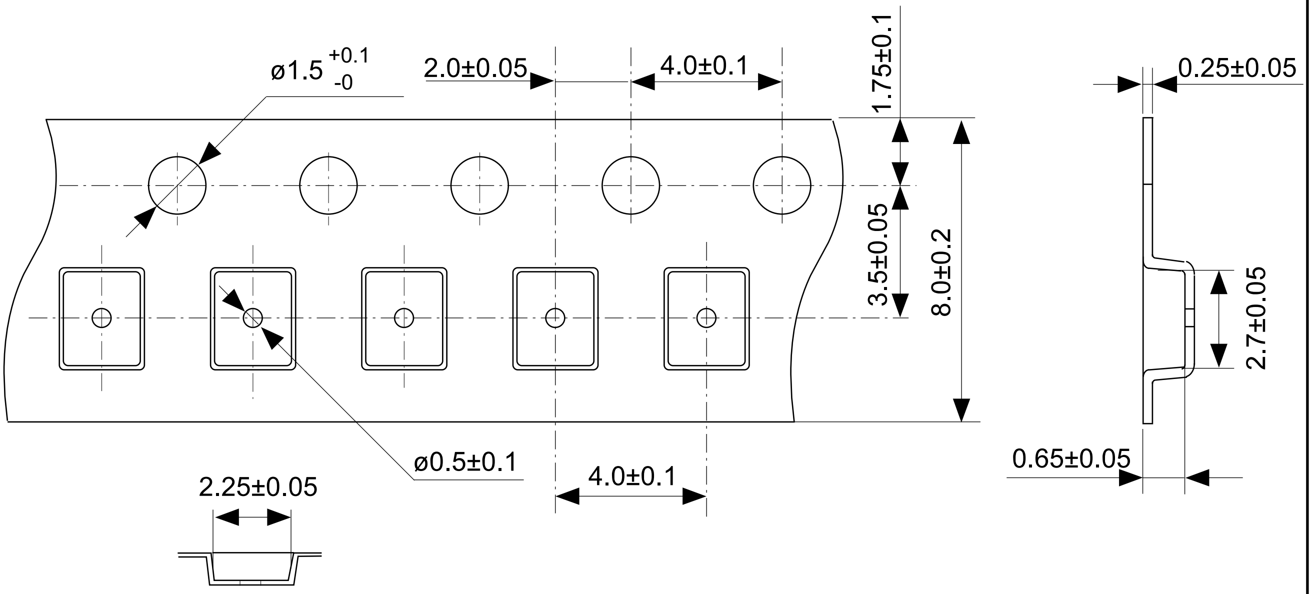
ABLIC Inc.

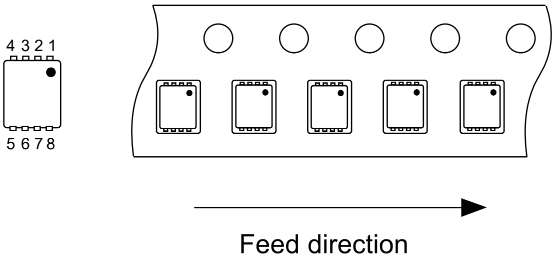

1.97±0.03
8
7
6
5
2.23±0.04
2.46±0.03
(0.1)
1
2
3
4
0.5
0.08 +0.05 -0.02
0.48±0.02
(0.2)
(0.2)
0.2±0.05

No. PH008-A-P-SD-2.1

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.1
ANGLE	
UNIT	mm

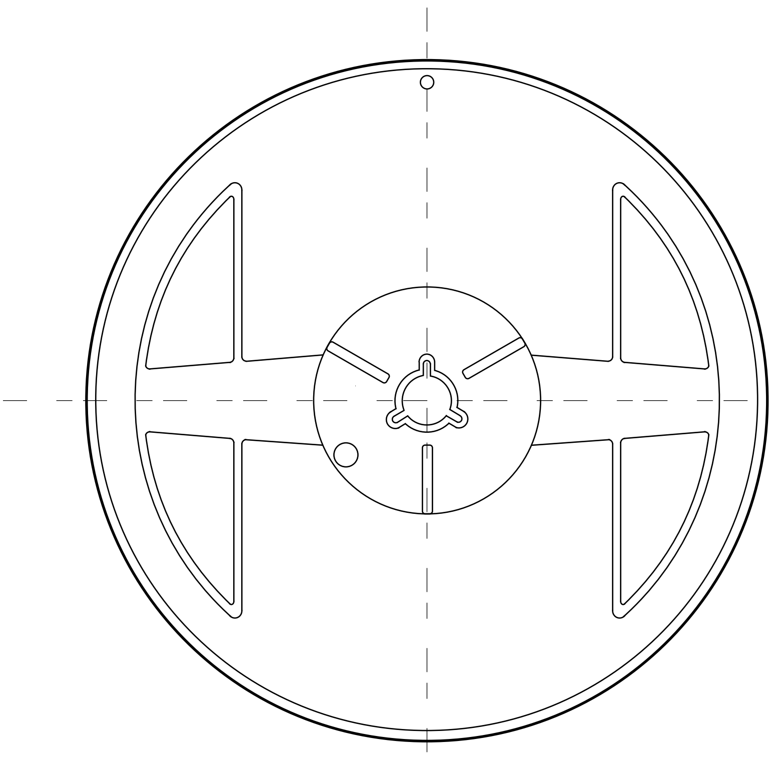
ABLIC Inc.

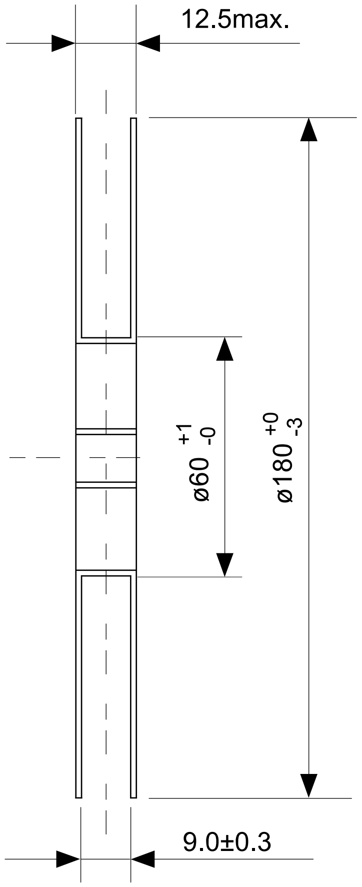

ø1.5 +0.1 -0
2.0±0.05
4.0±0.1
1.75±0.1
0.25±0.05
3.5±0.05
8.0±0.2
2.7±0.05
ø0.5±0.1
4.0±0.1
0.65±0.05
2.25±0.05


4 3 2 1
5 6 7 8
Feed direction

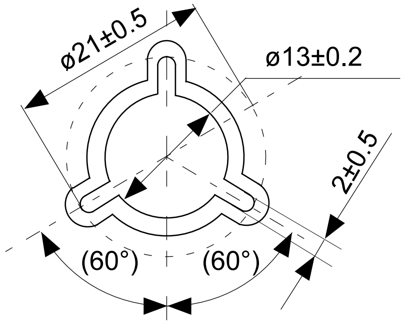
No. PH008-A-C-SD-2.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	




12.5max.
ø60 +1 -0
ø180 +0 -3
9.0±0.3

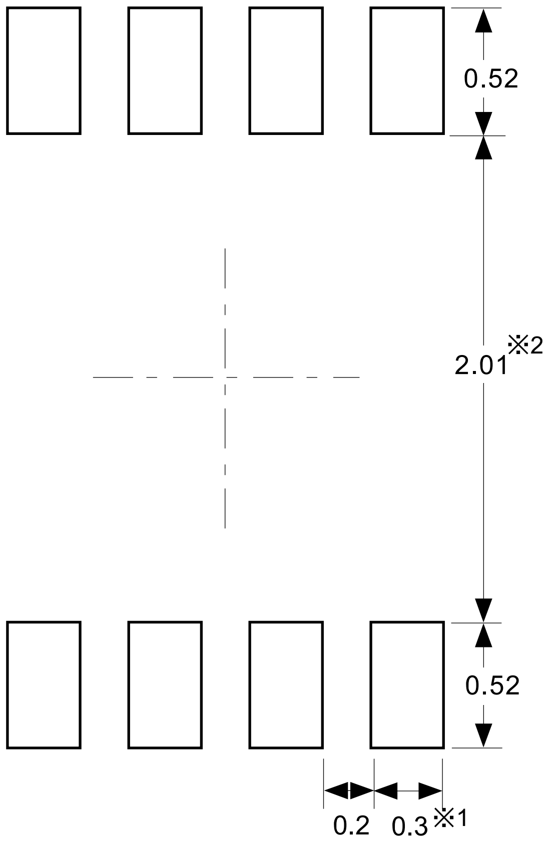
Enlarged drawing in the central part


ø21±0.5
ø13±0.2
2±0.5
(60°)
(60°)

No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		

ABLIC Inc.



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〞を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度（从焊盘模式表面起）请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PH008-A-L-SD-4.1

TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
ANGLE	
UNIT	mm
	ABLIC Inc.

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   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
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2.4-2019.07

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Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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