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RF6509

2.7V TO 3.6V MODULE FOR INTEGRATION WITH 900MHz SMART ENERGY AMI

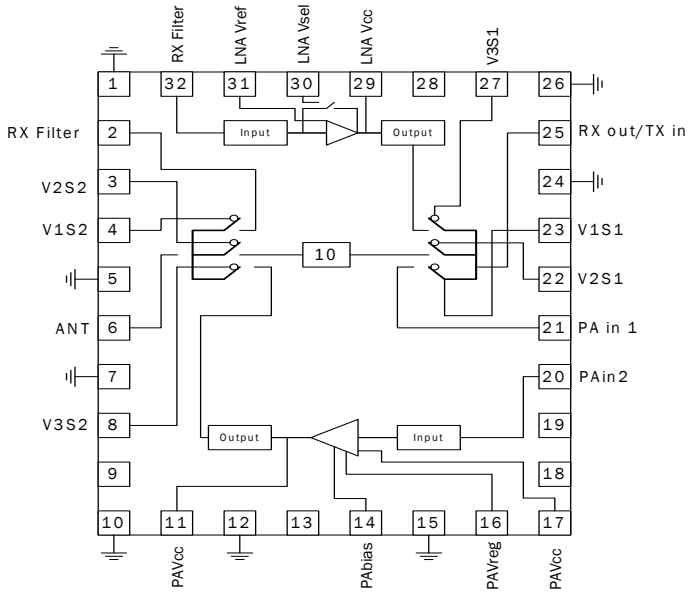
Package Style: LGA, 32 pin, 8mm x 8mm x 1.2mm

Features

- Tx Output Power: 29.5dBm
- Tx Gain: 31dBm
- Rx Gain: 18dB
- Rx Noise Figure: 2.5dB
- Integrated LNA with Bypass Mode

Applications

- 868MHz/900MHz ISM Band Application
- Single Chip RF Front End Module
- Portable Battery Powered Equipment
- Wireless Automatic Metering Applications



Functional Block Diagram

Product Description

The RF6509 integrates a complete solution in a single Front-End Module (FEM) for AMR and Smart Grid solutions. The RF6509 integrates a 915MHz PA, some transmit (Tx) filtering, input and output switches, a Tx or receive (Rx) attenuation path, and an LNA with bypass mode. The RF6509 has a single-ended input and output for optimized ease of use and implementation. The pin-out of the FEM enables users to implement additional filtering external to the module, if needed. The device is provided in a LGA, 32 pin, 8mm x 8mm x 1.2mm package.

Ordering Information

RF6509	2.7V to 3.6V Module for Integration with 900MHz Smart Energy AMI
RF6509PCK-410	Fully Assembled Evaluation Board and 5 loose pieces.

Optimum Technology Matching® Applied

☑ GaAs HBT	☐ SiGe BiCMOS	☑ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ BiFET HBT
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Overall		
DC Supply Voltage	+5.0	V
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Low Noise Amplifier		
DC Supply Current	32	mA
Input RF Power	5	dBm
Power Amplifier		
DC Supply Current	1200	mA
Input RF Power	10	dBm
Transmit/Receive Switch		
Input RF Power	33	dBm

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS (Restriction of Hazardous Substances): Compliant per EU Directive 2002/95/EC.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T = 25°C, PAV_{CC1} and PAV_{CC1} = 3.2V, PA_{BIAS} = 3.2V PAV_{REG} = 2.85V, unless otherwise noted
Usable Frequency Range	868	902 to 928		MHz	
Input Impedance		50		Ω	
Input VSWR		2:1			
Output Load VSWR		6:1			
PA Section					
CW Output Power	29	29.5		dBm	PA_{BIAS}, P_{IN} = -3 < 0 < 3dBm
Small Signal Gain	29	31		dB	PA_{BIAS}, P_{IN} = -20dBm
Second Harmonic		-42.5		dBc	PA_{BIAS}, P_{OUT} = 29.5dBm at ANT port
Third Harmonic		-72.5		dBc	PA_{BIAS}, P_{OUT} = 29.5dBm at ANT port
Fourth Harmonic		-42.5		dBc	PA_{BIAS}, P_{OUT} = 29.5dBm at ANT port
Input VSWR		2:1			
Output VSWR		6:1			Oscillations <-60dBc
Power Supply Voltage	2.7	3.2	3.6	V	
Power Supply Current		730	850	mA	PA_{BIAS}
		70	100	µA	V_{CCPA} = 3.2V, PA_{BIAS} = 3.2V, PAV_{REG} = 0V,
Power Supply Current for PA V_{BIAS}		18.0	20.0	mA	
Power Supply Current for PA V_{REG}		70.0	100.0	µA	
LNA Section					
HIGH GAIN MODE					$LNAV_{CC}$ = 3.0V, $LNAV_{REF}$ = 3.0V, $LNAV_{SEL}$ = 0.0V, PA_{BIAS} = 0.0V, PAV_{REG} = 0.0V
Gain	17.5	18	18.5	dB	902MHz to 928MHz
	15.5	16.5	17.5	dB	868MHz
Noise Figure		2.4	3.4	dB	
Input IP3	7.5	9.5	12	dBm	
Output VSWR	1.6:1	2:1	2.4:1		
Supply Current			12	mA	

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
LNA Section (continued)					
LOW GAIN MODE					$LNAV_{CC}$ = 3.0V, $LNAV_{REF}$ = 3.0V, $LNAV_{SEL}$ = 0.0V, PA_{BIAS} = 0.0V, PAV_{REG} = 0.0V
Gain		-6		dB	
Noise Figure		6		dB	
Supply Current		3		mA	
$LNAV_{CC}$ Voltage	2.7	3.0		V	
$LNAV_{REF}$ Logic Level HIGH	2.7	3.0		V	
$LNAV_{REF}$ Logic Level LOW	0.0		0.3	V	
$LNAV_{SEL}$ Logic Level HIGH	1.8	3.0		V	
$LNAV_{SEL}$ Logic Level LOW			0.8	V	
Power Down Current			10	µA	LNA_EN = LOW, $LNAV_{SEL}$ = LOW
Transceiver Switch Section					
Insertion Loss TXin-PAin	0.9	1	1.1	dB	V_{1S1} = 3.0V, V_{2S1} = 0.0V, V_{3S1} = 0.0V
Isolation TXin-PAin	25	27		dB	V_{1S1} = 0.0V, V_{2S1} = 3.0V, V_{3S1} = 0.0V or V_{1S1} = 0.0V, V_{2S1} = 0.0V, V_{3S1} = 3.0V
TXin/RXout Return Loss (Thru path)		-15	-14	dB	V_{1S1} = 0.0V, V_{2S1} = 3.0V, V_{3S1} = 0.0V and V_{1S2} = 0.0V, V_{2S2} = 3.0V, V_{3S2} = 0.0V
TXin/RXout Return Loss (Transmit path)‘			-9	dB	V_{1S1} = 3.0V, V_{2S1} = 0.0V, V_{3S1} = 0.0V and V_{1S2} = 0.0V, V_{2S2} = 0.0V, V_{3S2} = 3.0V
TXin/RXout Return Loss (Receive path)			-9	dB	V_{1S1} = 0.0V, V_{2S1} = 0.0V, V_{3S1} = 3.0V and V_{1S2} = 3.0V, V_{2S2} = 0.0V, V_{3S2} = 0.0V
Switch Control Logic HIGH	2.7	3.0		V	
Switch Control Logic LOW	0.0		0.4	V	
Switch Control Current		13.0	15.0	µA	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Antenna Switch Section					
Insertion Loss ANT-LNAin	0.9	1	1.1	dB	V_{1S2} = 3.0V, V_{2S2} = 0.0V, V_{3S2} = 0.0V
Isolation ANT-LNAin	25	27		dB	V_{1S2} = 0.0V, V_{2S2} = 3.0V, V_{3S2} = 0.0V or V_{1S2} = 0.0V, V_{2S2} = 3.0V, V_{3S2} = 0.0V
ANT Return Loss (Thru Path)		-15	-14	dB	V_{1S1} = 0.0V, V_{2S1} = 3.0V, V_{3S1} = 0.0V or V_{1S2} = 0.0V, V_{2S2} = 3.0V, V_{3S2} = 0.0V
ANT Return Loss (Transmit Path)			-9	dB	V_{1S1} = 3.0V, V_{2S1} = 0.0V, V_{3S1} = 0.0V or V_{1S2} = 0.0V, V_{2S2} = 0.0V, V_{3S2} = 3.0V
ANT Return Loss (Receive Path)			-9	dB	V_{1S1} = 0.0V, V_{2S1} = 0.0V, V_{3S1} = 3.0V or V_{1S2} = 3.0V, V_{2S2} = 0.0V, V_{3S2} = 0.0V
Switch Control Logic HIGH	2.7	3.0		V	
Switch Control Logic LOW	0.0		0.4	V	
Switch Control Current		13.0	15.0	μA	

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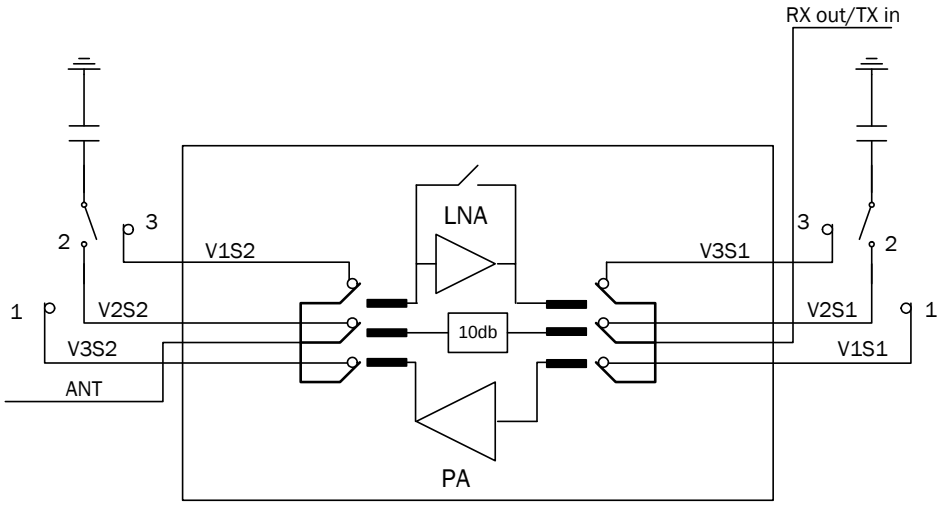
Pin	Function	Description
1	GND	Ground.
2	RX Filter Input	RF output to enter the Rx filter (if used), 50Ω nominal impedance.
3	V2S2	Logic input to the Tx Switch arm 2 , selects/deselects thru path if Logic high/low respectively, see truth table.
4	V1S2	Logic input to the Tx Switch arm 1, selects/deselects Low Noise Amplifier if Logic high/low respectively, see truth table.
5	GND	Ground.
6	ANT	RF output to Antenna for the Tx/thru path and RF input from Antenna for the Rx/thru path, 50Ω nominal impedance.
7	GND	Ground.
8	V3S2	Logic input to the Tx Switch arm 3, selects/deselects PA if Logic high/low respectively, see truth table.
9	NC	Not connected.
10	GND	Ground.
11	PA VCC2	Collector power supply for Power Amplifier. Nominal 3.6V.
12	GND	Ground.
13	NC	Not connected.
14	PA BIAS	Power supply for the PA Bias Network. Nominal 3.6V.
15	GND	Ground.
16	PA VREG	Voltage set to PA Bias Level. Nomial 2.85V.
17	PA VCC1	Collector power supply for PA driver stage. Nominal 3.6V.
18	NC	Not connected.
19	NC	Not connected.
20	PA IN	RF Input to the PA, 50Ω nominal impedance, needs to be connected externally to PA IN to SWITCH PIN through as short as possible 50Ω transmission line.
21	PA IN to SWITCH	PA input to be connected to the Rx Switch through this pin, 50Ω nominal Impedance.
22	V2S1	Logic input to the Rx switch arm 2, selects/deselects Thru path if Logic high/low respectively, see truth table.
23	V1S1	Logic input to the Rx switch arm 1, selects/deselects PA if Logic high/low respectively, see truth table.
24	GND	Ground.
25	RX OUT/TX IN	Transceiver IN/OUT.
26	GND	Ground.
27	V3S1	Logic input to the Rx switch arm 3, selects/deselects LNA if Logic high/low respectively, see truth table.
28	NC	Not connected.
29	LNA VCC	Collector power cupply for LNA. Nominal 3.0V.
30	LNA VSEL	A logic low selects the high gain mode of the LNA, logic high selects the low gain mode.
31	LNA VREF	Voltage to set the bias of the LNA, nominal 3.0V, can be adjusted to shut the LNA off or set the quiescent current of the LNA to desired level.
32	LNA IN	RF input to LNA, nominal impedance 50Ω, the Rx filter output should be connected to this pin, If Rx filter is bypassed, pin 2 should be connected to this pin htough an external 50Ω transmission line as short as possible.

Control Logic Table



SW1			SW2			LNA			PA			
V1S1	V2S1	V3S1	V1S2	V2S2	V3S2	LNA VSEL	LNA VREF	LNA VCC	PA VCC1 and 2	PA Bias	PA VREG	PATH
High	Low	Low	Low	Low	High	High	OFF	OFF	ON	ON	ON	Tx path thru PA
Low	High	Low	Low	High	Low	High	OFF	OFF	X*	OFF	OFF	Tx/Rx Thru path with 10dB attenuation
Low	Low	High	High	Low	Low	Low	ON	ON	X*	OFF	OFF	Rx path thru LNA (High gain mode)
Low	Low	High	High	Low	Low	High	ON	ON	X*	OFF	OFF	Rx path thru LNA (Low gain mode)

High indicates logic High of >2.7V and Low indicates logic Low of <0.2V.
*An X means that the state of the pin doesn't matter.

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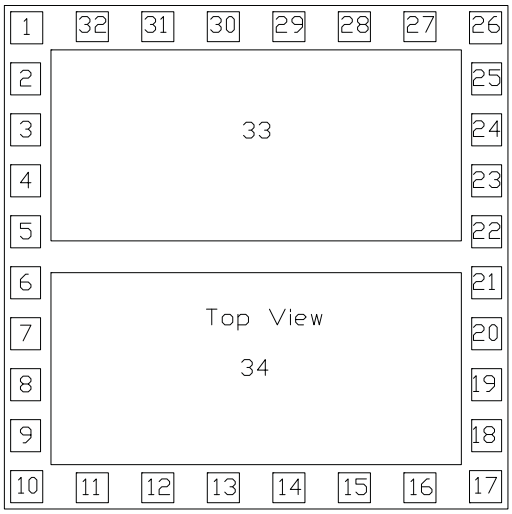
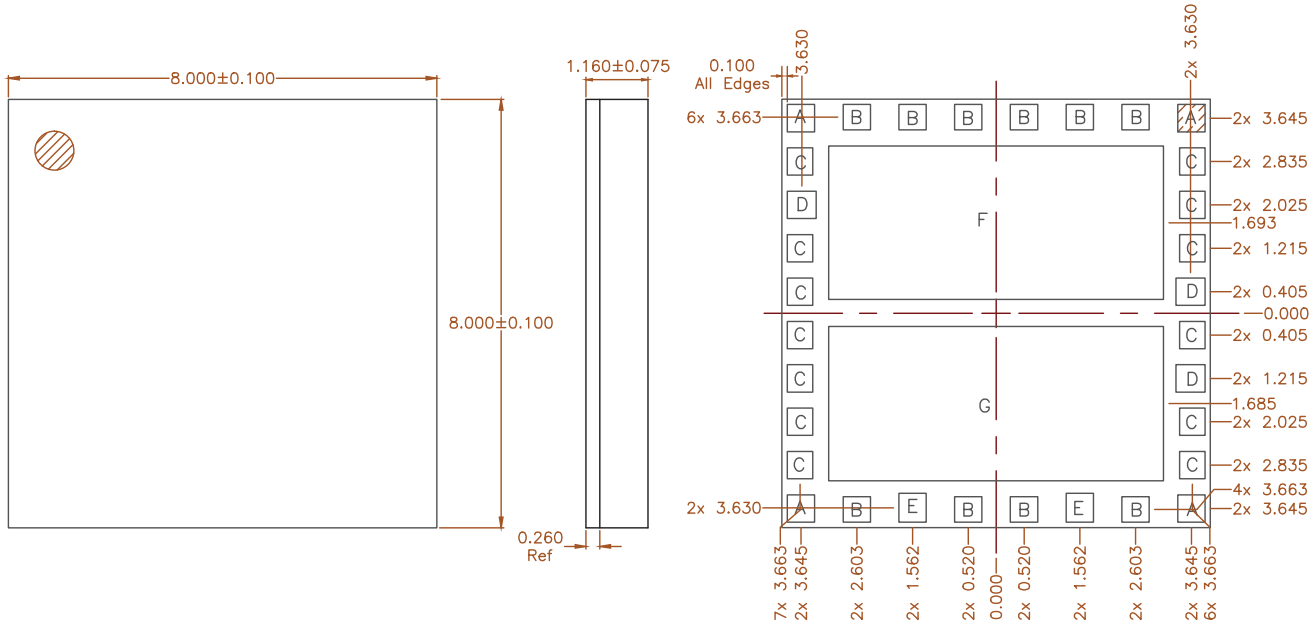
Pin Out



Package Drawing



Notes:
1. Shaded area represents Pin 1 location.

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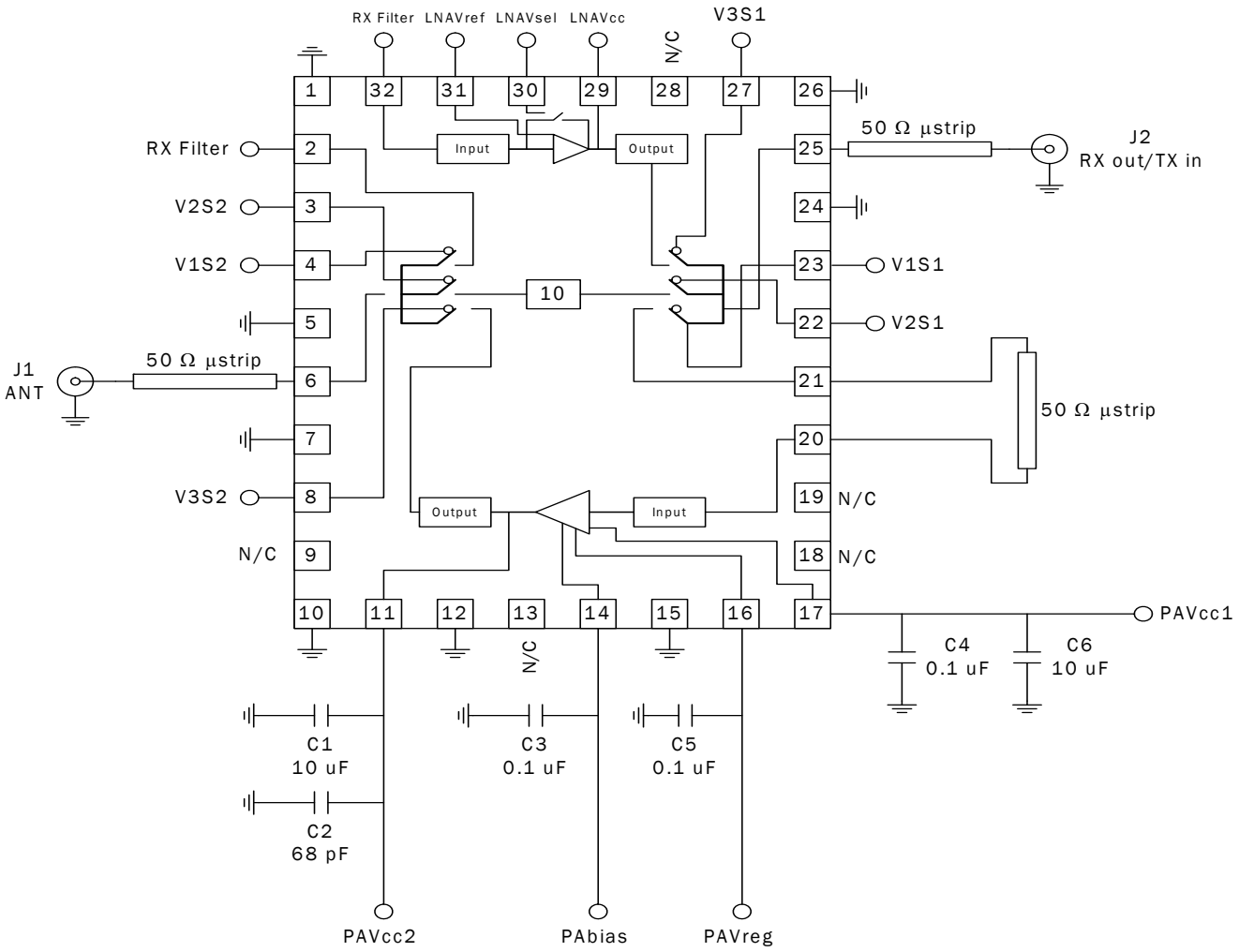
Evaluation Board Schematic



Note: 1. If extra isolation is needed between Tx and Rx path, the filter can be used otherwise for ≤50dB isolation, 50Ω microstrip shoud be okay.

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PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Solder Mask Pattern

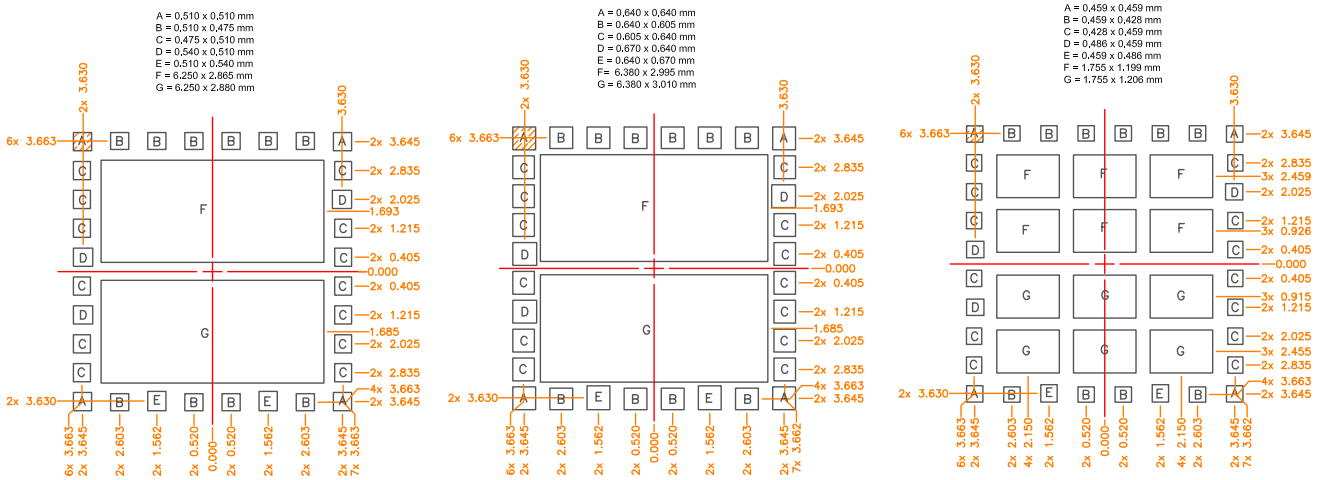
Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

Thermal Pad and Via Design

The PCB metal land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

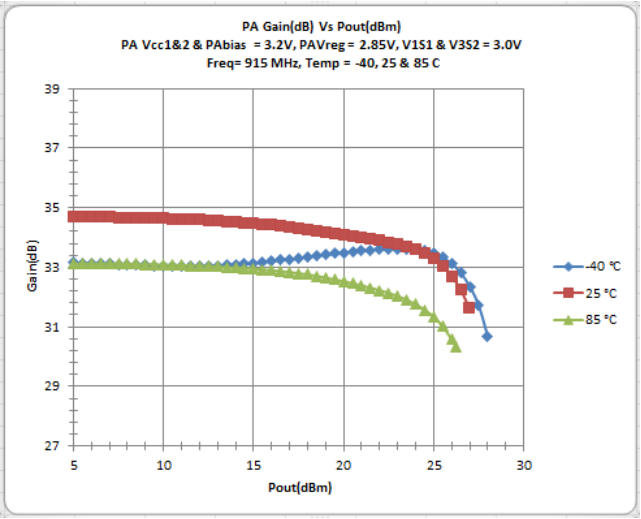
The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

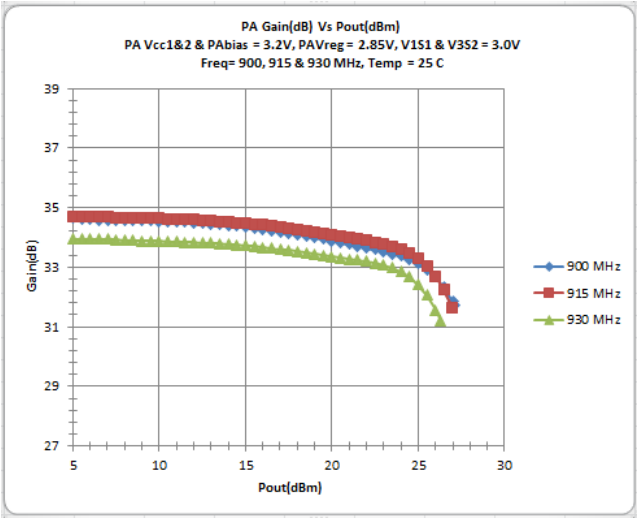


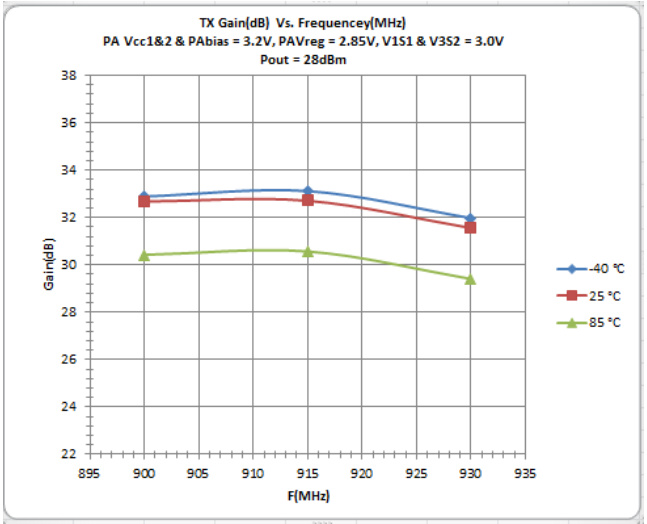
PCB Metal Land Pattern | PCB Solder Mask Pattern | PCB Stencil Pattern

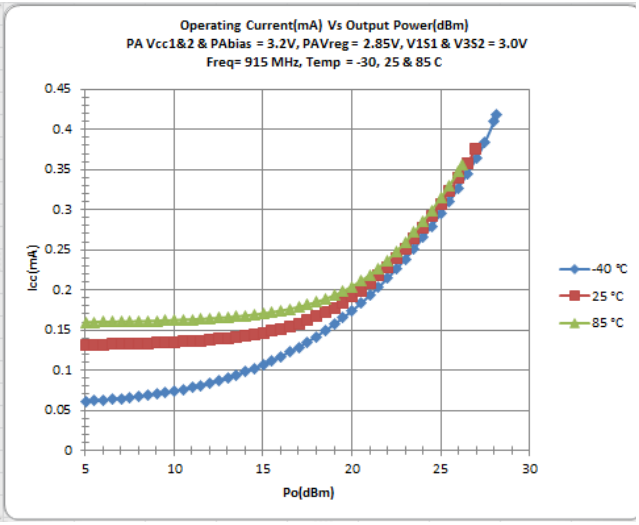
Notes:
1. Shaded area represents Pin 1 location.

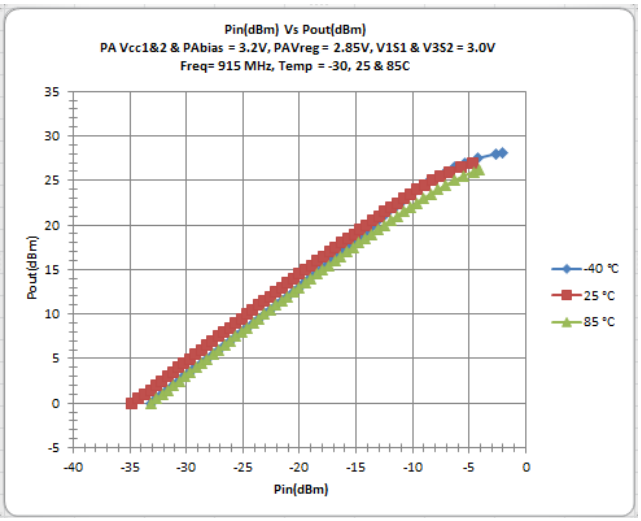
Typical Performance

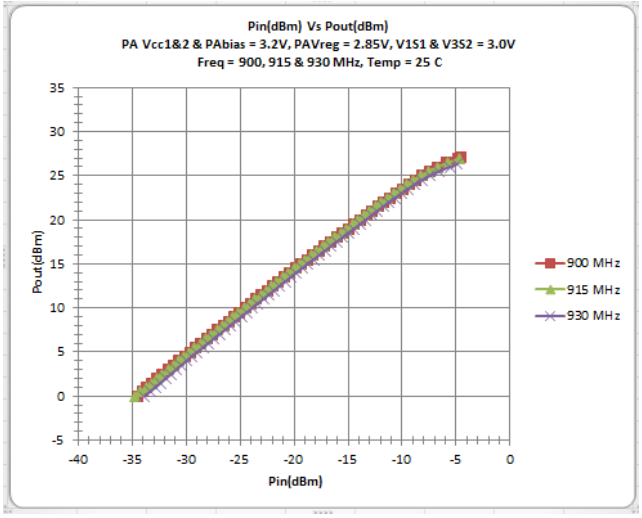












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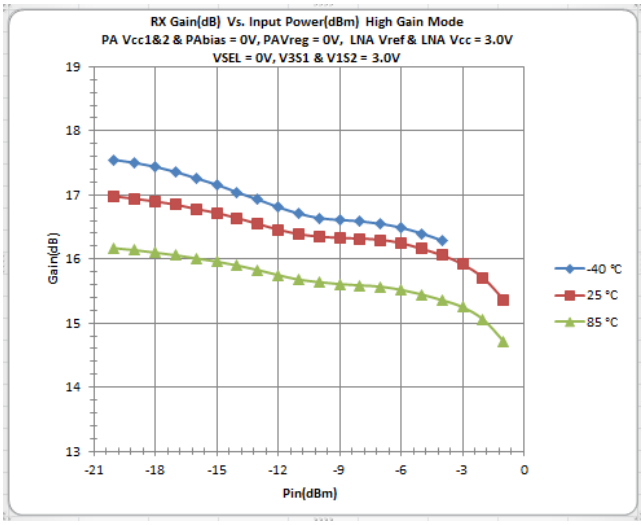

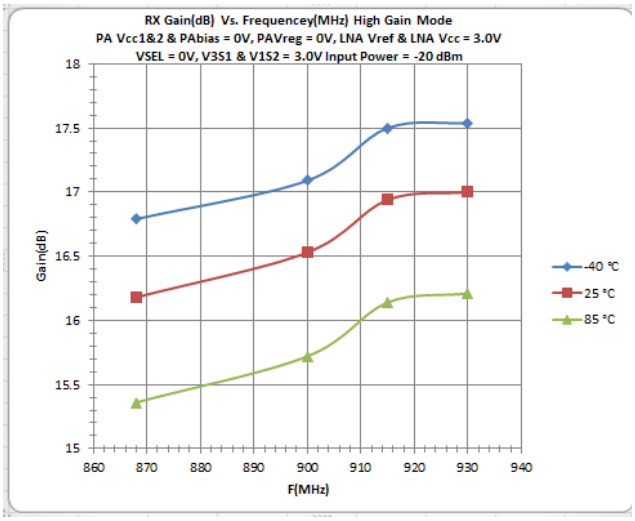

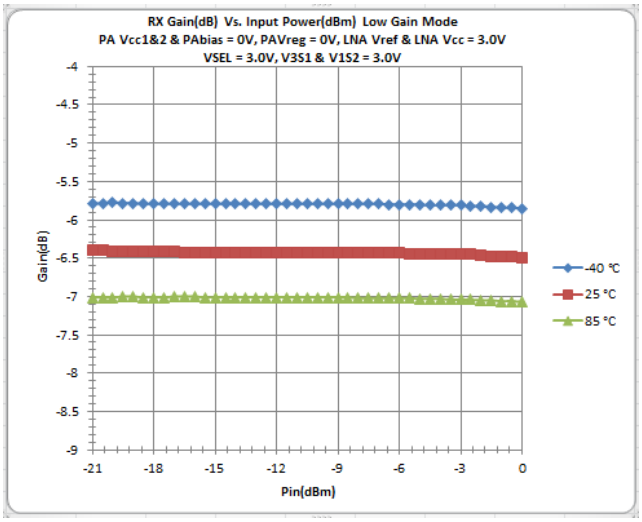

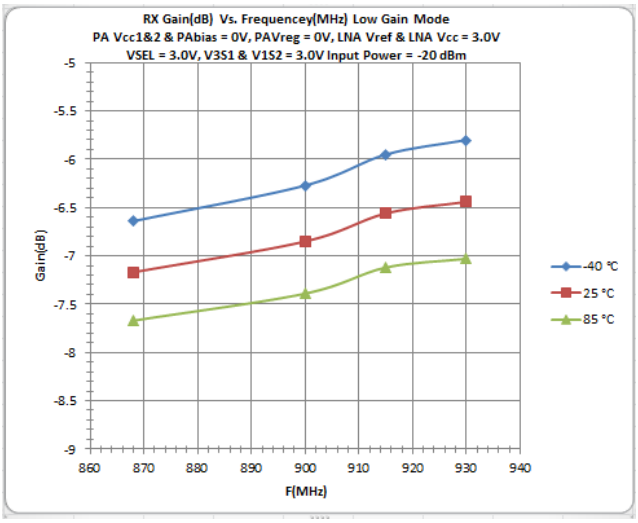

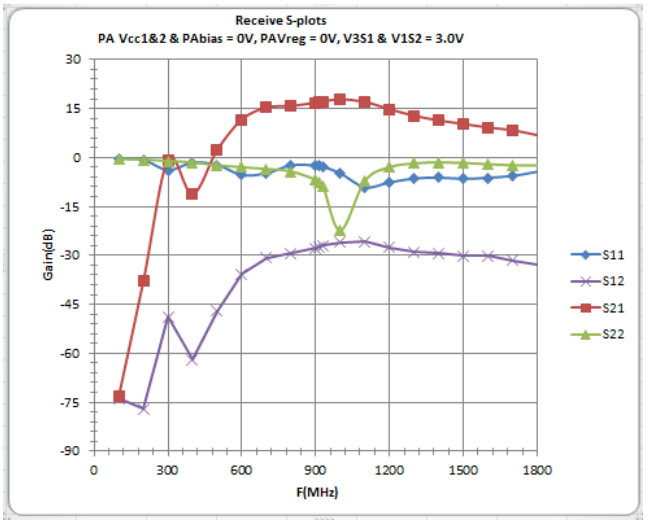

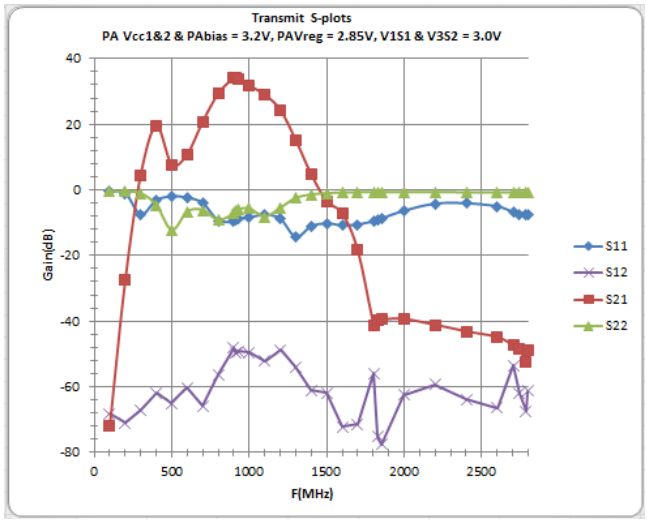

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RoHS* Banned Material Content

RoHS Compliant:	Yes
Package total weight in grams (g):	0.038
Compliance Date Code:	0547
Bill of Materials Revision:	A
Pb Free Category:	e3

Bill of Materials	Parts Per Million (PPM)					
	Pb	Cd	Hg	Cr VI	PBB	PBDE
Die	0	0	0	0	0	0
Molding Compound	0	0	0	0	0	0
Lead Frame	0	0	0	0	0	0
Die Attach Epoxy	0	0	0	0	0	0
Wire	0	0	0	0	0	0
Solder Plating	0	0	0	0	0	0

This RoHS banned material content declaration was prepared solely on information, including analytical data, provided to RFMD by its suppliers, and applies to the Bill of Materials (BOM) revision noted above.

* DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment

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http://moschip.ru/get-element

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На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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