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October 2013

FDMC8015L

N-Channel Power Trench[®] MOSFET 40 V, 18 A, 26 m Ω

Features

- Max $r_{DS(on)} = 26 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 7 \text{ A}$
- Max $r_{DS(on)}$ = 36 m Ω at V_{GS} = 4.5 V, I_D = 6 A
- Low Profile 1 mm max in Power 33
- 100% UIL Tested
- RoHS Compliant

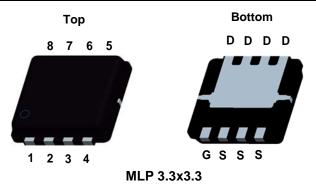
General Description

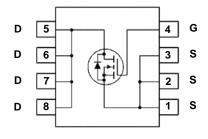
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Applications

- Load Switch
- Motor Bridge Switch







MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units	
V _{DS}	Drain to Source Voltage			40	V	
V_{GS}	Gate to Source Voltage			±20	V	
	Drain Current -Continuous (Package limited)	T _C = 25°C		18		
	-Continuous (Silicon limited)	T _C = 25°C		22		
^I D	-Continuous	T _A = 25°C	(Note 1a)	7	_ A	
	-Pulsed			30		
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	32	mJ	
Б	Power Dissipation	T _C = 25°C		24	10/	
P_{D}	Power Dissipation	T _A = 25°C	(Note 1a)	2.3	W	
T _J , T _{STG}	Operating and Storage Junction Temperature R	ange		-55 to + 150	°C	

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	5.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8015L	FDMC8015L	Power 33	13"	12 mm	3000 units

Electrical Characteristics $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		36		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 32 V, V _{GS} = 0 V			1	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	1	1.8	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		-6		mV/°C
		V _{GS} = 10 V, I _D = 7 A		19.7	26	
r _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 6 \text{ A}$		24	36	mΩ
		$V_{GS} = 10 \text{ V}, I_D = 7 \text{ A}, T_J = 125 \text{ °C}$		29	39	
9 _{FS}	Forward Transconductance	V _{DD} = 5 V, I _D = 7 A		30		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 20 V V 0 V	710	945	pF
C _{oss}	Output Capacitance	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz	94	125	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1011 12	58	90	pF
R_{q}	Gate Resistance		1.2		Ω

Switching Characteristics

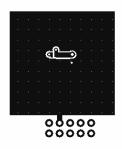
t _{d(on)}	Turn-On Delay Time		6.3	13	ns
t _r	Rise Time	$V_{DD} = 20 \text{ V}, I_D = 7 \text{ A},$	1.9	10	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	18	33	ns
t _f	Fall Time		1.7	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V _{GS} = 0 V to 10 V	13.6	19	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to } 4.5 \text{ V}$ $I_{DD} = 20 \text{ V},$ $I_{D} = 7 \text{ A}$	6.6	10	nC
Q_{gs}	Total Gate Charge	1 _D = 7 A	1.9		nC
Q_{gd}	Gate to Drain "Miller" Charge		2.5		nC

Drain-Source Diode Characteristics

V _{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 7 \text{ A}$	(Note 2)	0.84	1.2	V
		$V_{GS} = 0 \text{ V}, I_{S} = 2 \text{ A}$	(Note 2)	0.76	1.1	
t _{rr}	Reverse Recovery Time	$I_F = 7 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s}$		18	33	ns
Q _{rr}	Reverse Recovery Charge			8.6	18	nC

NOTES

^{1.} R_{0,1A} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0,IC} is guaranteed by design while R_{0,CA} is determined by the user's board design.



 a. 53 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 125 °C/W when mounted on a minimum pad of 2 oz copper

- 2. Pulse Test: Pulse Width < 300 $\mu\text{s},$ Duty cycle < 2.0%.
- 3. Starting T_J = 25 °C; N-ch: L = 1 mH, $I_{\mbox{\scriptsize AS}}$ = 8 A, $V_{\mbox{\scriptsize DD}}$ = 36 V, $V_{\mbox{\scriptsize GS}}$ = 10 V.

Typical Characteristics T_{.I} = 25 °C unless otherwise noted

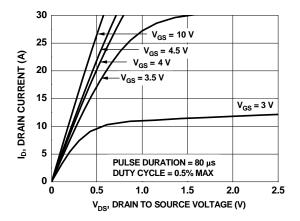


Figure 1. On Region Characteristics

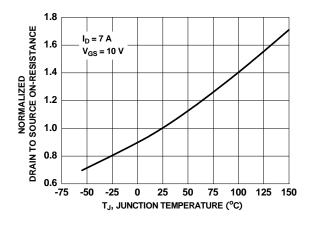


Figure 3. Normalized On Resistance vs Junction Temperature

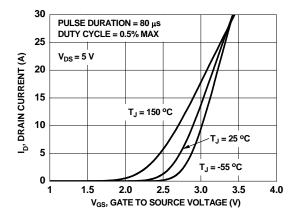


Figure 5. Transfer Characteristics

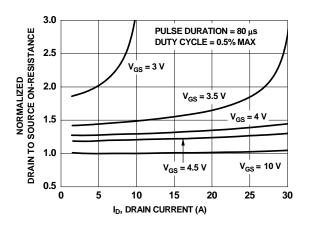


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

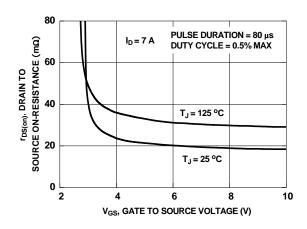


Figure 4. On-Resistance vs Gate to Source Voltage

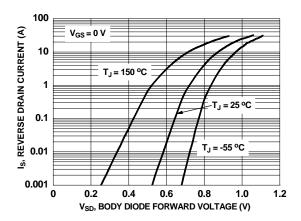


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

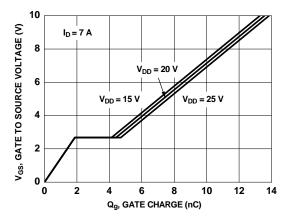


Figure 7. Gate Charge Characteristics

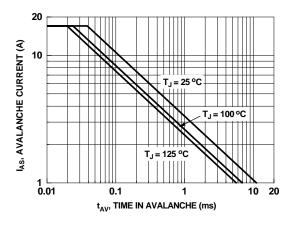


Figure 9. Unclamped Inductive Switching Capability

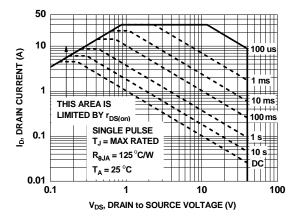


Figure 11. Forward Bias Safe Operating Area

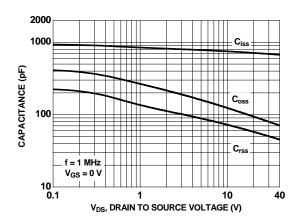


Figure 8. Capacitance vs Drain to Source Voltage

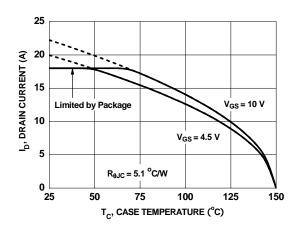


Figure 10. Maximum Continuous Drain Current vs Case Temperature

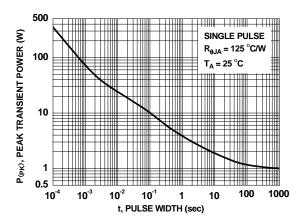


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25$ °C unless otherwise noted

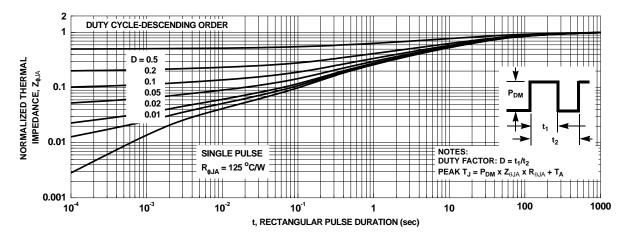
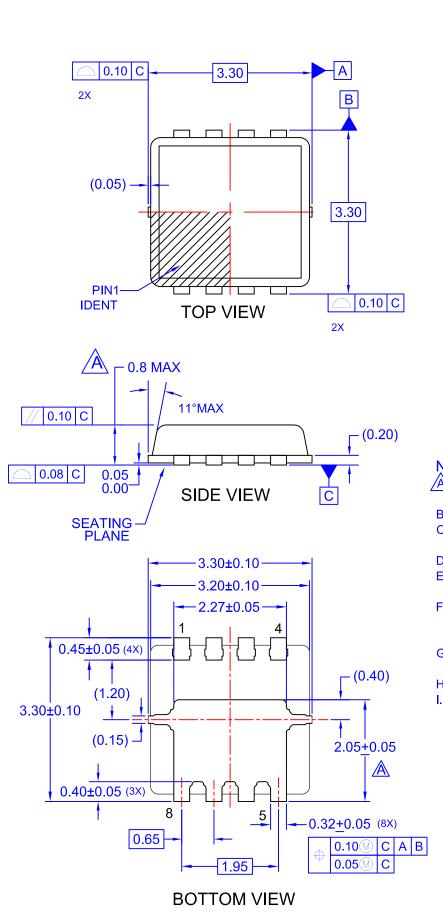
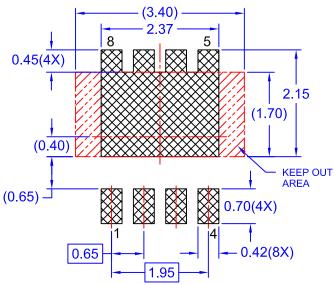


Figure 13. Junction-to-Ambient Transient Thermal Response Curve





RECOMMENDED LAND PATTERN

NOTES:

- A EXCEPT AS NOTED, PACKAGE CONFORMS TO JEDEC REGISTRATION MO-240 VARIATION BA.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
- E. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS.
- F. FLANGE DIMENSIONS INCLUDE INTERTERMINAL FLASH OR PROTRUSION. INTERTERMINAL FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.
- G. IT IS RECOMMENDED TO HAVE NO TRACES OR VIA WITHIN THE KEEP OUT AREA.
- H. DRAWING FILENAME: MKT-MLP08Trev4.
- GENERAL RADII FOR ALL CORNERS SHALL BE 0.20MM MAX.



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