Finisar

Product Specification

Multiprotocol 80Km, 10Gb/s DWDM XFP Optical Transceiver FTLX3815M3xx

PRODUCT FEATURES

- Supports 8.5Gb/s to 11.35Gb/s
- Hot-pluggable XFP footprint
- RoHS-6 Compliant (lead-free)
- 100GHz ITU Grid, C-Band
- Duplex LC connector
- Power dissipation <3.5W
- Built-in digital diagnostic functions
- Temperature range: 0°C to 70°C
- Point-to-Point & OSNR optimized versions
- Reference Clock Not Required



APPLICATIONS

- ITU G.698.1, DW100S-2Dx compliant DWDM 10G SONET/SDH
- ITU G.698.2, DW100C-2Ax compliant DWDM 10G SONET/SDH
- DWDM, IEEE 10GBASE-ZR based Ethernet
- 10GFC (SM-1200-LL-L) & 8GFC (SM-800-LC-L) compliant
- ITU G.709 / OTN FEC applications

Finisar's FTLX3815M3xx Small Form Factor 10Gb/s (XFP) transceiver complies with the XFP Multi-Source Agreement (MSA) Specification¹. It supports amplified DWDM 10Gb/s SONET/SDH, 10 Gigabit Ethernet, and 10 Gigabit Fibre Channel applications over 80km of fiber without dispersion compensation. Digital diagnostics functions are available via a 2-wire serial interface, as specified in the XFP MSA. The transceiver is RoHS compliant and lead free per Directive 2002/95/EC³, and Finisar Application Note AN-2038⁴.

PRODUCT SELECTION

FTLX3815M3xx

xx: 100GHz ITU-T channel

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I. **Pin Descriptions**

II.

| Pin | Logic | Symbol | Name/Description | Ref. |
|-----|---------|------------|---|------|
| 1 | Logic | GND | Module Ground | 1 |
| 2 | | VEE5 | Optional –5.2 Power Supply – Not used | |
| 3 | LVTTL-I | Mod-Desel | Module De-select; When held low allows the module to | |
| 3 | LVIILI | Wiod Descr | respond to 2-wire serial interface commands | |
| 4 | LVTTL-O | | Interrupt (bar); Indicates presence of an important condition | 2 |
| • | 2,112 0 | Interrupt | which can be read over the serial 2-wire interface | _ |
| 5 | LVTTL-I | TX DIS | Transmitter Disable; Transmitter laser source turned off | |
| 6 | | VCC5 | +5 Power Supply | |
| 7 | | GND | Module Ground | 1 |
| 8 | | VCC3 | +3.3V Power Supply | |
| 9 | | VCC3 | +3.3V Power Supply | |
| 10 | LVTTL-I | SCL | Serial 2-wire interface clock | 2 |
| 11 | LVTTL- | SDA | Serial 2-wire interface data line | 2 |
| | I/O | | | |
| 12 | LVTTL-O | Mod_Abs | Module Absent; Indicates module is not present. Grounded | 2 |
| | | _ | in the module. | |
| 13 | LVTTL-O | Mod NR | Module Not Ready; Finisar defines it as a logical OR | 2 |
| | | _ | between RX LOS and Loss of Lock in TX/RX. | |
| 14 | LVTTL-O | RX LOS | Receiver Loss of Signal indicator | 2 |
| 15 | | GND | Module Ground | 1 |
| 16 | | GND | Module Ground | 1 |
| 17 | CML-O | RD- | Receiver inverted data output | |
| 18 | CML-O | RD+ | Receiver non-inverted data output | |
| 19 | | GND | Module Ground | 1 |
| 20 | | VCC2 | +1.8V Power Supply – Not used | |
| 21 | LVTTL-I | P Down/RST | Power Down; When high, places the module in the low | |
| | | _ | power stand-by mode and on the falling edge of P_Down | |
| | | | initiates a module reset | |
| | | | Reset; The falling edge initiates a complete reset of the | |
| | | | module including the 2-wire serial interface, equivalent to a | |
| | | | power cycle. | |
| 22 | | VCC2 | +1.8V Power Supply – Not used | |
| 23 | | GND | Module Ground | 1 |
| 24 | PECL-I | RefCLK+ | Reference Clock non-inverted input, AC coupled on the | |
| | | | host board – Not Required | |
| 25 | PECL-I | RefCLK- | Reference Clock inverted input, AC coupled on the host | |
| | | | board – Not Required | |
| 26 | | GND | Module Ground | 1 |
| 27 | | GND | Module Ground | 1 |
| 28 | CML-I | TD- | Transmitter inverted data input | |
| 29 | CML-I | TD+ | Transmitter non-inverted data input | |
| 30 | | GND | Module Ground | 1 |

Notes:

- Module circuit ground is isolated from module chassis ground within the module.
 Open collector; should be pulled up with 4.7k 10kohms on host board to a voltage between 3.15V and 3.6V.

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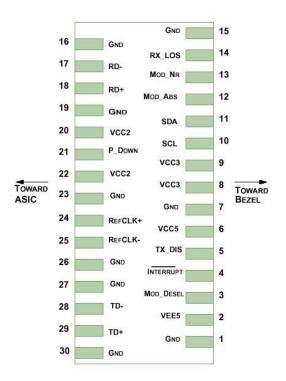


Diagram of Host Board Connector Block Pin Numbers and Names

II. Absolute Maximum Ratings

| Parameter | Symbol | Min | Тур | Max | Unit | Ref. |
|----------------------------|------------|------|-----|-----|------|------|
| Maximum Supply Voltage #1 | Vcc3 | -0.5 | | 4.0 | V | |
| Maximum Supply Voltage #2 | Vcc2 | -0.5 | | 6.0 | V | |
| Storage Temperature | T_{S} | -40 | | 85 | °C | |
| Case Operating Temperature | T_{OP} | 0 | | 70 | °C | |
| Receiver Damage Threshold | P_{Rdmg} | +5 | | | dBm | |

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III. Electrical Characteristics ($T_{OP} = -5$ to 70 °C, $V_{CC5} = 4.75$ to 5.25 Volts)

| | FTLX3815M3xx | | | | | | | |
|-----------------------------------|------------------------|-----------|----------|---------------------|------|------|--|--|
| Parameter | Symbol | Min | Тур | Max | Unit | Ref. | | |
| Supply Voltage #1 | Vcc3 | 3.13 | | 3.46 | V | | | |
| Supply Voltage #2 | Vcc5 | 4.75 | | 5.25 | V | | | |
| Supply Current – Vcc5 supply | Icc5 | | | 450 | mA | | | |
| Supply Current – Vcc3 supply | Icc3 | | | 750 | mA | | | |
| Module total power dissipation | P | | | 3.5 | W | 1 | | |
| Transmitter | | | | | | | | |
| Input differential impedance | R _{in} | | 100 | | Ω | 2 | | |
| Differential data input swing | Vin,pp | 120 | | 820 | mV | | | |
| Transmit Disable Voltage | V_{D} | 2.0 | | Vcc | V | 3 | | |
| Transmit Enable Voltage | V_{EN} | GND | | GND+ 0.8 | V | | | |
| Receiver | | | | | | | | |
| Differential data output swing | Vout,pp | | 500 | 850 | mV | 4 | | |
| Data output rise time | $t_{\rm r}$ | | | 40 | ps | 5 | | |
| Data output fall time | t_{f} | | | 40 | ps | 5 | | |
| LOS Fault | V _{LOS fault} | Vcc - 0.5 | | Vcc _{HOST} | V | 6 | | |
| LOS Normal | $V_{LOS\ norm}$ | GND | | GND+0.5 | V | 6 | | |
| Power Supply Rejection | PSR | | See Note | e 7 below | | 7 | | |
| Reference Clock (AC-Coupled) | | | | | | | | |
| Single-ended peak to peak voltage | V_{SEPP} | 200 | | 450 | mV | | | |
| swing | | | | | | | | |
| Single-ended resistance | $R_{\rm L}$ | 40 | 50 | 60 | | | | |
| Frequency clock tolerance | Δf | -100 | | +100 | ppm | | | |
| Duty cycle | - | 40 | | 60 | % | | | |

Notes:

- 1. Maximum total power value is specified across the full temperature and voltage range.
- 2. After internal AC coupling.
- 3. Or open circuit.
- 4. Into 100 ohms differential termination.
- 5. 20 80 %
- 6. Loss Of Signal is open collector to be pulled up with a 4.7k 10kohm resistor to 3.15 3.6V. Logic 0 indicates normal operation; logic 1 indicates no signal detected.
- 7. Per Section 2.7.1. in the XFP MSA Specification¹.

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XII. Optical Characteristics (EOL, $T_{OP} = -5$ to 70° C, $V_{CCS} = 4.75$ to 5.25 Volts)

| Transmitter | | | | | | |
|-------------------------------------|-------------|-------|-----|-------|------|-----|
| Parameter | Symbol | Min | Тур | Max | Unit | Ref |
| Output Opt. Pwr: 9/125 SMF | P_{OUT} | -1 | | +3 | dBm | |
| Optical Extinction Ratio | ER | 8.2 | | | dB | |
| Center Wavelength Spacing | | | 100 | | GHz | 1 |
| Transmitter Center Wavelength – | λc | X-100 | X | X+100 | pm | 2 |
| End Of Life | | | | | | |
| Transmitter Center Wavelength – | λc | X-25 | X | X+25 | pm | 2 |
| Beginning Of Life | | | | | | |
| Sidemode Suppression ratio | SSR_{min} | 35 | | | dB | |
| Tx Jitter Generation (peak-to-peak) | Tx_j | | | 0.1 | UI | 3 |
| Tx Jitter Generation (RMS) | Tx_{jRMS} | | | 0.01 | UI | 4 |
| Tx Locked Eye (Cold Start) | | | | 30 | S | |

| Receiver | | | | | |
|---------------------------|------------------|------|------|-----|--|
| Overload | P_{MAX} | -6 | | dBm | |
| Optical Center Wavelength | $\lambda_{ m C}$ | 1270 | 1615 | nm | |
| Receiver Reflectance | R_{rx} | | -27 | dB | |
| LOS De-Assert | LOS_D | | -30 | dBm | |
| LOS Assert | LOS_A | -37 | | dBm | |
| LOS Hysteresis | | 0.5 | | dB | |

| | FTLX3815M3xx | | | | | | | | |
|------------------|-----------------------------------|--------------------|---|---------------------------------------|---------------------------------|--|--|--|--|
| Receiver S | Receiver Sensitivity ⁵ | | | | | | | | |
| Data rate (Gb/s) | BER | Dispersion (ps/nm) | Sensitivity back-to- back at OSNR>30dB (dBm) | Power Penalty at OSNR>30dB (dB) | Threshold Adjust Required | | | | |
| 8.5 | 1e-12 | -500 to 1450 | -24 | 3 | No | | | | |
| 9.95 | 1e-12 | -500 to 1450 | -24 | 3 | No | | | | |
| 10.3 | 1e-12 | -500 to 1450 | -24 | 3 | No | | | | |
| 10.7 | 1e-4 | -500 to 1450 | -27 | 3 | Yes | | | | |
| 11.1 | 1e-4 | -500 to 1450 | -27 | 3 | Yes | | | | |
| 11.3 | 1e-4 | -500 to 1450 | -27 | 3 | Yes | | | | |

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| OSNR Performan | ce ⁶ | | | 6 |
|---------------------|-----------------|--------------------|---|-----------------------------------|
| Data rate (Gb/s) | BER | Dispersion (ps/nm) | Max OSNR w/ dispersion at Power: -7 to -18dBm (dB) | Threshold Adjustm. Required |
| 8.5 | 1e-12 | -500 to 1450 | 28 | No |
| 9.95 | 1e-12 | -500 to 1450 | 28 | No |
| 10.3 | 1e-12 | -500 to 1450 | 28 | No |
| 10.7 | 1e-4 | -500 to 1300 | 22 | Yes |
| 11.1 | 1e-4 | -500 to 1300 | 22 | Yes |
| 11.3 | 1e-4 | -500 to 1100 | 22 | Yes |

Notes:

- 1. Corresponds to approximately 0.8 nm.
- 2. X = Specified ITU Grid wavelength. Wavelength stability is achieved within 10 seconds of power up.
- 3. Measured with a host jitter of 50 mUI peak-to-peak.
- 4. Measured with a host jitter of 7 mUI RMS.
- 5. Measured at 1528-1600nm with worst ER; PRBS31.
- 6. All OSNR measurements are performed with 0.1nm resolution.

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Part Numbers for Amplified (OSNR) Applications:

| Channel # | Product Code | Frequency (THz) | Center Wavelength (nm) |
|-----------|--------------|-----------------|------------------------|
| 17 | FTLX3815M317 | 191.7 | 1563.86 |
| 18 | FTLX3815M318 | 191.8 | 1563.05 |
| 19 | FTLX3815M319 | 191.9 | 1562.23 |
| 20 | FTLX3815M320 | 192.0 | 1561.42 |
| 21 | FTLX3815M321 | 192.1 | 1560.61 |
| 22 | FTLX3815M322 | 192.2 | 1559.79 |
| 23 | FTLX3815M323 | 192.3 | 1558.98 |
| 24 | FTLX3815M324 | 192.4 | 1558.17 |
| 25 | FTLX3815M325 | 192.5 | 1557.36 |
| 26 | FTLX3815M326 | 192.6 | 1556.55 |
| 27 | FTLX3815M327 | 192.7 | 1555.75 |
| 28 | FTLX3815M328 | 192.8 | 1554.94 |
| 29 | FTLX3815M329 | 192.9 | 1554.13 |
| 30 | FTLX3815M330 | 193.0 | 1553.33 |
| 31 | FTLX3815M331 | 193.1 | 1552.52 |
| 32 | FTLX3815M332 | 193.2 | 1551.72 |
| 33 | FTLX3815M333 | 193.3 | 1550.92 |
| 34 | FTLX3815M334 | 193.4 | 1550.12 |
| 35 | FTLX3815M335 | 193.5 | 1549.32 |
| 36 | FTLX3815M336 | 193.6 | 1548.51 |
| 37 | FTLX3815M337 | 193.7 | 1547.72 |
| 38 | FTLX3815M338 | 193.8 | 1546.92 |
| 39 | FTLX3815M339 | 193.9 | 1546.12 |
| 40 | FTLX3815M340 | 194.0 | 1545.32 |
| 41 | FTLX3815M341 | 194.1 | 1544.53 |
| 42 | FTLX3815M342 | 194.2 | 1543.73 |
| 43 | FTLX3815M342 | 194.3 | 1542.94 |
| 44 | FTLX3815M344 | 194.4 | 1542.14 |
| 45 | FTLX3815M345 | 194.5 | 1541.35 |
| 46 | FTLX3815M346 | 194.6 | 1540.56 |
| 47 | FTLX3815M347 | 194.7 | 1539.77 |
| 48 | FTLX3815M348 | 194.7 | 1538.98 |
| 49 | FTLX3815M349 | 194.9 | 1538.19 |
| 50 | FTLX3815M350 | 194.9 | 1537.40 |
| | | | |
| 51 | FTLX3815M351 | 195.1 | 1536.61 |
| 52 | FTLX3815M352 | 195.2 | 1535.82 |
| 53 | FTLX3815M353 | 195.3 | 1535.04 |
| 54 | FTLX3815M354 | 195.4 | 1534.25 |
| 55 | FTLX3815M355 | 195.5 | 1533.47 |
| 56 | FTLX3815M356 | 195.6 | 1532.68 |
| 57 | FTLX3815M357 | 195.7 | 1531.90 |
| 58 | FTLX3815M358 | 195.8 | 1531.12 |
| 59 | FTLX3815M359 | 195.9 | 1530.33 |
| 60 | FTLX3815M360 | 196.0 | 1529.55 |
| 61 | FTLX3815M361 | 196.1 | 1528.77 |

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V. Additional Specifications and Response Timing

| Parameter | Symbol | Min | Тур | Max | Units | Ref. |
|-------------------------------|-----------|-----|-----|-------|-------|------|
| Bit Rate | BR | 8.5 | | 11.35 | Gb/s | 1 |
| Maximum Supported Link Length | L_{MAX} | | 80 | | km | 2 |

Notes:

- Amplified SONET OC-192, 10G Ethernet, SONET OC-192 with FEC, 10G Ethernet with FEC, 10GFC, and 8GFC
- 2. Distance indicates dispersion budget. Optical amplification may be required to achieve maximum distance.

Response timing:

| Parameter | | Min | Тур | Max | Units | Ref. |
|---------------------------------|-----------|-----|-----|-----|-------|------|
| Tx_Dis | Assert | | | 10 | us | |
| | De-assert | | | 2 | ms | |
| Rx_LOS | Asset | | | 100 | us | |
| | De-assert | | | 100 | us | |
| Mod_NR | Asset | | | 1 | ms | |
| | De-assert | | | 1 | ms | |
| Interrupt | Asset | | | 200 | ms | |
| | De-assert | | | 500 | us | |
| P_Down/RST Time | | 10 | | | us | |
| P_Down/RST Asser Delay | | | | 100 | us | |
| Start-up time (Initialize time) | | | | 300 | ms | 1 |

1. Time required for transponder to be ready to begin I2C communication with host from a cold start or a hardware reset condition.

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VI. **Environmental Specifications**

Finisar XFP transceivers have an operating temperature range from 0°C to +70°C case temperature.

| Parameter | Symbol | Min | Тур | Max | Units | Ref. |
|----------------------------|-----------|-----|-----|-----|-------|------|
| Case Operating Temperature | T_{op} | 0 | | 70 | °C | |
| Storage Temperature | T_{sto} | -40 | | 85 | °C | |

VII. **Regulatory Compliance**

Finisar XFP transceivers are Class 1 Laser Products. They are certified per the following standards:

| Feature | Agency | Standard | Certificate Number |
|----------------------|----------|--|-----------------------|
| Laser Eye Safety | FDA/CDRH | CDRH 21 CFR 1040 and Laser Notice 50 | TBD |
| Laser Eye Safety | TÜV | EN 60825-1: 1994+A11:1996+A2:2001 IEC 60825-1: 1993+A1:1997+A2:2001 IEC 60825-2: 2000, Edition 2 | TBD |
| Electrical Safety | TÜV | EN 60950 | TBD |
| Electrical Safety | UL/CSA | CLASS 3862.07 CLASS 3862.87 | TBD |

Copies of the referenced certificates are available at Finisar Corporation upon request.

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VIII. Digital Diagnostics Functions

As defined by the XFP MSA¹, Finisar XFP transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current
- Transmitted optical power
- Received optical power
- Transceiver supply voltage
- TEC Temperature

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the XFP transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the XFP transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

For more detailed information, including memory map definitions, please see the XFP MSA documentation¹.

Receiver Threshold Adjustment

The FTLX3815M3xx also provide access to receiver decision threshold adjustment via 2-wire serial interface, in order to improve receiver OSNR performance based on specific link conditions. It is implemented as follows:

• Rx Threshold of XFP transceivers will be factory-set for optimized performance in non-FEC applications. This will be the default value during both cold start (power-up) and warm start (module reset).

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- The transceiver supports adjustment of Rx Threshold value by the host through register 76d, table 01h. This is intended to be used in FEC applications.
- Register 76d, table 01h is a volatile memory. Therefore if the transceiver is power-cycled, the register starts up with a value of 00h which corresponds to the default Rx Threshold value.
- The threshold adjustment input value is 2's complement 7 bit value (-128 to +127). The default Rx threshold value will be approximately 0. Full range of adjustment provides at least a $\pm 10\%$ change in Rx threshold from the default value.

SBS suppression, dither tone

Set Address 111, bit 1 to "0" to enable tone, "1" to disable dither tone (defaults: frequency = 40kHz, tone is disabled). Please contact your Finisar RSM or PLM if specific amplitudes and frequencies are needed for SBS suppression.

8.5Gb/s Fibre-Channel CDR Bypass rate select:

For 8G FC operation, write "1" to Byte 116, bit 1. Every time that the module is power cycled, this will need to be re-written (bit goes back to "0" and CDR is now set for 10Gb/s operation) in order to operate properly at 8G FC.

Contact your Finisar RSM or PLM for details on the CDR Bypass.

Write "1" to Byte 116, bit 1. Every time that the module is power cycled, this will need to be re-written (bit goes back to "0" and CDR is now set for 10Gb/s operation) in order to operate properly at 8G FC.

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Alarm and Warning Threshold Values

| Address | Parameter | Threshold Values | UNITS |
|---------|-----------------------|---------------------|-------|
| 02-03 | Temp High Alarm | 78 | С |
| 04-05 | Temp Low Alarm | -13 | С |
| 06-07 | Temp High Warning | 73 | C |
| 08-09 | Temp Low Warning | -8 | C |
| 10-17 | Reserved | | |
| 18-19 | Bias High Alarm | 120 | mA |
| 20-21 | Bias Low Alarm | 10 | mA |
| 22-23 | Bias High Warning | 100 | mA |
| 24-25 | Bias Low Warning | 15 | mA |
| 26-27 | TX Power High Alarm | +5 | dBm |
| 28-29 | TX Power Low Alarm | -3 | dBm |
| 30-31 | TX Power High Warning | +4 | dBm |
| 32-33 | TX Power Low Warning | -2 | dBm |
| 34-35 | RX Power High Alarm | -4 | dBm |
| 36-37 | RX Power Low Alarm | -31 | dBm |
| 38-39 | RX Power High Warning | -5 | dBm |
| 40-41 | RX Power Low Warning | -25 | dBm |
| 42-43 | AUX 1 High Alarm | 57 | С |
| 44-45 | AUX 1 Low Alarm | 20 | С |
| 46-47 | AUX 1 High Warning | 54 | С |
| 48-49 | AUX 1 Low Warning | 25 | С |
| 50-51 | AUX 2 High Alarm | 3.564 | V |
| 52-53 | AUX 2 Low Alarm | 3.036 | V |
| 54-55 | AUX 2 High Warning | 3.465 | V |
| 56-57 | AUX 2 Low Warning | 3.135 | V |

A/D Table

| Address | Parameter | Accuracy | Resolution | Units | Note s |
|---------|--------------------|-----------|------------|-------|---------------------|
| 96-97 | Internal module | +/-3 | +/- 0.1 | degC | PCB mounted |
| | Temp | | | | thermocouple |
| 98-99 | Reserved | | | | |
| 100-101 | TX bias current | +/-8 | +/-2 | uA | |
| 102-103 | Transmit Power | +/-1.5 dB | 0.1 | uW | |
| 104-105 | Receive Power | +/-1.5 dB | +/-0.1 | uW | |
| 106-107 | Auxiliary monitor1 | +/-3 | +/-0.1 | degC | Laser Temperature |
| 108-109 | Auxiliary monitor2 | +/-3 | +/-100 | uV | 3.3V Supply Voltage |

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EEPROM (Table A0h)

| | | 01 | | Table Auli) | | | |
|--|--|--|--|--|--|---|---------------------------------------|
| Byte | | ıcn | Bit | Na | De contration | Value | Haw Value |
| Addr | | _ | _ | | Description | Value | Hex Value |
| 0 | 00 | 0 | _ | | Type of serial transceiver | 6 | 6 |
| 1 | 01 | 0 | _ | 5 | Signal Conditioner Control | 0 | 0 |
| 2 | 02 | 0 | | | MSB at low address | 78 | |
| 4 | 04 | 0 | | | MSB at low address | -13 | |
| 6 | 06 | 0 | | | MSB at low address | 73 | |
| 8 | 08 | 0 | | | MSB at low address | -8 | 00.00 |
| 10 | OA | 0 | , | 9 | MSB at low address | 0 | 00 00 |
| 12 | 0C | 0 | , | | MSB at low address | 0 | 00 00 |
| 14 | 0E | 0 | _ | 3 3 | MSB at low address | 0 | 00 00 |
| 16 | 10 | 0 | _ | - | MSB at low address | 0 | 00 00 |
| 18 | 12 | 0 | _ | | MSB at low address | 120 | |
| 20 | 14 | 0 | _ | | MSB at low address | 10 | |
| 22 | 16 | 0 | _ | | MSB at low address | 110 | |
| 24 | 18 | 0 | | - | MSB at low address | 15 | |
| 26 | 1A | 0 | _ | | MSB at low address | +5 | |
| 28 | 1C | 0 | | | MSB at low address | -3 | |
| 30 | 1E | 0 | | ŭ ŭ | MSB at low address | +4 | |
| 32 | 20 | 0 | _ | | MSB at low address | -2 | |
| 34 | 22 | 0 | _ | | MSB at low address | -4 | |
| 36 | 24 | 0 | _ | | MSB at low address | -31 | |
| 38 | 26 | 0 | _ | | VISB at low address | -5 | |
| 40 | 28 | 0 | _ | - | VISB at low address | -25 | |
| 42 | 2A | 0 | | | VISB at low address | 57 | |
| 44 | 2C | 0 | | | VISB at low address | 20 | |
| 46 | 2E | 0 | | Ü | VISB at low address | 54 | |
| 48 | 30 | 0 | | Ü | VISB at low address | 25 | |
| 50 | 32 | 0 | , | | MSB at low address | 3.564 | |
| 52 | 34 | 0 | _ | | MSB at low address | 3.036 | |
| 54 | 36 | 0 | , | | MSB at low address | 3.465 | |
| 56 | 38 | 0 | 16 | AUX 2 Low Warning | MSB at low address | 3.135 | |
| 58 | 3A | 0 | 16 | | Optional VPS Control Registers | 0 | |
| 60 | 3C | 0 | 80 | RESERVED I | RESERVED | NA | NA |
| · | | ĺ | ĺ | , | Acceptable BER Reported by the FEC to the | | |
| 70 | 46 | 0 | 8 | Acceptable BER I | Module | 0 | 0 |
| | | | ĺ | / | Actual BER Reported by the FEC to the | | |
| 71 | 47 | 0 | 8 | Actual BER I | Module | 0 | 0 |
| | | | ĺ | Į. | User input of Wavelength setpoint. (Units of | | |
| 72 | 48 | 0 | 8 | Wavelength Set MSB (| 0.05nm) | 0 | 0 |
| <i>*</i> | | ĺ | ĺ | Į. | User input of Wavelength setpoint. (Units of | | |
| 73 | 49 | 0 | 8 | Wavelength Set LSB (| 0.05nm) | 0 | 0 |
| | | | ľ | I | Monitor of Current Wavelength Error. (Units | | |
| 74 | 4A | 0 | 8 | Wavelength Error MSB | of 0.005nm) | 0 | 0 |
| 75 | 4B | 0 | 8 | Wavelength Error MSB | Signed 2's complement value | 0 | 0 |
| | | | ľ | I | Relative amplitude of receive quantization | (| |
| 76 | 4C | 0 | 8 | Amplitude Adjustment t | hreshold | 0 | 0 |
| | | | | | Phase of receive quantization relative to 0.5 | | |
| | | | | | | _ | 0 |
| 77 | 4D | 0 | 8 | Phase Adjustment | JI | 0 | |
| 77 78 | 4D 4E | 0 | _ | | JI RESERVED | 0 NA | NA |
| _ | - | | 16 | RESERVED | | | |
| 78 | 4E | 0 | 16 1 | RESERVED I L- TX Power Low Alarm I | RESERVED | NA | NA |
| 78 80 | 4E 50 | 0 | 16 1 | RESERVED I L- TX Power Low Alarm I L- TX Power High Alarm | RESERVED Latched low TX Power alarm. | NA FALSE | NA 0 |
| 78 80 80 | 4E 50 50 | 0 0 1 | 16 1 1 | RESERVED I L- TX Power Low Alarm I L- TX Power High Alarm I L- TX Bias Low Alarm I | RESERVED .atched low TX Power alarm. .atched high TX Power alarm. | NA FALSE FALSE | NA 0 0 |
| 78 80 80 80 | 4E 50 50 50 | 0 0 1 2 | 16 1 1 1 | RESERVED I L- TX Power Low Alarm I L- TX Power High Alarm I L- TX Bias Low Alarm I L- TX Bias High Alarm I L- TX Bias High Alarm I | RESERVED .atched low TX Power alarmatched high TX Power alarmatched low TX Bias alarm. | NA FALSE FALSE FALSE | NA 0 0 0 |
| 78 80 80 80 80 | 4E 50 50 50 50 | 0 0 1 2 3 | 16 1 1 1 1 1 | RESERVED I L- TX Power Low Alarm I L- TX Power High Alarm I L- TX Bias Low Alarm I L- TX Bias High Alarm I L- TX Bias High Alarm I L- Vcc Low Alarm I | RESERVED .atched low TX Power alarmatched high TX Power alarmatched low TX Bias alarmatched high TX Bias alarm. | NA FALSE FALSE FALSE FALSE | NA 0 0 0 0 |
| 78 80 80 80 80 80 | 4E 50 50 50 50 | 0 0 1 2 3 4 | 16 1 1 1 1 1 1 | RESERVED I L- TX Power Low Alarm I L- TX Power High Alarm I L- TX Bias Low Alarm I L- TX Bias High Alarm I L- TX Bias High Alarm I L- Vcc Low Alarm I L- Vcc High Alarm I L- Vcc High Alarm I L- Vcc High Alarm I | RESERVED .atched low TX Power alarmatched high TX Power alarmatched low TX Bias alarmatched high TX Bias alarmatched high TX Bias alarmatched low Vcc alarm. | NA FALSE FALSE FALSE FALSE FALSE FALSE FALSE | NA 0 0 0 0 0 |
| 78 80 80 80 80 80 | 4E 50 50 50 50 50 50 | 0 0 1 2 3 4 5 | 16 1 1 1 1 1 1 | RESERVED L- TX Power Low Alarm L- TX Power High Alarm L- TX Bias Low Alarm L- TX Bias High Alarm L- TX Bias High Alarm L- VCc Low Alarm L- Vcc Low Alarm L- Vcc High Alarm L- Temp Low Alarm | RESERVED .atched low TX Power alarmatched high TX Power alarmatched low TX Bias alarmatched high TX Bias alarmatched low Vcc alarmatched high Vcc alarm. | NA FALSE FALSE FALSE FALSE FALSE FALSE FALSE FALSE | NA 0 0 0 0 0 0 |
| 78 80 80 80 80 80 80 | 4E 50 50 50 50 50 50 | 0 0 1 2 3 4 5 6 | 16 1 1 1 1 1 1 1 1 | RESERVED L- TX Power Low Alarm L- TX Bias Low Alarm L- TX Bias Low Alarm L- TX Bias High Alarm L- TX Bias High Alarm L- VCC LOW Alarm L- VCC High Alarm L- TEmp Low Alarm L- Temp Low Alarm | AESERVED Latched low TX Power alarm. Latched high TX Power alarm. Latched low TX Bias alarm. Latched high TX Bias alarm. Latched low Vcc alarm. Latched high Vcc alarm. Latched low TX Bias alarm. Latched high Vcc alarm. Latched low Temperature alarm. | NA FALSE | NA 0 0 0 0 0 0 0 |
| 78 80 80 80 80 80 80 80 | 4E 50 50 50 50 50 50 50 | 0 0 1 2 3 4 5 6 7 | 16 1 1 1 1 1 1 1 1 | RESERVED L- TX Power Low Alarm L- TX Bias Low Alarm L- TX Bias High Alarm L- TX Bias High Alarm L- Vcc Low Alarm L- Vcc High Alarm L- TC mp Low Alarm L- Temp Low Alarm L- Temp High Alarm RESERVED | AESERVED Latched low TX Power alarm. Latched high TX Power alarm. Latched low TX Bias alarm. Latched high TX Bias alarm. Latched low Vcc alarm. Latched low Vcc alarm. Latched low Tecnarm. Latched low Temperature alarm. Latched high Temperature alarm. | NA FALSE | NA 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |
| 78 80 80 80 80 80 80 80 81 81 | 4E 50 50 50 50 50 50 50 51 51 | 0 0 1 2 3 4 5 6 7 0 | 16 1 1 1 1 1 1 1 1 1 | RESERVED L- TX Power Low Alarm L- TX Bias Low Alarm L- TX Bias High Alarm L- TX Bias High Alarm L- Vcc Low Alarm L- Vcc High Alarm L- Temp Low Alarm L- Temp High Alarm RESERVED RESERVED | AESERVED Latched low TX Power alarm. Latched high TX Power alarm. Latched low TX Bias alarm. Latched high TX Bias alarm. Latched low Vcc alarm. Latched high Vcc alarm. Latched low Temperature alarm. Latched high Temperature alarm RESERVED | NA FALSE NA NA | NA 0 0 0 0 0 0 0 0 0 0 NA NA |
| 78 80 80 80 80 80 80 80 81 81 | 4E 50 50 50 50 50 50 50 51 51 | 0 0 1 2 3 4 5 6 7 0 1 | 16 1 1 1 1 1 1 1 1 1 1 1 | RESERVED L- TX Power Low Alarm L- TX Power High Alarm L- TX Bias Low Alarm L- TX Bias High Alarm L- Vcc Low Alarm L- Vcc High Alarm L- Temp Low Alarm L- Temp High Alarm RESERVED RESERVED L- AUX 2 Low Alarm | AESERVED Latched low TX Power alarm. Latched high TX Power alarm. Latched high TX Bias alarm. Latched high TX Bias alarm. Latched low Vcc alarm. Latched high Vcc alarm. Latched low TEmperature alarm. Latched high TEmperature alarm RESERVED RESERVED Latched low AUX2 monitor alarm. | NA FALSE NA NA FALSE | NA 0 0 0 0 0 0 0 0 0 0 NA NA 0 |
| 78 80 80 80 80 80 80 80 81 81 81 | 4E 50 50 50 50 50 50 51 51 51 | 0 0 1 2 3 4 5 6 7 0 1 2 3 | 16 1 1 1 1 1 1 1 1 1 1 1 | RESERVED L- TX Power Low Alarm L- TX Power High Alarm L- TX Bias Low Alarm L- TX Bias High Alarm L- TX Bias High Alarm L- YCC Low Alarm L- VCC High Alarm L- Temp Low Alarm L- Temp High Alarm RESERVED RESERVED L- AUX 2 Low Alarm L- AUX 2 Low Alarm | RESERVED Latched low TX Power alarm. Latched high TX Power alarm. Latched high TX Bias alarm. Latched high TX Bias alarm. Latched low Vcc alarm. Latched high Vcc alarm. Latched low Temperature alarm. Latched high Temperature alarm RESERVED RESERVED Latched low AUX2 monitor alarm. Latched high AUX2 monitor alarm. | NA FALSE NA NA NA FALSE FALSE FALSE | NA 0 0 0 0 0 0 0 0 0 0 NA NA 0 0 |
| 78 80 80 80 80 80 80 81 81 81 81 | 4E 50 50 50 50 50 50 50 51 51 51 51 | 0 0 1 2 3 4 5 6 7 0 1 2 3 4 | 16 1 1 1 1 1 1 1 1 1 1 1 1 1 | RESERVED L- TX Power Low Alarm L- TX Power High Alarm L- TX Bias Low Alarm L- TX Bias High Alarm L- TX Bias High Alarm L- VCc Low Alarm L- VCc Low Alarm L- Temp Low Alarm L- Temp High Alarm RESERVED RESERVED L- AUX 2 Low Alarm L- AUX 2 Low Alarm L- AUX 2 Low Alarm | AESERVED Latched low TX Power alarm. Latched high TX Power alarm. Latched high TX Bias alarm. Latched high TX Bias alarm. Latched low Vcc alarm. Latched high Vcc alarm. Latched low Vcc alarm. Latched low Temperature alarm. Latched high Temperature alarm RESERVED RESERVED Latched low AUX2 monitor alarm. Latched high AUX2 monitor alarm. Latched low AUX1 monitor alarm. Latched low AUX1 monitor alarm. Latched low AUX1 monitor alarm. | NA FALSE NA NA NA FALSE FALSE FALSE | NA 0 0 0 0 0 0 0 0 0 0 NA NA 0 0 0 |
| 78 80 80 80 80 80 80 80 81 81 81 | 4E 50 50 50 50 50 50 51 51 51 | 0 0 1 2 3 4 5 6 7 0 1 2 3 | 16 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 | RESERVED L- TX Power Low Alarm L- TX Power High Alarm L- TX Bias Low Alarm L- TX Bias High Alarm L- TX Bias High Alarm L- VCC Low Alarm L- VCC High Alarm L- Temp Low Alarm L- Temp High Alarm RESERVED RESERVED L- AUX 2 Low Alarm L- AUX 2 Ligh Alarm L- AUX 1 Ligh Alarm L- AUX 1 Ligh Alarm | RESERVED Latched low TX Power alarm. Latched high TX Power alarm. Latched high TX Bias alarm. Latched high TX Bias alarm. Latched low Vcc alarm. Latched high Vcc alarm. Latched low Temperature alarm. Latched high Temperature alarm RESERVED RESERVED Latched low AUX2 monitor alarm. Latched high AUX2 monitor alarm. | NA FALSE NA NA NA FALSE FALSE FALSE | NA 0 0 0 0 0 0 0 0 0 0 NA NA 0 0 |

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EEPROM (Table A0h) continued

| | | · | 141 | (Table Aon) continue | | | |
|----------------|----------|--------|-----|--|---|----------------|---------|
| 82 | 52 | 0 | | L- TX Power Low Warning | Latched low TX Power warning. | FALSE | 0 |
| 82 | 52 | 1 | 1 | L- TX Power High Warning | Latched high TX Power warning. | FALSE | 0 |
| 82 | 52 | 2 | 1 | L- TX Bias Low Warning | Latched low TX Bias warning. | FALSE | 0 |
| 82 | 52 | 3 | 1 | L- TX Bias High Warning | Latched high TX Bias warning. | FALSE | 0 |
| 82 | 52 | 4 | 1 | L- Vcc Low Warning | Latched low Vcc warning. | FALSE | 0 |
| 82 | 52 | 5 | 1 | L- Vcc High Warning | Latched high Vcc warning. | FALSE | 0 |
| 82 | 52 | 6 | 1 | L- Temp Low Warning | Latched low Temperature warning. | FALSE | 0 |
| 82 | 52 | 7 | | L- Temp High Warning | Latched high Temperature warning. | FALSE | 0 |
| 83 | 53 | 0 | 1 | RESERVED | RESERVED | NA | NA |
| 83 | 53 | 1 | _ | RESERVED | RESERVED | NA | NA |
| 83 | 53 | 2 | | L- AUX 3 Low Warning | Latched low AUX2 monitor warning. | FALSE | 0 |
| 83 | 53 | 3 | | L- AUX 2 High Warning | Latched high AUX2 monitor warning. | FALSE | 0 |
| 83 | 53 | 4 | | L- AUX 1 Low Warning | Latched low AUX1 monitor warning. | FALSE | 0 |
| | | 5 | | | | | 0 |
| 83 | 53 | | | L- AUX 1 High Warning | Latched high AUX1 monitor warning. | FALSE | |
| 83 | 53 | 6 | | L- RX Power Low Warning | Latched low RX Power warning. | FALSE | 0 |
| 83 | 53 | 7 | _ | L- RX Power High Warning | Latched high RX Power warning. | FALSE | 0 |
| 84 | 54 | 0 | | L- Reset Complete | Latched Reset Complete Flag | FALSE | 0 |
| 84 | 54 | 1 | | L- MOD_NR | Latched Mirror of MOD_NR pin | FALSE | 0 |
| 84 | 54 | 2 | 1 | L- RX CDR not Locked | Latched RX CDR Loss of Lock | FALSE | 0 |
| | | | | | Latched mirror of LOS pin (RX optical loss of | | |
| 84 | 54 | 3 | 1 | L- LOS | signal) | FALSE | 0 |
| 84 | 54 | 4 | 1 | L- RX_NR | Latched RX_NR Status | FALSE | 0 |
| 84 | 54 | 5 | 1 | L- TX CDR not Locked | Latched TX CDR Loss of Lock | FALSE | 0 |
| | | | | | Latched Laser Fault condition. Generated by | | |
| 84 | 54 | 6 | 1 | L- TX Fault | laser safety system. | FALSE | 0 |
| 84 | 54 | 7 | | L- TX NR | Latched TX NR Status. | FALSE | 0 |
| 85 | 55 | 0 | | RESERVED | RESERVED | NA | NA |
| 85 | 55 | 5 | | L- Wavelength Unlocked | Latched Wavelength Unlocked Condition | FALSE | 0 |
| 85 | 55 | 6 | _ | L- TEC Fault | Latched TEC Fault | FALSE | 0 |
| | | 7 | | L- APD Supply Fault | | | 0 |
| 85 | 55 | | | | Latched APD Supply Fault | FALSE | |
| 86 | 56 | 0 | | RESERVED | RESERVED | NA 51165 | NA 0 |
| 88 | 58 | 0 | | M- TX Power Low Alarm | Masking bit for low TX Power alarm. | FALSE | 0 |
| 88 | 58 | 1 | 1 | M- TX Power High Alarm | Masking bit for high TX Power alarm. | FALSE | 0 |
| 88 | 58 | 2 | | M- TX Bias Low Alarm | Masking bit for low TX Bias alarm. | FALSE | 0 |
| 88 | 58 | 3 | 1 | M- TX Bias High Alarm | Masking bit for high TX Bias alarm. | FALSE | 0 |
| 88 | 58 | 4 | 1 | M- Vcc Low Alarm | Masking bit for low Vcc alarm. | FALSE | 0 |
| 88 | 58 | 5 | 1 | M- Vcc High Alarm | Masking bit for high Vcc alarm. | FALSE | 0 |
| 88 | 58 | 6 | 1 | M- Temp Low Alarm | Masking bit for low Temperature alarm. | FALSE | 0 |
| 88 | 58 | 7 | 1 | M- Temp High Alarm | Masking bit for high Temperature alarm. | FALSE | 0 |
| 89 | 59 | 0 | 1 | RESERVED | RESERVED | NA | NA |
| 89 | 59 | 1 | 1 | RESERVED | RESERVED | NA | NA |
| 89 | 59 | 2 | 1 | M- AUX 2 Low Alarm | Masking bit for low AUX2 monitor alarm. | FALSE | 0 |
| 89 | 59 | 3 | 1 | M- AUX 2 High Alarm | Masking bit for high AUX2 monitor alarm. | FALSE | 0 |
| 89 | 59 | 4 | 1 | M- AUX 1 Low Alarm | Masking bit for low AUX1 monitor alarm. | FALSE | 0 |
| 89 | 59 | 5 | | M- AUX 1 High Alarm | Masking bit for high AUX1 monitor alarm. | FALSE | 0 |
| 89 | 59 | 6 | _ | M- RX Power Low Alarm | Masking bit for low RX Power alarm. | FALSE | 0 |
| 89 | 59 | 7 | 1 | M- RX Power High Alarm | Masking bit for high RX Power alarm. | FALSE | 0 |
| _ | | _ | _ | | | | 0 |
| 90 | 5A 5A | 0 | | M-TX Power Low Warning | Masking bit for low TX Power warning. | FALSE FALSE | 0 |
| 90 | | _ | | M- TX Power High Warning | Masking bit for high TX Power warning. | | |
| 90 | 5A | 2 | | M- TX Bias Low Warning | Masking bit for low TX Bias warning. | FALSE | 0 |
| 90 | 5A | 3 | _ | M- TX Bias High Warning | Masking bit for high TX Bias warning. | FALSE | 0 |
| 90 | 5A | 4 | 1 | M- Vcc Low Warning | Masking bit for low Vcc warning. | FALSE | 0 |
| 90 | 5A | 5 | | M- Vcc High Warning | Masking bit for high Vcc warning. | FALSE | 0 |
| 90 | 5A | 6 | | M- Temp Low Warning | Masking bit for low Temperature warning. | FALSE | 0 |
| 90 | 5A | 7 | 1 | M- Temp High Warning | Masking bit for high Temperature warning. | FALSE | 0 |
| 91 | 5B | 0 | 1 | RESERVED | RESERVED | NA | NA |
| 91 | 5B | 1 | 1 | RESERVED | RESERVED | NA | NA |
| 91 | 5B | 2 | 1 | M- AUX 2 Low Warning | Masking bit for low AUX2 monitor warning. | FALSE | 0 |
| 91 | 5B | 3 | 1 | M- AUX 2 High Warning | Masking bit for high AUX2 monitor warning. | FALSE | 0 |
| 91 | 5B | 4 | 1 | M- AUX 1 Low Warning | Masking bit for low AUX1 monitor warning. | FALSE | 0 |
| 91 | 5B | 5 | _ | M- AUX 1 High Warning | Masking bit for high AUX1 monitor warning. | FALSE | 0 |
| 91 | 5B | 6 | 1 | M- RX Power Low Warning | Masking bit for low RX Power warning. | FALSE | 0 |
| 91 | 5B | 7 | 1 | M- RX Power Low Warning M- RX Power High Warning | Masking bit for low KX Power warning. Masking bit for high RX Power warning. | FALSE | 0 |
| | 5C | _ | 1 | | Masking bit for Reset Complete Flag | | 0 |
| 92 | | 0 | | M- Reset Complete | | FALSE | |
| 92 | 5C | 1 | 1 | M- MOD_NR | Masking bit for Mirror of MOD-NR pin | FALSE | 0 |
| | 5C | 2 | 1 | M- RX CDR not Locked | Masking bit for RX CDR Loss of Lock | FALSE | 0 |
| 92 | | | | | Masking bit for mirror of LOS pin (RX optical | ſ | |
| | | | 1 | M- LOS | loss of signal) | FALSE | 0 |
| 92 | 5C | 3 | | 1 | Masking bit for RX NR Status | | |
| | 5C | 3 4 | 1 | M- RX_NR | IVIASKITIE DIL TOT KX_NK STATUS | FALSE | 0 |
| 92 | | | 1 | M- TX CDR not Locked | Masking bit for TX CDR Loss of Lock | FALSE FALSE | 0 |
| 92 92 | 5C | 4 | _ | _ | - | | |
| 92 92 | 5C 5C | 4 | _ | M- TX CDR not Locked | Masking bit for TX CDR Loss of Lock | | |
| 92 92 92 | 5C | 5 | 1 | _ | Masking bit for TX CDR Loss of Lock Masking bit for Laser Fault condition. | FALSE | 0 |

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EEPROM (Table A0h) continued

| Masking bit for Wavelength Unlocked FALSE | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | FALSE FALSE FALSE NA 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | Masking bit for Wavelength Unlocked Condition Masking bit for TEC Fault Masking bit for APD Supply Fault RESERVED Internally measured module temperature Internally measured module temperature Internally measured supply voltage in transceiver Internally measured TS Bias Current Internally measured TX Bias Current Internally measured TX Bias Current Measured TX output power Auxiliary measurement 1 defined in Byte 222 Page O1h Auxiliary measurement 1 defined in Byte 222 | M- Wavelength Unlocked M- TEC Fault M- TEC Fault M- APD Supply Fault RESERVED Temperature MSB Temperature LSB Vcc MSB Vcc LSB TX Bias MSB TX Bias MSB TX Power MSB TX Power MSB RX Power MSB RX Power LSB RX Power LSB | 1 1 1 16 8 8 8 8 8 8 8 8 8 8 8 8 | 5 6 7 0 0 0 0 0 0 | 5D 5D 5E 60 61 62 63 64 65 66 67 68 | 93 93 93 94 96 97 98 99 100 101 102 |
|--|---|---|--|--|---|---|--|---|
| 93 50 5 1 M-Wavelength Unlocked Condition FALSE 93 50 6 1 M-TEC Fault Masking bit for TEC Fault FALSE 93 50 7 1 M-APD Supply Fault Masking bit for APD Supply Fault FALSE 94 5E 0 16 RESERVED RESERVED RESERVED NA NA NA NA NA NA NA N | 0 0 0 NA 0 0 0 0 0 0 0 0 0 0 | FALSE FALSE NA 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | Condition Masking bit for TEC Fault Masking bit for APD Supply Fault RESERVED Internally measured module temperature Internally measured module temperature Internally measured supply voltage in transceiver Internally measured Supply voltage in transceiver Internally measured TX Bias Current Internally measured TX Bias Current Internally measured TX Bias Current Measured TX output power Auxiliary measurement 1 defined in Byte 222 Page 01h Auxiliary measurement 1 defined in Byte 222 | M- TEC Fault M- APD Supply Fault RESERVED Temperature MSB Temperature LSB Vcc MSB Vcc LSB TX Bias MSB TX Bias LSB TX Power MSB TX Power MSB RX Power MSB RX Power MSB RX Power LSB | 1 16 8 8 8 8 8 8 8 8 | 6 7 0 0 0 0 0 0 0 | 5D 5E 60 61 62 63 64 65 66 67 68 | 93 94 96 97 98 99 100 101 102 |
| 93 50 5 1 M-Wavelength Unlocked Condition FALSE 93 50 6 1 M-TEC Fault Masking bit for TEC Fault FALSE 93 50 7 1 M-APD Supply Fault Masking bit for APD Supply Fault FALSE 94 5E 0 16 RESERVED RESERVED RESERVED NA NA NA NA NA NA NA N | 0 0 0 NA 0 0 0 0 0 0 0 0 0 0 | FALSE FALSE NA 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | Condition Masking bit for TEC Fault Masking bit for APD Supply Fault RESERVED Internally measured module temperature Internally measured module temperature Internally measured supply voltage in transceiver Internally measured Supply voltage in transceiver Internally measured TX Bias Current Internally measured TX Bias Current Internally measured TX Bias Current Measured TX output power Auxiliary measurement 1 defined in Byte 222 Page 01h Auxiliary measurement 1 defined in Byte 222 | M- TEC Fault M- APD Supply Fault RESERVED Temperature MSB Temperature LSB Vcc MSB Vcc LSB TX Bias MSB TX Bias LSB TX Power MSB TX Power MSB RX Power MSB RX Power MSB RX Power LSB | 1 16 8 8 8 8 8 8 8 8 | 6 7 0 0 0 0 0 0 0 | 5D 5E 60 61 62 63 64 65 66 67 68 | 93 94 96 97 98 99 100 101 102 |
| 93 5D 6 1 M-TEC Fault Masking bit for TEC Fault FALSE 93 5D 7 M-APD Supply Fault Masking bit for APD Supply Fault FALSE 94 5E 0 16 RESERVED RESERVED NA 96 60 0 8 Temperature MSB Internally measured module temperature 0 97 61 0 8 Temperature LSB Internally measured module temperature 0 98 62 0 8 Vcc MSB Internally measured supply voltage in 98 62 0 8 Vcc LSB Internally measured supply voltage in 99 63 0 8 Vcc LSB Internally measured TX Bias Current 0 100 64 0 8 TX Bias MSB Internally measured TX Bias Current 0 101 65 0 8 TX Bias LSB Internally measured TX Bias Current 0 102 66 0 8 TX Power MSB Measured TX output power 0 103 67 0 8 TX Power MSB Measured TX output power 0 105 69 0 8 RX Power MSB Measured TX output power 0 106 6A 0 8 RX Power MSB Measured RX output power 0 107 68 0 8 RX Power MSB Measured TX output power 0 108 6C 0 8 AUX 1LSB Page 01h 0 109 6D 0 8 AUX 1LSB Page 01h 0 100 | 0 0 0 NA 0 0 0 0 0 0 0 0 0 0 | FALSE FALSE NA 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | Masking bit for TEC Fault Masking bit for APD Supply Fault RESERVED Internally measured module temperature Internally measured module temperature Internally measured supply voltage in transceiver Internally measured supply voltage in transceiver Internally measured TX Bias Current Internally measured TX Bias Current Internally measured TX Bias Current Measured TX output power Measured TX output power Measured RX output power Measured RX output power Auxiliary measurement 1 defined in Byte 222 Page 01h Auxiliary measurement 1 defined in Byte 222 | M- TEC Fault M- APD Supply Fault RESERVED Temperature MSB Temperature LSB Vcc MSB Vcc LSB TX Bias MSB TX Bias LSB TX Power MSB TX Power MSB RX Power MSB RX Power MSB RX Power LSB | 1 16 8 8 8 8 8 8 8 8 | 6 7 0 0 0 0 0 0 0 | 5D 5E 60 61 62 63 64 65 66 67 68 | 93 94 96 97 98 99 100 101 102 |
| 93 5D 7 1 M-APD Supply Fault Masking bit for APD Supply Fault FALSE 94 5E 0 16 RESERVED RESERVED NA 96 60 0 8 Temperature NSB Internally measured module temperature 0 97 61 0 8 Temperature LSB Internally measured module temperature 0 98 62 0 8 Vcc MSB Internally measured supply voltage in 100 64 0 8 Tx Bias MSB Internally measured supply voltage in 101 65 0 8 TX Bias MSB Internally measured TX Bias Current 0 102 66 0 8 TX Power MSB Measured TX Dias Current 0 103 67 0 8 TX Power MSB Measured TX Output power 0 104 68 0 8 RX Power MSB Measured TX Output power 0 105 69 0 8 RX Power LSB Measured RX Output power 0 106 6A 0 8 AUX 1 MSB Measured RX Output power 0 107 6B 0 8 AUX 1 LSB AUX 1 MSB Page 01h 0 108 6C 0 8 AUX 2 LSB Page 01h 0 109 6D 0 8 AUX 2 LSB Page 01h 0 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 | 0 NA 0 0 0 0 0 0 0 0 0 0 0 0 | FALSE NA 0 0 0 0 0 0 0 0 0 0 0 0 0 | Masking bit for APD Supply Fault RESERVED Internally measured module temperature Internally measured module temperature Internally measured supply voltage in transceiver Internally measured Supply voltage in transceiver Internally measured TX Bias Current Internally measured TX Bias Current Internally measured TX Bias Current Measured TX output power Measured TX output power Measured TX output power Measured RX output power Measured RX output power Measured RX output power Auxiliary measurement 1 defined in Byte 222 Page 01h Auxiliary measurement 1 defined in Byte 222 | M- APD Supply Fault RESERVED Temperature MSB Temperature LSB Vcc MSB Vcc LSB TX Bias MSB TX Bias LSB TX Power MSB TX Power MSB RX Power MSB RX Power MSB RX Power LSB RX Power LSB | 1 16 8 8 8 8 8 8 8 8 | 7 0 0 0 0 0 0 0 0 | 5D 5E 60 61 62 63 64 65 66 67 68 | 93 94 96 97 98 99 100 101 102 |
| 94 SE 0 16 RESERVED RESERVED RESERVED NA 96 60 0 8 Temperature MSB Internally measured module temperature 0 97 61 0 8 Temperature LSB Internally measured module temperature 0 98 62 0 8 Vcc MSB Internally measured supply voltage in 98 62 0 8 Vcc LSB Internally measured supply voltage in 99 63 0 8 Vcc LSB Internally measured Supply voltage in 100 64 0 8 TX Bias MSB Internally measured TX Bias Current 0 101 65 0 8 TX Bias LSB Internally measured TX Bias Current 0 102 66 0 8 TX Power MSB Measured TX Dutput power 0 103 67 0 8 TX Power LSB Measured TX output power 0 104 68 0 8 RX Power MSB Measured RX output power 0 105 69 0 8 RX Power LSB Measured RX output power 0 106 6A 0 8 AUX 1 MSB Page 01h 0 107 6B 0 8 AUX 1 LSB Page 01h 0 108 6C 0 8 AUX 2 MSB Page 01h 0 109 6D 0 8 AUX 2 LSB Page 01h 0 100 100 100 100 100 100 101 6E 0 1 Data_Not_Ready Sets the bit low. 0 100 6E 1 1 LOS 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 100 10 | NA 0 0 0 0 0 0 0 0 0 0 0 | NA 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | RESERVED Internally measured module temperature Internally measured module temperature Internally measured supply voltage in transceiver Internally measured supply voltage in transceiver Internally measured TX Bias Current Internally measured TX Bias Current Internally measured TX Bias Current Measured TX output power Measured TX output power Measured RX output power Measured RX output power Measured RX output power Auxiliary measurement 1 defined in Byte 222 Page 01h Auxiliary measurement 1 defined in Byte 222 | RESERVED Temperature MSB Temperature LSB Vcc MSB Vcc LSB TX Bias MSB TX Bias LSB TX Power MSB TX Power LSB RX Power MSB RX Power MSB RX Power LSB | 16 8 8 8 8 8 8 8 8 | 0 0 0 0 0 0 0 0 | 5E 60 61 62 63 64 65 66 67 | 94 96 97 98 99 100 101 102 |
| 96 60 0 8 Temperature MSB Internally measured module temperature 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 0 | | Internally measured module temperature Internally measured module temperature Internally measured supply voltage in transceiver Internally measured supply voltage in transceiver Internally measured TX Bias Current Internally measured TX Bias Current Internally measured TX Bias Current Measured TX output power Measured TX output power Measured TX output power Measured RX output power Measured RX output power Auxiliary measurement 1 defined in Byte 222 Page 01h Auxiliary measurement 1 defined in Byte 222 | Temperature MSB Temperature LSB Vcc MSB Vcc LSB TX Bias MSB TX Bias LSB TX Power MSB TX Power LSB RX Power MSB RX Power LSB | 8 8 8 8 8 8 8 | 0 0 0 0 0 0 0 | 60 61 62 63 64 65 66 67 68 | 96 97 98 99 100 101 102 |
| 97 61 0 8 Temperature LSB | 0 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 | Internally measured module temperature Internally measured supply voltage in transceiver Internally measured supply voltage in transceiver Internally measured TX Bias Current Internally measured TX Bias Current Internally measured TX Bias Current Measured TX output power Measured TX output power Measured RX output power Measured RX output power Auxiliary measurement 1 defined in Byte 222 Page 01h Auxiliary measurement 1 defined in Byte 222 | Temperature LSB Vcc MSB Vcc LSB TX Bias MSB TX Bias LSB TX Power MSB TX Power LSB RX Power MSB RX Power LSB | 8 8 8 8 8 8 8 | 0 0 0 0 0 | 61 62 63 64 65 66 67 68 | 97 98 99 100 101 102 |
| Internally measured supply voltage in transceiver | 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 2 0 | Internally measured supply voltage in transceiver Internally measured supply voltage in transceiver Internally measured TX Bias Current Internally measured TX Bias Current Measured TX output power Measured TX output power Measured RX output power Auxiliary measurement 1 defined in Byte 222 Page 01h Auxiliary measurement 1 defined in Byte 222 | Vcc MSB Vcc LSB TX Bias MSB TX Bias LSB TX Power MSB TX Power MSB RX Power MSB RX Power MSB RX Power MSB | 8 8 8 8 8 8 | 0 0 0 0 0 | 62 63 64 65 66 67 68 | 98 99 100 101 102 |
| Internally measured supply voltage in transceiver | 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 2 0 | transceiver Internally measured supply voltage in transceiver Internally measured TX Bias Current Internally measured TX Bias Current Measured TX output power Measured TX output power Measured TX output power Measured RX output power Measured RX output power Auxiliary measurement 1 defined in Byte 222 Page 01h Auxiliary measurement 1 defined in Byte 222 | Vcc LSB TX Bias MSB TX Bias LSB TX Power MSB TX Power LSB RX Power MSB RX Power LSB | 8 8 8 8 8 | 0 0 0 0 | 62 63 64 65 66 67 68 | 98 99 100 101 102 |
| 98 62 0 8 Vcc MSB | 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 | transceiver Internally measured supply voltage in transceiver Internally measured TX Bias Current Internally measured TX Bias Current Measured TX output power Measured TX output power Measured TX output power Measured RX output power Measured RX output power Auxiliary measurement 1 defined in Byte 222 Page 01h Auxiliary measurement 1 defined in Byte 222 | Vcc LSB TX Bias MSB TX Bias LSB TX Power MSB TX Power LSB RX Power MSB RX Power LSB | 8 8 8 8 8 | 0 0 0 0 | 63 64 65 66 67 68 | 99 100 101 102 |
| Internally measured supply voltage in transceiver | 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 | Internally measured supply voltage in transceiver Internally measured TX Bias Current Internally measured TX Bias Current Measured TX output power Measured TX output power Measured RX output power Measured RX output power Measured RX output power Auxiliary measurement 1 defined in Byte 222 Page 01h Auxiliary measurement 1 defined in Byte 222 | Vcc LSB TX Bias MSB TX Bias LSB TX Power MSB TX Power LSB RX Power MSB RX Power LSB | 8 8 8 8 8 | 0 0 0 0 | 63 64 65 66 67 68 | 99 100 101 102 |
| 99 63 0 8 Vcc LSB | 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 2 0 | transceiver Internally measured TX Bias Current Internally measured TX Bias Current Measured TX output power Measured TX output power Measured RX output power Measured RX output power Measured RX output power Auxiliary measurement 1 defined in Byte 222 Page 01h Auxiliary measurement 1 defined in Byte 222 | TX Bias MSB TX Bias LSB TX Power MSB TX Power LSB RX Power MSB RX Power LSB | 8 8 8 8 | 0 0 0 0 | 64 65 66 67 68 | 100 101 102 |
| 100 64 0 8 TX Bias MSB | 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 2 0 | Internally measured TX Bias Current Internally measured TX Bias Current Measured TX output power Measured TX output power Measured RX output power Measured RX output power Auxiliary measurement 1 defined in Byte 222 Page 01h Auxiliary measurement 1 defined in Byte 222 | TX Bias MSB TX Bias LSB TX Power MSB TX Power LSB RX Power MSB RX Power LSB | 8 8 8 8 | 0 0 0 0 | 64 65 66 67 68 | 100 101 102 |
| 101 65 0 8 TX Bias LSB Internally measured TX Bias Current 0 | 0 0 0 0 0 0 | 0 | Internally measured TX Bias Current Measured TX output power Measured TX output power Measured RX output power Measured RX output power Measured RX output power Auxiliary measurement 1 defined in Byte 222 Page 01h Auxiliary measurement 1 defined in Byte 222 | TX Bias LSB TX Power MSB TX Power LSB RX Power MSB RX Power LSB | 8 8 8 | 0 0 0 | 65 66 67 68 | 101 102 |
| 102 66 0 8 TX Power MSB Measured TX output power 0 | 0 0 0 0 0 | 0 | Measured TX output power Measured TX output power Measured RX output power Measured RX output power Measured RX output power Auxiliary measurement 1 defined in Byte 222 Page 01h Auxiliary measurement 1 defined in Byte 222 | TX Power MSB TX Power LSB RX Power MSB RX Power LSB | 8 8 | 0 0 | 66 67 68 | 102 |
| 102 66 0 8 TX Power MSB Measured TX output power 0 | 0 0 0 0 0 0 | 0 | Measured TX output power Measured TX output power Measured RX output power Measured RX output power Measured RX output power Auxiliary measurement 1 defined in Byte 222 Page 01h Auxiliary measurement 1 defined in Byte 222 | TX Power LSB RX Power MSB RX Power LSB | 8 | 0 | 67 68 | |
| 103 67 0 8 TX Power LSB Measured TX output power 0 | 0 0 0 0 0 0 | 0 | Measured TX output power Measured RX output power Measured RX output power Auxiliary measurement 1 defined in Byte 222 Page 01h Auxiliary measurement 1 defined in Byte 222 | TX Power LSB RX Power MSB RX Power LSB | 8 | 0 | 67 68 | |
| 104 68 0 8 RX Power MSB Measured RX output power 0 | 0 0 0 | 0 | Measured RX output power Measured RX output power Auxiliary measurement 1 defined in Byte 222 Page 01h Auxiliary measurement 1 defined in Byte 222 | RX Power MSB RX Power LSB | 8 | 0 | 68 | |
| 105 69 0 8 RX Power LSB | 0 0 0 | 0 | Measured RX output power Auxiliary measurement 1 defined in Byte 222 Page 01h Auxiliary measurement 1 defined in Byte 222 | RX Power LSB | _ | | _ | |
| Auxiliary measurement 1 defined in Byte 222 0 0 | 0 0 | 0 | Auxiliary measurement 1 defined in Byte 222 Page 01h Auxiliary measurement 1 defined in Byte 222 | | 8 | 0 | | |
| 106 6A 0 8 AUX 1 MSB | 0 | 0 | Page 01h Auxiliary measurement 1 defined in Byte 222 | AUX 1 MSB | | | 05 | 105 |
| Auxiliary measurement 1 defined in Byte 222 108 6C 0 8 AUX 2 MSB Page 01h Auxiliary measurement 2 defined in Byte 222 109 6D 0 8 AUX 2 LSB Page 01h O Auxiliary measurement 2 defined in Byte 222 Page 01h O Indicates transceiver has achieved power up and data is ready. Bit remains high until data is ready to be read at which time the device sets the bit low. 110 6E 0 1 Data_Not_Ready sets the bit low. O Indicates Optical Loss of Signal (per relevant optical link standard). Updated within 110 6E 1 1 LOS 100msec of change on pin FALSE 110 6E 2 1 Interrupt Digital state of the Interrupt output pin FALSE Read/write bit that allows the module to be placed in the power down mode. This is | 0 | 0 0 | Auxiliary measurement 1 defined in Byte 222 | AUX 1 MSB | | | | |
| 107 68 0 8 AUX 1 LSB | 0 | 0 0 | | | 8 | 0 | 6A | 106 |
| 107 68 0 8 AUX 1 LSB | 0 | 0 0 | | | | | | |
| Auxiliary measurement 2 defined in Byte 222 Page 01h O Auxiliary measurement 2 defined in Byte 222 Page 01h O Auxiliary measurement 2 defined in Byte 222 Page 01h O Indicates transceiver has achieved power up and data is ready. Bit remains high until data is ready to be read at which time the device sets the bit low. O Indicates Optical Loss of Signal (per relevant optical link standard). Updated within 110 6E 1 1 LOS 100msec of change on pin FALSE 110 6E 2 1 Interrupt Digital state of the Interrupt output pin FALSE Read/write bit that allows the module to be placed in the power down mode. This is | 0 | 0 | | ALIX 1 I SR | R | n | 6B | 107 |
| 108 6C 0 8 AUX 2 MSB Page 01h 0 Auxiliary measurement 2 defined in Byte 222 Page 01h 0 Indicates transceiver has achieved power up and data is ready. Bit remains high until data is ready to be read at which time the device sets the bit low. 0 Indicates Optical Loss of Signal (per relevant optical link standard). Updated within 110 6E 1 1 LOS 100msec of change on pin FALSE 110 6E 2 1 Interrupt 1 1 1 1 1 1 1 1 1 | | 0 | | AOX 1130 | Ü | Ü | OD | 107 |
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| 109 6D 0 8 AUX 2 LSB Page 01h 0 0 0 0 0 0 0 0 0 | 0 | | 9 | AUX 2 MSB | 8 | 0 | 6C | 108 |
| Indicates transceiver has achieved power up and data is ready. Bit remains high until data is ready. Bit remains high until data is ready to be read at which time the device sets the bit low. 110 6E 0 1 Data_Not_Ready sets the bit low. 110 6E 1 1 LOS Indicates Optical Loss of Signal (per relevant optical link standard). Updated within 100msec of change on pin FALSE 110 6E 2 1 Interrupt Digital state of the Interrupt output pin FALSE Read/write bit that allows the module to be placed in the power down mode. This is | 0 | 4 | Auxiliary measurement 2 defined in Byte 222 | | | | | |
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| and data is ready. Bit remains high until data is ready to be read at which time the device sets the bit low. 110 6E 0 1 Data_Not_Ready sets the bit low. 0 Indicates Optical Loss of Signal (per relevant optical link standard). Updated within 100 sets of change on pin 100 sets of the Interrupt output pin 100 sets of the Interrupt output pin 100 sets of Read/write bit that allows the module to be placed in the power down mode. This is | | | Indicates transceiver has achieved power up | | | | | |
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| 110 6E 0 1 Data_Not_Ready sets the bit low. 0 Indicates Optical Loss of Signal (per relevant optical link standard). Updated within 110 6E 1 1 LOS 100msec of change on pin FALSE 110 6E 2 1 Interrupt Digital state of the Interrupt output pin FALSE Read/write bit that allows the module to be placed in the power down mode. This is | | | | | | | | |
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| optical link standard). Updated within 110 6E 1 1 LOS 100msec of change on pin FALSE 110 6E 2 1 Interrupt Digital state of the Interrupt output pin FALSE Read/write bit that allows the module to be placed in the power down mode. This is | 0 | 0 | | Data_Not_Ready | 1 | 0 | 6E | 110 |
| 110 6E 1 1 LOS 100msec of change on pin FALSE 110 6E 2 1 Interrupt Digital state of the Interrupt output pin FALSE Read/write bit that allows the module to be placed in the power down mode. This is placed in the power down mode. This is | | | Indicates Optical Loss of Signal (per relevant | | | | | |
| 110 6E 2 1 Interrupt Digital state of the Interrupt output pin FALSE Read/write bit that allows the module to be placed in the power down mode. This is | | | optical link standard). Updated within | | | | | |
| 110 6E 2 1 Interrupt Digital state of the Interrupt output pin FALSE Read/write bit that allows the module to be placed in the power down mode. This is | 0 | FALSE | 100msec of change on pin | LOS | 1 | 1 | 6E | 110 |
| Read/write bit that allows the module to be placed in the power down mode. This is | 0 | | | | | | | |
| placed in the power down mode. This is | | TALSE | | птеттире | ÷ | _ | OL | 110 |
| | | | | | | | | |
| l | | | | | | | | |
| The state of the s | | | identical to the P_Down hardware pin | | | | | |
| function except that it does not initiate a | | | function except that it does not initiate a | | | | | |
| 110 6E 3 1 Soft P_Down system reset FALSE | 0 | FALSE | system reset | Soft P Down | 1 | 3 | 6E | 110 |
| Digital state of the P Down Pin. Updated | | 1 | | _ | | | | |
| 110 6E 4 1 P Down State within 100msec of change on pin FALSE | 0 | EALSE | | P. Down State | 1 | 4 | 6E | 110 |
| | | TALSE | | r_bown state | | | UL | 110 |
| Digital state of the MOD_NR Pin. Updated | _ | | | | ١. | _ | | |
| 110 6E 5 1 MOD_NR State within 100msec of change on pin FALSE | 0 | FALSE | within 100msec of change on pin | MOD_NR State | 1 | 5 | 6E | 110 |
| | | ſ | | | ĺ | ĺ | | |
| Read/write bit that allows software disable | | | Read/write bit that allows software disable | | | | | |
| of laser. Writing '1' disables laser. Turn on/off | | f | of laser, Writing '1' disables laser, Turn on/off | | | | | |
| time is 100msc max from acknowledgement | | | | | | | | |
| | | | = | | | | | |
| of serial byte transmission. This bit is "OR"d | | | | | | | | |
| | | | | | | | | |
| per SFP MSA TX_DISABLE pin is default | | | with the hard TX_DISABLE pin value. Note, | | | | | |
| enabled unless pulled low by hardware. If | | | | | | | | |
| | | | per SFP MSA TX_DISABLE pin is default | | | | | |
| | | | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If | | | | | |
| | | | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the | | | | | |
| | 0 | | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. | Soft TV Disable | 4 | - | er. | 110 |
| Digital state of the TV Disable Innuit Dia | 0 | 0 | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0. | Soft TX Disable | 1 | 6 | 6E | 110 |
| | | | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0. Digital state of the TX Disable Input Pin. | | | | | |
| Digital state of the 1X Disable Input Pin. 110 6E 7 1 TX Disable State Updated within 100msec of change on pin FALSE | 0 | | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0. Digital state of the TX Disable Input Pin. | | | | | |
| | | | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0. Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin | TX Disable State | 1 | 7 | 6E | 110 |
| 110 6E 7 1 TX Disable State Updated within 100msec of change on pin FALSE 111 6F 0 3 RESERVED RESERVED | | FALSE | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0. Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin RESERVED | TX Disable State RESERVED | 1 | 7 | 6E 6F | 110 111 |
| 110 6E 7 1 TX Disable State Updated within 100msec of change on pin FALSE 111 6F 0 3 RESERVED RESERVED 111 6F 3 1 RX_CDR not Locked Identifies Loss of Lock in RX path CDR FALSE | 0 | FALSE | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0. Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin RESERVED Identifies Loss of Lock in RX path CDR | TX Disable State RESERVED | 1 | 7 | 6E 6F | 110 111 |
| 110 6E 7 1 TX Disable State Updated within 100msec of change on pin FALSE 111 6F 0 3 RESERVED RESERVED 111 6F 3 1 RX_CDR not Locked Identifies Loss of Lock in RX path CDR FALSE Identifies Not Ready condition as specific to Identifies Not Ready condition as specific to Identifies Not Ready condition as specific to | 0 | FALSE FALSE | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0. Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin RESERVED Identifies Loss of Lock in RX path CDR Identifies Not Ready condition as specific to | TX Disable State RESERVED RX_CDR not Locked | 1 3 1 | 7 0 3 | 6E 6F 6F | 110 111 111 |
| 110 6E 7 1 TX Disable State Updated within 100msec of change on pin FALSE 111 6F 0 3 RESERVED RESERVED 111 6F 3 1 RX_CDR not Locked Identifies Loss of Lock in RX path CDR FALSE 111 6F 4 1 RX_NR State Identifies Not Ready condition as specific to the TX path FALSE | 0 0 | FALSE FALSE FALSE | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0. Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin RESERVED Identifies Loss of Lock in RX path CDR Identifies Not Ready condition as specific to the TX path | TX Disable State RESERVED RX_CDR not Locked RX_NR State | 1 3 1 | 7 0 3 | 6E 6F 6F | 110 111 111 111 |
| 110 6E 7 1 TX Disable State Updated within 100msec of change on pin FALSE 111 6F 0 3 RESERVED RESERVED 111 6F 3 1 RX_CDR not Locked Identifies Loss of Lock in RX path CDR FALSE 111 6F 4 1 RX_NR State the TX path FALSE 111 6F 5 1 TX_CDR not Locked Identifies Loss of Lock in TX path CDR FALSE | 0 | FALSE FALSE FALSE | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0. Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin RESERVED Identifies Loss of Lock in RX path CDR Identifies Not Ready condition as specific to the TX path Identifies Loss of Lock in TX path CDR | TX Disable State RESERVED RX_CDR not Locked RX_NR State | 1 3 1 | 7 0 3 | 6E 6F 6F | 110 111 111 111 |
| 110 6E 7 1 TX Disable State Updated within 100msec of change on pin FALSE 111 6F 0 3 RESERVED RESERVED 111 6F 3 1 RX_CDR not Locked Identifies Loss of Lock in RX path CDR FALSE 111 6F 4 1 RX_NR State Identifies Not Ready condition as specific to the TX path FALSE | 0 0 | FALSE FALSE FALSE | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0. Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin RESERVED Identifies Loss of Lock in RX path CDR Identifies Not Ready condition as specific to the TX path Identifies Loss of Lock in TX path CDR | TX Disable State RESERVED RX_CDR not Locked RX_NR State | 1 3 1 | 7 0 3 | 6E 6F 6F | 110 111 111 111 |
| 110 6E 7 1 TX Disable State Updated within 100msec of change on pin FALSE 111 6F 0 3 RESERVED RESERVED 111 6F 3 1 RX_CDR not Locked Identifies Loss of Lock in RX path CDR FALSE 111 6F 4 1 RX_NR State the TX path FALSE 111 6F 5 1 TX_CDR not Locked Identifies Loss of Lock in TX path CDR FALSE | 0 0 | FALSE FALSE FALSE FALSE | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0. Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin RESERVED Identifies Loss of Lock in RX path CDR Identifies Not Ready condition as specific to the TX path Identifies Loss of Lock in TX path CDR Identifies Laser fault condition (Generated | TX Disable State RESERVED RX_CDR not Locked RX_NR State TX_CDR not Locked | 1 3 1 1 | 7 0 3 4 5 | 6E 6F 6F 6F | 110 111 111 111 111 |
| 110 6E 7 1 TX Disable State | 0 0 0 | FALSE FALSE FALSE FALSE | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0. Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin RESERVED Identifies Loss of Lock in RX path CDR Identifies Not Ready condition as specific to the TX path Identifies Loss of Lock in TX path CDR Identifies Loss of Lock in TX path CDR Identifies Loss of Lock in TX path CDR Identifies Laser fault condition (Generated by laser safety system) | TX Disable State RESERVED RX_CDR not Locked RX_NR State TX_CDR not Locked | 1 3 1 1 | 7 0 3 4 5 | 6E 6F 6F 6F | 110 111 111 111 111 |
| 110 6E 7 1 TX Disable State | 0 0 0 0 | FALSE FALSE FALSE FALSE FALSE | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0. Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin RESERVED Identifies Loss of Lock in RX path CDR Identifies Not Ready condition as specific to the TX path Identifies Loss of Lock in TX path CDR Identifies Loss of Lock in TX path CDR Identifies Loss of Lock in Generated by laser safety system) Identifies Not Ready condition as specific to | TX Disable State RESERVED RX_CDR not Locked RX_NR State TX_CDR not Locked TX_Fault State | 1 3 1 1 1 | 7 0 3 4 5 | 6E 6F 6F 6F | 110 111 111 111 111 111 |
| 110 6E 7 1 TX Disable State Updated within 100msec of change on pin FALSE 111 6F 0 3 RESERVED RESERVED 111 6F 3 1 RX_CDR not Locked Identifies Loss of Lock in RX path CDR FALSE 111 6F 4 1 RX_NR State the TX path FALSE 111 6F 5 1 TX_CDR not Locked Identifies Loss of Lock in TX path CDR FALSE 111 6F 6 TX_Fault State Identifies Loss of Lock in TX path CDR FALSE 111 6F 7 1 TX_NR State Identifies Loss of Lock in TX path CDR FALSE 111 6F 7 1 TX_NR State TX_NR State TALSE 111 6F 7 1 TX_NR State TALSE TALSE 111 | 0 0 0 0 | FALSE FALSE FALSE FALSE FALSE FALSE | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0. Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin RESERVED Identifies Loss of Lock in RX path CDR Identifies Not Ready condition as specific to the TX path Identifies Loss of Lock in TX path CDR Identifies Laser fault condition (Generated by laser safety system) Identifies Not Ready condition as specific to the TX path CDR | TX Disable State RESERVED RX_CDR not Locked RX_NR State TX_CDR not Locked TX_Fault State TX_NR State | 1 3 1 1 1 | 7 0 3 4 5 | 6E 6F 6F 6F 6F | 110 111 111 111 111 111 |
| 110 6E 7 1 TX Disable State Updated within 100msec of change on pin FALSE 111 6F 0 3 RESERVED RESERVED 111 6F 3 1 RX_CDR not Locked Identifies Loss of Lock in RX path CDR FALSE 111 6F 4 1 RX_NR State the TX path FALSE 111 6F 5 1 TX_CDR not Locked Identifies Loss of Lock in TX path CDR FALSE 111 6F 6 1 TX_Fault State by laser safety system) FALSE 111 6F 7 1 TX_NR State the TX path FALSE 111 6F 7 1 TX_NR State TX_PATH FALSE 112 70 0 48 RESERVED RESERVED NA | 0 0 0 0 | FALSE FALSE FALSE FALSE FALSE FALSE NA | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0. Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin RESERVED Identifies Loss of Lock in RX path CDR Identifies Not Ready condition as specific to the TX path Identifies Loss of Lock in TX path CDR Identifies Laser fault condition (Generated by laser safety system) Identifies Not Ready condition as specific to the TX path Identifies Not Ready condition as specific to the TX path | TX Disable State RESERVED RX_CDR not Locked RX_NR State TX_CDR not Locked TX_Fault State TX_NR State | 1 3 1 1 1 | 7 0 3 4 5 | 6E 6F 6F 6F 6F | 110 111 111 111 111 111 |
| 110 6E 7 | 0 0 0 0 | FALSE FALSE FALSE FALSE FALSE FALSE NA | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disables is not implemented, the transceiver ignores the value of this bit. Default power up value is 0. Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin RESERVED Identifies Loss of Lock in RX path CDR Identifies Not Ready condition as specific to the TX path Identifies Loss of Lock in TX path CDR Identifies Not Ready condition (Generated by laser safety system) Identifies Not Ready condition as specific to the TX path | TX Disable State RESERVED RX_CDR not Locked RX_NR State TX_CDR not Locked TX_Fault State TX_NR State | 1 3 1 1 1 | 7 0 3 4 5 6 | 6E 6F 6F 6F 6F | 110 111 111 111 111 111 |
| 110 6E 7 1 TX Disable State Updated within 100msec of change on pin FALSE 111 6F 0 3 RESERVED RESERVED 111 6F 3 1 RX_CDR not Locked Identifies Loss of Lock in RX path CDR FALSE 111 6F 4 1 RX_NR State the TX path FALSE 111 6F 5 1 TX_CDR not Locked Identifies Loss of Lock in TX path CDR FALSE 111 6F 6 1 TX_Fault State by laser safety system) FALSE 111 6F 7 1 TX_NR State the TX path FALSE 111 6F 7 1 TX_NR State TX_PATH FALSE 112 70 0 48 RESERVED RESERVED NA | 0 0 0 0 | FALSE FALSE FALSE FALSE FALSE ALSE FALSE PALSE NA Packet error checking not | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disables is not implemented, the transceiver ignores the value of this bit. Default power up value is 0. Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin RESERVED Identifies Loss of Lock in RX path CDR Identifies Not Ready condition as specific to the TX path Identifies Loss of Lock in TX path CDR Identifies Not Ready condition (Generated by laser safety system) Identifies Not Ready condition as specific to the TX path | TX Disable State RESERVED RX_CDR not Locked RX_NR State TX_CDR not Locked TX_Fault State TX_NR State TX_NR State RESERVED | 1 3 1 1 1 1 48 | 7 0 3 4 5 6 | 6E 6F 6F 6F 6F 70 | 110 111 111 111 111 111 111 111 |
| 110 6E 7 1 TX Disable State | 0 0 0 0 0 | FALSE FALSE FALSE FALSE FALSE NA Packet error checking not supported | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0. Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin RESERVED Identifies Loss of Lock in RX path CDR Identifies Not Ready condition as specific to the TX path Identifies Loss of Lock in TX path CDR Identifies Laser fault condition (Generated by laser safety system) Identifies Not Ready condition as specific to the TX path RESERVED Error Checking | TX Disable State RESERVED RX_CDR not Locked RX_NR State TX_CDR not Locked TX_Fault State TX_NR State TX_NR State TC_NR State TC_NR State TC_NR State TC_NR State TC_NR State TC_CDR not Locked | 1 3 1 1 1 1 48 | 7 0 3 4 5 6 7 0 | 6E 6F 6F 6F 6F 70 | 110 111 111 111 111 111 111 111 111 111 |
| 110 6E 7 | 0 0 0 0 0 0 0 NA | FALSE FALSE FALSE FALSE FALSE ANA Packet error checking not supported NA | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0. Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin RESERVED Identifies Loss of Lock in RX path CDR Identifies Not Ready condition as specific to the TX path Identifies Loss of Lock in TX path CDR Identifies Not Ready condition (Generated by laser safety system) Identifies Not Ready condition as specific to the TX path RESERVED Error Checking RESERVED | TX Disable State RESERVED RX_CDR not Locked RX_NR State TX_CDR not Locked TX_Fault State TX_NR State TX_NR State TEX_NR State RESERVED Error Checking RESERVED | 1 3 1 1 1 1 48 1 7 | 7 0 3 4 5 6 7 0 | 6E 6F 6F 6F 6F 70 76 | 110 111 111 111 111 111 111 111 112 118 |
| 110 6E 7 | 0 0 0 0 0 0 NA 0 NA | FALSE FALSE FALSE FALSE FALSE AA Packet error checking not supported NA 0 | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0. Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin RESERVED Identifies Loss of Lock in RX path CDR Identifies Not Ready condition as specific to the TX path Identifies Loss of Lock in TX path CDR Identifies Laser fault condition (Generated by laser safety system) Identifies Not Ready condition as specific to the TX path RESERVED Error Checking RESERVED Location of Entry of New Optional Password | TX Disable State RESERVED RX_CDR not Locked RX_NR State TX_CDR not Locked TX_Fault State TX_NR State TX_NR State RESERVED Error Checking RESERVED New Password Entry | 1 3 1 1 1 1 48 1 7 | 7 0 3 4 5 6 7 0 0 | 6E 6F 6F 6F 6F 70 76 77 | 110 111 111 111 111 111 111 111 112 118 118 |
| 110 6E 7 | 0 0 0 0 0 0 0 NA | FALSE FALSE FALSE FALSE FALSE FALSE NA Packet error checking not supported NA 0 0 | per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0. Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin RESERVED Identifies Loss of Lock in RX path CDR Identifies Not Ready condition as specific to the TX path Identifies Loss of Lock in TX path CDR Identifies Not Ready condition (Generated by laser safety system) Identifies Not Ready condition as specific to the TX path RESERVED Error Checking RESERVED Location of Entry of New Optional Password Location for Entry of Optional Password | TX Disable State RESERVED RX_CDR not Locked RX_NR State TX_CDR not Locked TX_Fault State TX_NR State TX_NR State RESERVED Error Checking RESERVED New Password Entry Password Entry | 1 3 1 1 1 1 48 1 7 32 32 | 7 0 3 4 5 6 7 0 0 | 6E 6F 6F 6F 6F 70 76 76 77 78 | 110 111 111 111 111 111 111 111 112 118 118 |

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EEPROM (Table 01h)

| | Pr | W | | (Table UIn) | | , | |
|--------------|----------|--------|-------------|-------------------------------------|-------------------------------------|--------------------------|-----------|
| Byte Addr | Hex | LSB | Bit Size | Name Desc | cription | Value | Hex Value |
| 128 | 80 | 0 | 8 | | e of serial transceiver | XFP | 6 |
| 129 | _ | 0 | 3 | | ERVED | NA | NA |
| | | | | | | No CLEI code present in | |
| 129 | 81 | 3 | 1 | CLEI code present in Table 02h CLEI | code present in Table 02h | Table 02h | 0 |
| 129 | 81 | 4 | 1 | · | Ref Clock Input Required | Not Required | 1 |
| 129 | 81 | 5 | 1 | | dule with CDR | with CDR | 0 |
| 129 | 81 | 6 | 2 | | ines Module Power Class | Power level 3 (< 3.5W) | 2 |
| 130 | 82 | 0 | 8 | | e for connector type | LC | 7 |
| 131 | 83 | 0 | 1 | | ERVED | NA FALCE | NA O |
| 131 | 83 83 | 2 | 1 | | BASE-EW | FALSE FALSE | 0 |
| 131 131 | 83 | 3 | 1 | | BASE-LW BASE-SW | FALSE | 0 |
| 131 | 83 | 4 | 1 | | BASE-LRM | FALSE | 0 |
| 131 | 83 | 5 | 1 | | BASE-ER | FALSE | 0 |
| 131 | 83 | 6 | 1 | | BASE-LR | FALSE | 0 |
| 131 | 83 | 7 | 1 | | BASE-SR | FALSE | 0 |
| 132 | 84 | 0 | 4 | | ERVED | NA | NA |
| 132 | 84 | 4 | 1 | Intermediate Reach 1300 nm FP Inter | rmediate Reach 1300 nm FP | FALSE | 0 |
| 132 | 84 | 5 | 1 | Extented Reach 1550 nm Exter | ented Reach 1550 nm | FALSE | 0 |
| 132 | 84 | 6 | 1 | 1200-SM-LL-L 1200- | 0-SM-LL-L | FALSE | 0 |
| 132 | 84 | 7 | 1 | | 0-MX-SN-I | FALSE | 0 |
| 133 | 85 | 0 | 8 | | ERVED | NA | NA |
| 134 | 86 | 0 | 1 | i | ERVED | NA | NA |
| 134 | 86 | 1 | 1 | | ver speed link compliance code | FALSE | 0 |
| 134 | 86 | 2 | 1 | | ver speed link compliance code | FALSE | 0 |
| 134 | 86 | 3 | 1 | | ver speed link compliance code | FALSE | 0 |
| 134 | 86 | 4 | 1 | | ver speed link compliance code | FALSE | 0 |
| 134 | 86 86 | 5 6 | 1 | i | ver speed link compliance code | FALSE FALSE | 0 |
| 134 134 | 86 | 7 | 1 | · | ver speed link compliance code | FALSE | 0 |
| 135 | 87 | 0 | 2 | | ERVED | NA NA | NA NA |
| 135 | 87 | 2 | 1 | i | et codes | FALSE | 0 |
| 135 | 87 | 3 | 1 | i | et codes | FALSE | 0 |
| 135 | 87 | 4 | 1 | | et codes | FALSE | 0 |
| 135 | 87 | 5 | 1 | | et codes | FALSE | 0 |
| 135 | 87 | 6 | 1 | I-64.1 Sone | et codes | FALSE | 0 |
| 135 | 87 | 7 | 1 | I-64.1r Sone | et codes | FALSE | 0 |
| 136 | 88 | 0 | 1 | RESERVED RESE | ERVED | NA | NA |
| 136 | 88 | 1 | 1 | S-64.5b Sone | et Short Haul Link codes | FALSE | 0 |
| 136 | 88 | 2 | 1 | | et Short Haul Link codes | FALSE | 0 |
| 136 | 88 | 3 | 1 | | et Short Haul Link codes | FALSE | 0 |
| 136 | 88 | 4 | 1 | | et Short Haul Link codes | FALSE | 0 |
| 136 | 88 88 | 5 6 | 1 | | et Short Haul Link codes | FALSE FALSE | 0 |
| 136 136 | 88 | 7 | 1 | i | et Short Haul Link codes | FALSE | 0 |
| 137 | 89 | 0 | 1 | i | et Short Haul Link codes ERVED | NA NA | NA |
| 137 | 89 | 1 | 1 | DWDM DWD | | FALSE | 0 |
| 137 | 89 | 2 | 1 | | et Long Haul Link codes | TRUE | 1 |
| 137 | 89 | 3 | 1 | | et Long Haul Link codes | FALSE | 0 |
| 137 | 89 | 4 | 1 | i | et Long Haul Link codes | FALSE | 0 |
| 137 | 89 | 5 | 1 | i | et Long Haul Link codes | FALSE | 0 |
| 137 | 89 | 6 | 1 | L-64.2a Sone | et Long Haul Link codes | FALSE | 0 |
| 137 | 89 | 7 | 1 | L-64.1 Sone | et Long Haul Link codes | FALSE | 0 |
| | 8A | 0 | | | ERVED | NA | NA |
| 138 | 8A | 5 | _ | | et Very Long Haul Link codes | FALSE | 0 |
| 138 | 8A | 6 | 1 | | et Very Long Haul Link codes | FALSE | 0 |
| 138 | | 7 | 1 | i | et Very Long Haul Link codes | FALSE | 0 |
| 139 | 8B | 0 | 2 | ļ | ERVED | NA TRUE | NA 1 |
| 139 139 | 8B 8B | 3 | 1 | Tx Dither Supported RZ Enco | oding Support | FALSE | 0 |
| 139 | 8B | 4 | 1 | | oding Support | TRUE | 1 |
| 139 | 8B | 5 | 1 | | oding Support | TRUE | 1 |
| 139 | 8B | 6 | 1 | i | oding Support | TRUE | 1 |
| 139 | 8B | 7 | 1 | | oding Support | TRUE | 1 |
| 140 | 8C | 0 | 8 | | imum Supported Bitrate (/100Mb) | 99 | 63 |
| 141 | 8D | 0 | 8 | | kimumSupported Bitrate (/100Mb) | 113 | 71 |
| | | | | | · · · · · · | | |
| 142 | 8E | 0 | 8 | Length(SMF)-km | GTH (STANDARD SINGLE MODE FIBER)-KM | 80 | 50 |
| | | | ľ | | GTH (EXTENDED BANDWIDTH 50 um | | |
| 143 | 8F | 0 | 8 | Length(EMM-50um)-meter MUL | LTIMODE FIBER) (/2m) | 0 | 0 |
| | | | | | | | |

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EEPROM (Table 01h) continued

| 144 | _ | - | 1111 | (Table 0111) continu | cu | | _ |
|--|----------------------|-------------|-------------|---|--|---------------------------|--|
| | 90 | 0 | 8 | Length(50)-meter | LENGTH (50 UM MULTIMODE FIBER) (/1meter) | 0 | 0 |
| 1 | 30 | Ů | Ů | zengan(so) meter | LENGTH (62.5 UM MULTIMODE | , | Ů |
| 145 | 91 | 0 | 8 | Length(62.5)-meter | FIBER)(/1meter) | 0 | 0 |
| 146 | 92 | 0 | 8 | Length(Copper)-km | LENGTH (COPPER) (/1meter) | 0 | 0 |
| 147 | 93 | 0 | 1 | Tunable Transmitter | Device Technology | FALSE | 0 |
| 147 | 93 | 1 | 1 | Detector Type Cooled Transmitter | Device Technology Device Technology | APD | 1 |
| 147 147 | 93 93 | 3 | 1 | Wavelength Control | Device Technology Device Technology | TRUE FALSE | 0 |
| 147 | 93 | 4 | 4 | Transmitter Technology | Device Technology Device Technology | 1550 nm EML | 7 |
| | - | · | Ť | Transmitter realmonogy | Device realmology | 1550 1111 21112 | 46 69 6E 69 73 61 |
| | | | | | | | 72 20 20 20 20 20 |
| 148 | 94 | 0 | 128 | Vendor Name | Vendor Name (ascii) | Finisar | 20 20 20 20 |
| 164 | Α4 | 0 | 1 | XFI Loopback Supported | CDR support | TRUE | 1 |
| 164 | A4 | 1 | 1 | Lineside Loopback Mode Supported | CDR support | FALSE | 0 |
| 164 | A4 | 2 | 1 | RESERVED | RESERVED | NA | NA |
| 164 | A4 | 3 | 1 | CDR support for 11.1 Gb/s | CDR support | TRUE | 1 |
| 164 | A4 A4 | 4 5 | 1 | CDR support for 10.7 Gb/s CDR support for 10.5 Gb/s | CDR support | TRUE | 1 |
| 164 164 | A4 | 6 | 1 | CDR support for 10.3 Gb/s | CDR support CDR support | TRUE TRUE | 1 |
| 164 | A4 | 7 | 1 | CDR support for 9.95 Gb/s | CDR support | TRUE | 1 |
| 165 | A5 | 0 | 24 | Vendor OUI | SFP vendor IEEE company ID | 00 90 65h (36965 Decimal) | 00 90 65 |
| 168 | A8 | 0 | _ | Vendor PN | Part number provided by vendor (ASCII) | FTLX3815M3xx | Variable |
| | | | | | Revision level for part number provided by | | |
| 184 | В8 | 0 | 16 | Vendor Rev | vendor (ASCII) | 0 | Variable |
| ľ | 1 | | | | Nominal laser wavelength | | |
| 186 | BA | 0 | 16 | Wavelength | (Wavelength=value/20 in nm) | Variable | Variable |
| | | | | | Guaranteed range of laser wavelength (+/- | | |
| | l | _ | | | value) from Nominal wavelength. | | |
| 188 | BC | 0 | | Wavelength Tolerance | (Wavelength Tol. = value/200 in nm) | 04 | 00 04 |
| 190 191 | BE BF | 0 | 8 | Max Case Temp CC BASE | MAXIMUM CASE TEMPERATURE | 70 | 46 Variable |
| 191 | БГ | 0 | • | CC_BA3E | Checksum (128 to 190) Maximum Power Dissipation, Max power is 8 | | Vallable |
| 192 | СО | 0 | 8 | Maximum Power | bit value * 20 mW. | 175 | AF |
| 132 | | Ť | Ŭ | The American | Maximum Total Power Dissipation in Power | 1,3 | 7.0 |
| | | | | | Down Mode, Max Power is 8 bit value * 10 | | |
| 193 | C1 | 0 | 8 | Max Power in Power Down Mode | mW. | 100 | 64 |
| | | | | | Maximum current required by +3.3V Supply. | | |
| 194 | C2 | 0 | 4 | Max Current +3.3v | Max current is 4 bit value * 100 mA. | 8 | 8 |
| ĺ | | | ĺ | | Maximum current required by +5V | | |
| | | | | | Supply.Max current is 4 bit value * 50 mA. | | |
| 194 | C2 | 4 | 4 | Max Current +5v | [500 mA max] | 9 | 9 |
| | | | | | Maximum current required by -5.2V | | |
| 195 | С3 | 0 | 1 | Max Current -5v | Supply.Max current is 4 bit value * 50 mA. [500 mA max] | 0 | 0 |
| 133 | CJ | - | 7 | IVIAX CUITETIC-5V | Maximum current required by +1.8V Supply. | , | - |
| 195 | С3 | 4 | 4 | Max Current +1.8v | Max current is 4 bit value * 100 mA. | 0 | 0 |
| 196 | C4 | 0 | 128 | Vendor SN | Serial number provided by vendor (ASCII) | Variable | Variable |
| | | | | | Two low order digits of year (00 = 2000) - | | |
| 212 | D4 | 0 | 16 | Date Code - Year | ASCII code | Variable | Variable |
| | | | | | Digits of month (01=JAN ~ 12=DEC) - ASCII | | |
| 214 | D6 | 0 | | Date Code - Month | code | Variable | Variable |
| 216 | D8 | 0 | 16 | Date Code - Day | Digits of day (01-31) - ASCII code | Variable | Variable |
| | | _ | | | Vendor specific lot code, may be left blank - | _ | _ |
| 218 | DA | 0 | | Date Code - Vendor specific lot code | ASCII code | 0 | 0 |
| 220 | DC DC | 0 | | RESERVED Received power mass. Type | RESERVED Special functions | NA Average power | NA 1 |
| 220 220 | DC | 3 | _ | Received power meas. Type FEC BER support | Special functions Special functions | Average power FALSE | 0 |
| 220 | DC | 5 | | AUX3 (Finisar) | Aux3 minitor (1612 only) | RESERVED | 0 |
| 221 | | 0 | | Optional CMU support mode | Enhanced Options | FALSE | 0 |
| 221 | DD | 1 | 1 | Wavelength Tunability implemented | Enhanced Options | FALSE | 0 |
| 221 | DD | 2 | 1 | Active FEC control function umplemented | Enhanced Options | TRUE | 1 |
| | DD | 3 | 1 | Support VPS bypass regulator mode | Enhanced Options | FALSE | 0 |
| 221 | DD | 4 | 1 | Suport VPS LV regulator mode | Enhanced Options | FALSE | 0 |
| 221 221 | | 5 | 1 | Soft P_Down | Enhanced Options | TRUE | 1 |
| 221 221 | DD | | 1 | Soft TX_DISABLE | Enhanced Options | TRUE | 1 |
| 221 221 221 | DD | 6 | _ | | Enhanced Options | FALSE | 0 |
| 221 221 221 221 | DD DD | 7 | 1 | Variable Power Supply Support | | | |
| 221 221 221 221 222 | DD DD DE | 7 | 1 | Aux A/D Input 2 | Enhanced Options | +3.3V Supply Voltage | 7 |
| 221 221 221 221 222 222 | DD DD DE DE | 7 0 4 | 1 4 4 | Aux A/D Input 2 Aux A/D Input 1 | Enhanced Options Enhanced Options | | 7 4 |
| 221 221 221 221 222 | DD DD DE | 7 | 1 | Aux A/D Input 2 | Enhanced Options | +3.3V Supply Voltage | 7 4 Variable |
| 221 221 221 221 222 222 | DD DD DE DE | 7 0 4 | 1 4 4 | Aux A/D Input 2 Aux A/D Input 1 | Enhanced Options Enhanced Options | +3.3V Supply Voltage | 7 4 Variable 000000000000000000000000000000000000 |
| 221 221 221 221 222 222 | DD DD DE DE | 7 0 4 | 1 4 4 | Aux A/D Input 2 Aux A/D Input 1 | Enhanced Options Enhanced Options | +3.3V Supply Voltage | 7 4 Variable |
| 221 221 221 221 222 222 | DD DD DE DE | 7 0 4 | 1 4 4 | Aux A/D Input 2 Aux A/D Input 1 | Enhanced Options Enhanced Options | +3.3V Supply Voltage | 7 4 Variable 000000000000000000000000000000000000 |

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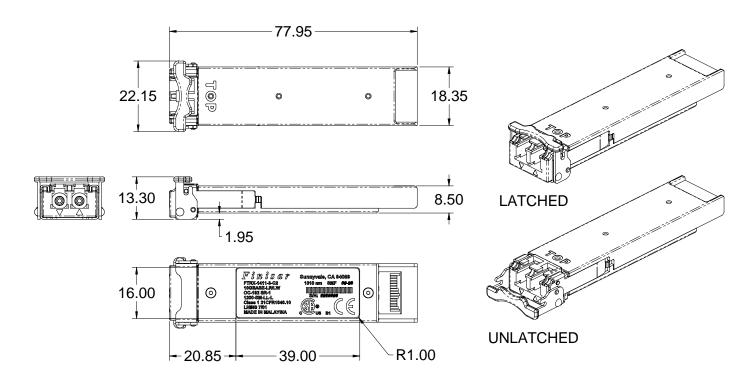
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EEPROM (Table 02h)

All Bytes except 128 and 129 filled with "00" unless otherwise specified by customer requirements. Addresses 128 and 129 are filled with "FF".

IX. Mechanical Specifications

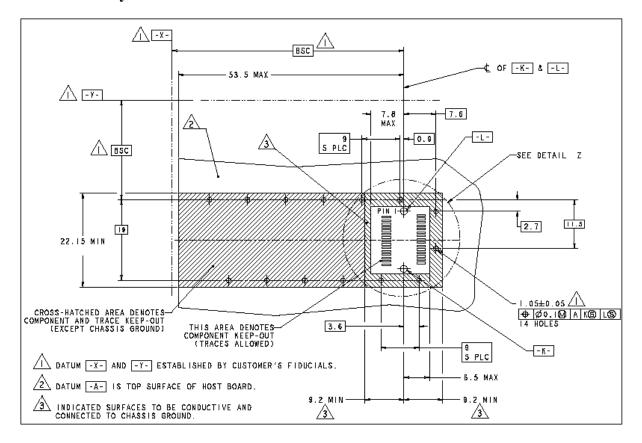
Finisar's XFP transceivers are compliant with the dimensions defined by the XFP Multi-Sourcing Agreement (MSA).



XFP Transceiver (dimensions are in mm)

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|---------|---|------------------|---------------|--|--|
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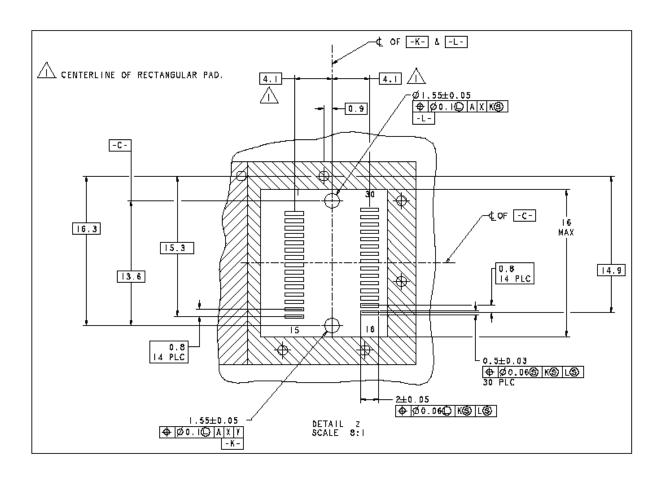
X. PCB Layout and Bezel Recommendations



XFP Host Board Mechanical Layout (dimensions are in mm)

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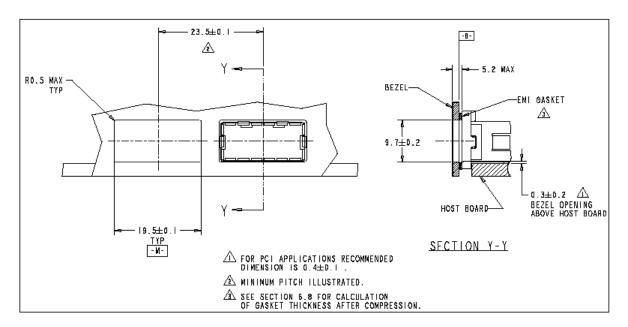
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XFP Detail Host Board Mechanical Layout (dimensions are in mm)

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XFP Recommended Bezel Design (dimensions are in mm)

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XI. Notes & Exceptions

- The FTLX3815 product family has the following exceptions to the XFP MSA;
 - o Initialize time of 2 sec maximum (MSA requires 300ms).
- XFI loopback operation:
 - When XFI Loopback is enabled, the Transmitter output is disabled.
 - When Line Loopback is enabled, the Receiver input is disabled.
- 8.5Gb/s operation requires configuration change via I2C vendor reserved command.

XIII. References

- 2. 10 Gigabit Small Form Factor Pluggable Module (XFP) Multi-Source Agreement (MSA), Rev 4.5 August 2005. Documentation is currently available at http://www.xfpmsa.org/
- 3. Application Note AN-2035: "Digital Diagnostic Monitoring Interface for XFP Optical Transceivers" Finisar Corporation, December 2003
- 4. Directive 2002/95/EC of the European Council Parliament and of the Council, "on the restriction of the use of certain hazardous substances in electrical and electronic equipment". January 27, 2003.
- "Application Note AN-2038: Finisar Implementation Of RoHS Compliant Transceivers", Finisar Corporation, January 21, 2005.

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XIII. Product Selection Details

FTLX3815M3xx

FT: FT Series L: RoHS-6

X: 10G Bit Rate Class

38: 80km (asymmetric chirp)

1: XFP form factor

5: Standard Performance Class

M: Multiprotocol

3: Commercial temperature range

xx: Sub-Band start channel (please refer to page 6 for channel definition)

XIV. Revision History

| Revision | Date | Description | |
|----------|------------|--|--|
| A00 | 8/15/2012 | Preliminary document created | |
| A01 | 10/22/2012 | Update EEPROM Table A0h and 01h | |
| A02 | 10/31/2012 | Include cold start timing, correct initialization timing, SBS/Dither Byte | |
| A03 | 6/11/2014 | Update TX Bias High Warning; EEPROM: update values for Bytes 188, 1 193 in Table 01h, and values for Bytes 128 and 129 in Table 02h. | |
| A04 | 11/1/2014 | Data output Rise and Fall times adjusted to 40ps max. | |

XV. For more information

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ПОСТАВКА ЭЛЕКТРОННЫХ КОМПОНЕНТОВ

многоканальный

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001 Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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