

### Typical Applications

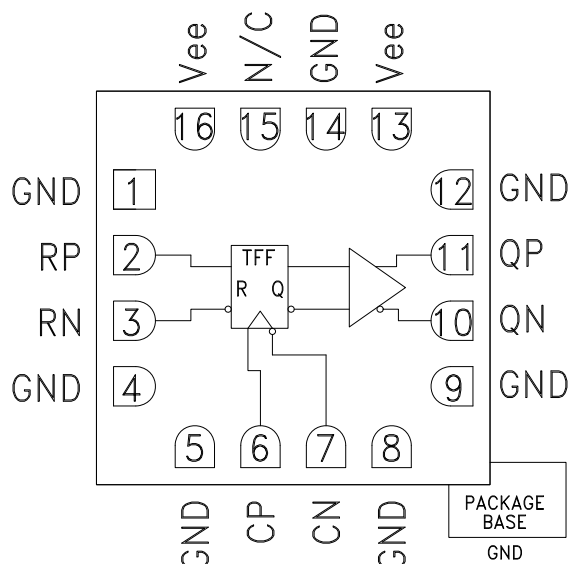
The HMC729LC3C is ideal for:

- Serial Data Transmission up to 26 Gbps
- High Speed Frequency Divider (up to 26 GHz)
- Broadband Test & Measurement
- RF ATE Applications

### Features

Supports Clock Frequencies up to 26 GHz  
Differential or Single-Ended Operation  
Fast Rise and Fall Times: 18 / 17 ps  
Low Power Consumption: 270 mW typ.  
Propagation Delay: 95 ps  
Single Supply: -3.3 V  
16 Lead Ceramic 3x3 mm SMT Package: 9 mm<sup>2</sup>

### Functional Diagram



### General Description

The HMC729LC3C is a T-Type Flip-Flop w/Reset designed to support clock frequencies as high as 26 GHz. During normal operation, with the reset pin not asserted, the output toggles from its prior state on the positive edge of the clock. This results in a divide-by-two function of the clock input. Asserting the reset pin forces the Q output low regardless of the clock edge state (asynchronous reset assertion). Reversing the clock inputs allows for negative-edge triggered applications.

All differential inputs to the HMC729LC3C are CML and terminated on-chip with 50 Ohms to the positive supply, GND, and may be DC or AC coupled. The differential CML outputs are source terminated to 50 Ohms and may also be AC or DC coupled. Outputs can be connected directly to a 50 Ohm ground-terminated system or drive devices with CML logic input. The HMC729LC3C operates from a single -3.3 V supply and is available in ROHS-compliant 3x3 mm SMT package.

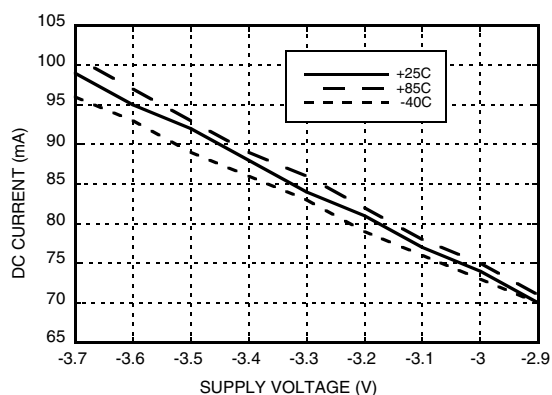
### Electrical Specifications, $T_A = +25\text{ }^{\circ}\text{C}$ , $V_{ee} = -3.3\text{ V}$

| Parameter                | Conditions                 | Min. | Typ. | Max  | Units |
|--------------------------|----------------------------|------|------|------|-------|
| Power Supply Voltage     |                            | -3.6 | -3.3 | -3.0 | V     |
| Power Supply Current     |                            |      | 82   |      | mA    |
| Maximum Clock Rate       |                            |      | 26   |      | GHz   |
| Input Voltage Range      |                            | -1.5 |      | 0.5  | V     |
| Input Differential Range |                            | 0.1  |      | 2.0  | Vp-p  |
| Input Return Loss        | Frequency <13 GHz          |      | 10   |      | dB    |
| Output Amplitude         | Single-Ended, peak-to-peak |      | 550  |      | mVp-p |
|                          | Differential, peak-to-peak |      | 1100 |      | mVp-p |
| Output High Voltage      |                            |      | -10  |      | mV    |
| Output Low Voltage       |                            |      | -560 |      | mV    |

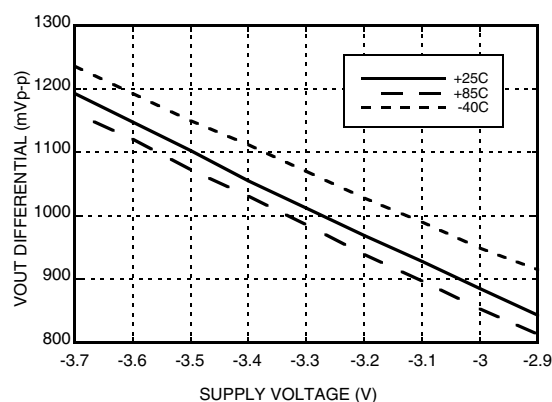
### Electrical Specifications (continued)

| Parameter                         | Conditions              | Min. | Typ.    | Max | Units   |
|-----------------------------------|-------------------------|------|---------|-----|---------|
| Output Rise / Fall Time           | Differential, 20% - 80% |      | 18 / 17 |     | ps      |
| Output Return Loss                | Frequency <13 GHz       |      | 10      |     | dB      |
| Random Jitter Jr                  | rms                     |      |         | 0.2 | ps rms  |
| Deterministic Jitter, Jd          | peak-to-peak            |      | 2       |     | ps, p-p |
| Propagation Delay Clock to Q, td  |                         |      | 95      |     | ps      |
| Propagation Delay Reset to Q, tdr |                         |      | 125     |     | ps      |

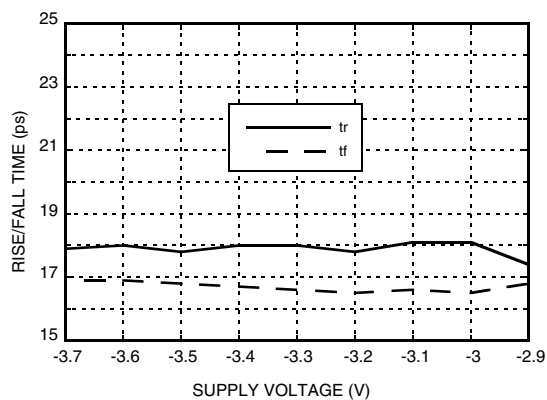
**DC Current vs. Supply Voltage [1]**



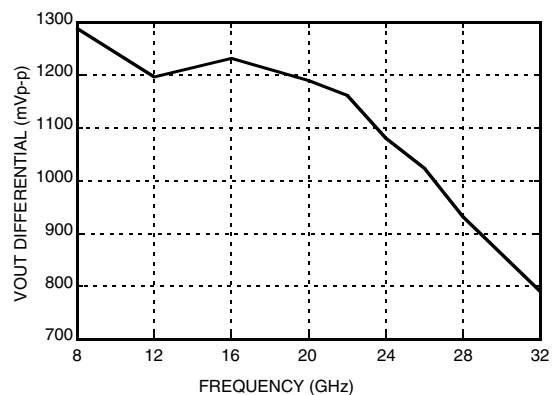
**Output Differential Voltage vs. Supply Voltage [2]**



**Rise / Fall Time vs. Supply Voltage [2]**



**Output Differential Voltage vs. Input Frequency [3]**



[1] Data rate = 13 Gbps

[2] Frequency = 24 GHz

[3] Vee = -3.3 V



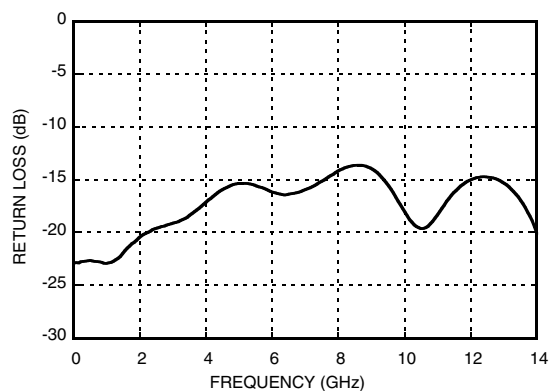
MICROWAVE CORPORATION v05.1010



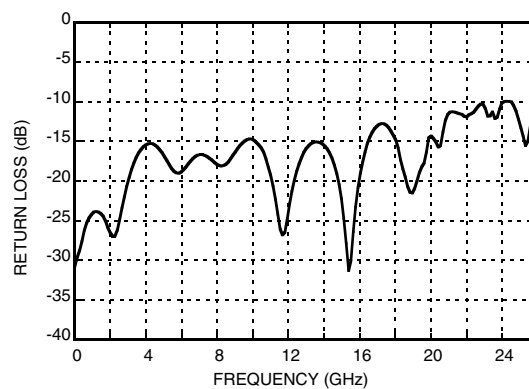
## HMC729LC3C

**26 GHz, T-FLIP-FLOP  
w/ RESET**

**Output Return Loss vs. Frequency**



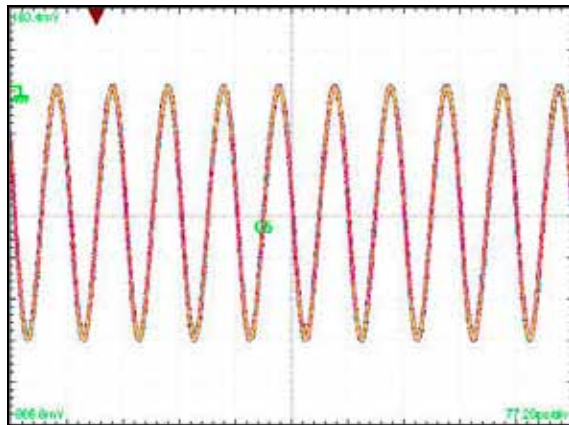
**Input Return Loss vs. Frequency**



3

HIGH SPEED LOGIC - SMT

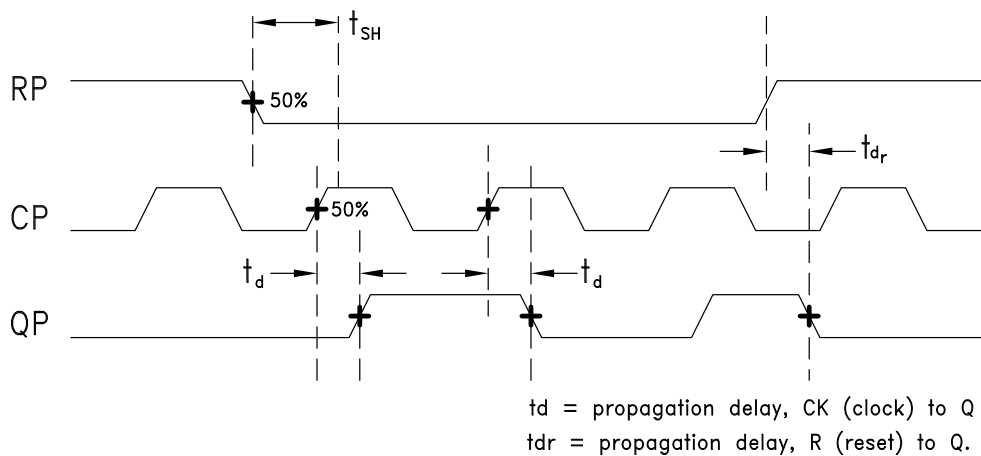
### Output Waveform



[1] Test Conditions:

Waveform generated with a CW signal source input at 26 GHz.  
Diagram data presented on a Tektronix CSA 8000.

### Timing Diagram



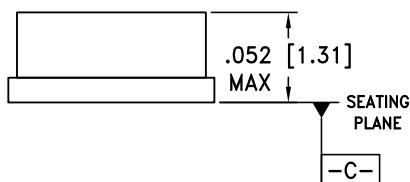
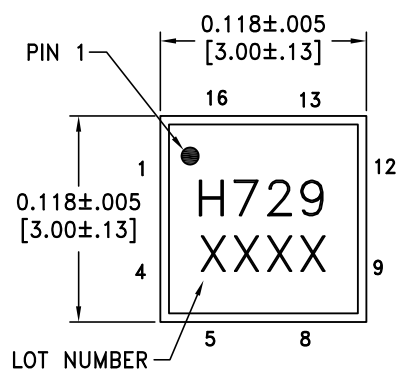
### Absolute Maximum Ratings

|                                                                                    |                   |
|------------------------------------------------------------------------------------|-------------------|
| Power Supply Voltage (Vee)                                                         | -3.75 V to +0.5 V |
| Input Signals                                                                      | -2 V to +0.5 V    |
| Output Signals                                                                     | -1.5 V to +1 V    |
| Continuous P <sub>diss</sub> (T = 85 °C)<br>(derate 17 mW/°C above 85 °C)          | 0.68 W            |
| Thermal Resistance (R <sub>th j-p</sub> ) Worst<br>case junction to package paddle | 59 °C/W           |
| Maximum Junction Temperature                                                       | 125 °C            |
| Storage Temperature                                                                | -65 °C to +150 °C |
| Operating Temperature                                                              | -40 °C to +85 °C  |
| ESD Sensitivity (HBM)                                                              | Class 1C          |

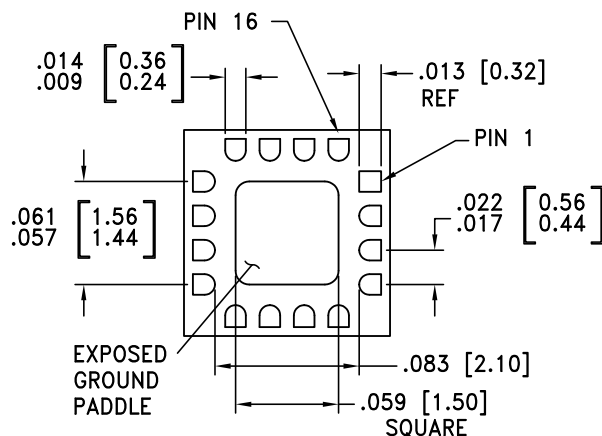


ELECTROSTATIC SENSITIVE DEVICE  
OBSERVE HANDLING PRECAUTIONS

### Outline Drawing



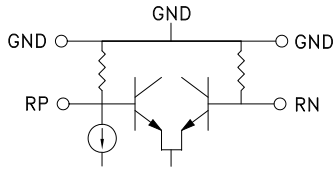
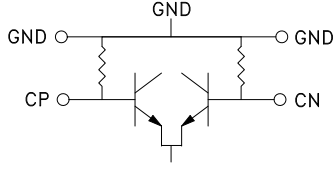
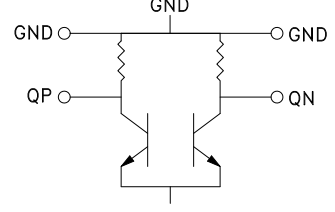
### BOTTOM VIEW



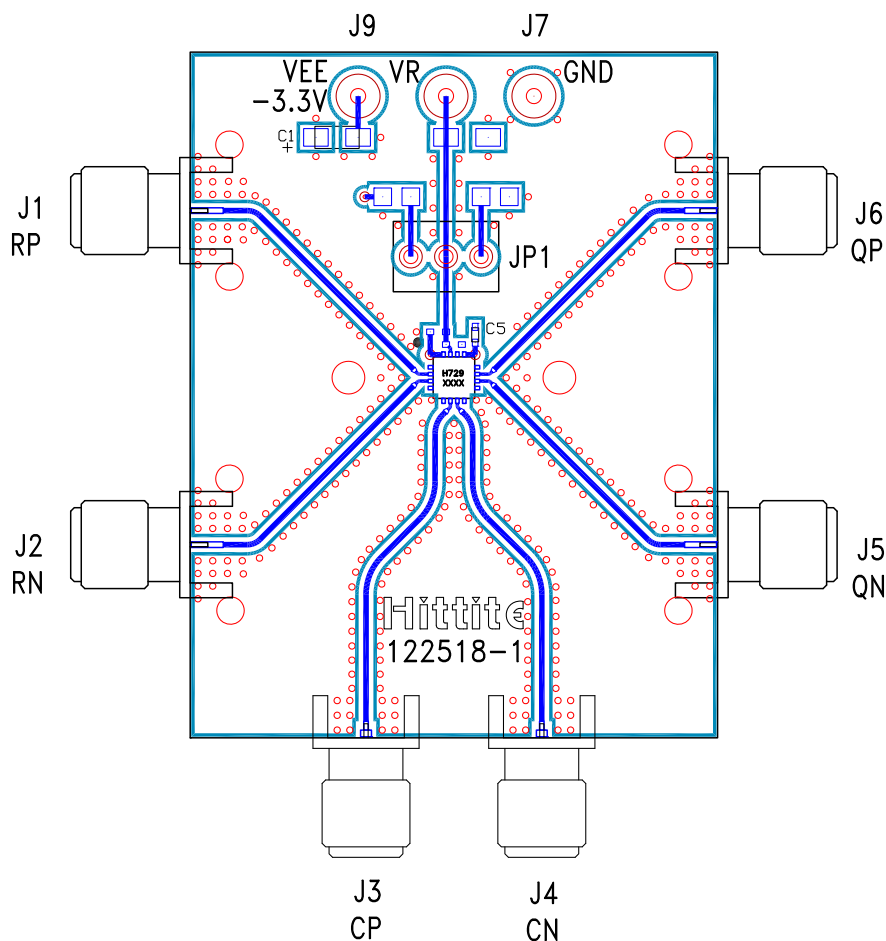
#### NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:  
30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05 mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO GND.

### Pin Descriptions <sup>[1]</sup>

| Pin Number          | Function | Description                                                                         | Interface Schematic                                                                   |
|---------------------|----------|-------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| 1, 4, 5, 8, 9, 12   | GND      | Signal Grounds                                                                      |    |
| 2, 3                | RP, RN   | Differential Reset Inputs: Current Mode Logic (CML) referenced to positive supply.  |    |
| 6, 7                | CP, CN   | Differential Clock Inputs: Current Mode Logic (CML) referenced to positive supply.  |    |
| 10, 11              | QN, QP   | Differential Clock Outputs: Current Mode Logic (CML) referenced to positive supply. |   |
| 13, 16              | Vee      | Negative Supply                                                                     |                                                                                       |
| 14,<br>Package Base | GND      | Supply Ground                                                                       |  |
| 15                  | N/C      | No Connection                                                                       |                                                                                       |

[1] Contact HMC for alternate pinouts

**Evaluation PCB**

**List of Materials for Evaluation PCB 122518-1<sup>[1]</sup>**

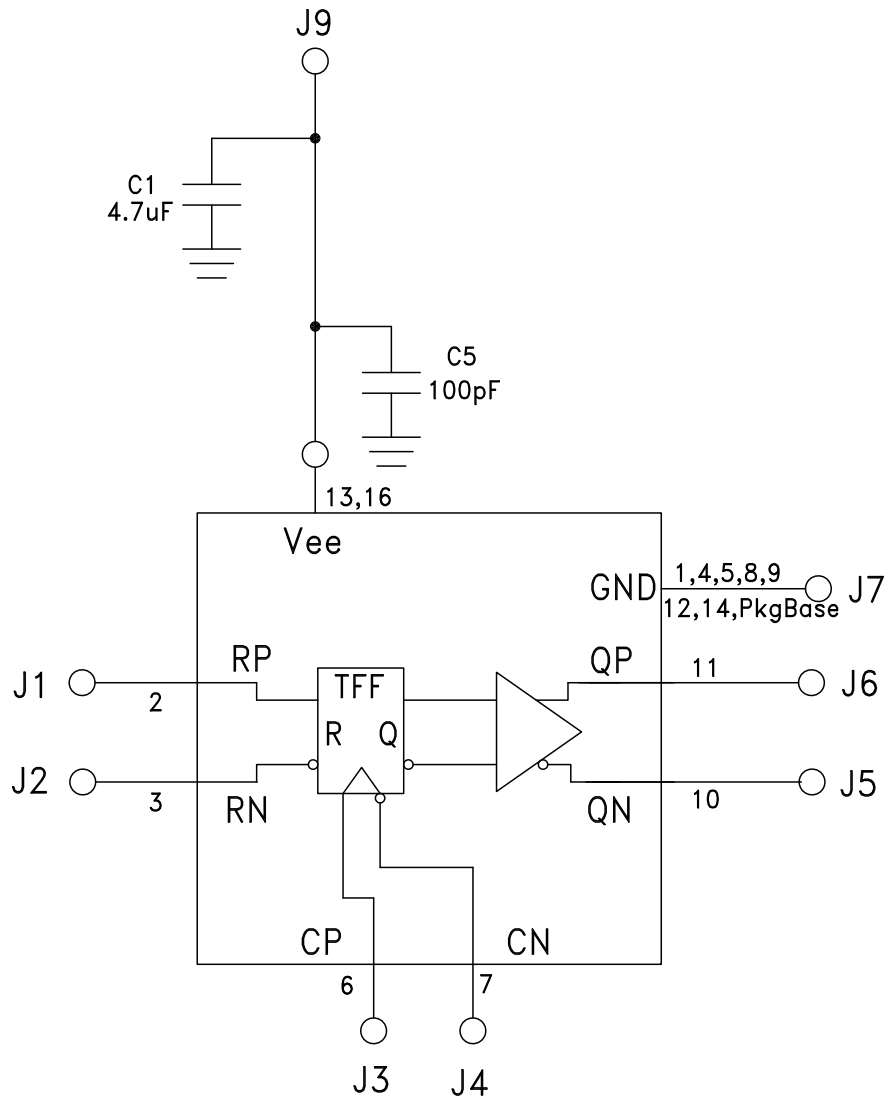
| Item           | Description                                      |
|----------------|--------------------------------------------------|
| J3, J4         | PCB Mount 2.92mm RF Connectors                   |
| J1, J2, J5, J6 | PCB Mount SMA RF Connectors                      |
| J7 - J9        | DC Pin                                           |
| C1             | 4.7 $\mu$ F Capacitor, Tantalum                  |
| C5             | 100 pF Capacitor, 0402 Pkg.                      |
| U1             | HMC729LC3C<br>High Speed Logic, T Type Flip-Flop |
| PCB [2]        | 122518 Evaluation Board                          |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed packaged base should be connected to GND. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

### Application Circuit



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### Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

Skype отдела продаж:

moschip.ru

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