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January 2013

### FDN537N

# Single N-Channel Power Trench<sup>®</sup> MOSFET 30 V, 6.5 A, 23 m $\Omega$

#### **Features**

- Max  $r_{DS(on)}$  = 23 m $\Omega$  at  $V_{GS}$  = 10 V,  $I_D$  = 6.5 A
- Max  $r_{DS(on)}$  = 36 m $\Omega$  at  $V_{GS}$  = 4.5 V,  $I_D$  = 6.0 A
- High performance trench technology for extremely low r<sub>DS(on)</sub>
- High power and current handling capability in a widely used surface mount package
- Fast switching speed
- 100% UIL Tested
- RoHS Compliant

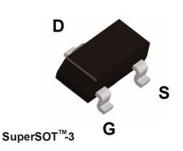


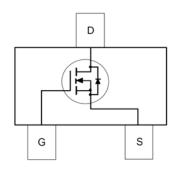
#### **General Description**

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been optimized for  $r_{DS(on)}$ , switching performance and ruggedness.

#### **Application**

■ Primary DC-DC Switch





#### MOSFET Maximum Ratings T<sub>A</sub> = 25 °C unless otherwise noted

Symbol	Parameter		Ratings	Units
$V_{DS}$	Drain to Source Voltage		30	V
$V_{GS}$	Gate to Source Voltage	(Note 3)	±20	V
	Drain Current -Continuous (Package limited) T <sub>C</sub> = 25 °C		8.0	
I <sub>D</sub>	-Continuous T <sub>A</sub> = 25 °C	(Note 1a)	6.5	Α
	-Pulsed		25	
D	Power Dissipation	(Note 1a)	1.5	W
$P_{D}$	Power Dissipation	(Note 1b)	0.6	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range		-55 to +150	°C

#### **Thermal Characteristics**

D	Thermal Resistance, Junction to Ambient	(Note 1a)	80	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	180	C/VV

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
537	FDN537N	SSOT-3	7 "	8 mm	3000 units

### **Electrical Characteristics** $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		18		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V			1	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA

#### **On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	1.2	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu A$ , referenced to 25 °C		-6		mV/°C
		$V_{GS} = 10 \text{ V}, I_D = 6.5 \text{ A}$		19	23	
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 6.0 \text{ A}$		25	36	$m\Omega$
	$V_{GS} = 10 \text{ V}, I_D = 6.5 \text{ A}, T_J = 125 ^{\circ}\text{C}$		25	30		
9 <sub>FS</sub>	Forward Transconductance	$V_{DD} = 5 \text{ V}, I_{D} = 6.5 \text{ A}$		24		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V 45 V V 0 V	360	465	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$	143	180	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 1011 12	22	35	pF
$R_{\alpha}$	Gate Resistance		1.0		Ω

#### **Switching Characteristics**

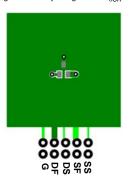
t <sub>d(on)</sub>	Turn-On Delay Time		5	10	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 6.5 A,	1	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	11	19	ns
t <sub>f</sub>	Fall Time		1	10	ns
(	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V	6.0	8.4	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to } 4.5 \text{ V}$ $V_{DD} = 15 \text{ V}$	3.0	4.2	nC
$Q_{gs}$	Total Gate Charge	I <sub>D</sub> = 6.5 A	1.2		nC
$Q_{ad}$	Gate to Drain "Miller" Charge		1.1		nC

#### **Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 6.5 \text{ A}$ (Note 2)		0.86	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 6.5 A, di/dt = 100 A/μs		14	22	ns
Q <sub>rr</sub>	Reverse Recovery Charge			3	10	nC

#### NOTES

 $<sup>1.</sup>R_{0,\mathrm{IA}}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{0,\mathrm{IC}}$  is guaranteed by design while  $R_{0,\mathrm{CA}}$  is determined by the user's board design.



a) 80 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b) 180 °C/W when mounted on a minimum pad.

- 2. Pulse Test: Pulse Width < 300  $\mu\text{s},$  Duty cycle < 2.0 %.
- 3. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

#### Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

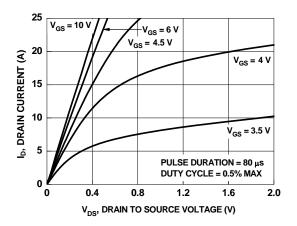


Figure 1. On Region Characteristics

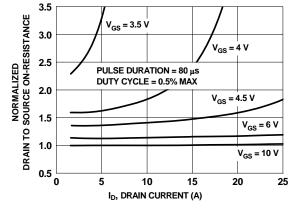


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

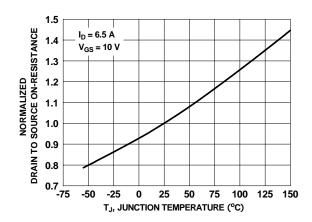


Figure 3. Normalized On Resistance vs Junction Temperature

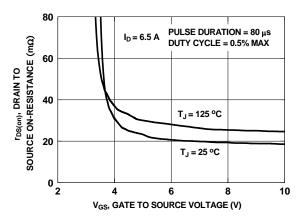


Figure 4. On-Resistance vs Gate to Source Voltage

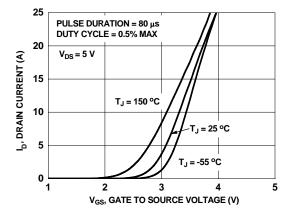


Figure 5. Transfer Characteristics

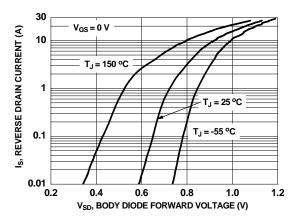


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

#### **Typical Characteristics** $T_J = 25$ °C unless otherwise noted

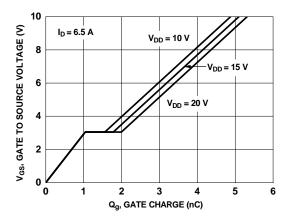


Figure 7. Gate Charge Characteristics

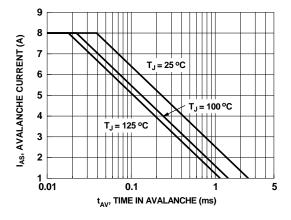


Figure 9. Unclamped Inductive Switching Capability

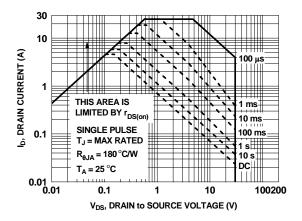


Figure 11. Forward Bias Safe Operating Area

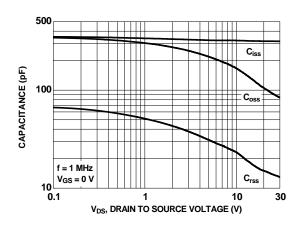


Figure 8. Capacitance vs Drain to Source Voltage

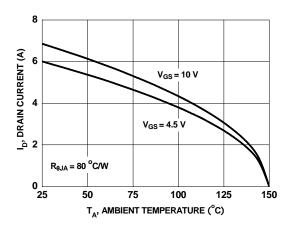


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

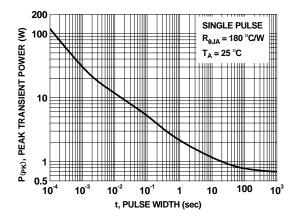


Figure 12. Single Pulse Maximum Power Dissipation

### Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

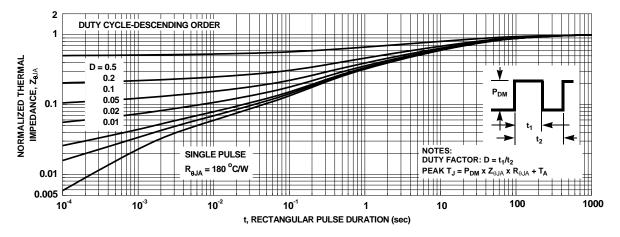


Figure 13. Junction-to-Ambient Transient Thermal Response Curve





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