



## Quad SPST CMOS Analog Switches

DG201A/DG211

### General Description

The DG201A and DG211 are normally closed, quad single-pole single-throw (SPST) analog switches. These CMOS switches can be continuously operated with power supplies ranging from  $\pm 4.5V$  to  $\pm 18V$ . Maxim guarantees that these switches will not latch up if the power supplies are disconnected with input signals still connected.

Both devices have guaranteed break-before-make switching. The DG201A differs from the DG211 primarily in switching speeds. The DG201A has a maximum turn-off time of 450ns and a maximum turn-on time of 600ns. The DG211 has a maximum turn-off time of 500ns and a maximum turn-on time of 1000ns.

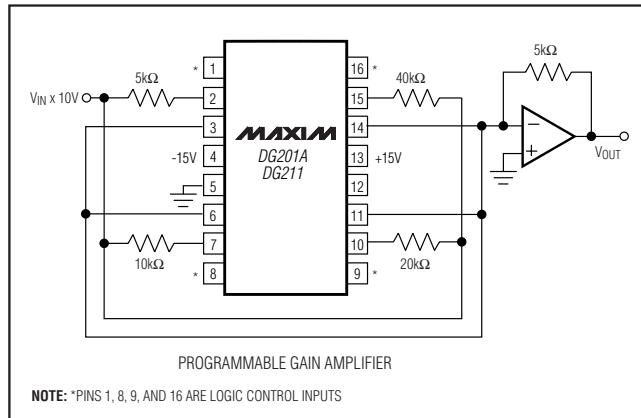
Compared to the original manufacturer's products, Maxim's DG201A and DG211 consume significantly lower power making them better suited for portable applications. Maxim has also eliminated the need for the third ( $V_L$ ) power supply that is required for the operation of the original manufacturer's DG211.

### Applications

- Winchester Disk Drives
- Test Equipment
- Communications Systems
- PBX, PABX
- Guidance and Control Systems
- Head Up Displays
- Military Radios

*Pin Configurations continued at end of data sheet.*

### Typical Operating Circuit



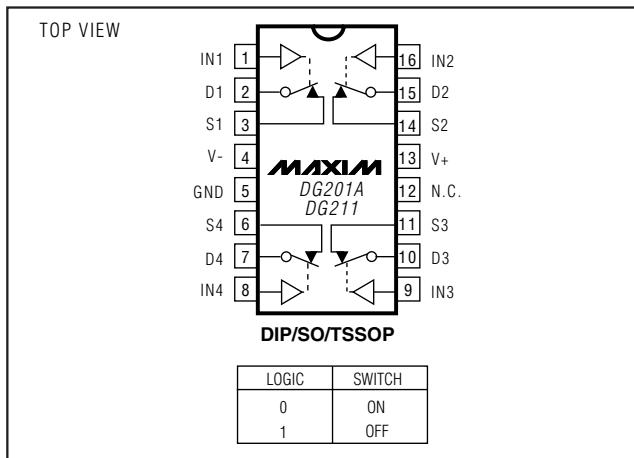
### Features

- ◆ Guaranteed  $\pm 4.5V$  to  $\pm 18V$  Operation
- ◆ No  $V_L$  Supply Required
- ◆ Nonlatching with Supplies Turned Off and Input Signals Present
- ◆ CMOS and TTL Logic Compatible
- ◆ Monolithic, Low-Power CMOS Design

### Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DG201ACUE	0°C to +70°C	16 TSSOP
DG201ACSE	0°C to +70°C	16 SO
DG201ACJ	0°C to +70°C	16 Plastic DIP
DG201C/D	0°C to +70°C	Dice
DG201AEQE	-40°C to +85°C	16 QFN (5 × 5)
DG201AEUE	-40°C to +85°C	16 TSSOP
DG201ADY	-40°C to +85°C	16 SO
DG201ADJ	-40°C to +85°C	16 Plastic DIP
DG201AAK	-55°C to +125°C	16 CERDIP
DG201ABK	-25°C to +85°C	16 CERDIP
<b>DG211CUE</b>	0°C to +70°C	16 TSSOP
DG211CSE	0°C to +70°C	16 SO
DG211CJ	0°C to +70°C	16 Plastic DIP
DG211C/D	0°C to +70°C	Dice
DG211EGE	-40°C to +85°C	16 QFN (5 × 5)
DG211EUE	-40°C to +85°C	16 TSSOP
DG211DY	-40°C to +85°C	16 SO
DG211DJ	-40°C to +85°C	16 Plastic DIP

### Pin Configurations



# Quad SPST CMOS Analog Switches

## ABSOLUTE MAXIMUM RATINGS (DG211)

V+ to V-	44V
V <sub>IN</sub> to Ground	V-, V+
V <sub>L</sub> to Ground	-0.3V, 25V
V <sub>S</sub> or V <sub>D</sub> to V+	0, -40V
V <sub>S</sub> or V <sub>D</sub> to V-	0, 40V
V+ to Ground	.25V
V- to Ground	-25V
Current, Any Terminal Except S or D	30mA
Continuous Current, S or D	20mA
Peak Current, S or D (pulsed at 1ms 10% duty cycle max)	70mA

Storage Temperature Range	-65°C to +125°C
Operating Temperature Range	
DG211C	0°C to +70°C
DG211D/E	-40°C to +85°C
Power Dissipation ( $T_A = +70^\circ\text{C}$ ) (Note 1)	
16-Pin Plastic Dip (derate 10.5mW/°C above +70°C)	.842mW
16-Pin Narrow SO (derate 8.3mW/°C above +70°C)	.696mW
16-Pin TSSOP (derate 9.4mW/°C above +70°C)	.755mW
16-Pin QFN (5 × 5) (derate 19.2mW/°C above +70°C)	1.538mW

**Note 1:** Device mounted with all leads soldered to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS (DG211)

(V+ = +15V, V- = -15V, GND = 0,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.) (For more information on TYP values see Note 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SWITCH</b>						
Analog Signal Range	V <sub>ANALOG</sub>		-15	15		V
Drain-Source ON-Resistance	R <sub>DSON</sub>	V <sub>D</sub> = ±10V, V <sub>IN</sub> = 0.8V, I <sub>S</sub> = 1mA	115	175		Ω
Source OFF-Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN</sub> = 2.4V	V <sub>S</sub> = 14V, V <sub>D</sub> = -14V	0.01	5.0	nA
			V <sub>S</sub> = -14V, V <sub>D</sub> = 14V	-5.0	-0.02	
Drain OFF-Leakage Current	I <sub>D(OFF)</sub>	V <sub>IN</sub> = 2.4V	V <sub>S</sub> = 14V, V <sub>D</sub> = -14V	0.01	5.0	
			V <sub>S</sub> = -14V, V <sub>D</sub> = 14V	-5.0	-0.02	
Drain ON-Leakage Current (Note 3)	I <sub>D(ON)</sub>	V <sub>IN</sub> = 0.8V	V <sub>S</sub> = V <sub>D</sub> = -14V	0.1	5.0	
			V <sub>S</sub> = V <sub>D</sub> = 14V	-5.0	-0.15	
<b>INPUT</b>						
Input Current with Input Voltage High	I <sub>INH</sub>	V <sub>IN</sub> = 2.4V	-1.0	-0.0004		μA
		V <sub>IN</sub> = 15V		0.003	1.0	
Input Current with Input Voltage Low	I <sub>INL</sub>	V <sub>IN</sub> = 0	-1.0	-0.0004		
<b>DYNAMIC</b>						
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit V <sub>S</sub> = 2V, R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 35pF	460	1000		ns
Turn-OFF Time	t <sub>OFF1</sub>		360	500		
	t <sub>OFF2</sub>		450			
Source OFF-Capacitance	C <sub>S(OFF)</sub>	V <sub>S</sub> = 0, V <sub>IN</sub> = 5V, f = 1MHz	5			pF
Drain OFF-Capacitance	C <sub>D(OFF)</sub>	V <sub>D</sub> = 0, V <sub>IN</sub> = 5V, f = 1MHz	5			
Channel ON-Capacitance	C <sub>D+S(ON)</sub>	V <sub>D</sub> = V <sub>S</sub> = 0, V <sub>IN</sub> = 0, f = 1MHz	16			
OFF-Isolation (Note 4)	OIRR	V <sub>IN</sub> = 5V, R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 15pF, V <sub>S</sub> = 1VRMS, f = 100kHz	70			dB
Crosstalk (Channel to Channel)	CCRR			90		

# Quad SPST CMOS Analog Switches

## ELECTRICAL CHARACTERISTICS (DG211) (continued)

( $V_+ = +15V$ ,  $V_- = -15V$ , GND = 0,  $T_A = +25^\circ C$ , unless otherwise noted.) (For more information on TYP values see Note 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SUPPLY</b>						
Positive Supply Current	$I^+$	$V_{IN} = 0$ and $2.4V$ (all)	0.02	0.4	mA	
Negative Supply Current	$I^-$		0.01	0.4		
Logic Supply Current	$I_L$		0	0		
Power-Supply Range for Continous Operation	$V_{OP}$		$\pm 4.5$	$\pm 18$	V	

**Note 2:** Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

**Note 3:**  $I_{D(ON)}$  is leakage from driver into "ON" switch.

**Note 4:** OFF-Isolation =  $20 \log V_S/V_D$ ,  $V_S$  = input to OFF switch,  $V_D$  = output.

## ABSOLUTE MAXIMUM RATINGS (DG201A)

Voltages Reference to V-

$V_+$ .....	44V
GND.....	25V
Digital Inputs (Note 1), $V_S$ , $V_D$ .....	-2V to ( $V_+$ + 2V) or 20mA, whichever occurs first
Current, Any Terminal Except S or D.....	30mA
Continuous Current, S or D.....	20mA
Peak Current, S or D (pulsed at 1ms 10% duty cycle max).....	70mA

Operating Temperature Range

DG201AA.....	-55°C to +125°C
DG201AD/E.....	-40°C to +85°C
DG201AC.....	0°C to +70°C

Storage Temperature Range.....-65°C to +150°C

Power Dissipation (Note 2)

16-Pin Plastic Dip (derate 10.5mW/°C above +70°C).....	842mW
16-Pin SO (derate 8.7mW/°C above +70°C).....	696mW
16-Pin TSSOP (derate 9.4mW/°C above +70°C).....	755mW
16-Pin QFN (5 x 5) (derate 19.2mW/°C above +70°C).....	1538mW
16-Pin CERDIP (derate 10.0mW/°C above +70°C).....	800mW

**Note 1:** Signals on S, D, or IN exceeding  $V_+$  or  $V_-$  on Maxim's DG201A will be clamped by internal diodes, and are also internally current limited to 25mA.

**Note 2:** Device mounted with all leads soldered to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS (DG201A)

( $V_+ = +15V$ ,  $V_- = -15V$ , GND = 0,  $T_A = +25^\circ C$ , unless otherwise noted.) (For more information on TYP values see Note 3.)

PARAMETER	SYMBOL	CONDITIONS	DG201AA			DG201AC, D, E			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>SWITCH</b>									
Analog Signal Range	$V_{ANALOG}$		-15	15	-15	15			V
Drain-Source ON Resistance	$R_{DS(ON)}$	$V_D = \pm 10V$ , $V_{IN} = 0.8V$ , $I_S = 1mA$	115	175	115	200			$\Omega$
Source OFF-Leakage Current	$I_{S(OFF)}$	$V_{IN} = 2.4V$	$V_S = 14V$ , $V_D = -14V$	0.01	1.0	0.01	5.0		nA
			$V_S = -14V$ , $V_D = 14V$	-1.0	-0.02	-5.0	-0.02		
Drain OFF-Leakage Current	$I_{D(OFF)}$	$V_{IN} = 2.4V$	$V_S = 14V$ , $V_D = -14V$	0.01	1.0	0.01	5.0		
			$V_S = -14V$ , $V_D = 14V$	-1.0	-0.02	-5.0	-0.02		
Drain ON-Leakage Current (Note 4)	$I_{D(ON)}$	$V_{IN} = 0.8V$	$V_S = -14V$	0.1	1.0	0.1	1.0		
			$V_S = 14V$	-1.0		-1.0			

# Quad SPST CMOS Analog Switches

## ELECTRICAL CHARACTERISTICS (DG201A) (continued)

(V<sub>+</sub> = +15V, V<sub>-</sub> = -15V, GND = 0, T<sub>A</sub> = +25°C, unless otherwise noted.) (For more information on TYP values see Note 3.)

PARAMETER	SYMBOL	CONDITIONS	DG201AA			DG201AC, D, E			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>INPUT</b>									
Input Current with Input Voltage High	I <sub>INH</sub>	V <sub>IN</sub> = 2.4V	-1.0		-1.0	1.0	1.0	1.0	μA
		V <sub>IN</sub> = 15V							
Input Current with Input Voltage Low	I <sub>INL</sub>	V <sub>IN</sub> = 0+	-1.0		-1.0				
<b>DYNAMIC</b>									
Turn-ON Time	t <sub>ON</sub>	See Figure 1 Switching Time Test Circuit	480	600		480	600		ns
Turn-OFF Time	t <sub>OFF1</sub>		370	450		370	450		
Charge Injection	Q	C <sub>L</sub> = 1000pF, V <sub>GEN</sub> = 0, R <sub>GEN</sub> = 0	20		20				pC
Source OFF-Capacitance	C <sub>S</sub> (OFF)	V <sub>S</sub> = 0, V <sub>IN</sub> = 5V	5		5	5	5	5	pF
Drain OFF-Capacitance	C <sub>D</sub> (OFF)		f = 140kHz	16					
Channel ON-Capacitance	C <sub>D</sub> (ON) + C <sub>S</sub> (ON)	V <sub>D</sub> = V <sub>S</sub> = 0, V <sub>IN</sub> = 0				16		16	
OFF-Isolation		V <sub>IN</sub> = 5V, Z <sub>L</sub> = 75Ω	70		70				dB
Crosstalk (Channel to Channel)		V <sub>S</sub> = 2.0V, f = 100kHz	90		90				
<b>SUPPLY</b>									
Positive Supply Current	I <sup>+</sup>	All channels ON or OFF	0.02	0.1		0.02	0.1		mA
Negative Supply Current	I <sup>-</sup>	All channels ON or OFF	-0.1	-0.01		-0.1	-0.01		
Power-Supply Range for Continuous Operation	V <sub>OP</sub>		±4.5	±18		±4.5	±18		V

**Note 3:** Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

**Note 4:** I<sub>D</sub> (ON) is leakage from driver into "ON" switch.

# Quad SPST CMOS Analog Switches

## ELECTRICAL CHARACTERISTICS (DG201A)

(V<sub>+</sub> = +15V, V<sub>-</sub> = -15V, GND = 0, T<sub>A</sub> = full operating temperature range, unless otherwise noted.) (For more information on TYP values see Note 3.)

PARAMETER	SYMBOL	CONDITIONS	DG201AA			DG201AC, D, E			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>SWITCH</b>									
Analog Signal Range	V <sub>ANALOG</sub>		-15	15	-15	15	15	V	
Drain-Source ON Resistance (Note 5)	R <sub>DS</sub> (ON)	V <sub>D</sub> = ±10V, V <sub>IN</sub> = 0.8V, I <sub>S</sub> = 1mA		250		250		250	Ω
Source OFF Leakage Current	I <sub>S</sub> (OFF)	V <sub>IN</sub> = 2.4V	V <sub>S</sub> = 14V, V <sub>D</sub> = -14V		100		100		nA
			V <sub>S</sub> = -14V, V <sub>D</sub> = 14V	-100		-100		-100	
Drain OFF Leakage Current	I <sub>D</sub> (OFF)	V <sub>IN</sub> = 2.4V	V <sub>S</sub> = 14V, V <sub>D</sub> = -14V		100		100		
			V <sub>S</sub> = -14V, V <sub>D</sub> = 14V	-100		-100		-100	
Drain ON Leakage Current (Note 6)	I <sub>D</sub> (ON)	V <sub>IN</sub> = 0.8V	V <sub>S</sub> = -14V		200		200		
			V <sub>D</sub> = 14V	-200		-200		-200	
<b>INPUT</b>									
Input Current with Input Voltage High	I <sub>INH</sub>	V <sub>IN</sub> = 2.4V		-1.0		-1.0		-1.0	μA
		V <sub>IN</sub> = 15V			1.0		1.0		
Input Current with Input Voltage Low	I <sub>INL</sub>	V <sub>IN</sub> = 0		-1.0		-1.0		-1.0	

**Note 5:** Electrical characteristics, such as ON-Resistance, will change when power supplies other than ±15V, are used.

**Note 6:** I<sub>D</sub> (ON) is leakage from driver into "ON" switch.

## Pin Description

PIN		NAME	FUNCTION	
DIP/SO/TSSOP	QFN			
1, 16, 9, 8	15, 14, 7, 6	IN1-IN4	Input	
2, 15, 10, 7	16, 13, 8, 5	D1-D4	Analog Switch Drain Terminal	
3, 14, 11, 6	1, 12, 9, 4	S1-S4	Analog Switch Source Terminal	
4	2	V-	Negative-Supply Voltage Input	
5	3	GND	Ground	
12	10	N.C.	No Connection	
13	11	V+	Positive-Supply Voltage Input—Connected to Substrate	

## Switching Time Test Circuit

Switch output waveform shown for V<sub>S</sub> = constant with logic input waveform as shown. Note that V<sub>S</sub> may be +ve or -ve as per switching times test circuit. V<sub>O</sub> is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

# Quad SPST CMOS Analog Switches

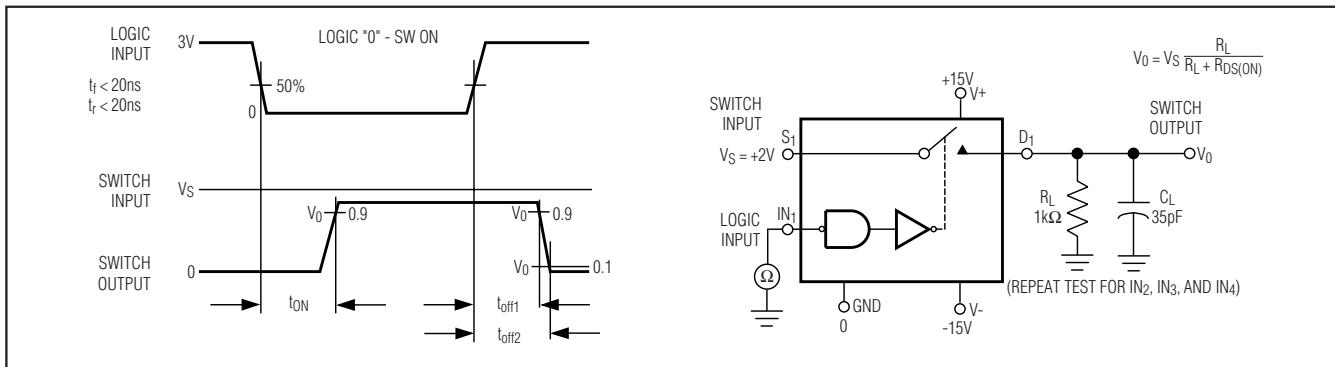


Figure 1. Switching Time

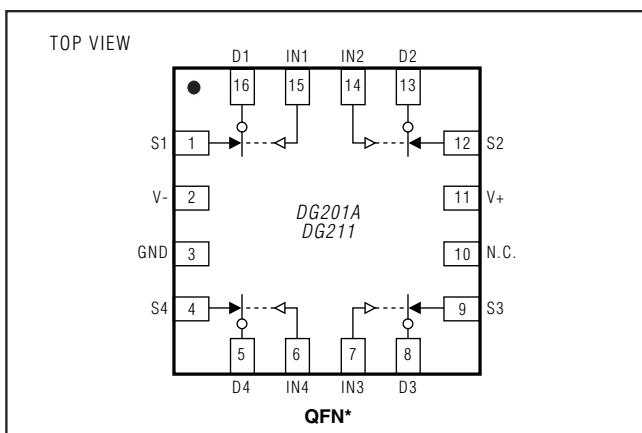
## Typical R<sub>DS(ON)</sub> vs. Power Supplies for Maxim's DG201A, and DG211

POWER SUPPLIES	R <sub>DS(ON)</sub> AT ANALOG SIGNAL LEVEL					
	-5V	+5V	-10V	+10V	-15V	+15V
±5V	350Ω	380Ω	—	—	—	—
±10V	—	—	165Ω	250Ω	—	—
±15V	—	—	125Ω	160Ω	135Ω	155Ω

## Protecting Against Fault Conditions

Fault conditions occur when power supplies are turned off when input signals are still present, or when overvoltages occur at the inputs during normal operation. In either case, source-to-body diodes can be forward biased and conduct current from the signal source. If this current is required to be kept to low ( $\mu$ A) levels then the addition of external protection diodes is recommended.

## Pin Configurations (continued)



To provide protection for overvoltages up to 20V above the supplies, a 1N4001 or 1N914 type diode should be placed in series with the positive and negative supplies as shown in Figure 2. The addition of these diodes will reduce the analog signal range to 1V below the positive supply and 1V above the negative supply.

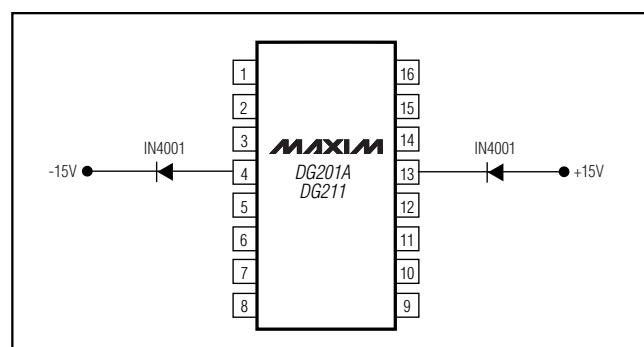
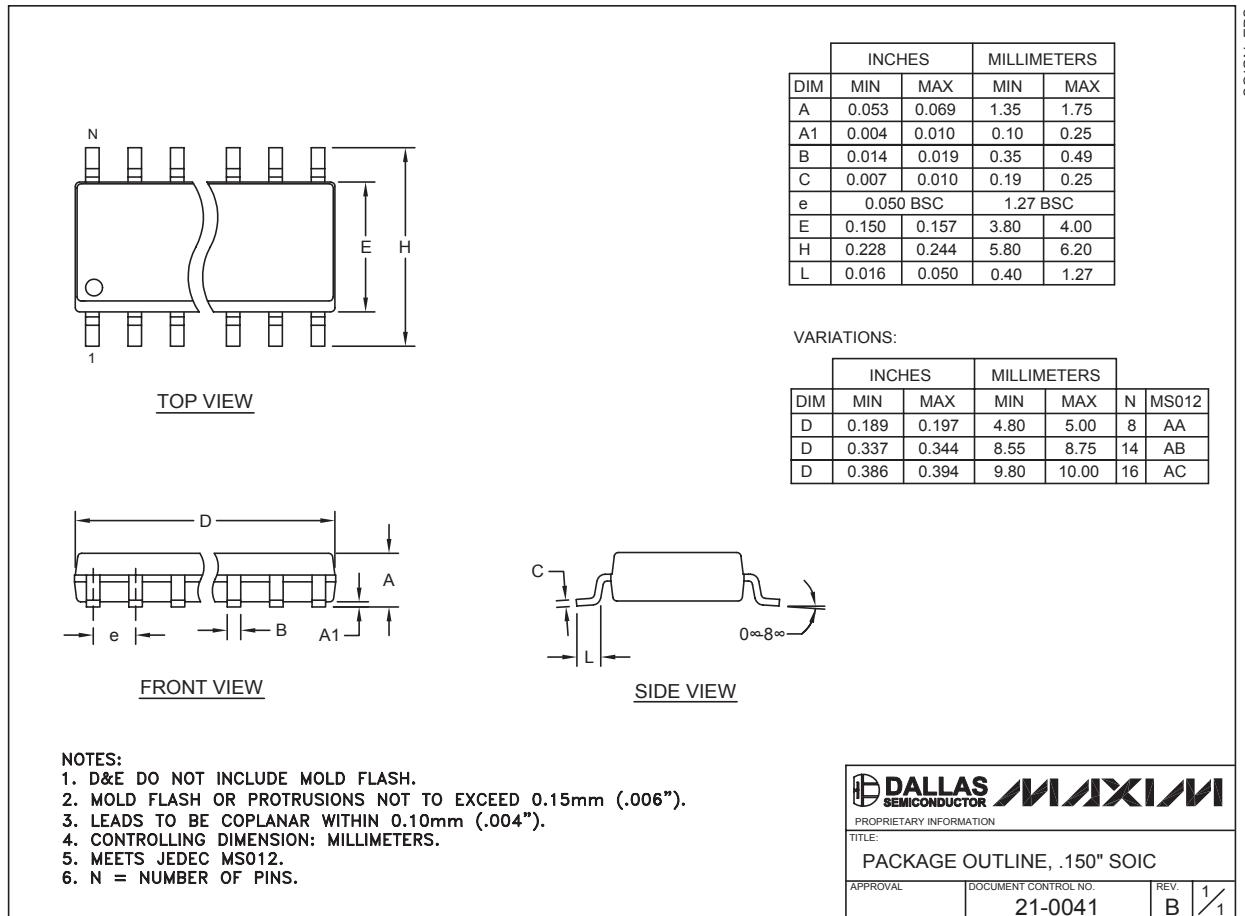


Figure 2. Protection against Fault Conditions

# Quad SPST CMOS Analog Switches

## Package Information

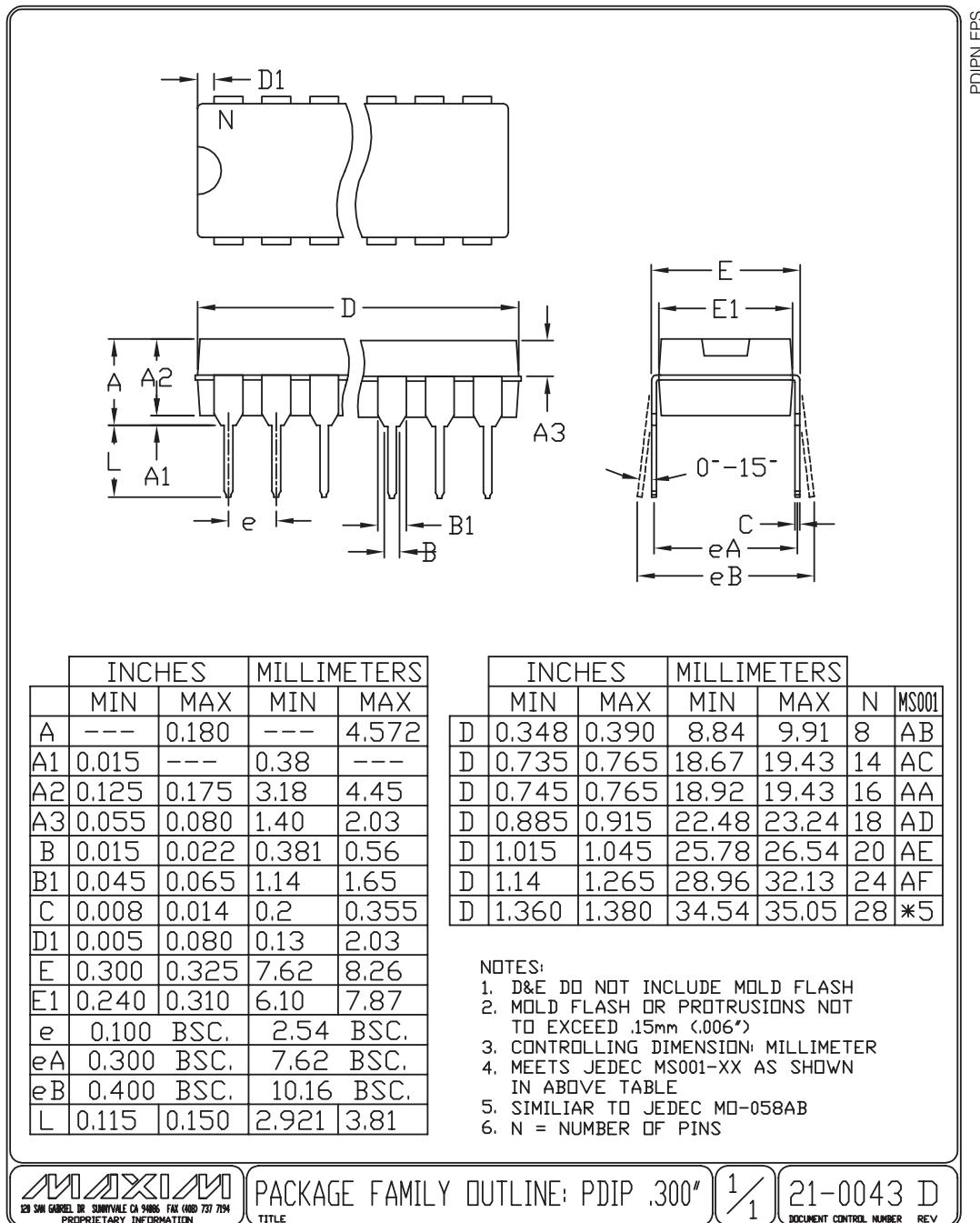
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



# Quad SPST CMOS Analog Switches

## Package Information (continued)

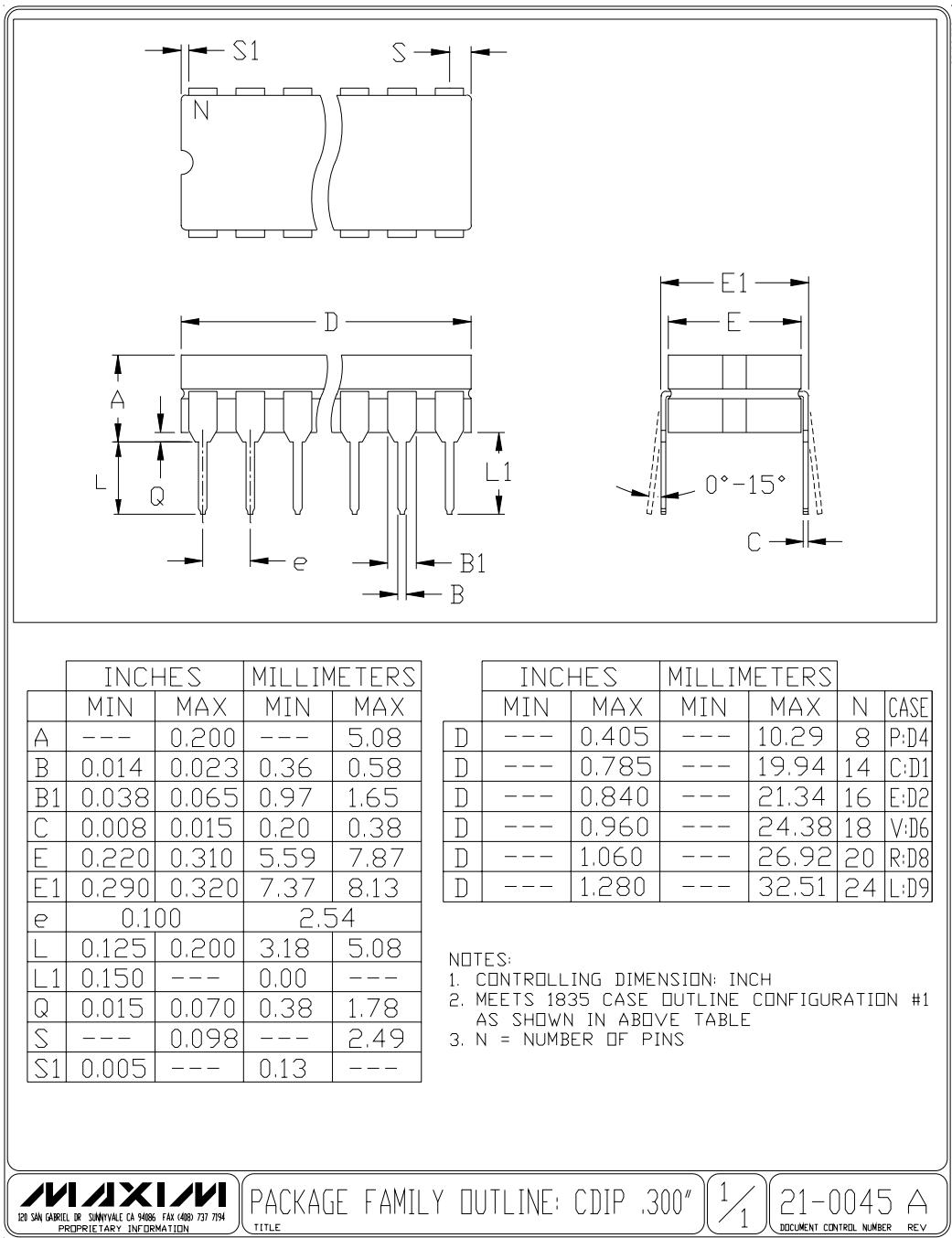
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# Quad SPST CMOS Analog Switches

## Package Information (continued)

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120 SAN GABRIEL DR. SUNNYVALE CA 94086 FAX (408) 737 7794  
PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: CDIP .300"  
TITLE

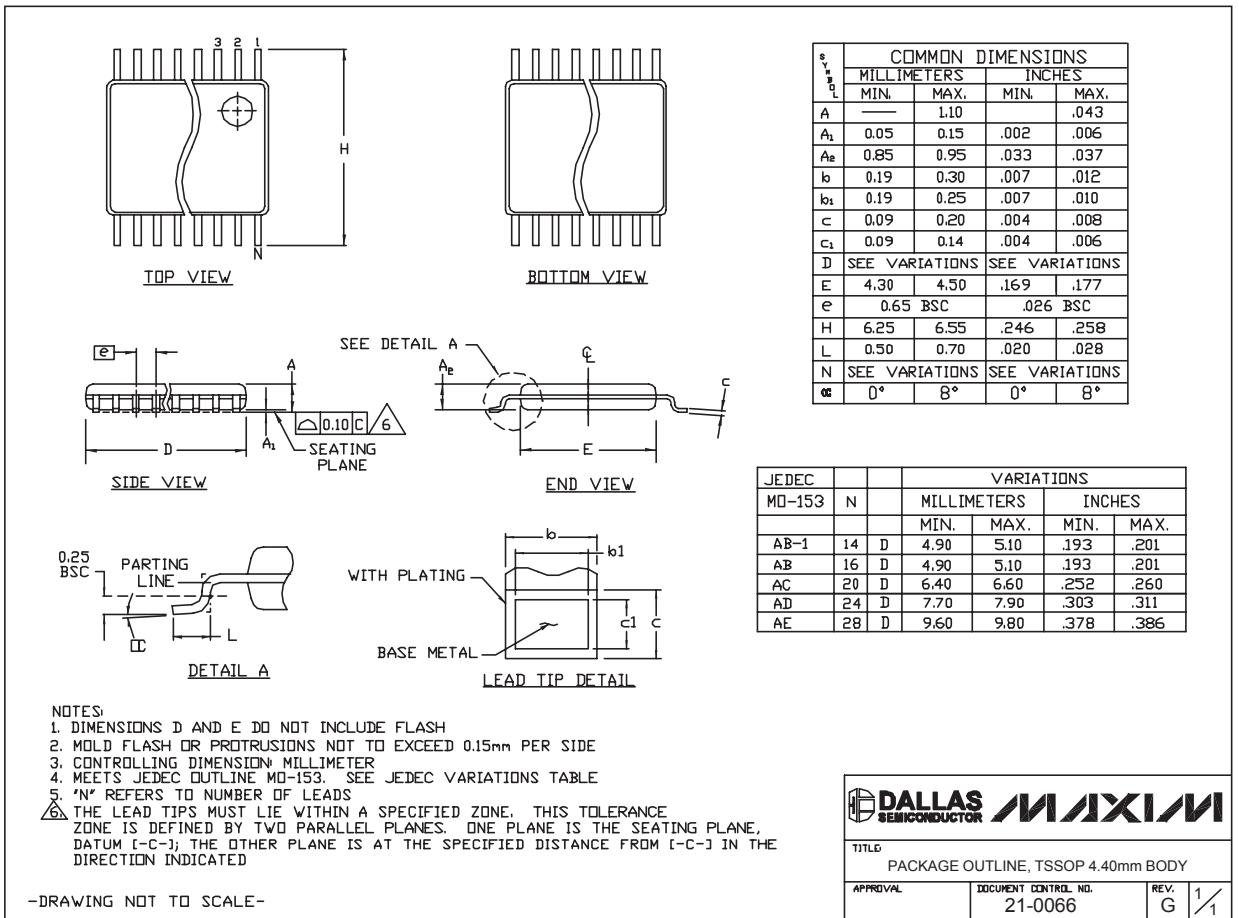
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DOCUMENT CONTROL NUMBER REV

# Quad SPST CMOS Analog Switches

## Package Information (continued)

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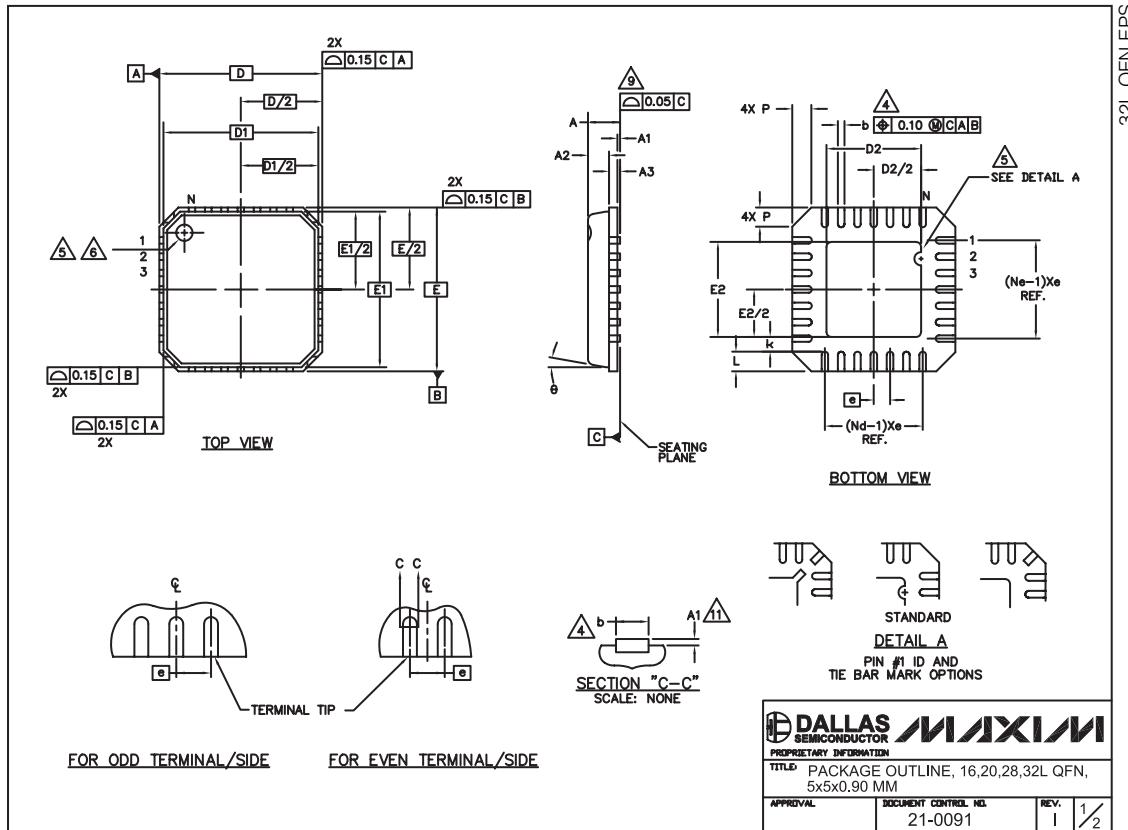


TSSOP4.40mm.EPS

# Quad SPST CMOS Analog Switches

## Package Information (continued)

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# Quad SPST CMOS Analog Switches

## Package Information (continued)

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COMMON DIMENSIONS												
PKG	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.									
A	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00
A3	0.20 REF											
b	0.28	0.33	0.40	0.23	0.28	0.35	0.18	0.23	0.30	0.18	0.23	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
D1	4.75 BSC											
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E1	4.75 BSC											
e	0.80 BSC			0.65 BSC			0.50 BSC			0.50 BSC		
k	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—
L	0.35	0.55	0.75	0.35	0.55	0.75	0.35	0.55	0.75	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
P	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60
θ	0°	12°	0°	12°	0°	12°	0°	12°	0°	12°	0°	12°

EXPOSED PAD VARIATIONS												
PKG CODES	D2			E2			MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.						
G1655-3	2.95	3.10	3.25	2.95	3.10	3.25						
G2055-1	2.55	2.70	2.85	2.55	2.70	2.85						
G2055-2	2.95	3.10	3.25	2.95	3.10	3.25						
G2855-1	2.55	2.70	2.85	2.55	2.70	2.85						
G2855-2	2.95	3.10	3.25	2.95	3.10	3.25						
G3255-1	2.95	3.10	3.25	2.95	3.10	3.25						

<b>DALLAS SEMICONDUCTOR</b> <small>PROPRIETARY INFORMATION</small>	<b>MAXIM</b>		
	TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM		
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0091	1 / 2	

### NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.  
 Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & N IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220; EXCEPT DIMENSION "b".
11. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
12. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES).

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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