TAIWAN SEMICONDUCTOR

TESDA5V0A

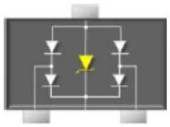
Low Capacitance ESD Protection Array

Small Signal Product

Features

SOT-23

◇ Meet IEC61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
◇ Meet IEC61000-4-4 (EFT) rating. 40A (5/50ns)
◇ Meet IEC61000-4-5 (Lightning) rating. 12A (8/20μs)
◇ Protects two directional I/O lines
◇ Working voltage : 5V
◇ Pb free version, RoHS compliant, and Halogn free
◇ Low leakage current



Mechanical Data

◇ Case : JEDEC SOT-23 standard package, molded plastic
◇ Terminal : Matte tin plated, lead free, solderable per MIL-STD-202, method 202 guaranteed
◇ High temperature soldering guaranteed : 260°C/10s
◇ Weight : 8 milligrams (approximately)
◇ Marking code : Y D05

Applications

◇ USB Power & Data Line Protection
◇ Ethernet 10BaseT
◇ T1/E1 Secondary IC Side Protection
◇ ISDN S/T Interface
◇ WAN/LAN Equipment

Ordering Information

Part No.	Package	Packing	Packing code	Packing code (Green)	Marking	Manufacture code
TESDA5V0A	SOT-23	3K / 7" Reel	RF	RFG	U5C2	

Note : Detail please see "Ordering Information(detail, example)" below.

Maximum Ratings and Electrical Characteristics

Rating at 25 °C ambient temperature unless otherwise specified.

Maximum Ratings

Parameter	Symbol	Value	Units
Peak Pulse Power (tp=8/20μs waveform)	P_{PP}	87.5	W
ESD per IEC 61000-4-2 (Air)	V_{ESD}	± 15	KV
ESD per IEC 61000-4-2 (Contact)		± 15	
Junction and Storage Temperature Range	T_J , T_{STG}	-55 to +150	°C

Electrical Characteristics

Parameter		Symbol	Min	Max	Units
Reverse Stand-Off Voltage		V_{RWM}	-	5	V
Reverse Breakdown Voltage	I_R = 1 mA	$V_{(BR)}$	6	-	V
Reverse Leakage Current	V_R = 5 V	I_R	-	1	μA
Clamping Voltage	I_{PP} = 15 A	V_C	-	15	V
	I_{PP} = 3.5 A		-	25	
Junction Capacitance	V_R = 0 V , f = 1.0 MHz	C_J	0.8 (Typ.)		pF

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RATINGS AND CHARACTERISTIC CURVES

Fig. 1 Admissible Power Dissipation Curve

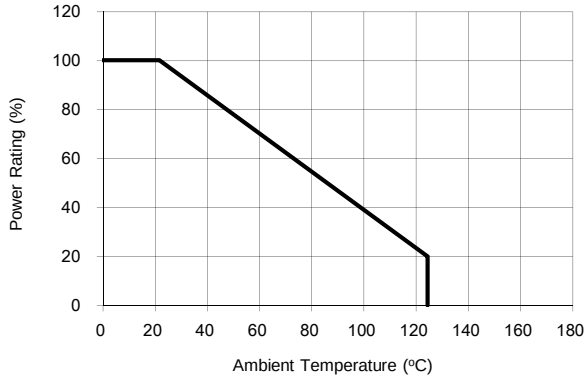


Fig. 2 Pulse Waveform

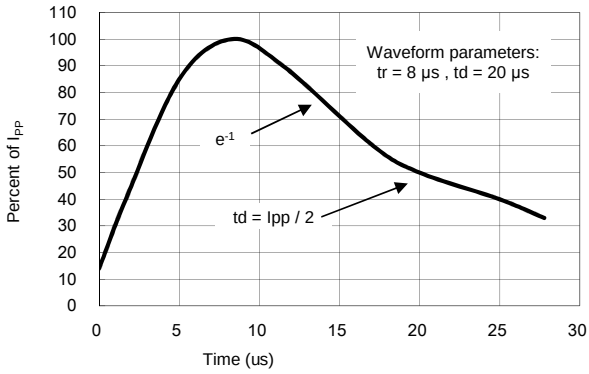


Fig. 3 Clamping Voltage VS. Peak Pulse Current

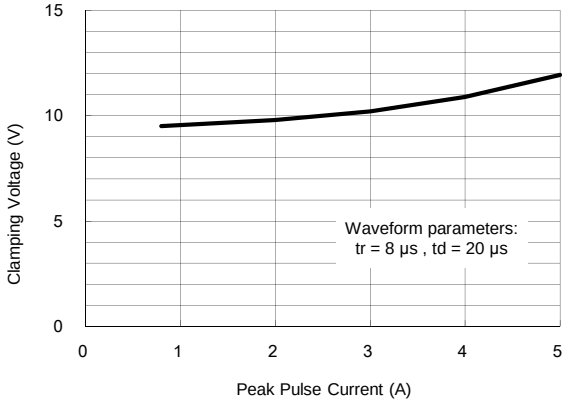
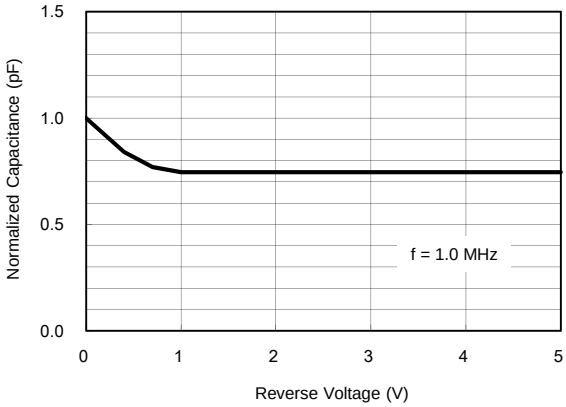


Fig. 4. Typical Junction Capacitance



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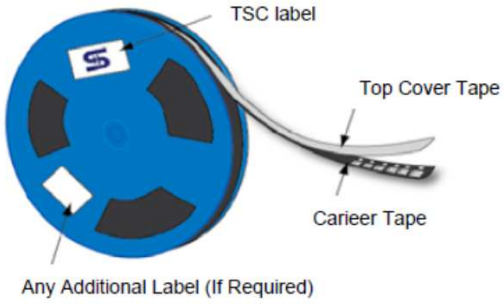
Ordering information (Detail, example)

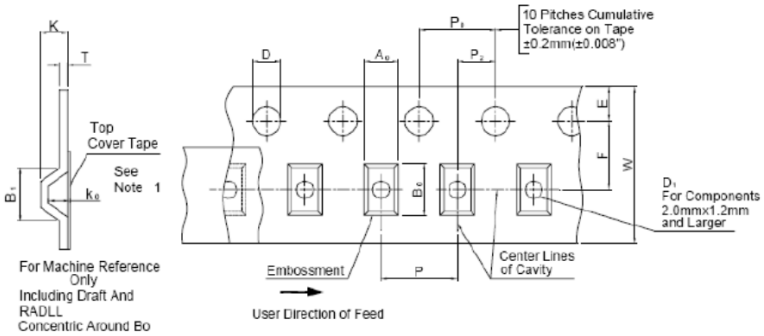
Part No.	Package	Packing	Packing code	Packing code (Green)	Marking	Manufacture code
TESDA5V0A	SOT-23	3K / 7" Reel	RF	RFG	U5C2	(Note)
TESDA5V0A	SOT-23	3K / 7" Reel	RF	RFG	U5C2	M0
TESDA5V0A	SOT-23	3K / 7" Reel	RF	RFG	U5C2	

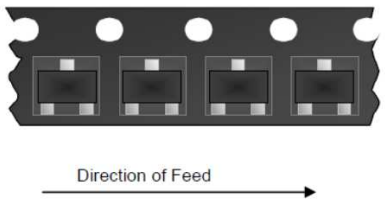
Note : Manufacture special control, if empty means no special control requirement.

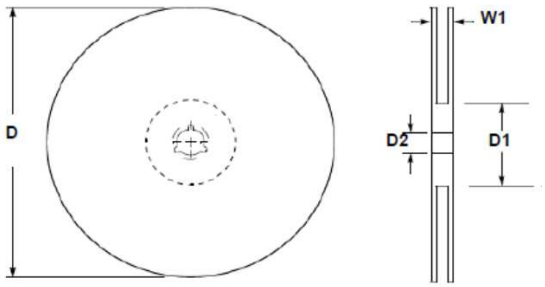
Tape & Reel specification



Item	Symbol	Dimension(mm)
Carrier depth	K	1.2 Max.
Sprocket hole	D	1.50 ± 0.10
Reel outside diameter	A	178 ± 1
Reel inner diameter	D1	50 Min.
Feed hole width	D2	13.0 ± 0.5
Sprocket hole position	E	1.75 ±0.10
Sprocket hole pitch	P0	4.00 ±0.10
Embossment center	P1	2.00 ±0.10
Overall tape thickness	T	0.6 Max.
Tape width	W	8.30 Max.
Reel width	W1	14.4 Max.







Note 1 : A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min. to 0.5 mm max. The component cannot rote more than 10^o within the determined cavity.

Note 2 : If B_1 exceeds 4.2mm(0.165") for 8 mm embossed tape, the tape may not feed through all tape f

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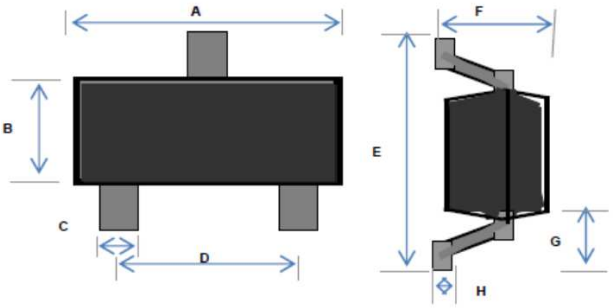
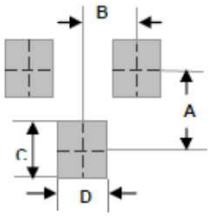
Dimensions



DIM.	Unit (mm)		Unit (inch)	
	Min	Max	Min	Max
A	2.70	3.10	0.106	0.122
B	1.10	1.50	0.043	0.059
C	0.30	0.51	0.012	0.020
D	1.78	2.04	0.070	0.080
E	2.10	2.64	0.083	0.104
F	0.89	1.30	0.035	0.051
G	0.55 REF		0.022 REF	
H	0.1 REF		0.004 REF	

Suggested PAD Layout



DIM.	Unit(mm)	Unit(inch)
	Typ.	Typ.
A	2.00	0.079
B	0.95	0.037
C	0.90	0.035
D	0.80	0.031

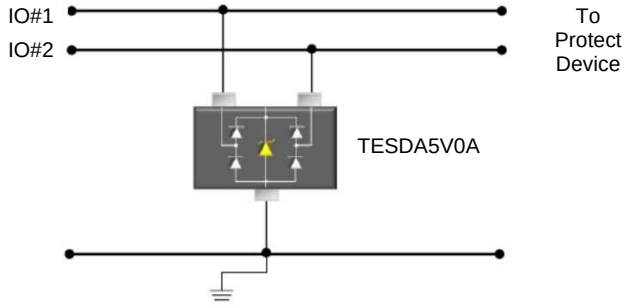
Notes : 1. The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application.

Applications Information

◇ Designed for the bi-directional protection of 2 lines form the damage caused by Electro Static Discharge (ESD) and surge pulses
◇ Be used on lines where the signal polarities are above and below ground
◇ Provides a surge capability of 350 Watts peak Ppp per line for an 8/20 ms waveform

Circuit Board Layout Recommendations

◇ Place the ESD Protection array as close to the input terminal or connector as possible
◇ Keep parallel signal paths to a minimum
◇ Minimize all printed-circuit board conductive loops including power and group loops
◇ Advoid using shared transient return paths to a common ground point
◇ Ground planes should be used. For multilayer printed-circuit boards, use ground vias
◇ Below picture is the typical application for bi-directional protection of two lines



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