

N-Channel Power MOSFET

60V, 38A, 17mΩ

FEATURES

- 100% avalanche tested
- Suitable for 5V drive applications
- Pb-free plating
- RoHS compliant
- Halogen-free mold compound

KEY PERFORMANCE PARAMETERS

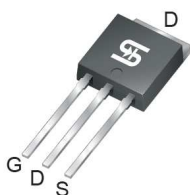
PARAMETER		VALUE	UNIT
V_{DS}		60	V
$R_{DS(on)}$ (max)	$V_{GS}=10V$	17	mΩ
	$V_{GS}=4.5V$	20	
Q_g		15	nC

APPLICATION

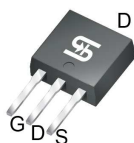
- SMPS Synchronous Rectification
- Networking DC-DC Power System



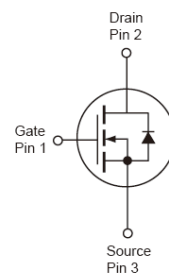
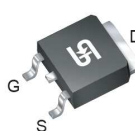
TO-251 (IPAK)



TO-251S (IPAK SL)



TO-252 (DPAK)


Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current (Note 1)	$T_C = 25^\circ\text{C}$	I_D	38	A
	$T_C = 100^\circ\text{C}$		24	
Pulsed Drain Current (Note 2)		I_{DM}	152	A
Single Pulsed Avalanche Energy (Note 3)		E_{AS}	20	mJ
Single Pulsed Avalanche Current (Note 3)		I_{AS}	20	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$		P_{DTOT}	46	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	2.7	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62	$^\circ\text{C/W}$

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air

ELECTRICAL SPECIFICATIONS (T _A = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static ^(Note 4)						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	BV _{DSS}	60	--	--	V
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250uA	V _{GS(TH)}	1.2	1.7	2.5	V
Gate Body Leakage	V _{GS} = ±20V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V _{DS} = 60V, V _{GS} = 0V	I _{DSS}	--	--	1	μA
	V _{DS} = 48V, V _{GS} = 0V, T _J = 125°C		--	--	10	
Drain-Source On-State Resistance	V _{GS} = 10V, I _D = 20A	R _{DS(ON)}	--	15	17	mΩ
	V _{GS} = 4.5V, I _D = 10A		--	17.5	20	
Dynamic ^(Note 5)						
Total Gate Charge	V _{DS} = 30V, I _D = 10A, V _{GS} = 4.5V	Q _g	--	15	--	nC
Gate-Source Charge		Q _{gs}	--	5.5	--	
Gate-Drain Charge		Q _{gd}	--	5	--	
Input Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	900	--	pF
Output Capacitance		C _{oss}	--	130	--	
Reverse Transfer Capacitance		C _{rss}	--	90	--	
Gate Resistance	F = 1MHz, open drain	R _g	--	2.2	--	Ω
Switching ^(Note 6)						
Turn-On Delay Time	V _{GS} = 10V, V _{DS} = 15V, R _G = 6Ω, I _D = 1A	t _{d(on)}	--	8.6	--	ns
Turn-On Rise Time		t _r	--	24.2	--	
Turn-Off Delay Time		t _{d(off)}	--	32.3	--	
Turn-Off Fall Time		t _f	--	7.9	--	
Source-Drain Diode ^(Note 4)						
Diode Forward Voltage	V _{GS} =0V, I _S =10A	V _{SD}	--	--	1	V
Reverse Recovery Time	V _{GS} = 0V, I _S = 10A	t _{rr}	--	18	--	ns
Reverse Recovery Charge	dl _F /dt = 100A/μs	Q _{rr}	--	10	--	nC

Notes:

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3. $L = 0.1\text{mH}, I_{AS} = 20A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
4. Pulse test: $PW \leq 300\mu s$, duty cycle $\leq 2\%$
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM170N06CP ROG	TO-252(DPAK)	2,500pcs / 13" Reel
TSM170N06CH C5G	TO-251(IPAK)	75pcs / Tube
TSM170N06CH X0G	TO-251S(IPAK SL)	75pcs / Tube

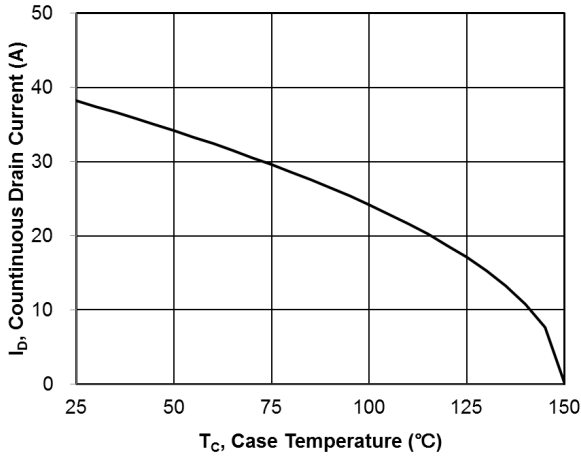
Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

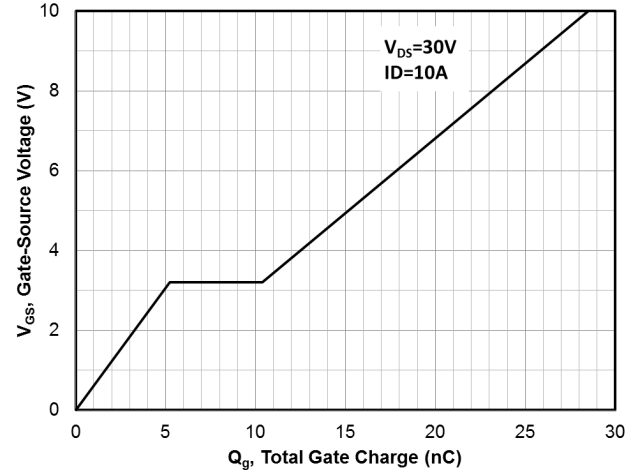
CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

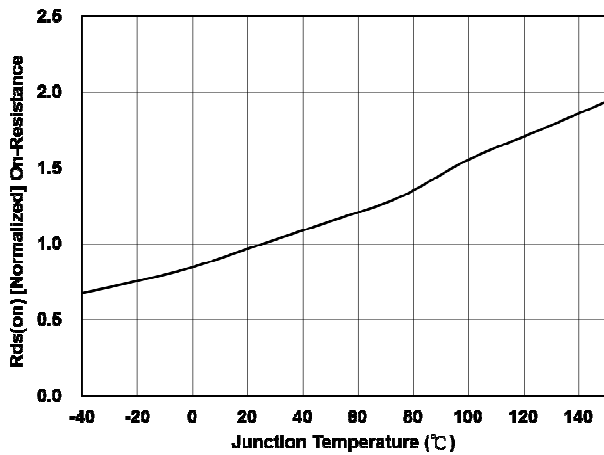
Continuous Drain Current vs. T_C



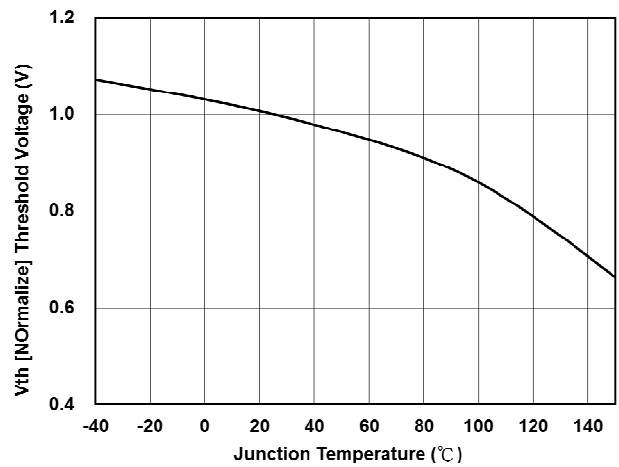
Gate Charge



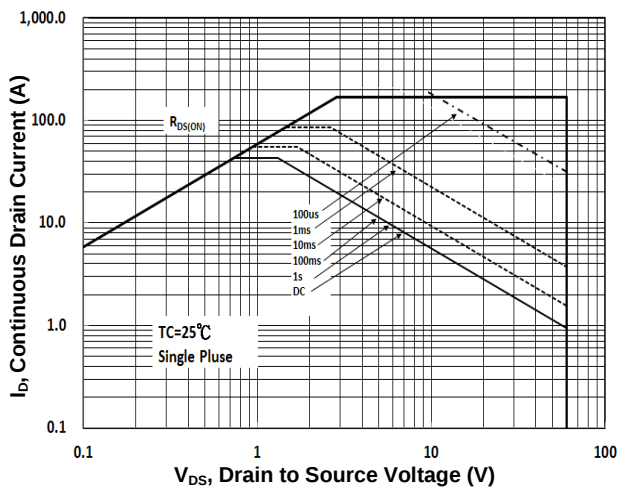
On-Resistance vs. Junction Temperature



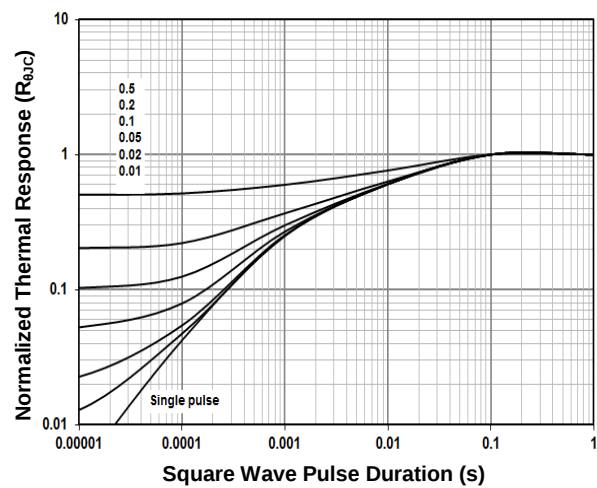
Threshold Voltage vs. Junction Temperature



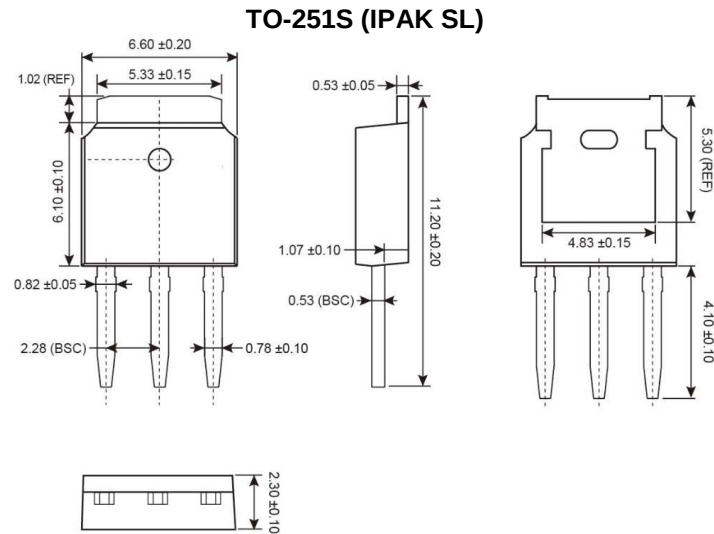
Maximum Safe Operating Area



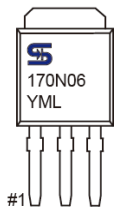
Normalized Thermal Transient Impedance Curve



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

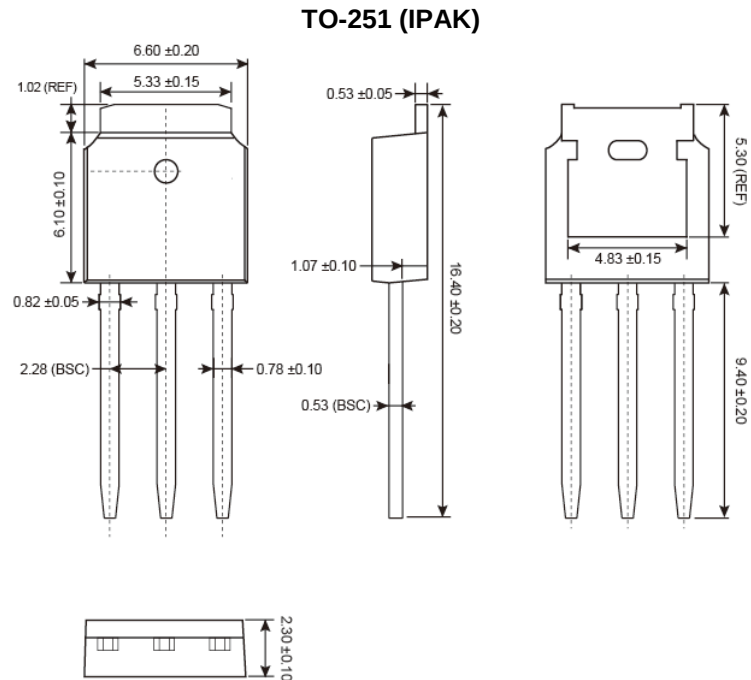


MARKING DIAGRAM

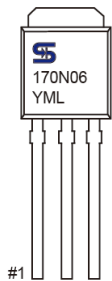


Y = Year Code
M = Month Code for Halogen Free Product
O =Jan **P** =Feb **Q** =Mar **R** =Apr
S =May **T** =Jun **U** =Jul **V** =Aug
W =Sep **X** =Oct **Y** =Nov **Z** =Dec
L = Lot Code (1~9, A~Z)

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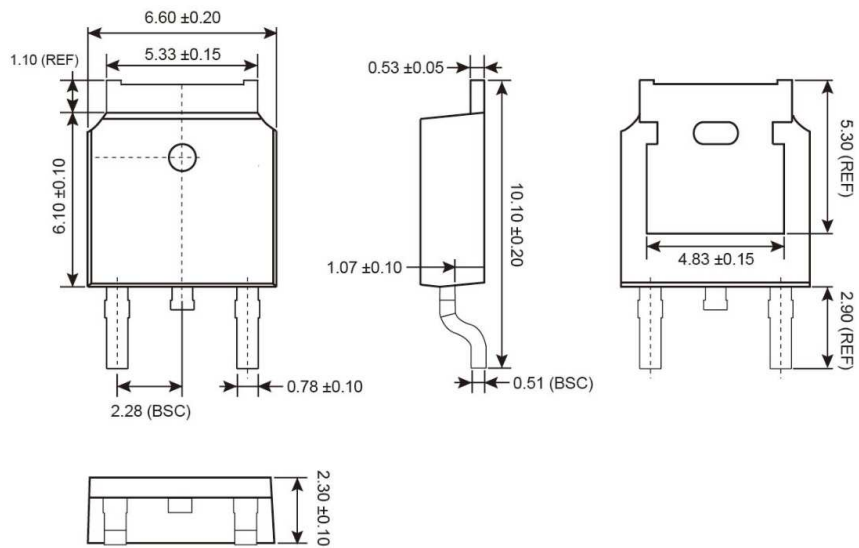
MARKING DIAGRAM



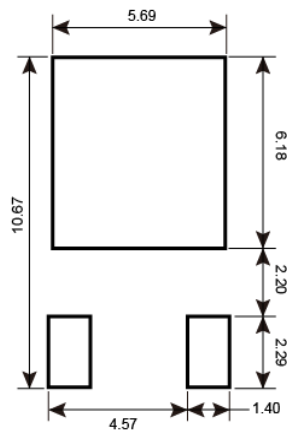
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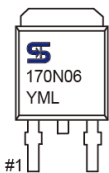
TO-252 (DPAK)



SUGGESTED PAD LAYOUT (Unit: Millimeters)



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