

16-Mbit (2M words × 8 bit) Static RAM with Error-Correcting Code (ECC)

Features

- High speed
 - $t_{AA} = 10 \text{ ns}$
- Embedded error-correcting code (ECC) for single-bit error correction
- Low active and standby currents
 - $I_{CC} = 90 \text{ mA}$ typical at 100 MHz
 - $I_{SB2} = 20 \text{ mA}$ typical
- Operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- ERR pin to indicate 1-bit error detection and correction
- Available in Pb-free 54-pin TSOP II, and 48-ball VFBGA packages

Functional Description

The CY7C1069G and CY7C1069GE are dual chip enable high-performance CMOS fast static RAM devices with embedded ECC. The CY7C1069G device is available in standard pin configurations. The CY7C1069GE device includes a single bit error indication pin (ERR) that signals the host

processor in the case of an ECC error-detection and correction event.

To write to the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable (WE) input LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{20}).

To read from the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins. See [Truth Table – CY7C1069G/CY7C1069GE on page 14](#) for a complete description of Read and Write modes. The input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and WE LOW).

On CY7C1069GE devices, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = High) ^[1].

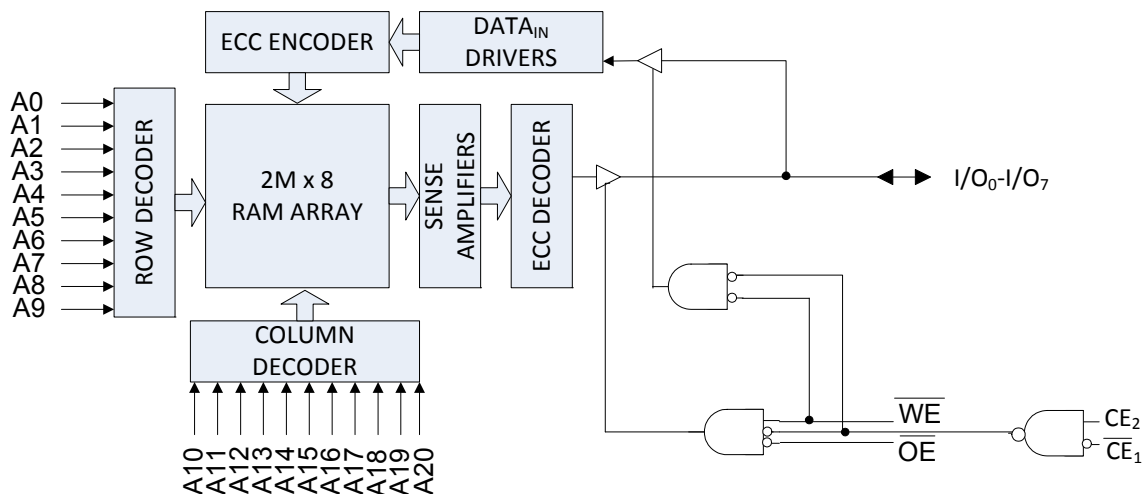
All I/Os (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), and control signals are de-asserted ($\overline{CE}_1$ / CE_2 , $\overline{OE}$, WE). CY7C1069G and CY7C1069GE devices are available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout, and in a 48-ball VFBGA package.

For a complete list of related documentation, [here](#).

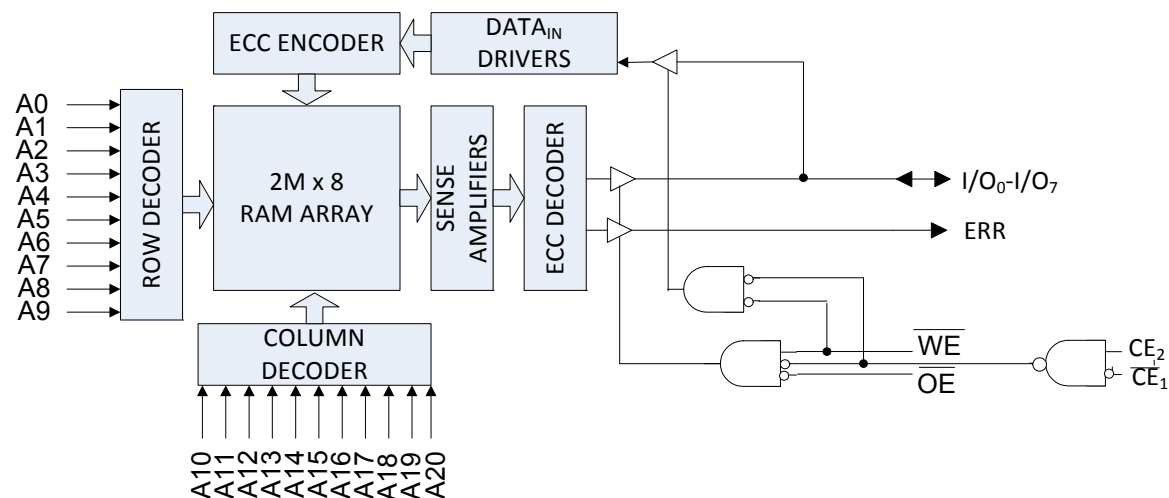
Note

1. Automatic write back on error detection feature is not supported in this device.

Logic Block Diagram – CY7C1069G



Logic Block Diagram – CY7C1069GE



Contents

Pin Configurations	4	Ordering Information	15
Product Portfolio	6	Ordering Code Definitions	15
Maximum Ratings	7	Package Diagrams	16
Operating Range	7	Acronyms	18
DC Electrical Characteristics	7	Document Conventions	18
Capacitance	8	Units of Measure	18
Thermal Resistance	8	Document History Page	19
AC Test Loads and Waveforms	8	Sales, Solutions, and Legal Information	20
Data Retention Characteristics	9	Worldwide Sales and Design Support	20
Data Retention Waveform	9	Products	20
AC Switching Characteristics	10	PSoC@Solutions	20
Switching Waveforms	11	Cypress Developer Community	20
Truth Table – CY7C1069G/CY7C1069GE	14	Technical Support	20
ERR Output – CY7C1069GE	14		

Pin Configurations

Figure 1. 54-pin TSOP II pinout (Top View) – CY7C1069G [2]

NC	1	54	NC
V _{CC}	2	53	V _{SS}
NC	3	52	NC
I/O ₆	4	51	I/O ₅
V _{SS}	5	50	V _{CC}
I/O ₇	6	49	I/O ₄
A ₄	7	48	A ₅
A ₃	8	47	A ₆
A ₂	9	46	A ₇
A ₁	10	45	A ₈
A ₀	11	44	A ₉
NC	12	43	NC
$\overline{CE}_1$	13	42	$\overline{OE}$
V _{CC}	14	41	V _{SS}
$\overline{WE}$	15	40	NC
CE ₂	16	39	A ₂₀
A ₁₉	17	38	A ₁₀
A ₁₈	18	37	A ₁₁
A ₁₇	19	36	A ₁₂
A ₁₆	20	35	A ₁₃
A ₁₅	21	34	A ₁₄
I/O ₀	22	33	I/O ₃
V _{CC}	23	32	V _{SS}
I/O ₁	24	31	I/O ₂
NC	25	30	NC
V _{SS}	26	29	V _{CC}
NC	27	28	NC

Figure 2. 54-pin TSOP II pinout (Top View) – CY7C1069GE [2, 3]

NC	1	54	NC
V _{CC}	2	53	V _{SS}
NC	3	52	NC
I/O ₆	4	51	I/O ₅
V _{SS}	5	50	V _{CC}
I/O ₇	6	49	I/O ₄
A ₄	7	48	A ₅
A ₃	8	47	A ₆
A ₂	9	46	A ₇
A ₁	10	45	A ₈
A ₀	11	44	A ₉
NC	12	43	ERR
$\overline{CE}_1$	13	42	$\overline{OE}$
V _{CC}	14	41	V _{SS}
$\overline{WE}$	15	40	NC
CE ₂	16	39	A ₂₀
A ₁₉	17	38	A ₁₀
A ₁₈	18	37	A ₁₁
A ₁₇	19	36	A ₁₂
A ₁₆	20	35	A ₁₃
A ₁₅	21	34	A ₁₄
I/O ₀	22	33	I/O ₃
V _{CC}	23	32	V _{SS}
I/O ₁	24	31	I/O ₂
NC	25	30	NC
V _{SS}	26	29	V _{CC}
NC	27	28	NC

Note

2. NC pins are not connected on the die.
3. ERR is an Output pin. If not used, this pin should be left floating.

Pin Configurations (continued)

Figure 3. 48-ball VFBGA pinout (Top View) – CY7C1069G ^[4]

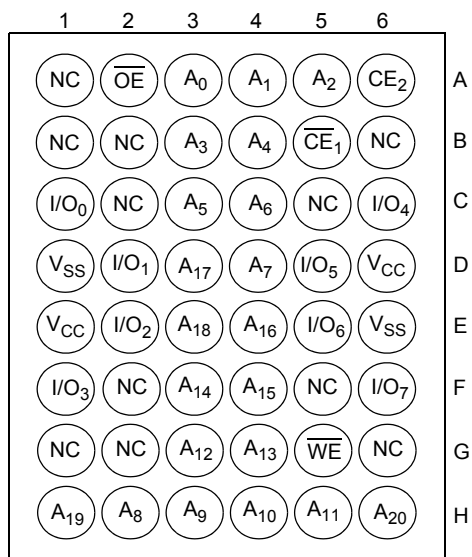
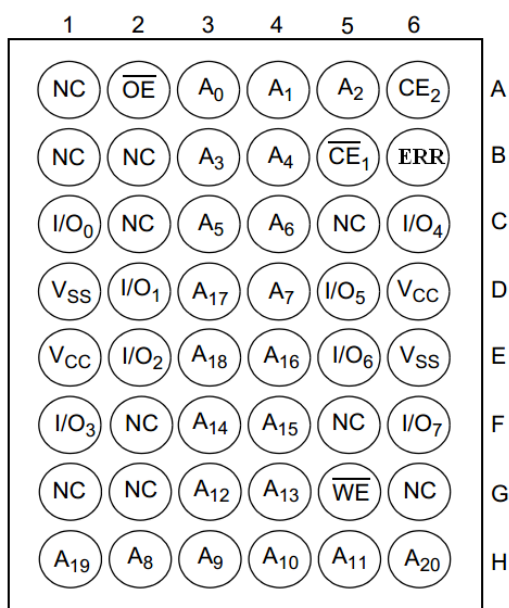


Figure 4. 48-ball VFBGA pinout (Top View) – CY7C1069GE ^[4, 5]



Note

4. NC pins are not connected on the die.
5. ERR is an Output pin. If not used, this pin should be left floating.

Product Portfolio

Product	Features and Options (see the Pin Configurations section)	Range	V _{CC} Range (V)	Speed (ns)	Power Dissipation			
					Operating I _{CC} , (mA)		Standby, I _{SB2} (mA)	
					f = f _{max}			
					Typ ^[6]	Max	Typ ^[6]	Max
CY7C1069G18	Dual-chip enable	Industrial	1.65 V–2.2 V	15	70	80	20	30
CY7C1069G30			2.2 V–3.6 V	10	90	110		
CY7C1069G			4.5 V–5.5 V	10	90	110		
CY7C1069GE18	Dual-chip enable and ERR output		1.65 V–2.2 V	15	70	80		
CY7C1069GE30			2.2 V–3.6 V	10	90	110		
CY7C1069GE			4.5 V–5.5 V	10	90	110		

Notes

6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature
with power applied -55 °C to +125 °C

Supply voltage
on V_{CC} relative to GND -0.5 V to +6.0 V

DC voltage applied to outputs
in High Z State ^[7] -0.5 V to $V_{CC} + 0.5$ V

DC input voltage ^[7] -0.5 V to $V_{CC} + 0.5$ V

Current into outputs (LOW) 20 mA

Static Discharge Voltage
(MIL-STD-883, Method 3015) > 2001 V

Latch up current > 140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Industrial	-40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

DC Electrical Characteristics

Over the Operating Range of -40 °C to 85 °C

Parameter	Description	Test Conditions	10 ns / 15 ns			Unit
			Min	Typ ^[8]	Max	
V_{OH}	Output HIGH voltage	1.65 V to 2.2 V $V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$	1.4	—	—	V
		2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OH} = -1.0 \text{ mA}$	2.0	—	—	
		2.7 V to 3.0 V $V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.2	—	—	
		3.0 V to 3.6 V $V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	—	—	
		4.5 V to 5.5 V $V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	—	—	
		4.5 V to 5.5 V $V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$	$V_{CC} - 0.4$ ^[9]	—	—	
V_{OL}	Output LOW voltage	1.65 V to 2.2 V $V_{CC} = \text{Min}, I_{OL} = 0.1 \text{ mA}$	—	—	0.2	V
		2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OL} = 2 \text{ mA}$	—	—	0.4	
		2.7 V to 3.6 V $V_{CC} = \text{Min}, I_{OL} = 8 \text{ mA}$	—	—	0.4	
		4.5 V to 5.5 V $V_{CC} = \text{Min}, I_{OL} = 8 \text{ mA}$	—	—	0.4	
V_{IH}	Input HIGH voltage	1.65 V to 2.2 V —	1.4	—	$V_{CC} + 0.2$	V
		2.2 V to 2.7 V —	2.0	—	$V_{CC} + 0.3$	
		2.7 V to 3.6 V —	2.0	—	$V_{CC} + 0.3$	
		4.5 V to 5.5 V —	2.0	—	$V_{CC} + 0.5$	
V_{IL}	Input LOW voltage ^[7]	1.65 V to 2.2 V —	-0.2	—	0.4	V
		2.2 V to 2.7 V —	-0.3	—	0.6	
		2.7 V to 3.6 V —	-0.3	—	0.8	
		4.5 V to 5.5 V —	-0.5	—	0.8	
I_{IX}	Input leakage current	$GND \leq V_{IN} \leq V_{CC}$	-1.0	—	+1.0	μA
I_{OZ}	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$, Output disabled	-1.0	—	+1.0	μA
I_{CC}	Operating supply current	$V_{CC} = \text{Max}, I_{OUT} = 0 \text{ mA}$, CMOS levels	—	90.0	110.0	mA
		$f = 100 \text{ MHz}$	—	70.0	80.0	
I_{SB1}	Automatic CE power down current – TTL inputs	$\text{Max } V_{CC}, \overline{CE} \geq V_{IH}$ ^[10] , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$	—	—	40.0	mA
I_{SB2}	Automatic CE power down current – CMOS inputs	$\text{Max } V_{CC}, \overline{CE} \geq V_{CC} - 0.2 \text{ V}$ ^[10] , $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, $f = 0$	—	20.0 ^[8]	30.0	mA

Notes

7. $V_{IL(\text{min})} = -2.0 \text{ V}$ and $V_{IH(\text{max})} = V_{CC} + 2 \text{ V}$ for pulse durations of less than 20 ns.

8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = 1.8 \text{ V}$ (for V_{CC} range of 1.65 V–2.2 V), $V_{CC} = 3 \text{ V}$ (for V_{CC} range of 2.2 V–3.6 V), and $V_{CC} = 5 \text{ V}$ (for V_{CC} range of 4.5 V–5.5 V), $T_A = 25 \text{ °C}$.

9. This parameter is guaranteed by design and is not tested.

10. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2 . When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.

Capacitance

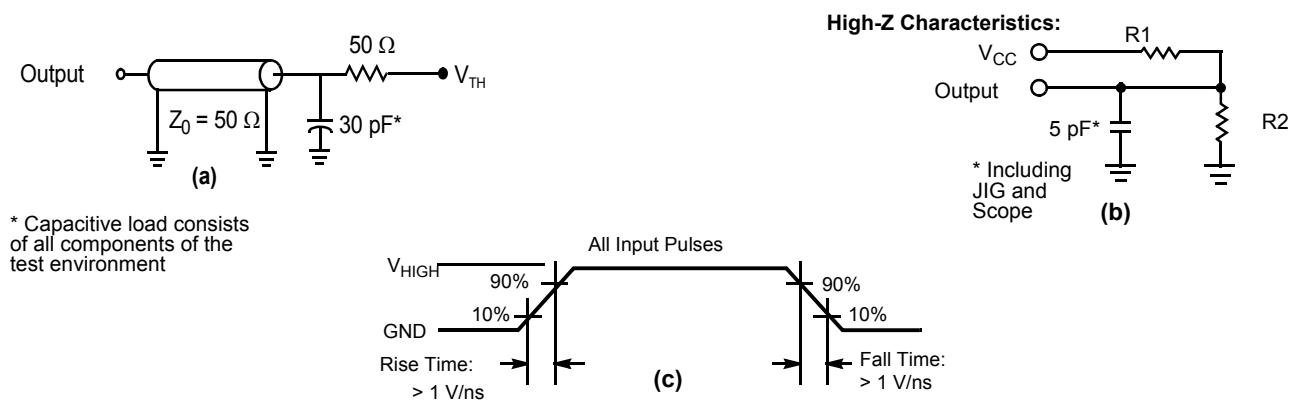
Parameter ^[11]	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	Unit
C_{IN}	Input capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC(\text{typ})}$	10	10	pF
C_{OUT}	I/O capacitance		10	10	pF

Thermal Resistance

Parameter ^[11]	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	93.63	31.50	$^\circ\text{C/W}$
Θ_{JC}	Thermal resistance (junction to case)		21.58	15.75	$^\circ\text{C/W}$

AC Test Loads and Waveforms

Figure 5. AC Test Loads and Waveforms^[12]



Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	Ω
R2	1538	351	351	Ω
V_{TH}	0.9	1.5	1.5	V
V_{HIGH}	1.8	3	3	V

Notes

11. Tested initially and after any design or process changes that may affect these parameters.

12. Full device AC operation assumes a 100- μs ramp time from 0 to $V_{CC(\text{min})}$ and 100- μs wait time after V_{CC} stabilization.

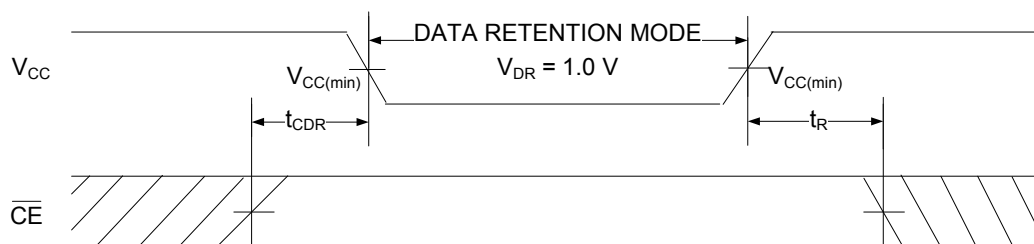
Data Retention Characteristics

Over the Operating Range of -40°C to 85°C

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention	–	1.0	–	V
I_{CCDR}	Data retention current	$V_{\text{CC}} = V_{\text{DR}}$, $\overline{\text{CE}} \geq V_{\text{CC}} - 0.2 \text{ V}$ ^[13] , $V_{\text{IN}} \geq V_{\text{CC}} - 0.2 \text{ V}$ or $V_{\text{IN}} \leq 0.2 \text{ V}$	–	30.0	mA
t_{CDR} ^[14]	Chip deselect to data retention time	–	0	–	ns
t_{R} ^[14, 15]	Operation recovery time	$V_{\text{CC}} \geq 2.2 \text{ V}$	10.0	–	ns
		$V_{\text{CC}} < 2.2 \text{ V}$	15.0	–	ns

Data Retention Waveform

Figure 6. Data Retention Waveform ^[13]



Notes

13. For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and CE_2 . When $\overline{\text{CE}}_1$ is LOW and CE_2 is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or CE_2 is LOW, $\overline{\text{CE}}$ is HIGH.
14. This parameter is guaranteed by design and is not tested.
15. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{\text{CC(min.)}} \geq 100 \mu\text{s}$ or stable at $V_{\text{CC(min.)}} \geq 100 \mu\text{s}$.

AC Switching Characteristics

Over the Operating Range of –40 °C to 85 °C

Parameter ^[16]	Description	10 ns		15 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t _{POWER}	V _{CC} stable to first access ^[17, 18]	100.0	–	100.0	–	μs
t _{RC}	Read cycle time	10.0	–	15.0	–	ns
t _{AA}	Address to data / ERR valid	–	10.0	–	15.0	ns
t _{OHA}	Data / ERR hold from address change	3.0	–	3.0	–	ns
t _{ACE}	CE LOW to data / ERR valid ^[19]	–	10.0	–	15.0	ns
t _{DOE}	OE LOW to data / ERR valid	–	5.0	–	8.0	ns
t _{LZOE}	OE LOW to low Z ^[20, 21, 22]	0	–	1.0	–	ns
t _{HZOE}	OE HIGH to high Z ^[20, 21, 22]	–	5.0	–	8.0	ns
t _{LZCE}	CE LOW to low Z ^[19, 20, 21, 22]	3.0	–	3.0	–	ns
t _{HZCE}	CE HIGH to high Z ^[19, 20, 21, 22]	–	5.0	–	8.0	ns
t _{PU}	CE LOW to power-up ^[18, 19]	0	–	0	–	ns
t _{PD}	CE HIGH to power-down ^[18, 19]	–	10.0	–	15.0	ns
Write Cycle ^[23, 24]						
t _{WC}	Write cycle time	10.0	–	15.0	–	ns
t _{SCE}	CE LOW to write end ^[19]	7.0	–	12.0	–	ns
t _{AW}	Address setup to write end	7.0	–	12.0	–	ns
t _{HA}	Address hold from write end	0	–	0	–	ns
t _{SA}	Address setup to write start	0	–	0	–	ns
t _{PWE}	WE pulse width	7.0	–	12.0	–	ns
t _{SD}	Data setup to write end	5.0	–	8.0	–	ns
t _{HD}	Data hold from write end	0	–	0	–	ns
t _{LZWE}	WE HIGH to low Z ^[20, 21, 22]	3.0	–	3.0	–	ns
t _{HZWE}	WE LOW to high Z ^[20, 21, 22]	–	5.0	–	8.0	ns

Notes

16. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for V_{CC} ≥ 3 V) and V_{CC}/2 (for V_{CC} < 3 V), and input pulse levels of 0 to 3 V (for V_{CC} ≥ 3 V) and 0 to V_{CC} (for V_{CC} < 3V). Test conditions for the read cycle use output loading shown in part (a) of Figure 5 on page 8, unless specified otherwise.
17. t_{POWER} gives minimum amount of time that the power supply is at stable V_{CC} until first memory access is performed.
18. These parameters are guaranteed by design and are not tested.
19. For all dual chip enable devices, CE is the logical combination of CE₁ and CE₂. When CE₁ is LOW and CE₂ is HIGH, CE is LOW; when CE₁ is HIGH or CE₂ is LOW, CE is HIGH.
20. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{LZOE}, t_{LZCE}, and t_{LZWE} are specified with a load capacitance of 5 pF as in (b) of Figure 5 on page 8. Transition is measured ±200 mV from steady state voltage.
21. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
22. Tested initially and after any design or process changes that may affect these parameters.
23. The internal write time of the memory is defined by the overlap of WE = V_{IL}, CE = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
24. The minimum write pulse width for write cycle No.2 (WE Controlled, OE LOW) should be sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 7. Read Cycle No. 1 of CY7C1069G (Address Transition Controlled) [25, 26]

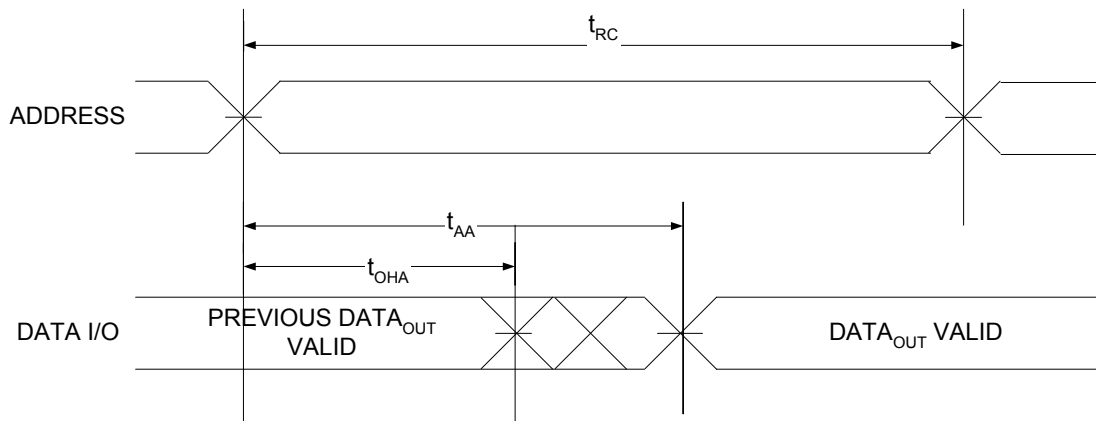
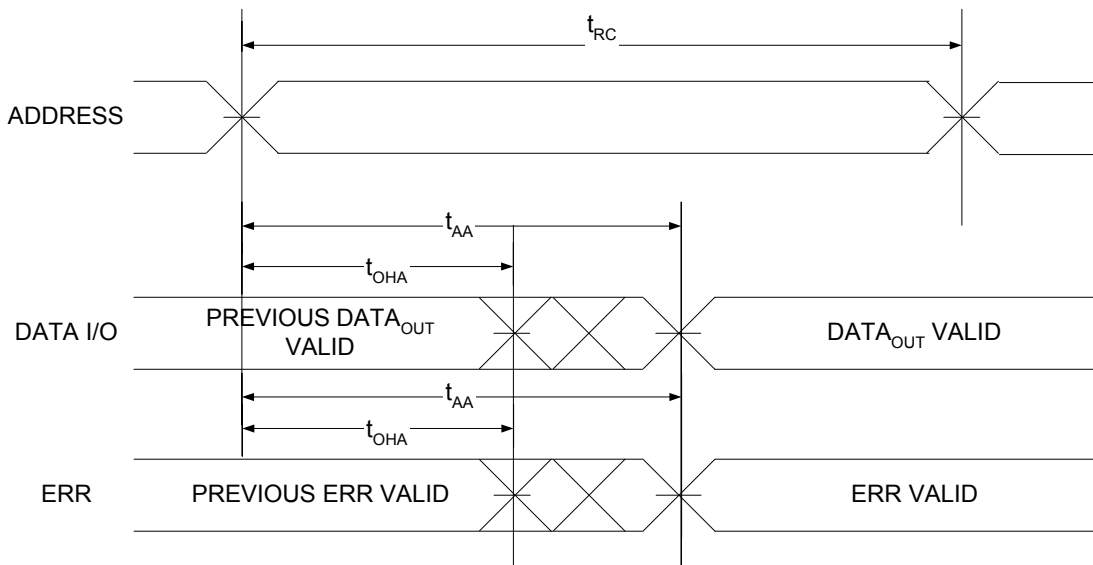


Figure 8. Read Cycle No. 2 of CY7C1069GE (Address Transition Controlled) [25, 26]

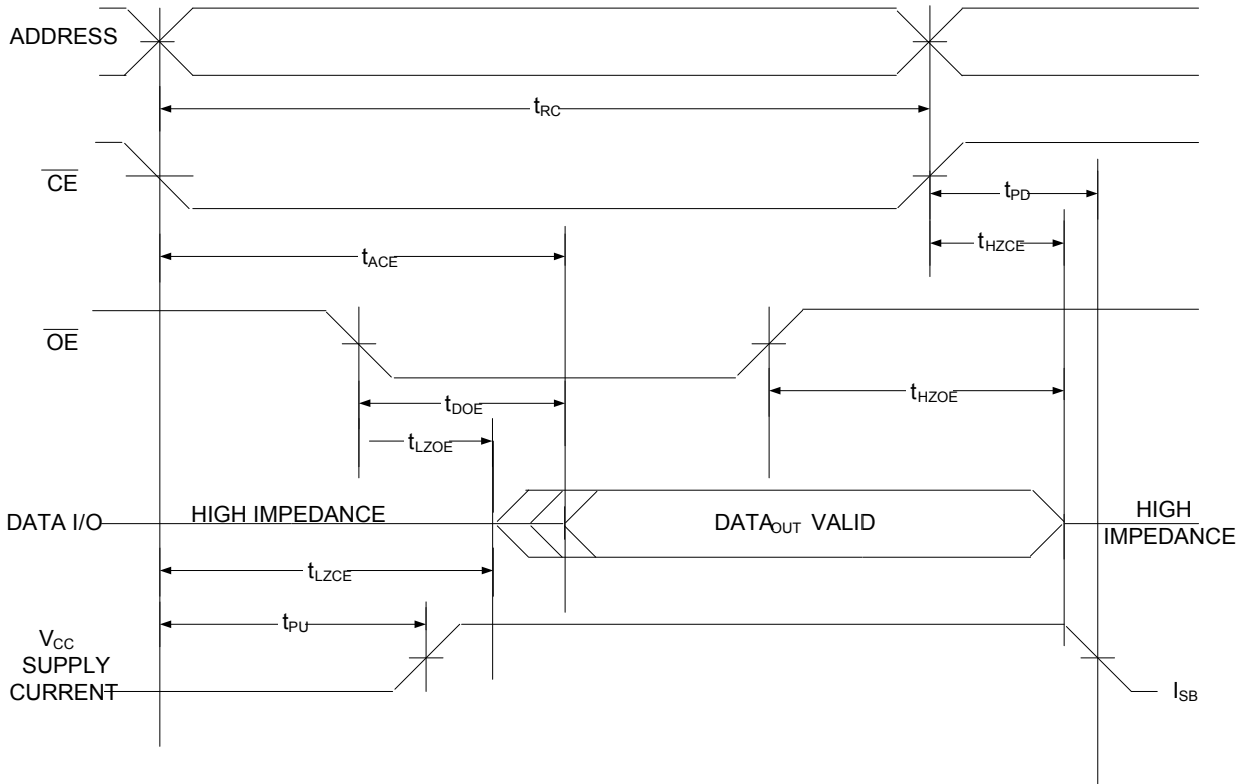


Notes

25. The device is continuously selected, $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$.
 26. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Figure 9. Read Cycle No. 3 ($\overline{\text{OE}}$ Controlled, $\overline{\text{WE}}$ HIGH) [27, 28, 29]



Notes

27. For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and CE_2 . When $\overline{\text{CE}}_1$ is LOW and CE_2 is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or CE_2 is LOW, $\overline{\text{CE}}$ is HIGH.

28. $\overline{\text{WE}}$ is HIGH for read cycle.

29. Address valid prior to or coincident with $\overline{\text{CE}}$ LOW transition.

Switching Waveforms (continued)

Figure 10. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [30, 31, 32]

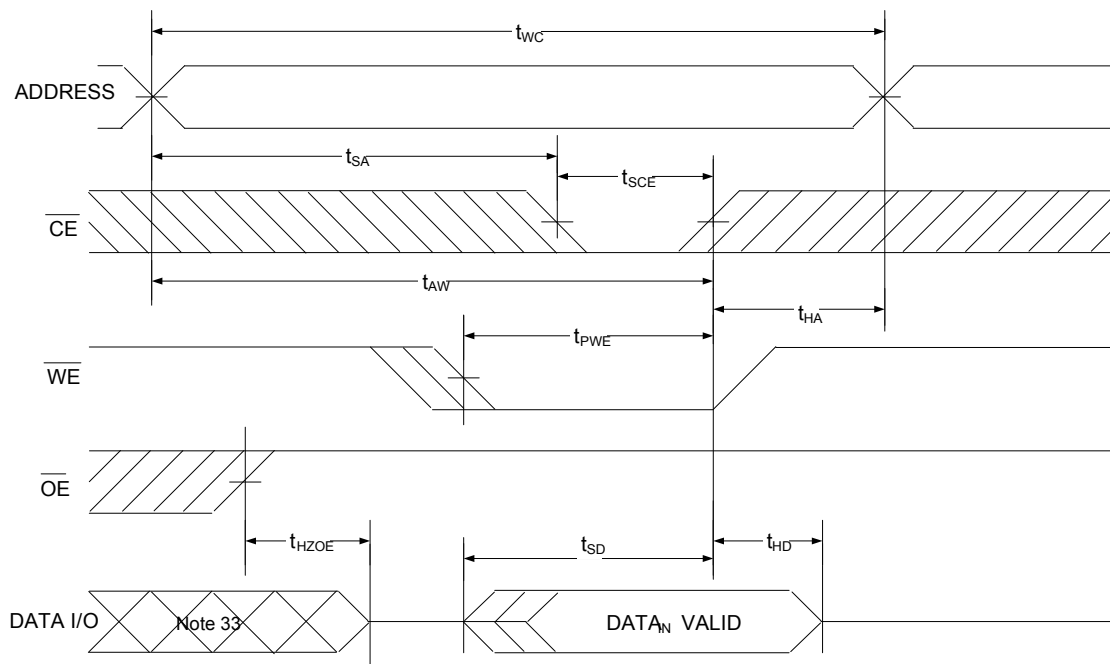
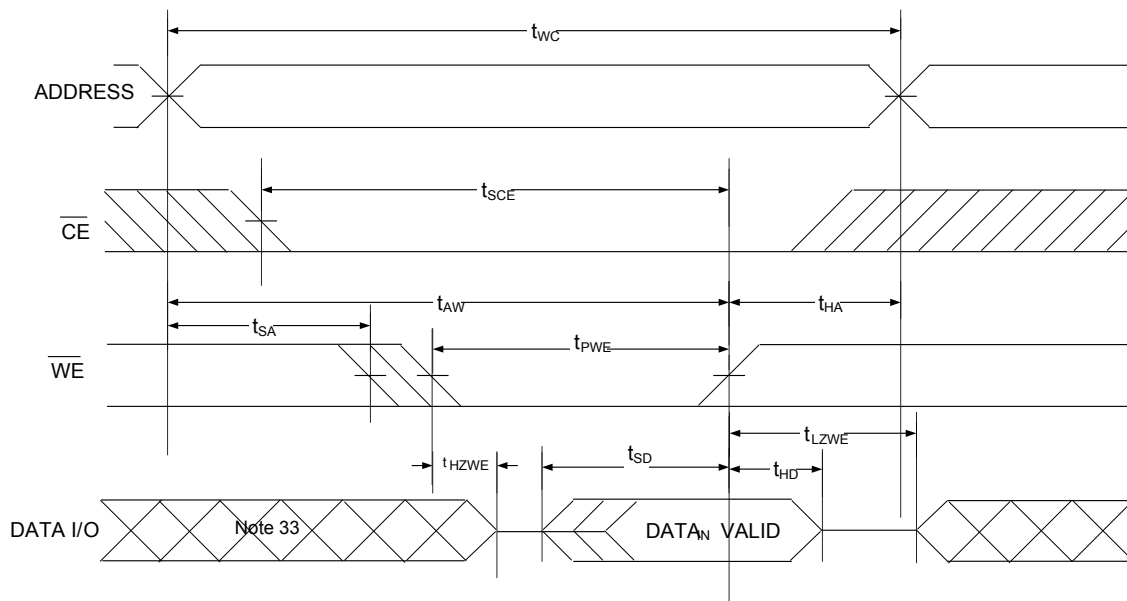


Figure 11. Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ Low) [30, 31, 32, 34]



Notes

30. For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and CE_2 . When $\overline{\text{CE}}_1$ is LOW and CE_2 is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or CE_2 is LOW, $\overline{\text{CE}}$ is HIGH.

31. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{IL}$, $\overline{\text{CE}} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

32. Data I/O is in high impedance state if $\overline{\text{CE}} = V_{IH}$, or $\overline{\text{OE}} = V_{IH}$.

33. During this time I/O are in output put state. Do not apply input signals.

34. The minimum write cycle width should be sum of t_{HZWE} and t_{SD} .

Truth Table – CY7C1069G/CY7C1069GE

$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O ₀ –I/O ₇	Mode	Power
H	X ^[35]	X ^[35]	X ^[35]	High Z	Power-down	Standby (I _{SB})
X ^[35]	L	X ^[35]	X ^[35]	High Z	Power-down	Standby (I _{SB})
L	H	L	H	Data out	Read all bits	Active (I _{CC})
L	H	X ^[35]	L	Data in	Write all bits	Active (I _{CC})
L	H	H	H	High Z	Selected, outputs disabled	Active (I _{CC})

ERR Output – CY7C1069GE

Output ^[36]	Mode
0	Read Operation, no single bit error in the stored data.
1	Read Operation, single bit error detected and corrected.
High Z	Device deselected or Outputs disabled or Write Operation

Note

35. The input voltage levels on these pins should be either at V_{IH} or V_{IL}.

36. ERR is an Output pin. If not used, this pin should be left floating.

Ordering Information

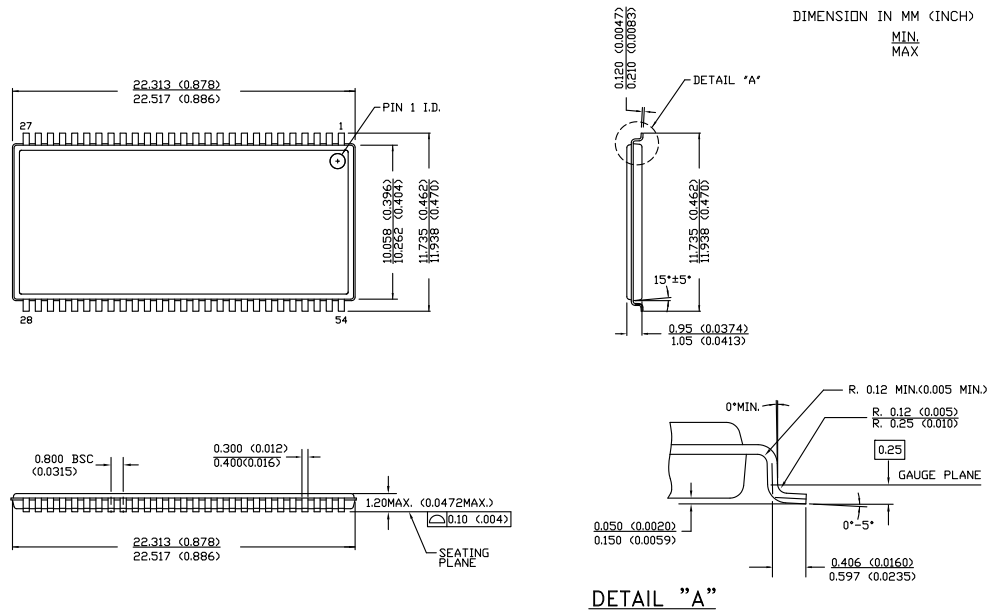
Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (All Pb-free)	ERR Pin / Ball	Operating Range
10	2.2 V–3.6 V	CY7C1069G30-10BVXI	51-85150	48-ball VFBGA	No	Industrial
		CY7C1069G30-10BVXIT	51-85150	48-ball VFBGA, Tape and Reel	No	
		CY7C1069G30-10ZSXI	51-85160	54-pin TSOP II	No	
		CY7C1069G30-10ZSXIT	51-85160	54-pin TSOP II, Tape and Reel	No	
		CY7C1069GE30-10ZSXI	51-85160	54-pin TSOP II	Yes	
		CY7C1069GE30-10ZSXIT	51-85160	54-pin TSOP II, Tape and Reel	Yes	
	4.5 V–5.5 V	CY7C1069G-10BVXI	51-85150	48-ball VFBGA	No	
		CY7C1069G-10BVXIT	51-85150	48-ball VFBGA, Tape and Reel	No	
		CY7C1069G-10ZSXI	51-85160	54-pin TSOP II	No	
		CY7C1069G-10ZSXIT	51-85160	54-pin TSOP II, Tape and Reel	No	

Ordering Code Definitions

CY	7	C	1	06	9	G	E	XX	-	XX	XX	X	I	X	
															X = blank or T blank = Bulk; T = Tape and Reel
															Temperature Range: I = Industrial
															Pb-free
															Package Type: XX = BV or ZS BV = 48-ball VFBGA; ZS = 54-pin TSOP II
															Speed: XX = 10 ns or 15 ns
															Voltage Range: 18 = 1.65 V–2.2 V; 30 = 2.2 V–3.6 V; no character = 4.5 V–5.5 V
															X = blank or E blank = without ERR output; E = with ERR output, single bit error indication
															Process Technology: G = ULL65, 65 nm
															Data Width: 9 = × 8-bits
															Density: 06 = 16-Mbit
															Family Code: 1 = Fast Asynchronous SRAM family
															Technology Code: C = CMOS
															Marketing Code: 7 = SRAM
															Company ID: CY = Cypress

Package Diagrams

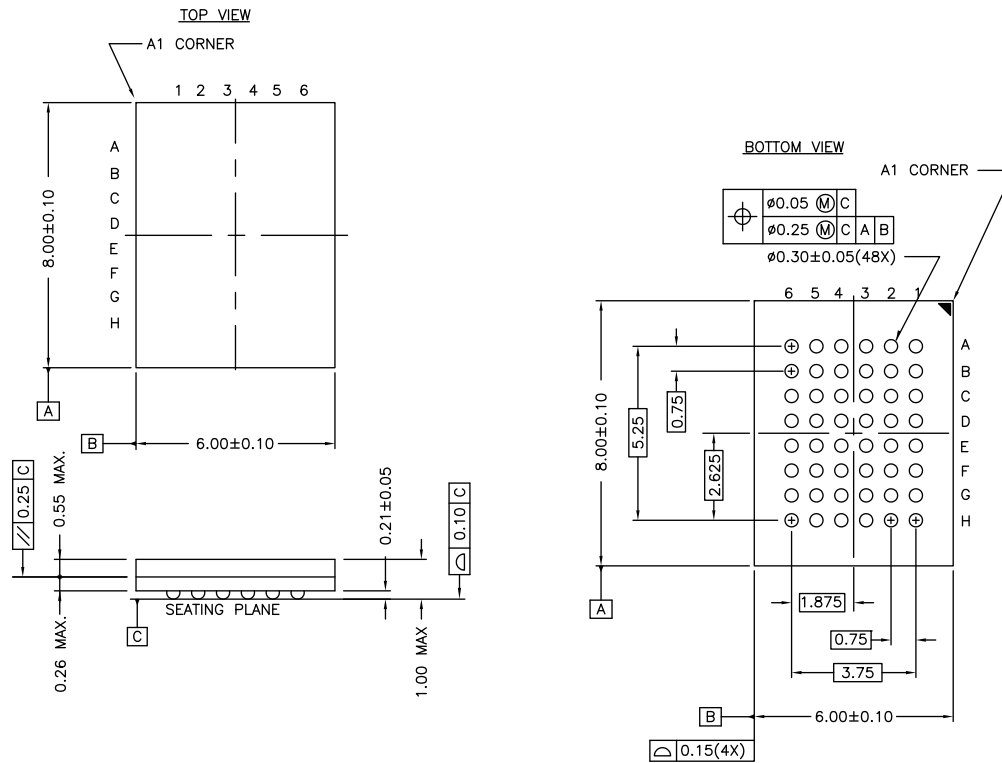
Figure 12. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Z54-II Package Outline, 51-85160



51-85160 *E

Package Diagrams (continued)

Figure 13. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:

PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Acronyms

Acronym	Description
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1069G/CY7C1069GE, 16-Mbit (2M words × 8 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-81539				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*H	4800609	NILE	07/31/2015	Changed status from Preliminary to Final.
*I	5436514	NILE	09/14/2016	Updated Maximum Ratings : Updated Note 7 (Replaced “2 ns” with “20 ns”). Updated DC Electrical Characteristics : Removed Operating Range “2.7 V to 3.6 V” and all values corresponding to V _{OH} parameter. Included Operating Ranges “2.7 V to 3.0 V” and “3.0 V to 3.6 V” and all values corresponding to V _{OH} parameter. Changed minimum value of V _{IH} parameter from 2.2 V to 2 V corresponding to Operating Range “4.5 V to 5.5 V”. Updated Ordering Information : Updated part numbers. Updated to new template.
*J	5984763	AESATMP9	12/05/2017	Updated logo and copyright.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6](#)

Cypress Developer Community

[Forums](#) | [WICED IOT Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2012-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9