# IQS266 Datasheet

## 2x3 Channel projected capacitive trackpad controller with self-capacitive wake-up

The IQS266 ProxSense® IC is a 2x3 projected capacitive trackpad designed for low power mobile applications. This trackpad is perfect to implement on a single sided ITO touch screen for wearables. A self-capacitive channel is used for wake-up which keeps the power consumption in low-power less than 5 uA. Other features include automatic tuning for sense electrodes, internal reference capacitor and internal regulator to reduce total system cost.

## Features

- **Capacitive sensing**
  - o Parasitic capacitive load cancellation
  - o Fully adjustable sensing options
  - o Self capacitive prox channel (CH0)
  - o 2x3 Projected capacitive trackpad (CH1-6)
- **Zoom and Low power options for minimal power consumption**
- **Multiple integrated UI** options based on years of experience in sensing on fixed and mobile platforms:
  - o **Proximity / Touch**
  - o **Proximity wake-up from low power** using distributed proximity channel
  - o **Gesture recognition**:
    - ▪ Swipes: Up, down, left, right (segment indication for left & right swipes)
    - ▪ Adjustable swipe length and time limitations
    - ▪ Taps: Single taps with segment indication
    - ▪ Adjustable tap size and time limitation
- **A**utomatic **T**uning **I**mplementation (**ATI**)
- Minimal external components
- Fast **I²C** compatible interface
- **RDY indication** for event mode operation
- **Event or Streaming mode**
- **Small package size: QFN(3x3)-16**
- **Supply voltage: 1.8V to 3.3V**

**RoHS compliant**

**QFN(3x3)-16 package**
Representation only
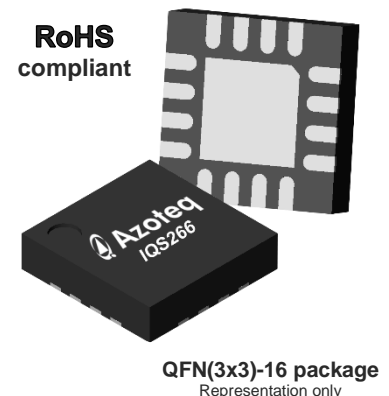
## Applications

- Wearables
- Navigational controls
- White goods and appliances
- Office equipment, toys, sanitary ware
- Proximity detection that enables backlighting activation (Patented)
- Wake-up from standby applications
- Replacement for electromechanical switches and keypads
- GUI trigger and GUI control proximity detection
- Electronic Keypads or Pin pads

| Available Packages | |
|---|---|
| T_A | QFN(3x3)-16 |
| -20°C to 85°C | IQS266 |

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# List of abbreviations

ATI      – Automatic Tuning Implementation

AC      – Alternating Current

ACF      – AC Filtered Counts

CH      – Channel

CS      – Sampling capacitor

CX      – Self capacitive electrode

I$^2$C      – Inter-Integrated Circuit

LTA      – Long Term Average

N/C      – Not connect

NM      – Normal Mode

LP      – Low Power

RX      – Receiving electrode

RDY      – Ready interrupt signal

SCL      – I$^2$C serial clock signal

SDA      – I$^2$C serial data signal

TX      – Transmitting electrode

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# 1 Introduction

## 1.1 Functional overview

The **IQS266** is a single self capacitive proximity and 6 channel projected trackpad sensor featuring an internal voltage regulator and reference capacitor ($C_S$).

The device has 6 pins for the connection of sense electrodes, which consist of 1 self electrode, for proximity wake-up, as well as 2 receivers and 3 transmitters, for a 2x3 trackpad. Three pins are used for serial data communication through the I²C™ compatible protocol, including an optional RDY pin.

The device automatically tracks slow varying environmental changes via various filters, detects swipe and tap gestures in various directions and segments on the trackpad. The device is equipped with an Automatic Tuning Implementation (ATI) to adjust the device for optimal sensitivity.

## 1.2 Packaging and Pin-Out
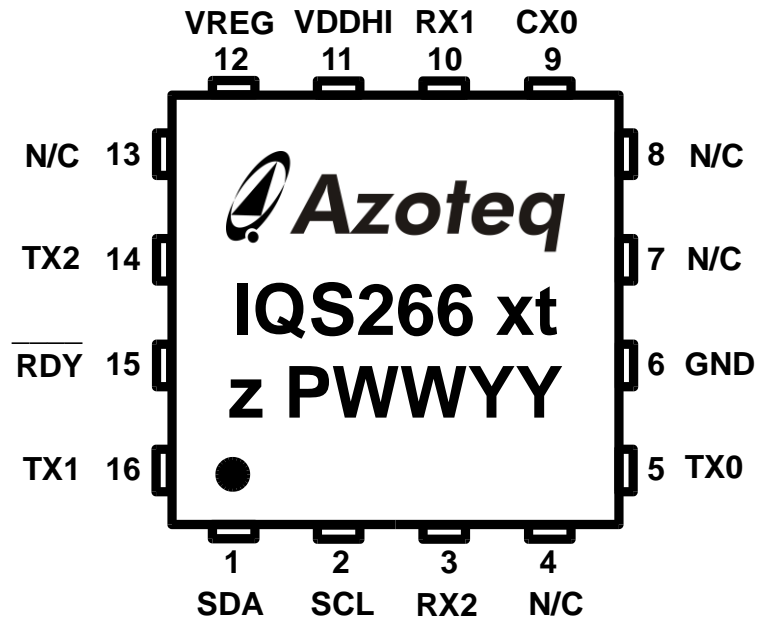


**Figure 1.1    IQS266 Pin layout (representation only device marking differs)**

**Table 1.1 IQS266 Pin-out**

| Pin | Name | Type | Function |
|-----|------|------|----------|
| 1 | SDA | Digital | I²C Serial Data |
| 2 | SCL | Digital | I²C Serial Clock |
| 3 | RX2 | Analogue | Receive Electrode |
| 4 | N/C | - | Not Connected |
| 5 | TX0 | Transmitter | Transmit Electrode |
| 6 | GND | Supply Input | GND Reference |
| 7 | N/C | - | Not Connected |
| 8 | N/C | - | Not Connected |
| 9 | CX0 | Analogue | Receive Electrode |
| 10 | RX1 | Analogue | Receive Electrode |
| 11 | VDDHI | Supply Input | Supply Voltage Input |
| 12 | VREG | Analogue Output | Internal Regulator Pin |
| 13 | N/C | - | Not connected |
| 14 | TX2 | Transmitter | Transmit electrode |
| 15 | RDY | Digital Output | Serial Ready Interrupt |
| 16 | TX1 | Transmitter | Transmit electrode |

## 1.3 Reference Design
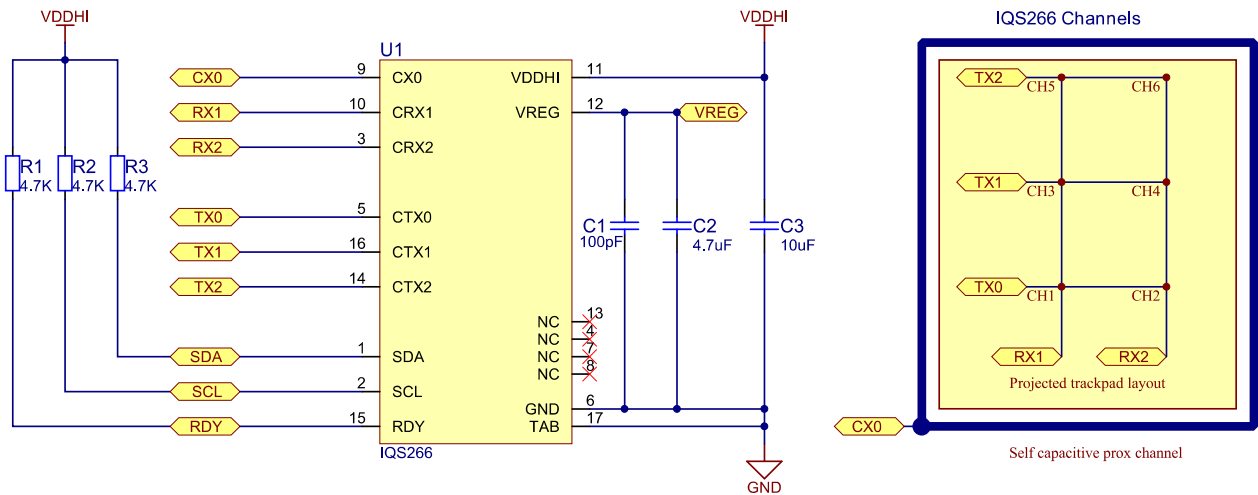


**Figure 1.2    IQS266 Reference Design**
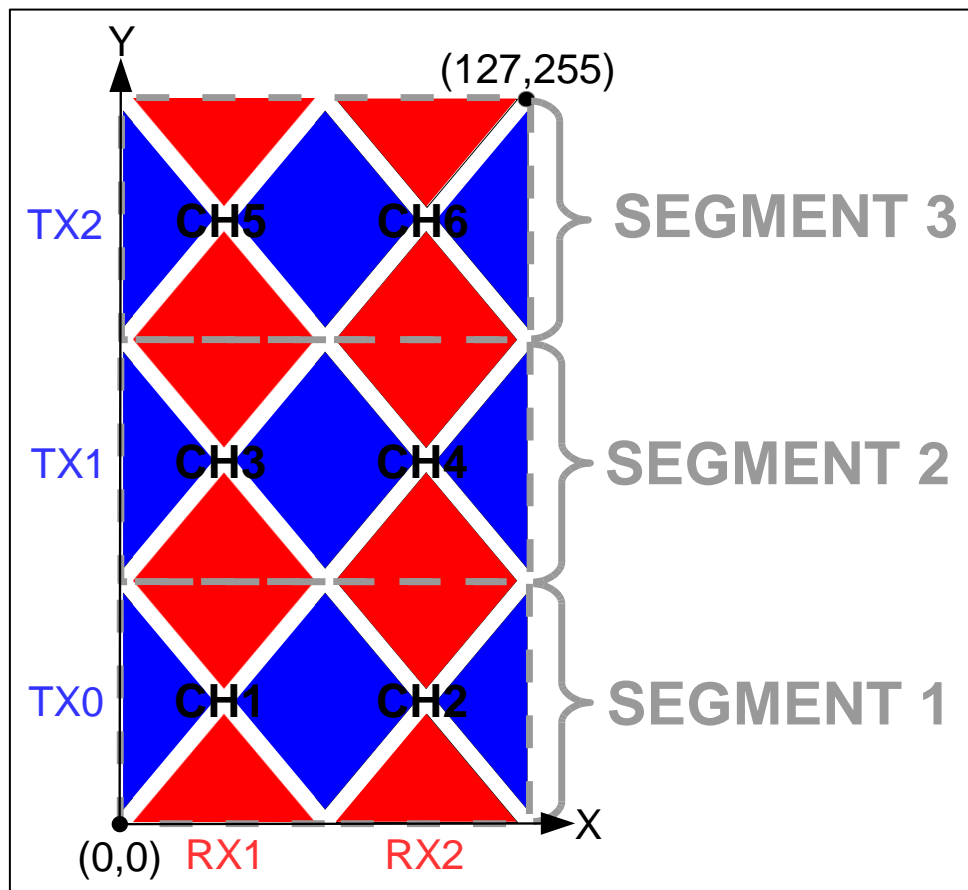


**Figure 1.3    IQS266 Recommended trackpad layout (top view) with coordinate system and segment allocation**

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# 2 User configurable options

## 2.1 ProxSetting0

### 2.1.1 Disable ATI

The **IQS266** can automatically retune sensor electrodes when the counts drift outside a pre-defined ATI band. This allows the **IQS266** to keep optimal sensitivity during different environment. To disable the feature, the "ATI OFF" bit needs to be set in the ProxSettings0 register (0x80; byte 0). Disabling this feature only disables the automatic retuning; the MCU can at any time still force retuning with the Redo-ATI command.

### 2.1.2 Partial ATI

If it is required to have the ATI time reduced, the **IQS266** can use partial ATI by setting the "ATI Partial" bit in the ProxSettings0 register (0x80; byte 0). The designer must also specify the sensitivity multiplier (option 1 to 4) as the **IQS266** will only calculate the compensation multiplier and compensation. The Partial ATI option reduces start-up and re-tuning times, but does require the designer to verify that the base values achieved are within the desired range.

### 2.1.3 ATI Band

The user has the option to select the re-tuning band as ¼ of the ATI target (default is 1/8 of the ATI target) if it is desired to have a wider range for the counts to drift with environmental change before the device retune the electrodes. The wider band is achieved by setting the "ATI BAND" bit in the ProxSettings0 register (0x80; byte 0).

### 2.1.4 Redo-ATI

The **IQS266** can be forced to ATI at any time, regardless of present events. To force retuning set the "Redo ATI" bit in the ProxSettings0 register (0x80; byte 0). The "Redo ATI" bit will automatically clear after having been set.

### 2.1.5 Reseed

The **IQS266** LTA filters can be reseeded to the count values at any time to clear any output event. If count values are outside the ATI band, retuning will be triggered. To reseed set the "Reseed" bit in the ProxSettings0 register (0x80; byte 0). The "Reseed" bit will automatically clear after having been set.

Setting the Reseed bit will shift all LTA filters to a value of $LTA_{new} = CS + 8$ (CS – 8 for Self). The LTA will then track the CS value until they are even.

Performing a reseed action on the LTA filters, will effectively clear any proximity and/or touch conditions that may have been established prior to the reseed call.

### 2.1.6 Debug ATI

In order to facilitate faster start-up and re-tuning times, the communication windows are stopped during ATI on the **IQS266.** If the designer would like to be able to read data after every charge cycle during ATI, the communication can be enabled by setting the "Debug ATI" bit in the ProxSettings0 register (0x80; byte 0). A communication window can still be forced by the MCU with a RDY handshake (pulling the RDY line low) at any time even if the "Debug ATI" bit is not set.

### 2.1.7 Increase stability

The **IQS266's** analogue circuitry settling time can be increased (at the cost of higher current consumption) in order to have a more stable conversion in respect to the internal regulator. The longer settling time is enabled by setting the "Increase stability" bit in the ProxSettings0 register (0x80; byte 0).

### 2.1.8 Force Halt

The user has the option to halt the LTA to avoid any reseed or re-tuning events from taking place. This can be used in situations where the counts are expected to go in the wrong direction as a result of a controlled action in the application. To freeze the LTA filters set the "Force Halt" bit in the ProxSettings0 register (0x80; byte 0).

## 2.2 ProxSettings1

### 2.2.1 Comms WDT off

The WDT (watchdog timer) is used to reset the IC if a problem (for example a voltage spike) occurs during communication. The WDT will time-out (and thus reset the device) after $t_{WDT}$ if no valid communication occurred during this time.

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The WDT can be disabled during development by setting the "WDT Off" bit in the ProxSettings1 register (0x80; byte 1). It is not recommended to disable the WDT for production.

### 2.2.2 Event Mode

By default, the device operates in full streaming mode. There is an option for an event-driven I$^2$C communication mode (also called "Event Mode"), with the RDY pin ONLY indicating a communication window after a prescribed event has occurred.

These events include:

- LP (low power) event
- Swipes (up / down / left / right)
- Tap
- ATI
- TP (trackpad) event
- Touch
- Proximity

The RDY pin will indicate events in the following manner:

1. **LP event:** Single RDY low on LP entry and again on exit
2. **Swipe Detected:** Single RDY low on swipes
3. **Tap Detected:** Single RDY low
4. **ATI:** RDY low on ATI start & again on ATI completing
5. **TP event:** RDY pin low after completion of every charge cycle while a touch remains detected on a channel.
6. **Touch:** RDY low on each touch entry and exit occurring.
7. **Prox:** RDY low on entry and exit

For trackpad events, the device will stream data continuously (after every charge cycle) when a touch is present on one of the channels, even if Event Mode is enabled.

Event Mode can be enabled by setting the "Event Mode" bit in the ProxSettings1 register (0x80; byte 1).

Note: The device is also capable of functioning **without** a RDY line on a polling basis. To change settings during event mode the RDY Hand-Shake Routine should be followed.

### 2.2.3 LTA Beta

The speed at which the LTA will follow the counts when no event is present (no filter halt) can be changed by adjusting the beta values for the LTA filter. Four options are available by setting the "LTA Beta" bits in the ProxSettings1 register (0x80; byte 1).

### 2.2.4 AC Filter

The AC filter is implemented to provide better stability of Counts (CS) in electrically noisy environments.

The filter also enforces a longer minimum sample time for detecting proximity events on CH0, which will result in a slower response rate when the device enters low power modes. The filter can be disabled.

The count filter is implemented only on CH0, to aid in the trackpad coordinate calculations, but touch events are (by default) determined on unfiltered count values.

The count filter can be disabled, or the speed (amount of filtering) adjusted by setting the "ACF" bits in the ProxSettings1 register (0x80; byte 1).

## 2.3 ProxSettings2

### 2.3.1 Wake both directions

The **IQS266** can wake from low power in both directions of count movement (of the proximity threshold). This could be used to sense release events from low power mode. To enable sensing in both directions, set the "Wake both dir" bit in the ProxSettings2 register (0x81; byte 0).

### 2.3.2 Clear TP flags

If the **IQS266** outputs a TP event by setting a TP flag, the flag will remain set until the TP flags register is read. To clear the TP flags with each valid comms window, set the "Clear TP flags" bit in the ProxSettings2 register (0x81; byte 0).

### 2.3.3 NP segment rate

The **IQS266** does a NP (normal power) conversion during low power where all active channels are charged even though the IC are

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only monitoring CH0 for a wake-up event. To change the rate of the NP segments, configure the lower three bits called "NP segment rate" in the ProxSettings2 register (0x81; byte 0). The rate is calculated as a desired multiple of the "Low power period"

## 2.4 ProxSettings3

### 2.4.1 ACK Reset

After start-up, and after every reset event, the "Show Reset" flag will be set in the System Flags register (0x01; byte 0).

The "Show Reset" bit can be read to determine whether a reset has occurred on the device (it is recommended to be continuously monitored). This bit will be set '1' after a reset.

The SHOW_RESET bit will be cleared (set to '0') by writing a '1' into the "ACK Reset" bit in Prox settings 3 register (0x81; byte 1). A reset will typically take place if a timeout during communication occurs.

### 2.4.2 Off mode

The **IQS266** has the option to switch the device off during inactive states of operation. The device will only wake up again on activity on the SDA line (all device register memory will be lost). A reset will occur when the device wakes up and the IC needs to be setup again. This is suitable for applications that require no device operation during defined operation states. To switch to off mode set the "Off mode" bit in the ProxSettings3 register (0x81; byte 1).

### 2.4.3 Projected Bias

The **IQS266** has the option to change the bias current of the Rx channels during projected sensing mode. A larger bias current is required when using larger electrodes, but will also increase the IC power consumption. The bias current is default on 5µA, and can be changed to 10µA. To select 10 µA set the "Proj Bias" bit in the ProxSettings3 register (0x81; byte 1).

### 2.4.4 Float CX

During the charge transfer process, the channels (CX0 electrode for CH0 Self or Rx electrodes for projected trackpad channels) that are not being processed during the current conversion are effectively grounded to decrease the effects of noise-coupling between the sense electrodes. Grounding these traces is useful in applications with long tracks between IC and sense electrode.

There is the option to float the CX (or Rx) lines in between charging. This is particularly useful for applications with a self-capacitive CH0 button with a thick overlay, where more sensitivity is required, or in application that need to avoid false triggers from water on the overlays. To float channels set the "Float Cx" bit in the ProxSettings3 register (0x81; byte 1).

### 2.4.5 Halt charge mode

The charging sequence of the **IQS266** can be halted on command. This function is useful for applications where the IQS266 can be completely halted without resetting the registers. The device will enter a low-power mode without doing conversions on the channels. To enable "Halt charge" set bit in the ProxSettings3 register (0x81; byte 1). To disable "Halt charge" toggle the RDY line. LP period register (0x84; byte 1) should be greater than 0 when "Halt charge" is activated. The LP period should be chosen based on the required low-power current consumption and the required time to wake up from halt-charge mode.

### 2.4.6 CH0 distributed

The **IQS266** device by default performs a self capacitive conversion for channel 0 on the CX0 pin. An option bit is provided to change channel 0 to a distributed self capacitive prox channel charging on pins CX0, RX1 & RX2 simultaneously. To enable this function for channel 0 set the "CH0 distributed" bit in the ProxSettings3 register (0x81; byte 1).

### 2.4.7 Charge transfer frequency slow CH1 – 6

The **IQS266** can reduce the charge transfer frequency for applications that require extra sensitivity (for example very thick overlays). The charge transfer frequency can be halved. The default charge transfer frequency for projected operation is 2MHz and can be slowed down to 1MHz by setting the "Xfer slow CH1 – 6" bit in the ProxSettings3 register (0x81; byte 1).

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### 2.4.8 Charge transfer frequency slow CH0

The **IQS266** can reduce the charge transfer frequency for applications that require extra sensitivity (for example very thick overlays). The charge transfer frequency can be halved. The default charge transfer frequency for self capacitive operation is 1MHz and can be slowed down to 500kHz. If the channel 0 distributed setting is used the charge transfer frequency for the projected operation is 2MHz and can be slowed down to 1MHz by setting the "Xfer slow CH0" bit in the ProxSettings3 register (0x81; byte 1).

## 2.5 Event mask

The **IQS266** can be configured to report only desired events by masking out unwanted events from the Events register (0x01; byte 1). This is only applied during event mode and is particularly useful where communication is only required on certain desired events while still having the **IQS266** waking from low power and sensing as required without interrupting the master/MCU. Clearing the corresponding bits in the Event mask register (0x82; byte 0) will disable or mask an event from reporting during event mode.

## 2.6 Zoom timeout

A normal power mode is defined for the **IQS266** during which normal power conversions is performed. The zoom timeout defines the time to remain in the normal power mode before switching to low power mode. The zoom timeout can be set in periods of 500ms. Any event triggered (proximity or touch) before timeout occurs will clear the timer and start timing again from the last reported event. Configure Zoom timeout register (0x82; byte 1).

## 2.7 Halt timeout

The LTA filter for all channels will halt on proximity or touch events. A halt timeout is implemented for the **IQS266** to terminate a halted filter condition to ensure that no stuck conditions remain indefinitely active. A halt timeout occurs during a stationary touch or prox condition on one or more channels without any change in events/flags for the configured timeout period. After timeout is reached a redo ATI command is self-induced by the **IQS266** in order to recalibrate all channels and clear any stuck activations. The halt timeout can be set in decimal increments of 500ms. Any additional event triggered or active event cleared before timeout occurs will clear the timer and start timing again. Configure Halt timeout register (0x83; byte 0).

## 2.8 RDY timeout

If no communication is initiated from the master/host MCU within the first $t_{COMMS}$ ($t_{COMMS}$ = 2.56ms default) of the RDY line indicating that data is available (i.e. RDY = low), the device will resume with the next cycle of charge transfers and the data from the previous conversions will be lost. The timeout time is adjustable in steps of 0.64ms in the RDY timeout register (0x83; byte 1). There is also a WDT ($t_{I2C}$) that cannot be disabled, for when communication has started but not been completed, for example when the bus is being held by another device. $t_{I2C}$ = 62ms.

## 2.9 Normal mode (NM) period

The **IQS266** normal mode period specifies the sampling time for normal mode conversions (fastest possible conversion period for all channels active). The default normal mode period is 10ms and can be configured in increments of 1ms using the NM period register (0x84; byte 0).

## 2.10 Low power (LP) period

The LP period of the **IQS266** specifies the sampling time for channel 0 during low power mode and halt charge mode. By default, the low power mode period is equal to zero which means that the **IQS266** will not enter low power. For any other configured period in increments of 16ms, low power will be entered

upon zoom timeout and use that sampling period. Use the LP period register (0x84; byte 1) to configure the low power sampling period of channel 0. The VREG voltage should not drop with more than 50 mV. A bigger capacitor on VREG can be used for longer LP periods.

## 2.11 Proximity threshold CH0

A proximity threshold for channel 0 can be selected for the application, to obtain the desired proximity trigger level. The proximity threshold is selectable between 1 (most sensitive) and 255 (least sensitive) counts. These threshold values (i.e. 1-255) are specified in Counts (CS) in the Proximity threshold CH0 register (0x85; byte 0). The default proximity threshold is 6 counts. For a proximity threshold, higher than CH0 touch threshold a proximity event will be forced during a touch.

## 2.12 Touch Thresholds

A touch threshold for each channel can be selected by the designer to obtain the desired touch sensitivity and is selectable between 1/256 (most sensitive) to 255/256 (least sensitive). The touch threshold is calculated as a fraction of the Long-Term Average (LTA) given by,

$$T_{THR} = {^x/_{256}} \times LTA$$

With lower target values (therefore lower LTA's) the touch threshold will be lower and vice versa.

Individual touch thresholds can be set for each channel (including channel 0), by writing to the touch threshold registers. Registers start from 0x85; byte 0 and continues to 0x88; byte 1 for channels 0 to 6. The default touch threshold is 40/256 times the LTA.

## 2.13 ATI target

The **IQS266** ATI targets for channel 0 and all the other channels (1-6) can be adjusted independently. The ATI target should be selected during product design and development and corresponding prox and

touch thresholds should be selected and evaluated according to the desired target value. The ATI target can be adjusted in multiple increments of 8 counts (0-255 * 8counts) using either ATI target CH1-6 register (0x89; byte 0) or ATI target CH0 (0x89; byte 1).

## 2.14 Base values

The **IQS266** has the option to change the base value of the proximity channel (CH0) and the trackpad channels (CH1 to CH6) during the Full ATI algorithm. This provides the user with another option to select the sensitivity of the **IQS266** without changes in the hardware (RX/TX sizes and routing, etc.).

The base values are set by writing to the Base value register (0x8A; byte 0). There are 16 different options to choose from. To choose a custom base value, select partial ATI.

The base value influences the overall sensitivity of the channel and establishes a base count which is used during the ATI algorithm. A lower base value will typically result in a higher sensitivity of the respective channel, as lower multipliers will be selected, and more compensation would be required.

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# 3  ProxSense® Module

The **IQS266** contains a ProxSense® module that uses patented technology to provide detection of proximity and touch conditions on numerous sensing lines.

The ProxSense® module is a combination of hardware and software, based on the principles of charge transfer measurements.

## 3.1  Charge Transfer Concept

On ProxSense® devices like the **IQS266,** capacitance measurements are taken with a charge transfer process that is periodically initiated.

For projected capacitive sensing, the device measures the capacitance between 2 electrodes referred to as the transmitter (TX) and receiver (RX).

The measuring process is referred to as a charge transfer cycle and consists of the following:

- Discharging of an internal sampling capacitor ($C_s$) and the electrode capacitors (mutual: TX & RX) on a channel.
- charging of TX's connected to the channel
- and then a series of charge transfers from the RX's to the internal sampling capacitors ($C_s$), until the trip voltage is reached.

The number of charge transfers required to reach the trip voltage on a channel is referred to as the Current Samples (**CS**) or Count value (Counts).

**Please note: Attaching scope probes to the CTX/CRX pins will influence the capacitance of the sense electrodes and therefore the related CS values of those channels. This will have an instant effect on the CS measurements.**

## 3.2  Rate of Charge Cycles

The **IQS266** samples all its active channels (up to 6 projected channels and 1 capacitive channel). The charge sequence (as measured on the receive electrodes) is shown in Figure 3.1. After the channels are charged the IQS266 process the channel data and go to sleep until the sampling period ends. If the sampling period ends a communication window will be available and is shown by RDy active low.

Typical timings of the charge sequence will differ with each application, depending on the setup of the **IQS266**. For example, the sense (or charge time) is affected by the target counts and charge transfer frequency, while process time is dependent on ATI checking for counts within the allowed band and filter settings. Communication time is affected by the amount of data read (as well as the sequence thereof) and I2C communication frequency.
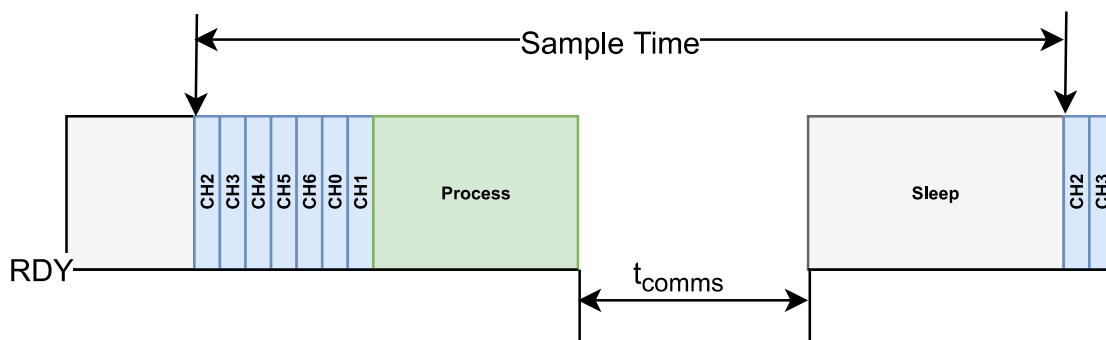


**Figure 3.1  IQS266 Charge Sequence timing diagram.**

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## 3.3 LTA vs Reference Values

The Long-term Average (LTA) and reference values can be seen as the baseline. The baseline values are calculated to continuously adapt to any environmental drift. These values are calculated from the CS value for each channel.

For **CH0** a Long Term Average (**LTA**) is calculated (16 bit unsigned integer values). The count (CS) values (16 bit unsigned integer values) are processed and compared to the LTA to detect Touch and Proximity events on **CH0**.

For **Ch1-Ch6** a reference value of each channel's counts is taken during the normal power update in Low Power. This reference value is compared to the counts during normal power to calculate the trackpad coordinates and detect proximity and touch events for each channel.

## 3.4 Determine Touch or Prox

An event is determined by comparing the CS value with the LTA (Ch0) or Reference (Ch1-6) Since the CS reacts differently when comparing the self- with the mutual capacitance technology, the user should consider only the conditions for the technology used.

An event is recorded if:

- Self (Ch0): CS < LTA – **Threshold**

- Projected(Ch1-6): CS > REF + **Threshold**

**Threshold** can be either a Proximity or Touch threshold, depending on the current channel being processed.

Note that a proximity condition will be forced enabled if there is a touch condition on any channel.

Please refer to **Section 2.11** and **2.12** for proximity and touch threshold selections.

## 3.5 ATI

The **A**utomatic **T**uning **I**mplementation (**ATI**) is a sophisticated technology implemented on the new ProxSense® series devices. It allows for optimal performance of the devices for a wide range of sense electrode capacitances, without modification or addition of external components.

The ATI allows the tuning of two parameters, an ATI Multiplier and an ATI Compensation, to adjust the Count values for an attached sense electrode.

ATI allows the designer to optimize a specific design by adjusting the sensitivity and stability of each channel through the adjustment of the ATI parameters.

The **IQS266** has a full ATI function. The full-ATI function is default enabled, but can be disabled by setting the AUTO_ATI_OFF bit, or changed to partial by setting the ATI_PARTIAL bit in PROX_SETTINGS_0.

The ATI_BUSY bit will be set while an ATI event is busy.

For more information regarding the ATI algorithm, please contact Azoteq at: ProxSenseSupport@azoteq.com

### 3.5.1 ATI Sensitivity

On the **IQS266** device, the user can specify the BASE value and the TARGET value for Channel 0 and for Channel 1-6.

A rough estimation of sensitivity can be calculated as:

$$Sensitivity \propto \frac{TARGET}{BASE}$$

As can be seen from this equation, the sensitivity can be increased by either increasing the Target value or decreasing the Base value. It should, however, be noted that a higher sensitivity will yield a higher noise susceptibility.

### 3.5.2 ATI Target

The target value is reached by adjusting the COMPENSATION bits for each channel (ATI target limited to 2048 counts).

The target value is written into the respective channel's TARGET registers. The value written into these registers multiplied by 8 will yield the new target value.

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### 3.5.3 ATI Base (Multiplier)

The following parameters will influence the base value:

• PROJ_BIAS bits: Adjusts the biasing of some analogue parameters in the mutual capacitive operated IC. (Only applicable in mutual capacitance mode.)

• Charge Transfer Frequency

• MULTIPLIER bits.

The base value used for the ATI function can be implemented in 2 ways:

1. ATI_PARTIAL = 0. ATI automatically adjusts MULTIPLIER bits to reach a selected base value[1].

2. ATI_PARTIAL = 1. The designer can specify the multiplier settings. These settings will give a custom base value from where the compensation bits will be automatically implemented to reach the required target value. The base value is determined by two sets of multiplier bits. Sensitivity Multipliers which will also scale the compensation to normalise the sensitivity and Compensation Multipliers to adjust the gain.

### 3.5.4 Re-ATI

An automatic re-ATI event will occur if the counts are outside its re-ATI limits. The re-ATI limit or ATI boundary is calculated as the target value divided by 8. For example:

- Target = 512, Re-ATI will occur if CS is outside 512±64.

A re-ATI event can also be issued by the host MCU by setting the REDO_ATI bit. The REDO_ATI bit will clear automatically after the ATI event was started.

Note: Re-ATI will automatically clear all proximity, touch and halt status bits.

### 3.5.5 ATI ERROR

The ATI error bit (read only) indicates to the user that the ATI targets where not reached. Adjustments of the base values or ATI BANDs are required.

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[1] ATI function will use PROJ_BIAS (if applicable) and will only adjust the MULTIPLIER bits to reach the base values.

# 4 Communication

The **IQS266** device interfaces to a master controller via a 3-wire (SDA, SCL and RDY) serial interface bus that is I²C™ compatible, with a maximum communication speed of 400kbit/s.

## 4.1 Control Byte

The Control byte indicates the 7-bit device address (44H default) and the Read/Write indicator bit. The structure of the control byte is shown in Figure 4.1.
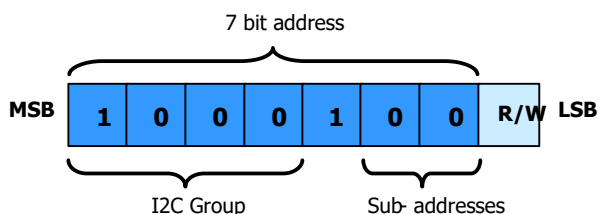


**Figure 4.1    IQS266 Control Byte.**

The I²C device has a 7-bit Slave Address (default 0x44H) in the control byte as shown in Figure 4.1. To confirm the address, the software compares the received address with the device address. Sub-address values can be set by OTP programming options.

## 4.2 I²C Read

To read from the device a *current address read* can be performed. This assumes that the address-command is already setup as desired.

Current Address Read

| Start | Control Byte | | Data n | | Data n+1 | | Stop |
|---|---|---|---|---|---|---|---|
| S | | ACK | | ACK | | NACK | S |
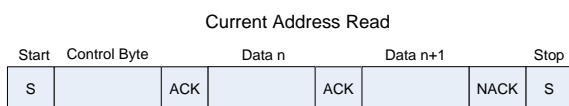
**Figure 4.2    Current Address Read.**

If the address-command must first be specified, then a *random read* must be performed. In this case a WRITE is initially performed to setup the address-command, and then a repeated start is used to initiate the READ section.

Random Read

| Start | Control Byte | | Address-command | | Start | Control Byte | | Data n | | Stop |
|---|---|---|---|---|---|---|---|---|---|---|
| S | Adr + WRITE | ACK | | ACK | S | Adr + READ | ACK | | NACK | S |

Random Read

## I²C Write

To write settings to the device a *Data Write* is performed. Here the Address-Command is always required, followed by the relevant data bytes to write to the device.

DATA WRITE

| Start | Control Byte | | Address-Command | | Data n | | Data n+1 | | Stop |
|---|---|---|---|---|---|---|---|---|---|
| S | Adr + WRITE | ACK | | ACK | | ACK | | ACK | S |

**Figure 4.3    I²C Write**

## 4.3 End of Communication Session / Window

Similar to other Azoteq I²C devices, to end the I²C communication session, a STOP command must be issued. When sending numerous read and write commands in one communication cycle, a repeated start command must be used to stack them together (since a STOP will jump out of the communication window, which is not desired).

The STOP will then end the communication, and the **IQS266** will return to process a new set of data. After the conversion, the communication window will again become available (RDY set LOW; after each conversion during streaming mode operation; only after an event detection during event mode operation).

## 4.4 I²C Sub-address

The **IQS266** has four available sub addresses, 44H (default) to 47H, which allows up to four devices on a single I²C bus.

### 4.4.1 Internal sub-address selection

Selecting the sub-address via OTP bits allows the user 4 different options:

**Table 4.1 I²C sub-address selection**

| FG25 | FG26 | Device Address |
|---|---|---|
| 0 | 0 | 0x44 |
| 0 | 1 | 0x45 |
| 1 | 0 | 0x46 |
| 1 | 1 | 0x47 |

## 4.5 RDY Hand-Shake Routine

The master or host MCU has the capability to request a communication window at any time, by pulling the RDY line low. The communication window will open directly following the current conversion cycle. For more details please refer to the communication interface guide.

## 4.6 I²C Specific Commands

### 4.6.1 Show Reset

After start-up, and after every reset event, the "Show Reset" flag will be set in the System Flags register (0x01H; byte 0).

The "Show Reset" bit can be read to determine whether a reset has occurred on the device (it is recommended to be continuously monitored). This bit will be set '1' after a reset.

The SHOW_RESET bit will be cleared (set to '0') by writing a '0' into the "Show Reset" bit. A reset will typically take place if a timeout during communication occurs.

### 4.6.2 I2C Timeout

If no communication is initiated from the master/host MCU within the first $t_{COMMS}$ ($t_{COMMS}$ = 2.56 ms default) of the RDY line indicating that data is available (i.e. RDY =

low), the device will resume with the next cycle of charge transfers and the data from the previous conversions will be lost. The timeout time is adjustable in steps of 0.64ms in the RDY timeout register (0x83; byte 1). There is also a timeout ($t_{I2C}$) that cannot be disabled, for when communication has started but not been completed, for example when the bus is being held by another device. $t_{I2C}$ = 62ms.

## 4.7 I²C I/O Characteristics

The **IQS266** requires the input voltages given in Table 4.2, for detecting high ("1") and low ("0") input conditions on the I²C communication lines (SDA, SCL and RDY).

### Table 4.2 IQS266 I²C Input voltage

|  | Input Voltage (V) |
|---|---|
| Vin$_{LOW}$ | 0.3*VDDHI |
| Vin$_{HIGH}$ | 0.7*VDDHI |

Table 4.3 provides the output voltage levels of the IQS266 device during I²C communication.

### Table 4.3 IQS266 I²C Output voltage

|  | Output Voltage (V) |
|---|---|
| Vout$_{LOW}$ | GND +0.2 (max.) |
| Vout$_{HIGH}$ | VDDHI – 0.2 (min.) |

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# 5 Memory map

## Table 5.1 IQS266 Memory map index

| Full Address | Byte offset | Group Name | Item Name | Data Access |
|---|---|---|---|---|
| 0x00 | 0 | Device info | PRODUCT_NUM | Read-Only |
|      | 1 |             | VERSION_NUM | Read-Only |
| 0x01 | 0 | Flags | SYSFLAGS0 | Read-Only |
|      | 1 |       | EVENTS | Read-Only |
| 0x02 | 0 | Trackpad data | TP_FLAGS | Read-Only |
|      | 1 |               | Reserved | Read-Only |
| 0x03 | 0 |               | X_CURR | Read-Only |
|      | 1 |               | Y_CURR | Read-Only |
| 0x04 | 0 | Prox & Touch data | PROX_CHANNEL0 | Read-Only |
|      | 1 |                   | TOUCH_CHANNELS | Read-Only |
| 0x05 | 0 | Channel Counts data | ACF_CH0_LOW | Read-Only |
|      | 1 |                     | ACF_CH0_HIGH | Read-Only |
| 0x06 | 0 |                     | CH1_LOW | Read-Only |
|      | 1 |                     | CH1_HIGH | Read-Only |
| 0x07 | 0 |                     | CH2_LOW | Read-Only |
|      | 1 |                     | CH2_HIGH | Read-Only |
| 0x08 | 0 |                     | CH3_LOW | Read-Only |
|      | 1 |                     | CH3_HIGH | Read-Only |
| 0x09 | 0 |                     | CH4_LOW | Read-Only |
|      | 1 |                     | CH4_HIGH | Read-Only |
| 0x0A | 0 |                     | CH5_LOW | Read-Only |
|      | 1 |                     | CH5_HIGH | Read-Only |
| 0x0B | 0 |                     | CH6_LOW | Read-Only |
|      | 1 |                     | CH6_HIGH | Read-Only |
| 0x0C | 0 | LTA and REF data | LTA_CH0_LOW | Read-Only |
|      | 1 |                  | LTA_CH0_HIGH | Read-Only |
| 0x0D | 0 |                  | REF_CH1_LOW | Read-Only |
|      | 1 |                  | REF_CH1_HIGH | Read-Only |
| 0x0E | 0 |                  | REF_CH2_LOW | Read-Only |
|      | 1 |                  | REF_CH2_HIGH | Read-Only |
| 0x0F | 0 |                  | REF_CH3_LOW | Read-Only |
|      | 1 |                  | REF_CH3_HIGH | Read-Only |
| 0x10 | 0 |                  | REF_CH4_LOW | Read-Only |
|      | 1 |                  | REF_CH4_HIGH | Read-Only |
| 0x11 | 0 |                  | REF_CH5_LOW | Read-Only |
|      | 1 |                  | REF_CH5_HIGH | Read-Only |
| 0x12 | 0 |                  | REF_CH6_LOW | Read-Only |
|      | 1 |                  | REF_CH6_HIGH | Read-Only |
| 0x13 | 0 | Deltas | DELTA_CH0_LOW | Read-Only |
|      | 1 |        | DELTA_CH0_HIGH | Read-Only |
| 0x14 | 0 |        | DELTA_CH1_LOW | Read-Only |
|      | 1 |        | DELTA_CH1_HIGH | Read-Only |
| 0x15 | 0 |        | DELTA_CH2_LOW | Read-Only |
|      | 1 |        | DELTA_CH2_HIGH | Read-Only |
| 0x16 | 0 |        | DELTA_CH3_LOW | Read-Only |
|      | 1 |        | DELTA_CH3_HIGH | Read-Only |
| 0x17 | 0 |        | DELTA_CH4_LOW | Read-Only |
|      | 1 |        | DELTA_CH4_HIGH | Read-Only |
| 0x18 | 0 |        | DELTA_CH5_LOW | Read-Only |

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| | | | | |
|---|---|---|---|---|
| | 1 | | DELTA_CH5_HIGH | Read-Only |
| **0x19** | 0 | | DELTA_CH6_LOW | Read-Only |
| | 1 | | DELTA_CH6_HIGH | Read-Only |
| **0x80** | 0 | Prox settings | PROX_SETTINGS0 | Read-Write |
| | 1 | | PROX_SETTINGS1 | Read-Write |
| **0x81** | 0 | | PROX_SETTINGS2 | Read-Write |
| | 1 | | PROX_SETTINGS3 | Read-Write |
| **0x82** | 0 | Event mask | EVENT_MASK | Read-Write |
| | 1 | Timeout periods | ZOOM_TIMEOUT | Read-Write |
| **0x83** | 0 | | HALT_TIMEOUT | Read-Write |
| | 1 | | RDY_TIMEOUT | Read-Write |
| **0x84** | 0 | Report rates | NM_PERIOD | Read-Write |
| | 1 | | LP_PERIOD | Read-Write |
| **0x85** | 0 | Thresholds | PROX_THR_CH0 | Read-Write |
| | 1 | | TOUCH_THR_CH0 | Read-Write |
| **0x86** | 0 | | TOUCH_THR_CH1 | Read-Write |
| | 1 | | TOUCH_THR_CH2 | Read-Write |
| **0x87** | 0 | | TOUCH_THR_CH3 | Read-Write |
| | 1 | | TOUCH_THR_CH4 | Read-Write |
| **0x88** | 0 | | TOUCH_THR_CH5 | Read-Write |
| | 1 | | TOUCH_THR_CH6 | Read-Write |
| **0x89** | 0 | Channel settings | ATI_TARGET_CH1-6 | Read-Write |
| | 1 | | ATI_TARGET_CH0 | Read-Write |
| **0x8A** | 0 | | BASE_VALUE_CH1-6_CH0 | Read-Write |
| | 1 | | ACTIVE_CHANNELS | Read-Write |
| **0x8B** | 0 | Tap gesture settings | TAP_TIMER_LIMIT | Read-Write |
| | 1 | | TAP_THRESHOLD | Read-Write |
| **0x8C** | 0 | Swipe gesture settings | SWIPE_TIMER_LIMIT | Read-Write |
| | 1 | | SWIPE_THRESHOLD | Read-Write |
| **0x8D** | 0 | Multipliers and compensation | SENS & COMP 0 | Read-Write |
| | 1 | | COMPENSATION 0 | Read-Write |
| **0x8E** | 0 | | SENS & COMP 1 | Read-Write |
| | 1 | | COMPENSATION 1 | Read-Write |
| **0x8F** | 0 | | SENS & COMP 2 | Read-Write |
| | 1 | | COMPENSATION 2 | Read-Write |
| **0x90** | 0 | | SENS & COMP 3 | Read-Write |
| | 1 | | COMPENSATION 3 | Read-Write |
| **0x91** | 0 | | SENS & COMP 4 | Read-Write |
| | 1 | | COMPENSATION 4 | Read-Write |
| **0x92** | 0 | | SENS & COMP 5 | Read-Write |
| | 1 | | COMPENSATION 5 | Read-Write |
| **0x93** | 0 | | SENS & COMP 6 | Read-Write |
| | 1 | | COMPENSATION 6 | Read-Write |

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## 5.2   0x00 Device info

### 5.2.1   Product number

| PRODUCT_NUM (0x00, offset 0) | | | | | | | |
|:---:|:---:|:---:|:---:|:---:|:---:|:---:|:---:|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R | R | R | R | R | R | R | R |
| **Name** | Product number | | | | | | | |
| **Default** | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| | 0x4A = D'74 | | | | | | | |

Bit definitions:
- Bit 7-0: Device product number

### 5.2.2   Version number

| VERSION_NUM (0x00, offset 1) | | | | | | | |
|:---:|:---:|:---:|:---:|:---:|:---:|:---:|:---:|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R | R | R | R | R | R | R | R |
| **Name** | Version Number | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | 0x02 = D'2 | | | | | | | |

Bit definitions:
- Bit 7-0: Device software version number

## 5.3   0x01 Flags

### 5.3.1   System flags

| SYSFLAGS0 (0x01, offset 0) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R | R | R | - | R | R | R | R |
| **Name** | SHOW RESET | NP_SEG LT_N_UP | ATI ERROR | - | NP SEG ACTIVE | IN ATI | IGNORE GLOBAL HALT | LP ACTIVE |

Bit definitions:
- Bit 7: Show reset
  - o   0: No reset event
  - o   1: A device reset has occurred and needs to be acknowledged.
- Bit 6: NP segment LTA Update
  - o   0: LTA updates enable
  - o   1: LTA updates blocked
- Bit 5: ATI error
  - o   0: No ATI error occurred
  - o   1: An ATI error occurred
- Bit 3: NP segment active
  - o   0: Normal power segment is inactive
  - o   1: Normal power segment is active
- Bit 2: In ATI
  - o   0: No channels are in ATI
  - o   1: System is busy executing an ATI
- Bit 1: Ignore global halt
  - o   0: Global halt is not ignored
  - o   1: Global halt is ignored
- Bit 0: Low power active
  - o   0: Low power mode is inactive
  - o   1: Low power mode is active

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### 5.3.2 Events

| Events (0x01, offset 1) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R | - | R | R | R | R | R | R |
| **Name** | LP EVENT | - | SWIPE EVENT | TAP EVENT | ATI EVENT | TP EVENT | TOUCH EVENT | PROX EVENT |

Bit definitions:

- Bit 7: Low power event flag
    - o 0: No event to report
    - o 1: A low power event has occurred to signal low power mode entry
- Bit 5: Swipe event flag
    - o 0: No event to report
    - o 1: A swipe event has occurred and should be handled
- Bit 4: Tap event flag
    - o 0: No event to report
    - o 1: A tap event has occurred and should be handled
- Bit 3: ATI event flag
    - o 0: No event to report
    - o 1: An ATI event has occurred and should be handled
- Bit 2: Trackpad event flag
    - o 0: No event to report
    - o 1: A trackpad event has occurred and should be handled
- Bit 1: Touch event flag
    - o 0: No event to report
    - o 1: A touch event has occurred and should be handled
- Bit 0: Proximity event flag
    - o 0: No event to report
    - o 1: A proximity event has occurred and should be handled

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## 5.4 0x02 – 0x03 Trackpad data

### 5.4.1 Trackpad flags

| TP_FLAGS (0x02, offset 0) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R | R | R | R | R | R | R | R |
| **Name** | SEG_1 | SEG_0 | SWIPE RIGHT | SWIPE LEFT | SWIPE DOWN | SWIPE UP | TAP | TP ACTIVE |

Bit definitions:
- Bit 7-6: Trackpad segment
  - 00: No trackpad segment event activation
  - 01: Segment 1 trackpad event activation (Y: 0 – 85)
  - 10: Segment 2 trackpad event activation (Y: 85 – 170)
  - 11: Segment 3 trackpad event activation (Y: 170 – 255)
- Bit 5: Swipe right
  - 0: No swipe event to report
  - 1: Swipe right event occurred
- Bit 4: Swipe left
  - 0: No swipe event to report
  - 1: Swipe left event occurred
- Bit 3: Swipe down
  - 0: No swipe event to report
  - 1: Swipe down event occurred
- Bit 2: Swipe up
  - 0: No swipe event to report
  - 1: Swipe up event occurred
- Bit 1: Tap
  - 0: No tap event to report
  - 1: Tap event occurred
- Bit 0: TP active
  - 0: Trackpad not actively in use
  - 1: Trackpad actively in use

### 5.4.2 X current position

| X_CURR (0x03, offset 0) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R | R | R | R | R | R | R | R |
| **Name** | X_CURR | | | | | | | |

Bit definitions:
- Bit 0 – 7:
  - 0 – 127: X current position in decimal

### 5.4.3 Y current position

| Y_CURR (0x03, offset 1) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R | R | R | R | R | R | R | R |
| **Name** | Y_CURR | | | | | | | |

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Bit definitions:
- Bit 0 – 7:
  - o 0 – 255: Y current position in decimal

## 5.5 0x04 Prox & Touch data

### 5.5.1 Prox channel 0

| | PROX_CHANNEL0 (0x04, offset 0) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | - | - | - | - | - | - | - | R |
| **Name** | - | - | - | - | - | - | - | CH0 |

Bit definitions:
- Bit 1: Channel 0 Prox
  - o 0: No prox condition present on channel 0
  - o 1: A prox condition is present on channel 0

### 5.5.2 Touch channels

| | TOUCH_CHANNELS (0x04, offset 1) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R | R | R | R | R | R | R | R |
| **Name** | - | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |

Bit definitions:
- Bit 6: Channel 6 touch
  - o 0: No touch on channel 6
  - o 1: Touch present on channel 6
- Bit 5: Channel 5 touch
  - o 0: No touch on channel 5
  - o 1: Touch present on channel 5
- Bit 4: Channel 4 touch
  - o 0: No touch on channel 4
  - o 1: Touch present on channel 4
- Bit 3: Channel 3 touch
  - o 0: No touch on channel 3
  - o 1: Touch present on channel 3
- Bit 2: Channel 2 touch
  - o 0: No touch on channel 2
  - o 1: Touch present on channel 2
- Bit 1: Channel 1 touch
  - o 0: No touch on channel 1
  - o 1: Touch present on channel 1
- Bit 0: Channel 0 touch
  - o 0: No touch on channel 0
  - o 1: Touch present on channel 0

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## 5.6  0x05 – 0x06 AC filtered channel count data

| ACF_CH0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R | R | R | R | R | R | R | R |
| **Name** | ACF Channel Low | | | | | | | |
| **Bit Number** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| **Data Access** | R | R | R | R | R | R | R | R |
| **Name** | ACF Channel High | | | | | | | |

Bit definitions:
- Bit 0-15: AC filtered or raw value counts

## 5.7  0x07 – 0x0B Channel count data

| Counts_CH1-6 | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R | R | R | R | R | R | R | R |
| **Name** | Channel Counts Low | | | | | | | |
| **Bit Number** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| **Data Access** | R | R | R | R | R | R | R | R |
| **Name** | Channel Counts High | | | | | | | |

Bit definitions:
- Bit 0-15: Raw value counts

## 5.8  0x0C – 0x0D LTA data

| LTA CH0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R | R | R | R | R | R | R | R |
| **Name** | LTA Channel Low | | | | | | | |
| **Bit Number** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| **Data Access** | R | R | R | R | R | R | R | R |
| **Name** | LTA Channel High | | | | | | | |

Bit definitions:
- Bit 0-15: LTA filter value output

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## 5.9  0x0E – 0x12 REF data

| REF CH1-6 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R | R | R | R | R | R | R | R |
| **Name** | REF Channel Low | | | | | | | |
| **Bit Number** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| **Data Access** | R | R | R | R | R | R | R | R |
| **Name** | REF Channel High | | | | | | | |

Bit definitions:
- Bit 0-15: Reference value output

## 5.10 0x13 – 0x19 Deltas

| Delta CHx | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R | R | R | R | R | R | R | R |
| **Name** | Delta Channel Low | | | | | | | |
| **Bit Number** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| **Data Access** | R | R | R | R | R | R | R | R |
| **Name** | Delta Channel High | | | | | | | |

Bit definitions:
- Bit 0-15: Delta value of channel
  - Delta = LTA - ACF (CH0)
  - Delta = ACF- REF (CH1-6)

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## 5.11 0x80 – 0x81 Prox settings

### 5.11.1 Prox settings 0

| PROX_SETTINGS_0 (0x80, offset 0) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | AUTO ATI_OFF | ATI PARTIAL | ATI BAND | REDO ATI | DO RESEED | DEBUG ATI | INC STABL | FORCE HALT |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Default** | 0x00 | | | | | | | |

Bit definitions:
- Bit 7: Auto ATI
  - 0: Auto ATI on
  - 1: Auto ATI off
- Bit 6: ATI partial
  - 0: Normal ATI active
  - 1: Partial ATI active (Sensitivity multipliers are selected by the user and kept fixed)
- Bit 5: ATI band
  - 0: Normal ATI band
  - 1: Large ATI band
- Bit 4: Redo ATI
  - 0: None
  - 1: Redo an ATI
- Bit 3: Do reseed
  - 0: None
  - 1: Do a reseed operation
- Bit 2: Debug ATI
  - 0: No communication during ATI
  - 1: Communication during ATI allowed
- Bit 1: Increase stability
  - 0: Normal analogue settling time
  - 1: Increased analogue settling time for more stability
- Bit 0: Force halt
  - 0: Normal halting
  - 1: Force halt Ch0 LTA and Ch1-6 REF

### 5.11.2 Prox settings 1

| PROX_SETTINGS_1 (0x80, offset 1) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | COMMS WDT OFF | EVENT MODE | Ch0 LTA FILTER | | - | - | Ch0 AC FILTER | |
| **Default** | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| **Default** | 0x11 | | | | | | | |

Bit definitions:
- Bit 7: Communication watch dog timer off
  - 0: Communication watch dog timer enabled. Reset will occur if timeout occurs.
  - 1: Communication watch dog timer disabled. Reset will not occur upon timeout. It is not advised to disable the communication watch dog timer.

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- Bit 6: Event mode:
    - 0: Streaming mode communication enabled
    - 1: Event mode communication enabled
- Bit 5-4: CH0 LTA filter beta selection
    - 00: LTA beta = 1/512
    - 01: LTA beta = 1/256
    - 10: LTA beta = 1/128
    - 11: LTA beta = 1/64
- Bit 1-0: CH0 AC filter beta selection
    - 00: AC filter off
    - 01: ACF beta = 1
    - 10: ACF beta = 2
    - 11: ACF beta = 3

### 5.11.3 Prox settings 2

| Bit Number | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | PROX_SETTINGS_2 (0x81, offset 0) | | | | | | | |
| Data Access | - | - | R/W | - | R/W | R/W | R/W | R/W |
| Name | - | - | WAKE BOTH DIR | - | CLEAR TP FLAGS | NP_SEGMENT_RATE | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| | 0x03 | | | | | | | |

Bit definitions:
- Bit 5: Wake both directions
    - 0: Normal activation in only one direction of count movement respective to LTA/REF.
    - 1: Activation in both directions of count movement respective to LTA/REF.
- Bit 4: Clear trackpad flags
    - 0: Trackpad flags stay set from last active trackpad event
    - 1: Trackpad flags are cleared after each communication window
- Bit 2-0: NP_SEGMENT_RATE
    - 0 - 7: Normal power segment rate = $2^{(NP\_SEGMENT\_RATE)}$
        - b'000 = 0: 1
        - b'001 = 1: 2
        - b'010 = 2: 4
        - b'011 = 3: 8
        - b'100 = 4: 16
        - b'101 = 5: 32
        - b'110 = 6: 64
        - b'111 = 7: 128

### 5.11.4 Prox settings 3

| Bit Number | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | PROX_SETTINGS_3 (0x81, offset 1) | | | | | | | |
| Data Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | ACK RESET | OFF MODE | PROJ BIAS | FLOAT CX | HALT CHARGE | CH0 DIST | XFER SLOW CH1-6 | XFER SLOW CH0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0x00 | | | | | | | |

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Bit definitions:
- Bit 7: Acknowledge reset
  - o 0: None
  - o 1: Command to clear the SHOW RESET flag
- Bit 6: Off mode
  - o 0: IC in on mode
  - o 1: IC in off mode
- Bit 5: Projected bias current setting
  - o 0: Normal projected biasing current (5µA)
  - o 1: Increased projected biasing current (10µA)
- Bit 4: Float Cx pins
  - o 0: Ground Cx pins while not actively charged
  - o 1: Float Cx pins while not actively charged
- Bit 3: Halt charge
  - o 0: Normal charging
  - o 1: Halt all channel charging
- Bit 2: Channel 0 distributed
  - o 0: Self capacitive charging on CX0 pin. No distributed prox channel.
  - o 1: Distributed self capacitive prox channel charging on pins CX0, RX1 & RX2 simultaneously.
- Bit 0: Slow charging frequency on channel 1-6
  - o 0: Normal charging frequency: 2MHz
  - o 1: Slow charging frequency: 1MHz
- Bit 0: Slow charging frequency on channel 0
  - o 0: Normal charging frequency: 1MHz
  - o 1: Slow charging frequency: 500kHz

## 5.12 0x82 Event mask

| Event mask (0x82, offset 0) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R | - | R | R | R | R | R | R |
| **Name** | LP EVENT AMSK | - | SWIPE EVENT MASK | TAP EVENT MASK | ATI EVENT MASK | TP EVENT MASK | TOUCH EVENT MASK | PROX EVENT MASK |
| **Default** | 1 | - | 1 | 1 | 1 | 1 | 1 | 1 |
| | 0xFF | | | | | | | |

Bit definitions:
- Bit 7: Low power event mask
  - o 0: Event is masked out
  - o 1: Event is active
- Bit 5: Swipe event mask
  - o 0: Event is masked out
  - o 1: Event is active
- Bit 4: Tap event mask
  - o 0: Event is masked out
  - o 1: Event is active
- Bit 3: ATI event mask
  - o 0: Event is masked out
  - o 1: Event is active
- Bit 2: Trackpad event mask

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- o  0: Event is masked out
- o  1: Event is active
- Bit 1: Touch event mask
  - o  0: Event is masked out
  - o  1: Event is active
- Bit 0: Proximity event mask
  - o  0: Event is masked out
  - o  1: Event is active

## 5.13 0x82 offset 1 – 0x83 offset 1 Timeout periods

### 5.13.1 Zoom timeout period

| Zoom timeout (0x82, offset 1) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Zoom timeout period | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| | 0x0A = D'10 * 500ms = 5sec | | | | | | | |

Bit definitions:
- Bit 7-0:
  - o  0-255: Zoom timeout period in 500ms increments.

### 5.13.2 Halt timeout period

| Halt timeout (0x83, offset 0) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Normal mode sampling period | | | | | | | |
| **Default** | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| | 0x28 = D'40 * 500ms = 20sec | | | | | | | |

Bit definitions:
- Bit 7-0:
  - o  0: Never halt
  - o  1-254: Halt timeout period in 500ms increments.
  - o  255: Always halt

### 5.13.3 RDY timeout period

| RDY timeout (0x83, offset 1) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | RDY timeout period | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| | 0x04 = D'4 * 0.64ms = 2.56ms | | | | | | | |

Bit definitions:
- Bit 7-0:
  - o  0-255: RDY timeout period in 0.64ms increments.

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## 5.14 0x84 Report rates

### 5.14.1 Normal mode period

| NM_PERIOD (0x84, offset 0) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Normal mode period | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| | 0x0A = D'10 = 10ms | | | | | | | |

Bit definitions:
- Bit 7-0:
    - 0-255: Normal mode sampling period in ms

### 5.14.2 Low power period

| LP_PERIOD (0x84, offset 1) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Low power period | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0x00 = Never in LP | | | | | | | |

Bit definitions:
- Bit 7-0:
    - 0: No low power mode entry. Always in normal mode sampling.
        - Warning: Trackpad LTA's are only updated during low power.
    - 1-255: Low power sampling period in 16ms increments

## 5.15 0x85 – 0x88 Thresholds

### 5.15.1 Prox threshold CH0

| PROX_THR_CH0 (0x85, offset 0) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Prox threshold CH0 | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| | 0x06 = D'6 | | | | | | | |

Bit definitions:
- Bit 7-0:
    - 0-255: CH0 prox threshold value in counts

### 5.15.2 Touch threshold CH0

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **TOUCH_THR_CH0 (0x85, offset 1)** | | | | | | | | |
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Touch threshold CH0 | | | | | | | |
| **Default** | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| | 0x28 = D'40 = x | | | | | | | |

Bit definitions:
- Bit 7-0:
    - 0-255: CH0 touch threshold = ( x / 256 ) * LTA

### 5.15.3 Touch threshold CH1

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **TOUCH_THR_CH1 (0x86, offset 0)** | | | | | | | | |
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Touch threshold CH1 | | | | | | | |
| **Default** | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| | 0x28 = D'40 | | | | | | | |

Bit definitions:
- Bit 7-0:
    - 0-255: CH1 touch threshold = ( x / 256 ) * LTA

### 5.15.4 Touch threshold CH2

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **TOUCH_THR_CH2 (0x86, offset 1)** | | | | | | | | |
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Touch threshold CH2 | | | | | | | |
| **Default** | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| | 0x28 = D'40 | | | | | | | |

Bit definitions:
- Bit 7-0:
    - 0-255: CH2 touch threshold = ( x / 256 ) * LTA

### 5.15.5 Touch threshold CH3

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **TOUCH_THR_CH3 (0x87, offset 0)** | | | | | | | | |
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Touch threshold CH3 | | | | | | | |
| **Default** | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| | 0x28 = D'40 | | | | | | | |

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Bit definitions:
- Bit 7-0:
  - 0-255: CH3 touch threshold = ( x / 256 ) * LTA

### 5.15.6 Touch threshold CH4

| TOUCH_THR_CH4 (0x87, offset 1) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Touch threshold CH4 | | | | | | | |
| **Default** | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| | 0x28 = D'40 | | | | | | | |

Bit definitions:
- Bit 7-0:
  - 0-255: CH4 touch threshold = ( x / 256 ) * LTA

### 5.15.7 Touch threshold CH5

| TOUCH_THR_CH5 (0x88, offset 0) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Touch threshold CH5 | | | | | | | |
| **Default** | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| | 0x28 = D'40 | | | | | | | |

Bit definitions:
- Bit 7-0:
  - 0-255: CH5 touch threshold = ( x / 256 ) * LTA

### 5.15.8 Touch threshold CH6

| TOUCH_THR_CH6 (0x88, offset 1) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Touch threshold CH6 | | | | | | | |
| **Default** | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| | 0x28 = D'40 | | | | | | | |

Bit definitions:
- Bit 7-0:
  - 0-255: CH6 touch threshold = ( x / 256 ) * LTA

## 5.16 0x89 – 0x8A Channel settings

### 5.16.1 ATI target CH1-6

| Bit Number | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | ATI_TARGET_CH1-6 (0x89, offset 0) | | | | | | | |
| Data Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | ATI target | | | | | | | |
| Default | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| | 0x20 = D'32 * 8 = 256 counts | | | | | | | |

Bit definitions:

- Bit 7-0:
    - 0-255: ATI target (0 – 2040) = (ATI target value) * 8 counts

### 5.16.2 ATI target CH0

| Bit Number | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | ATI_TARGET_CH0 (0x89, offset 1) | | | | | | | |
| Data Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | ATI target CH0 | | | | | | | |
| Default | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| | 0x20 = D'32 * 8 = 256 counts | | | | | | | |

Bit definitions:

- Bit 7-0:
    - 0-255: ATI target CH0 (0 – 2040) = (ATI target CH0 value) * 8 counts

### 5.16.3 Base value

| Bit Number | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | BASE_VALUE_BYTE_CH1-6_CH0 (0x8A, offset 0) | | | | | | | |
| Data Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Name | Base value Ch1 - 6 | | | | Base value Ch0 | | | |
| Default | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| | 0x42 | | | | | | | |
| | D'4 = 138 counts | | | | D'2 = 106 counts | | | |

Bit definitions:
- Bit 7-4: Base value Ch1 – 6
    - b'0000 = 0: Base = 74
    - b'0001 = 1: Base = 90
    - b'0010 = 2: Base = 106
    - b'0011 = 3: Base = 122
    - b'0100 = 4: Base = 138
    - b'0101 = 5: Base = 154
    - b'0110 = 6: Base = 170
    - b'0111 = 7: Base = 186
    - b'1000 = 8: Base = 202
    - b'1001 = 9: Base = 218
    - b'1010 = 10: Base = 234
    - b'1011 = 11: Base = 250
    - b'1100 = 12: Base = 266
    - b'1101 = 13: Base = 282
    - b'1110 = 14: Base = 298
    - b'1111 = 15: Base = 314

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- Bit 3-0: Base value Ch0
  - o b'0000 = 0: Base = 74
  - o b'0001 = 1: Base = 90
  - o b'0010 = 2: Base = 106
  - o b'0011 = 3: Base = 122
  - o b'0100 = 4: Base = 138
  - o b'0101 = 5: Base = 154
  - o b'0110 = 6: Base = 170
  - o b'0111 = 7: Base = 186
  - o b'1000 =  8: Base = 202
  - o b'1001 =  9: Base = 218
  - o b'1010 = 10: Base = 234
  - o b'1011 = 11: Base = 250
  - o b'1100 = 12: Base = 266
  - o b'1101 = 13: Base = 282
  - o b'1110 = 14: Base = 298
  - o b'1111 = 15: Base = 314

### 5.16.4  Active channels

| ACTIVE_CHANNELS (0x8A, offset 1) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | - | R/W | R/W | R/W | R/W | R/W | R/W | - |
| **Name** | - | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
| **Default** | - | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 0x7F | | | | | | | |

Bit definitions:
- Bit 6: Channel 6
  - o 0: Channel inactive
  - o 1: Channel active
- Bit 5: Channel 5
  - o 0: Channel inactive
  - o 1: Channel active
- Bit 4: Channel 4
  - o 0: Channel inactive
  - o 1: Channel active
- Bit 3: Channel 3
  - o 0: Channel inactive
  - o 1: Channel active
- Bit 2: Channel 2
  - o 0: Channel inactive
  - o 1: Channel active
- Bit 1: Channel 1
  - o 0: Channel inactive
  - o 1: Channel active
- Please note:
  - o Channel 0 will always be forced active to handle zoom and wake-up from sleep

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## 5.17 0x8B Tap gesture settings

### 5.17.1 Tap timer limit

| TAP_TIMER_LIMIT (0x8B, offset 0) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Tap timer limit | | | | | | | |
| **Default** | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| | 0x4B = D'75 * 2ms = 150ms | | | | | | | |

Bit definitions:
- Bit 7-0:
  - 0-255: Tap timer limit in 2ms increments.
    A touch and release within the tap threshold must occur in this maximum time limit to be a valid tap gesture

### 5.17.2 Tap threshold

| TAP_THRESHOLD (0x8B, offset 1) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Tap threshold | | | | | | | |
| **Default** | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| | 0x1E = D'30 | | | | | | | |

Bit definitions:
- Bit 7-0:
  - 0-255: Tap threshold.
    The threshold specifies the maximum length of a square area on the trackpad coordinate output data (0x03) in which the tap must occur. Exceeding this maximum square area will not recognise a valid tap gesture.

## 5.18 0x8C Swipe gesture settings

### 5.18.1 Swipe timer limit

| SWIPE_TIMER_LIMIT (0x8C, offset 0) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Swipe timer limit | | | | | | | |
| **Default** | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| | 0x96 = D'150 * 2ms = 300ms | | | | | | | |

Bit definitions:
- Bit 7-0:
    - 0-255: Swipe timer limit in 2ms increments.
      A touch, continuous swipe and a release exceeding the swipe threshold must occur in this maximum time limit to be a valid swipe gesture.

### 5.18.2 Swipe threshold

| Swipe threshold (0x8C, offset 1) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Swipe threshold | | | | | | | |
| **Default** | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| | 0x30 = D'48 | | | | | | | |

Bit definitions:
- Bit 7-0:
    - 0-255: Swipe threshold.
      This threshold specifies the minimum length of a continuous swipe on the trackpad coordinate output data (0x03). Any swipe shorter than this threshold in X and Y directions separately will not be recognised as a valid swipe gesture.

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# 5.19 0x8D – 0x93 Multipliers and compensation: CH0 – CH6

## 5.19.1 CH0 Multipliers

| Multipliers (0x8D, offset 0) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | - | - | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | - | - | Sens | | Comp | | | |

| Compensation (0x8D, offset 1) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Compensation | | | | | | | |

## 5.19.2 CH1 Multipliers

| Multipliers (0x8E, offset 0) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | - | - | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | - | - | Sens | | Comp | | | |

| Compensation (0x8E, offset 1) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Compensation | | | | | | | |

## 5.19.3 CH2 Multipliers

| Multipliers (0x8F, offset 0) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | - | - | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | - | - | Sens | | Comp | | | |

| Compensation (0x8F, offset 1) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Compensation | | | | | | | |

## 5.19.4 CH3 Multipliers

| Multipliers (0x90, offset 0) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | - | - | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | - | - | Sens | | Comp | | | |

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| Compensation (0x90, offset 1) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Compensation | | | | | | | |

### 5.19.5  CH4 Multipliers

| Multipliers (0x91, offset 0) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | - | - | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | - | - | Sens | | Comp | | | |

| Compensation (0x91, offset 1) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Compensation | | | | | | | |

### 5.19.6  CH5 Multipliers

| Multipliers (0x92, offset 0) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | - | - | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | - | - | Sens | | Comp | | | |

| Compensation (0x92, offset 1) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Compensation | | | | | | | |

### 5.19.7  CH6 Multipliers

| Multipliers (0x93, offset 0) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | - | - | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | - | - | Sens | | Comp | | | |

| Compensation (0x93, offset 1) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit Number** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Data Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Name** | Compensation | | | | | | | |

Bit definitions:
- Offset 0, Bit 5-4: Sensitivity multipliers:
    - 1 - 4: Sens = Sens value +1
- Bit3-0: Compensation multiplier:
    - 1-16: Comp = Comp value + 1
- Offset 1, Bit 7-0: Compensation
    - 0-255: Compensation = Compensation value

# 6  Electrical characteristics

## 6.1  Absolute Maximum Specifications

The following absolute maximum parameters are specified for the device:

*Exceeding these maximum specifications may cause damage to the device.*

### Table 6.1  Absolute maximum specification

| Parameter | Absolute maximum |
|---|---|
| Operating temperature | -20°C to 85°C |
| Supply Voltage (VDDHI – GND) | 3.6V |
| Maximum pin voltage | VDDHI + 0.5V (may not exceed VDDHI max) |
| Maximum continuous current (for specific Pins) | 10mA |
| Minimum pin voltage | GND - 0.5V |
| Minimum power-on slope | 100V/s |
| ESD protection | ±8kV (Human body model) |

### Table 6.2  IQS266 General Operating Conditions[i]

| DESCRIPTION | Conditions | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Supply voltage | | $V_{DDHI}$ | 1.8 | 3.3V | 3.6 | V |
| Internal regulator output | $1.8 \leq V_{DDHI} \leq 3.6$ | $V_{REG}$ | 1.63 | 1.66 | 1.69 | V |
| Default Operating Current | 3.3V | $I_{IQS266NP}$ | - | 263.81 | TBC | µA |
| Low Power Setting 1 | 3.3V, LP=32 | $I_{IQS266LP128}$ | - | 3.91 | TBC | µA |
| Low Power Setting 2 | 3.3V, LP=160 | $I_{IQS266LP160}$ | - | 3.40 | TBC | µA |
| Low Power Setting 3 | 3.3V, LP=320 | $I_{IQS266LP320}$ | - | 2.59 | TBC | µA |

### Table 6.3  Electrode specifications – Self capacitance

| DESCRIPTION | Conditions | PARAMETER | MAX | UNIT |
|---|---|---|---|---|
| Parasitic Capacitance CX to GND | | $C_P$ | 120 | pF |
| Series resistor | $C_P = 80pF$ | $R_S$ | 10 | kΩ |

---

[i]Operating current shown in this datasheet, does not include power dissipation through I2C pull up resistors.

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### Table 6.4  Electrode specifications – Projected capacitance

| DESCRIPTION | Conditions | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Parasitic Capacitance Tx to GND | | $C_T$ | | 100 | pF |
| Parasitic Capacitance Rx to GND | | $C_R$ | | 100 | pF |
| Mutual capacitance | | $C_M$ | 0.1 | 10 | pF |
| Series resistor | | $R_{TX}$ | | 10 | kΩ |
| Series resistor | $C_M = 1pF$ | $R_{RX}$ | | 1 | kΩ |

## 6.2  Power On-reset/Brown out

### Table 6.5  Power on-reset and brown out detection specifications

| DESCRIPTION | Conditions | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Power On Reset | $V_{DDHI}$ Slope ≥ 100V/s @25°C | POR | | 1.6 | V |
| Brown Out Detect | $V_{DDHI}$ Slope ≥ 100V/s @25°C | BOD | 1.15 | 1.55 | V |

## 6.3  Digital input/output trigger levels

### Table 6.6  Digital input/output trigger level specifications

| DESCRIPTION | Conditions | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Input low level voltage | 400kHz I$^2$C clock frequency | $V_{in\_LOW}$ | - | 30 | % of VDDHI |
| Input high level voltage | | $V_{in\_HIGH}$ | 70 | - | |

## 6.4 Current consumption

### 6.4.1 Capacitive sensing

**Table 6.7 Capacitive sensing current consumption**

| Power mode | Conditions | Report rate | TYPICAL AVG | MAX AVG[1] | UNIT |
|---|---|---|---|---|---|
| NP mode | VDD = 1.8V | 10ms | 257 | 373 | µA |
| NP mode | VDD = 3.3V | 10ms | 258 | 375 | µA |
| LP mode | VDD = 1.8V | 128ms | 3.2 | 5 | µA |
| LP mode | VDD = 3.3V | 128ms | 3.9 | 6 | µA |
| LP mode | VDD = 1.8V | 160ms | 2.8 | 4 | µA |
| LP mode | VDD = 3.3V | 160ms | 3.4 | 5 | µA |
| LP mode | VDD = 1.8V | 320ms | 1.9 | 3 | µA |
| LP mode | VDD = 3.3V | 320ms | 2.5 | 4 | µA |
| Off mode | VDD = 1.8V | None | 0.75 | 0.78 | µA |
| Off mode | VDD = 3.3V | None | 1.42 | 1.61 | µA |
| Halt Charge | VDD = 1.8V | 320ms | 1.36 | TBC | uA |
| Halt Charge | VDD = 3.3V | 320ms | 1.92 | TBC | uA |

CH0 ATI Target = 392; CH1-6 ATI Target = 328; Event Mode; NP Segment rate = 64; Bias Current = 5 uA

1- Average measured over a number of cycles

Note: Average measurements are subject to change

## 6.5 Device timing descriptions

### 6.5.1 I$^2$C communication timeout

The IQS266 employs a watch dog timer to ensure that the device may recover from any undefined state that might occur due to a loss of communications or external influences (such as an ESD strike). The following table specifies the timings related to a watch dog timeout.

**Table 6.8 Watch dog timeouts**

| Parameter | Minimum | Maximum |
|---|---|---|
| Terminated communication during an active communication window (streaming or event mode) | 62ms | |

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# 7 Package information

## 7.1 Package and footprint specifications

### Top View



### Transparent Top View



0.250±0.05 x 45°±1°

### Side View
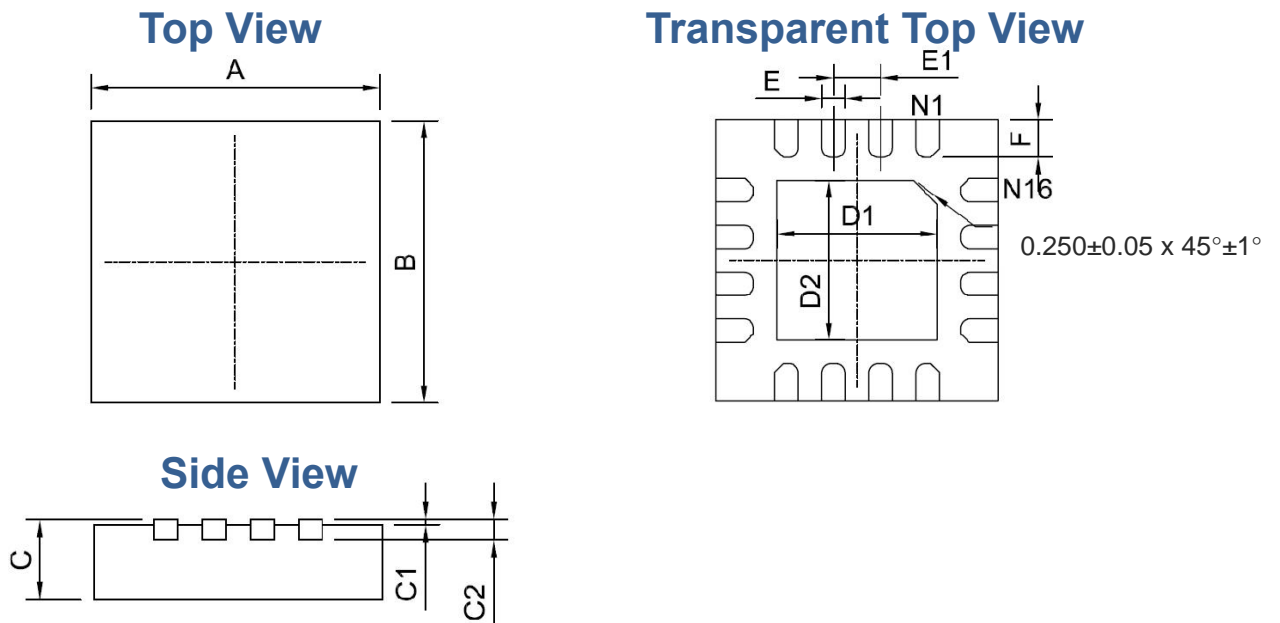


| Dimension | [mm] | Dimension | [mm] |
|-----------|------|-----------|------|
| A | 3.0±0.1 | D1 | 1.7±0.05 |
| B | 3.0±0.1 | D2 | 1.7±0.05 |
| C | 0.75±0.05 | E | 0.25±0.05 |
| C1 | 0.025±0.025 | E1 | 0.5±0.05 |
| C2 | 0.203±0.05 | F | 0.4±0.05 |

**Figure 7.1    QFN(3x3)–16 Package Dimensions**

## 7.2 Recommended PCB footprint



0.5mm

1.7mm

0.25mm

0.84mm

0.3mm
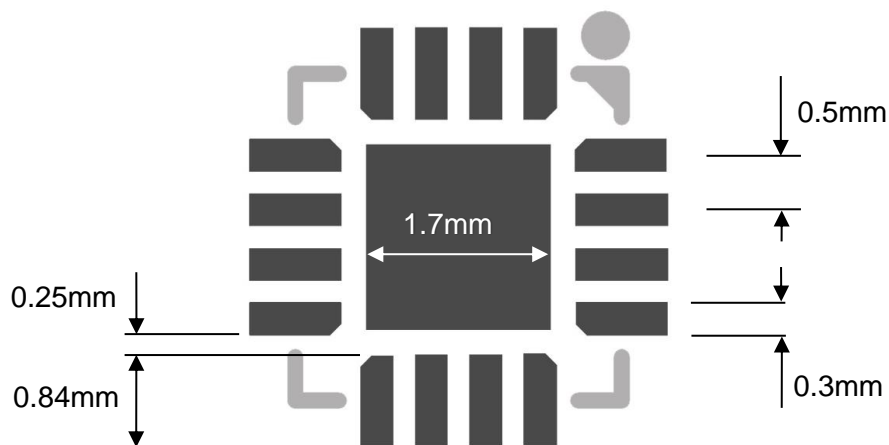
**Figure 7.2    IQS266 Recommended PCB footprint**

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## 7.3 Device marking
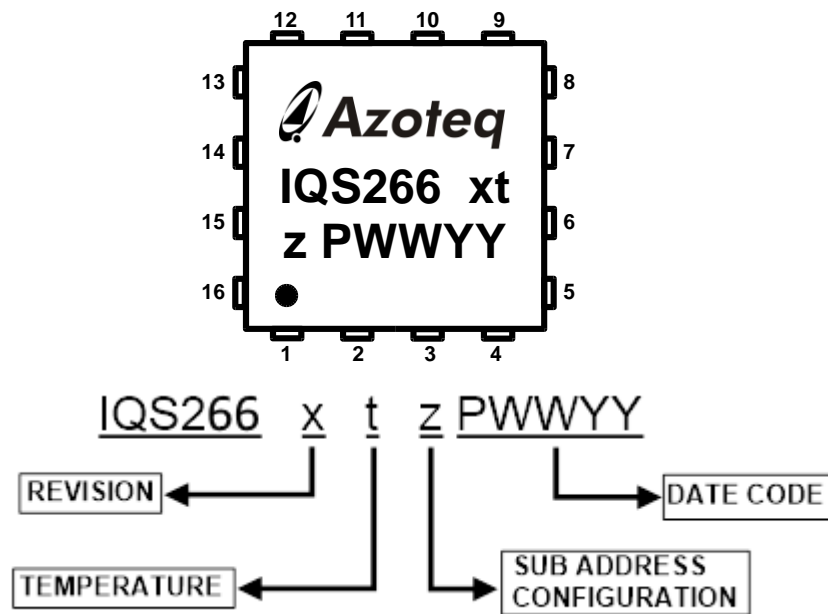


| REVISION | x | = | IC Revision Number |
| --- | --- | --- | --- |
| TEMPERATURE RANGE | t | = i | -20°C to 85°C (Industrial) |
| | | = c | 0°C to 70°C (Commercial) |
| IC CONFIGURATION | z | = | Sub Address Configuration (Hexadecimal) |
| | 0 | = | 44H |
| | 1 | = | 45H |
| | 2 | = | 46H |
| | 3 | = | 47H |
| DATE CODE | P | = | Package House |
| | WW | = | Week |
| | YY | = | Year |

## 7.4 Ordering Information

Order quantities will be subject to multiples of a full reel. Contact the official distributor for sample quantities. A list of the distributors can be found under the "Distributors" section of www.azoteq.com.
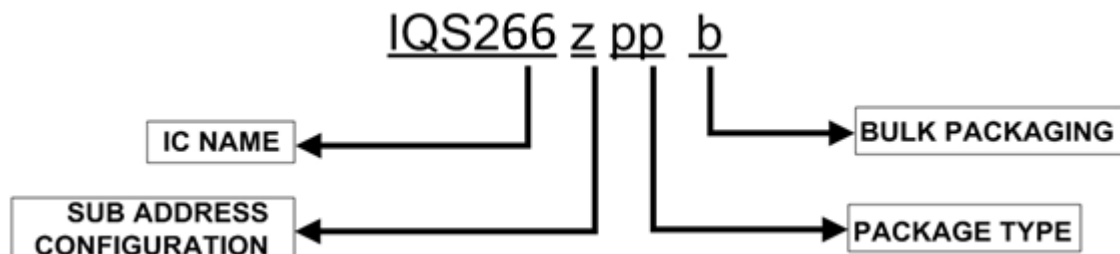


| IC NAME | IQSxxx | = | IQS266 |
| --- | --- | --- | --- |
| CONFIGURATION | | z = | Sub Address Configuration (hexadecimal) |
| PACKAGE TYPE | | QN = | QFN(3x3)-16 |
| BULK PACKAGING | | R = | Reel (3000pcs/reel) |

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## 7.5 Tape and reel specification

### 7.5.1 Tape specification



SECTION A - A

NOTES:
1、10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2、CAMBER IN COMPLIANCE WITH EIA 481
3、POCKET POSITION RELATIVE TO SPROCKET HOLE
MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

A0=3.30
B0=3.30
K0=1.10
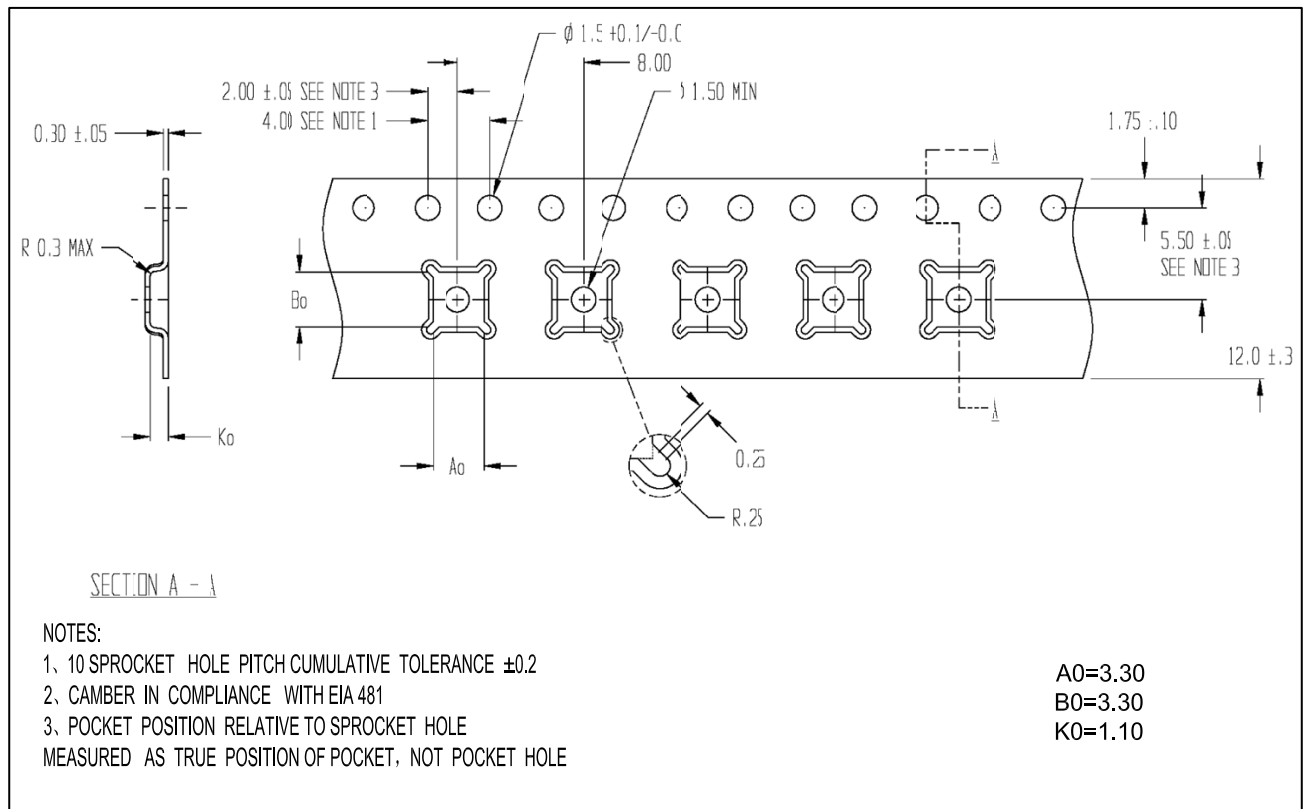
### 7.5.2 Cover tape specification



76.2(3.0 INCHES)NOMINAL INSIDE CORE DIAMETER

| 3202036005 | 9.2±0.1mm | 蓋 | 9.2mm 300m PS pale blue |
| 3202036115 | 13.3±0.1mm | 蓋 | 13.3mm 300m PS pale blue |
| 3202036205 | 21.0±0.1mm | 蓋 | 21mm 300m PS pale blue |
| 3202036300 | 25.5±0.1mm | 蓋 | 25.5mm 300m PS pale blue |

NOTE :
1、REEL TO CONTAIN 300 METERS OF
SPLICE FREE MATERIAL
2、Thickness: 0.050±0.010(mm)
3、THESE WIDTHS ARS ALSO AVAILABLE
IN 500 MERER LENGTHS

POLYESTER FILM

ANTI STATIC
TREATMENT
BOTH SIDES

HEAT ACTIVATED ADHESIVE

## 7.5.3   Reel specification



| PRODUCT SPECIFICATIONS | | | | | |
|---|---|---|---|---|---|
| TYPE WIDTH | ΦA | ΦN | W1(+2/0) | W2( Max) | W3( Max) |
| 12MM | 330±2.0 | 100±1.0 | 12.4 | 18.4 | 11.9/15.4 |
| 16MM | 330±2.0 | 100±1.0 | 16.4 | 22.4 | 15.9/19.4 |
| 24MM | 330±2.0 | 100±1.0 | 24.4 | 30.4 | 23.9~27.4 |

| | | |
|---|---|---|
| 3203013133 | 卷 | 13 dia Hub4 12mm width PS B(芯　) |
| 3203013213 | 卷 | 13 dia Hub4 16mm width PS B(芯　) |
| 3203013253 | 卷 | 13 dia Hub4 24mm width PS B(芯　) |
| 3203013134 | 卷 | 13 dia Hub4 12mm width PS blue |
| 3203013255 | 卷 | 13寸 Hub4 24mm　PS　色 |

# 7.6  MSL Level

**Moisture Sensitivity Level** (MSL) relates to the packaging and handling precautions for some semiconductors. The MSL is an electronic standard for the period in which a moisture sensitive device can be exposed to ambient room conditions (approximately 30°C/85%RH see J-STD033C for more info) before reflow occur.

| Package | Level (duration) |
|---|---|
| QFN(3x3)-16 | MSL 1 (Unlimited at ≤30°C / 85% RH) Reflow profile peak temperature < 260°C for < 25 seconds Number of reflows < 3 |

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# 8  Datasheet revisions

## 8.1  Revision history

V1.00 – Added current consumption

| | | |
|---|---|---|
| V1.01– Updated: | Ready Timeout | |
| V1.01– Updated: | Current consumption | |
| | Product Number Register | |
| V1.02– Updated: | Reference Schematic | |
| | Minor Updates | |
| V1.03 – Updated: | Current Measurements | |
| V1.04 – Updated: | Off Mode operation | |
| Added: | Off-mode Current Consumption | |
| V1.05 – Updated: | Halt Charge operation | |
| | Reference schematic | |
| Added: | Halt Charge current | |
| Added: | Digital input/output trigger levels | |
| V1.06 – Updated: | Package Information | |
| | MSL 1 | |
| V1.07 – Updated | Table 1.1 | |
| | Description of Clear TP Flags (2.3.2) | |
| | Description of Halt Charge (2.4.5) | |
| | Description of Zoom Timeout (2.6) | |
| | Register description 0x05-0x12 (5.6-5.7) | |
| | I2C Specifications (6.3) | |
| Added | Section 3: ProxSense Module | |

## 8.2  Errata

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# Appendix A. Contact information

|  | **USA** | **Asia** | **South Africa** |
|---|---|---|---|
| **Physical Address** | 6507 Jester Blvd Bldg 5, suite 510G Austin TX 78750 USA | Rm1227, Glittery City Shennan Rd Futian District Shenzhen, 518033 China | 109 Main Street Paarl 7646 South Africa |
| **Postal Address** | 6507 Jester Blvd Bldg 5, suite 510G Austin TX 78750 USA | Rm1227, Glittery City Shennan Rd Futian District Shenzhen, 518033 China | PO Box 3534 Paarl 7620 South Africa |
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