MCP3903

Six Channel Delta Sigma A/D Converter

Features

- Six Synchronous Sampling 16/24-bit Resolution Delta-Sigma A/D Converters with Proprietary Multi-Bit Architecture
- 91 dB SINAD, -100 dBc Total Harmonic Distortion (THD) (up to 35th harmonic), 102 dB Spurious-free Dynamic Range (SFDR) for Each Channel
- Programmable Data Rate up to 64 ksps
- Ultra Low-Power Shutdown Mode with <2 µA
- -115 dB Crosstalk Between any Two Channels
- Low Drift Internal Voltage Reference: 5 ppm/°C
- Differential Voltage Reference Input Pins
- High Gain PGA on Each Channel (up to 32 V/V)
- Phase Delay Compensation Between Each Pair of Channels with 1 µs Time Resolution
- High-Speed Addressable 10 MHz SPI Interface with Mode 0,0 and 1,1 Compatibility
- Independent Analog and Digital Power Supplies 4.5V - 5.5V AV_{DD}, 2.7V - 3.6V DV_{DD}
- Available in Small 28-lead SSOP Package
- Extended Temperature Range: -40°C to +125°C

Applications

- Energy Metering and Power Measurement
- Portable Instrumentation
- Medical and Power Monitoring

Description

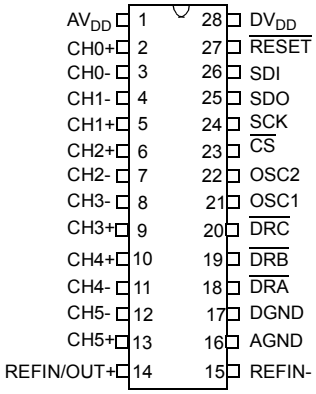
The MCP3903 is a six-channel Analog Front End (AFE) containing three pairs made out of two synchronous sampling Delta-Sigma Analog-to-Digital Converters (ADC) with PGA, a phase delay compensation block, internal voltage reference, and high-speed 10 MHz SPI compatible serial interface. The converters contain a proprietary dithering algorithm for reduced idle tones and improved THD.

The internal register map contains 24-bit wide ADC data words, a modulator output register as well as six 24-bit writable control registers to program gain, over-sampling ratio, phase, resolution, dithering, shut-down, reset and several communication features.

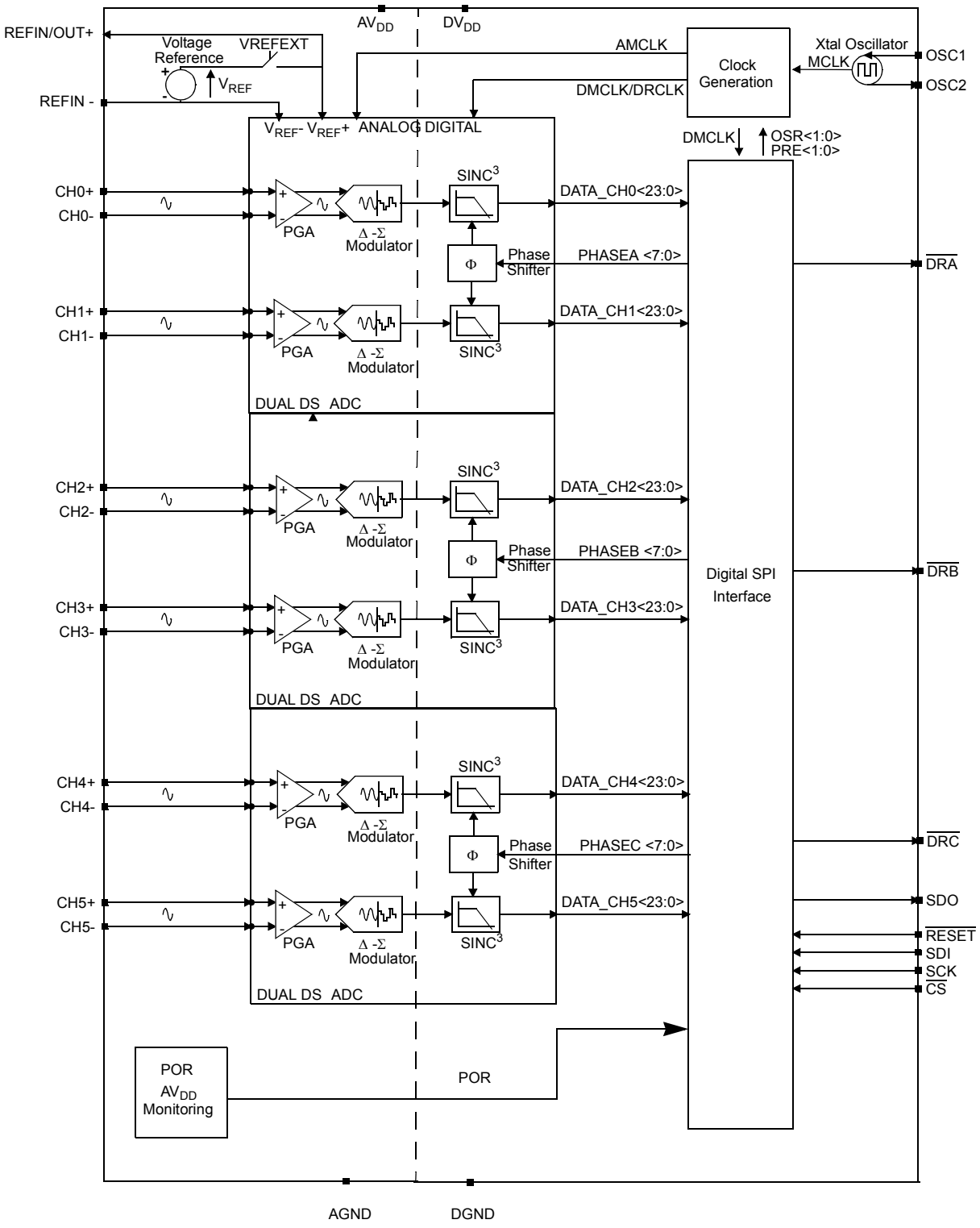
The communication is largely simplified with various Continuous Read modes that can be accessed by the Direct Memory Access (DMA) of an MCU and with separate Data Ready pins that can directly be connected to the Interrupt Request (IRQ) input of an MCU. The MCP3903 is capable of interfacing to a large variety of voltage and current sensors including shunts, current transformers, Rogowski coils, and Hall-effect sensors.

Package Type

28-Lead SSOP



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

The Reliability Targets section includes the absolute maximum ratings for the device, defining the values that will cause no long term damage regardless of duration.

These tables also represent the testing requirements per the Max. and Min. columns.

1.1 RELIABILITY TARGETS

ABSOLUTE MAXIMUM RATINGS †

V_{DD} 7.0V
Digital inputs and outputs w.r.t. A_{GND} .....-0.6V to V_{DD} +0.6V
Analog input w.r.t. A_{GND} ....-6V to +6V
V_{REF} input w.r.t. A_{GND}.....-0.6V to V_{DD} +0.6V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds)..... +300°C
ESD on the analog inputs (HBM,MM)..... 5.0 kV, 500V
ESD on all other pins (HBM,MM)..... 5.0 kV, 500V

TABLE 1-1: ANALOG SPECIFICATIONS TARGET TABLE

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = 4.5 to 5.5V, DV_{DD} = 2.7 to 3.6V, Internal V_{REF}, MCLK = 4 MHz;PRESCALE = 1; OSR = 64; f_S = 1 MHz; f_D = 15.625 ksps; T_A = -40°C to +125°C, GAIN = 1, V_{IN} = $1V_{PP}$ = $353mV_{RMS}$ @ 50/60 Hz.

Param. Num.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Conditions
Internal Voltage Reference							
A001	V_{REF}	Voltage	-2%	2.35	+2%	V	VREFEXT = 0
A002	TC_{REF}	Tempco	—	5	—	ppm/°C	VREFEXT = 0
A003	$ZOUT_{REF}$	Output Impedance		7	—	kΩ	AV_{DD}=5V, VREFEXT = 0
Voltage Reference Input							
A004		Input Capacitance	—	—	10	pF	
A005	V_{REF}	Differential Input Voltage Range (V_{REF+} - V_{REF-})	2.2	—	2.6	V	V_{REF} = (V_{REF+} - V_{REF-}), VREFEXT = 1
A006	V_{REF+}	Absolute Voltage on REFIN+ pin	1.9	—	2.9	V	VREFEXT = 1
A007	V_{REF-}	Absolute Voltage on REFIN- pin	-0.3	—	+0.3	V	V_{REF-} should be connected to AGND when VREFEXT=0
ADC Performance							
A008		Resolution (No Missing Codes)		24		bits	OSR = 256 (see Table 5-2)
A009	f_S	Sampling Frequency	See Table 4-2			kHz	f_S = DMCLK = MCLK / (4 x PRESCALE)
A010	f_D	Output Data Rate	See Table 4-2			ksps	f_D = DRCLK= DMCLK / OSR = MCLK / (4 x PRESCALE x OSR)

Note 1: This specification implies that the ADC output is valid over this entire differential range, i.e. there is no distortion or instability across this input range. Dynamic Performance is specified at -0.5 dB below the maximum signal range, V_{IN} = -0.5 dBFS @ 50/60 Hz = 333 mV_{RMS}, V_{REF} = 2.4V.

2: See terminology section for definition.

3: This parameter is established by characterization and not 100% tested.

4: For these operating currents, the following configuration bit settings apply: Config Register Settings: SHUTDOWN<5:0> = `000000`, RESET<5:0> = `000000`; VREFEXT = `0`, CLKEXT = `0`.

5: For these operating currents, the following configuration bit settings apply: Config Register Settings: SHUTDOWN<5:0> = `111111`, VREFEXT = `1`, CLKEXT = `1`.

6: Applies to all gains. Offset error is dependant on PGA gain setting.

7: Outside of this range, ADC accuracy is not specified. An extended input range of +/- 6V can be applied continuously to the part with no risk for damage.

8: For proper operation and to keep ADC accuracy, AMCLK should always be in the range of 1 to 5 MHz with BOOST bits off. With BOOST bits on, AMCLK should be in the range of 1 to 8.192 MHz. AMCLK = MCLK/PRESCALE. When using a crystal, CLKEXT bit should be equal to '0'.

TABLE 1-1: ANALOG SPECIFICATIONS TARGET TABLE (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = 4.5 to 5.5V, DV_{DD} = 2.7 to 3.6V, Internal V_{REF}, MCLK = 4 MHz;PRESCALE = 1; OSR = 64; f_S = 1 MHz; f_D = 15.625 ksps; T_A = -40°C to +125°C, GAIN = 1, V_{IN} = $1V_{PP}$ = $353mV_{RMS}$ @ 50/60 Hz.

Param. Num.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Conditions
A011	CHn+-	Analog Input Absolute Voltage	-1		+1	V	All analog input channels, measured to AGND **(Note 7)**
A012	A_{IN}	Analog Input Leakage Current		1		nA	**(Note 4)**
A013	(CH_{n+}-CH_{n-})	Differential Input Voltage Range			500 / GAIN	mV_P	**(Note 1)**
A014	V_{OS}	Offset Error	-3		3	mV	**(Note 6)(Note 2)**
A015		Offset Error Drift		1		µV/C	From -40°C to 125°C
A016	GE	Gain Error	-3		3	%	**All Gains**
A017		Gain Error Drift	—	2	—	ppm/°C	From -40°C to 125°C
A018	INL	Integral Non-Linearity		15		ppm	GAIN = 1, DITHER = ON
A019	Z_{IN}	Input Impedance	350	—	—	kΩ	Proportional to 1/AMCLK
A020	SINAD	Signal-to-Noise and Distortion Ratio	89	91	—	dB	T = 25°C
			80	81.5		dB	
A021	THD	Total Harmonic Distortion		-100	-97	dB	OSR = 256, DITHER = ON; **(Note 2)(Note 3)**
				-90	-87	dB	
A022	SNR	Signal To Noise Ratio	90	91.5		dB	T = 25°C
			80	81.5		dB	
A023	SFDR	Spurious Free Dynamic Range		102		dB	OSR = 256, DITHER = ON; **(Note 2) (Note 3)**
				91		dB	
A024	CTALK	Crosstalk (50 / 60 Hz)	—	-115	—	dB	OSR = 256, DITHER = ON; **(Note 2)(Note 3)**
A025	AC PSRR	AC Power Supply Rejection	—	-68	—	dB	AV_{DD} = 5V + 1Vpp @ 50 Hz
A026	DC PSRR	DC Power Supply Rejection	—	-68	—	dB	AV_{DD} = 4.5 to 5.5V, DV_{DD} = 3.3V
A027	CMRR	DC Common Mode Rejection Ratio	—	-75	—	dB	V_{CM} varies from -1V to +1V; **(Note 2)**
Oscillator Input							

Note 1: This specification implies that the ADC output is valid over this entire differential range, i.e. there is no distortion or instability across this input range. Dynamic Performance is specified at -0.5 dB below the maximum signal range, V_{IN} = -0.5 dBFS @ 50/60 Hz = 333 mV_{RMS}, V_{REF} = 2.4V.

2: See terminology section for definition.

3: This parameter is established by characterization and not 100% tested.

4: For these operating currents, the following configuration bit settings apply: Config Register Settings: SHUTDOWN<5:0> = `000000`, RESET<5:0> = `000000`; VREFEXT = `0`, CLKEXT = `0`.

5: For these operating currents, the following configuration bit settings apply: Config Register Settings: SHUTDOWN<5:0> = `111111`, VREFEXT = `1`, CLKEXT = `1`.

6: Applies to all gains. Offset error is dependant on PGA gain setting.

7: Outside of this range, ADC accuracy is not specified. An extended input range of +/- 6V can be applied continuously to the part with no risk for damage.

8: For proper operation and to keep ADC accuracy, AMCLK should always be in the range of 1 to 5 MHz with BOOST bits off. With BOOST bits on, AMCLK should be in the range of 1 to 8.192 MHz. AMCLK = MCLK/PRESCALE. When using a crystal, CLKEXT bit should be equal to '`0`'.

TABLE 1-1: ANALOG SPECIFICATIONS TARGET TABLE (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = 4.5 to 5.5V, DV_{DD} = 2.7 to 3.6V, Internal V_{REF}, MCLK = 4 MHz;PRESCALE = 1; OSR = 64; f_S = 1 MHz; f_D = 15.625 ksps; T_A = -40°C to +125°C, GAIN = 1, V_{IN} = $1V_{PP}$ = $353mV_{RMS}$ @ 50/60 Hz.

Param. Num.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Conditions
A028	MCLK	Master Clock Frequency Range	1	—	16.384	MHz	**(Note 8)**
Power Specifications							
P001	AV_{DD}	Operating Voltage, Analog	4.5	—	5.5	V	
P002	DV_{DD}	Operating Voltage, Digital	2.7	—	3.6	V	
P003	AI_{DD}	Operating Current, Analog **(Note 4)**		7.1	9	mA	BOOST bits low on all channels
				12.3	16.8	mA	BOOST bits high on all channels
P004	DI_{DD}	Operating Current, Digital	—	1.2	1.7	mA	DV_{DD} = 3.6V, MCLK = 4 MHz
			—	2.4	3.4	mA	DV_{DD} = 3.6V, MCLK = 8.192 MHz
P005	$I_{DDS,A}$	Shutdown Current, Analog	—	—	1	µA	-40°C to 85°C, AV_{DD} pin only, **(Note 5)**
			—	—	3	µA	-40°C to 125°C, AV_{DD} pin only, **(Note 5)**
P006	$I_{DDS,D}$	Shutdown Current, Digital	—	—	1	µA	-40°C to 85°C, DV_{DD} pin only, **(Note 5)**
			—	—	5	µA	-40°C to 125°C, DV_{DD} pin only, **(Note 5)**

Note 1: This specification implies that the ADC output is valid over this entire differential range, i.e. there is no distortion or instability across this input range. Dynamic Performance is specified at -0.5 dB below the maximum signal range, V_{IN} = -0.5 dBFS @ 50/60 Hz = 333 mV_{RMS}, V_{REF} = 2.4V.

2: See terminology section for definition.

3: This parameter is established by characterization and not 100% tested.

4: For these operating currents, the following configuration bit settings apply: Config Register Settings: SHUTDOWN<5:0> = `000000`, RESET<5:0> = `000000`; VREFEXT = `0`, CLKEXT = `0`.

5: For these operating currents, the following configuration bit settings apply: Config Register Settings: SHUTDOWN<5:0> = `111111`, VREFEXT = `1`, CLKEXT = `1`.

6: Applies to all gains. Offset error is dependant on PGA gain setting.

7: Outside of this range, ADC accuracy is not specified. An extended input range of +/- 6V can be applied continuously to the part with no risk for damage.

8: For proper operation and to keep ADC accuracy, AMCLK should always be in the range of 1 to 5 MHz with BOOST bits off. With BOOST bits on, AMCLK should be in the range of 1 to 8.192 MHz. AMCLK = MCLK/PRESCALE. When using a crystal, CLKEXT bit should be equal to '0'.

1.2 SERIAL INTERFACE CHARACTERISTICS

SERIAL INTERFACE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = 4.5 to 5.5V, DV_{DD} = 2.7 to 3.6V, -40°C < T_A <+125°C, C_{LOAD} = 30 pF.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Serial Clock frequency	f_{SCK}	—	—	10	MHz	$2.7 \le DV_{DD} < 3.6$
$\overline{CS}$ setup time	t_{CSS}	50	—	—	ns	$2.7 \le DV_{DD} < 3.6$
$\overline{CS}$ hold time	t_{CSH}	100	—	—	ns	$2.7 \le DV_{DD} < 3.6$
$\overline{CS}$ disable time	t_{CSD}	50	—	—	ns	—
Data setup time	t_{SU}	10	—	—	ns	$2.7 \le DV_{DD} < 3.6$
Data hold time	t_{HD}	20	—	—	ns	$2.7 \le DV_{DD} < 3.6$
Serial Clock high time	t_{HI}	40	—	—	ns	$2.7 \le DV_{DD} < 3.6$
Serial Clock low time	t_{LO}	40	—	—	ns	$2.7 \le DV_{DD} < 3.6$
Serial Clock delay time	t_{CLD}	50	—	—	ns	—
Serial Clock enable time	t_{CLE}	50	—	—	ns	—
Output valid from SCK low	t_{DO}	—	—	50	ns	$2.7 \le DV_{DD} < 3.6$
Output hold time	t_{HO}	0	—	—	ns	
Output disable time	t_{DIS}	—	—	50	ns	$2.7 \le DV_{DD} < 3.6$
Reset Pulse Width ($\overline{RESET}$)	t_{MCLR}	100	—	—	ns	$2.7 \le DV_{DD} < 3.6$
Data Transfer Time to $\overline{DR}$ (Data Ready)	t_{DODR}		—	50	ns	$2.7 \le DV_{DD} < 3.6$
Data Ready Pulse Low Time	t_{DRP}		1/ DMCLK	—	µs	$2.7 \le DV_{DD} < 3.6$
Schmitt Trigger High-level Input voltage (All digital inputs)	V_{IH1}	.7 DV_{DD}	—	DV_{DD} +1	V	
Schmitt Trigger Low-level input voltage (All digital inputs)	V_{IL1}	-0.3	—	0.25 DV_{DD}	V	
Hysteresis of Schmitt Trigger Inputs (All digital inputs)	V_{HYS}	50	—		mV	
Low-level output voltage, SDO pin	V_{OL}	—	—	0.4	V	SDO pin only, I_{OL} = 2 mA, DV_{DD} = 3.3V
Low-level output voltage, $\overline{DRn}$ pins	V_{OL}			0.4	V	$\overline{DRn}$ pins only, I_{OL} = +1.5 mA, DV_{DD} =3.3V
High-level output voltage, SDO pin	V_{OH}	DV_{DD} - 0.5	—	—	V	SDO pin only, I_{OH} = -2 mA, DV_{DD} = 3.3V
High-level output voltage, $\overline{DRn}$ pins only	V_{OH}	DV_{DD} - 0.5	—	—	V	$\overline{DRn}$ pins only, I_{OH} = -1.5 mA, DV_{DD}=3.3V
Input leakage current	I_{LI}	—	—	±1	µA	$\overline{CS}$ = DV_{DD}, Inputs tied to DV_{DD} OR DGND
Output leakage current	I_{LO}	—	—	±1	µA	$\overline{CS}$ = DV_{DD}, Inputs tied to DV_{DD} OR DGND
Internal capacitance (all inputs and outputs)	C_{INT}	—	—	7	pF	T_A = 25°C, SCK = 1.0 MHz DV_{DD} = 3.3V **(Note 1)**

Note 1: This parameter is periodically sampled and not 100% tested.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = 4.5 to 5.5V, DV_{DD} = 2.7 to 3.3 V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	**(Note 1)**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 28-lead SSOP	θ_{JA}	—	71	—	°C/W	

Note 1: The internal junction temperature (T_J) must not exceed the absolute maximum specification of +150°C.

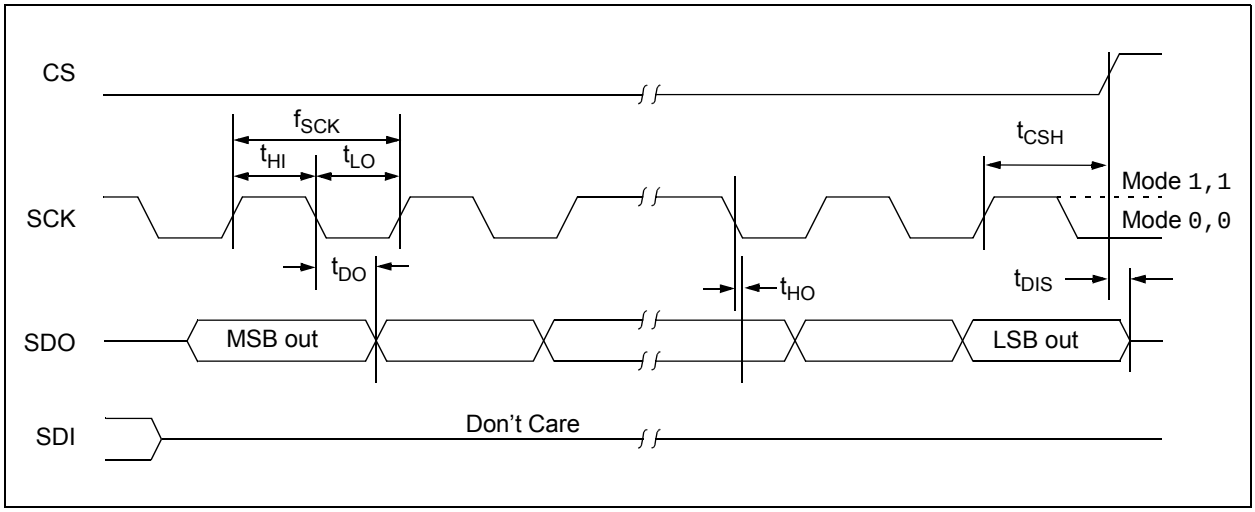


FIGURE 1-1: *Serial Output Timing Diagram.*

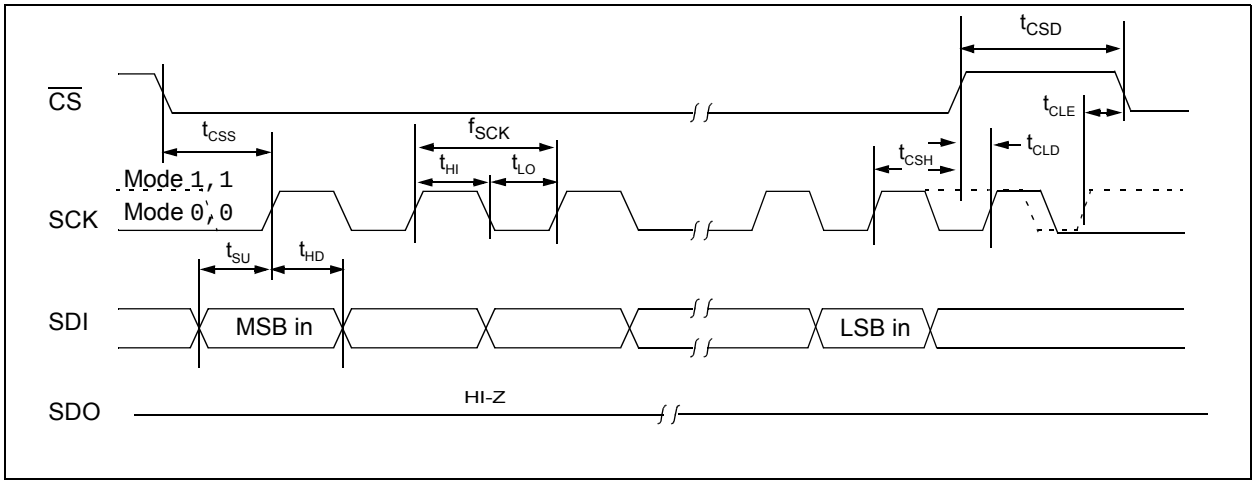


FIGURE 1-2: *Serial Input Timing Diagram.*

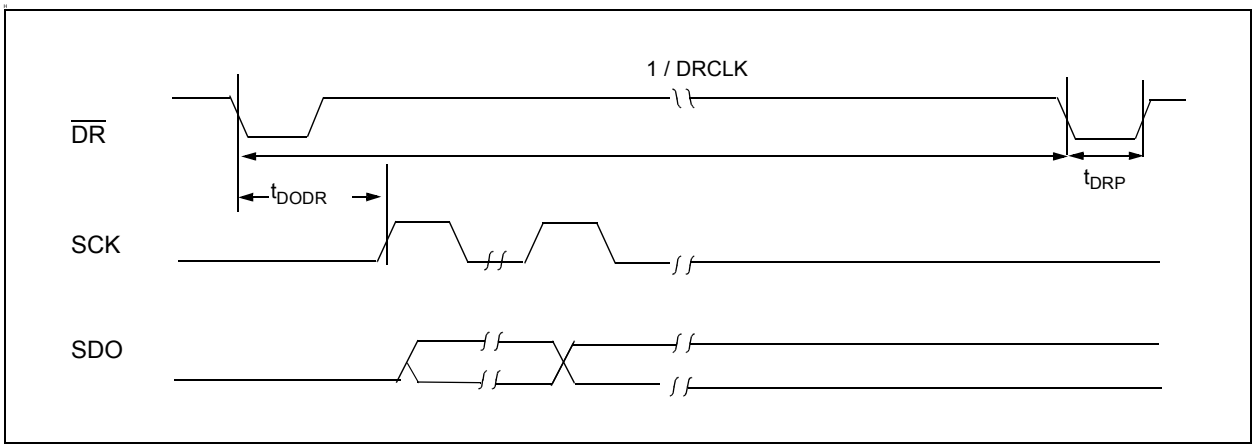


FIGURE 1-3: *Data Ready Pulse Timing Diagram.*

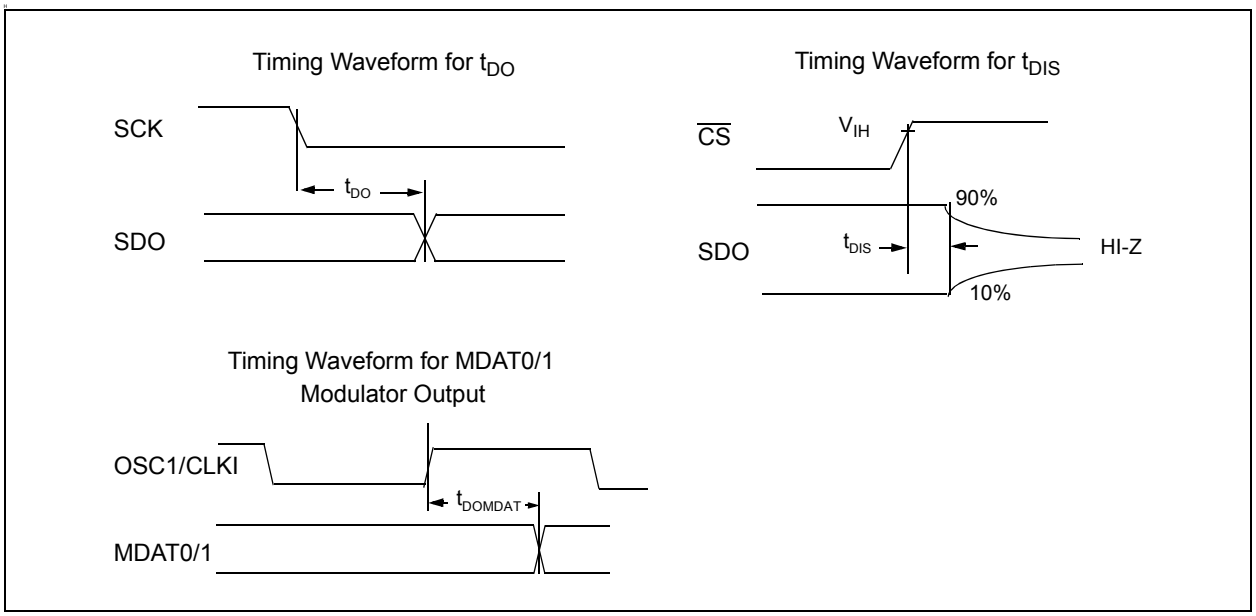


FIGURE 1-4: *Specific Timing Diagrams.*

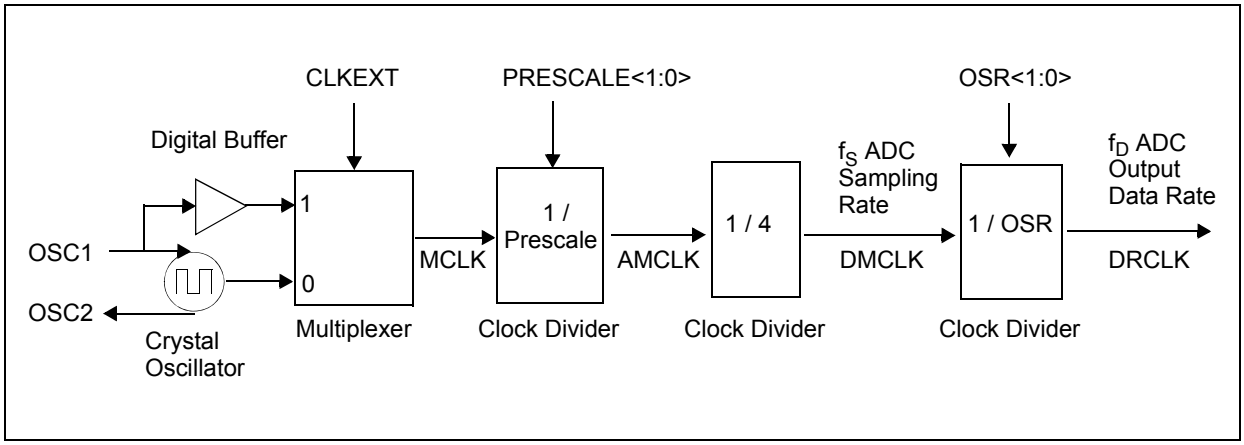


FIGURE 1-5: *MCP3903 Clock Detail.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, AV_{DD} = 5.0V, DV_{DD} = 3.3 V; Internal V_{REF}; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; V_{IN} = -0.5 dBFS @ 60 Hz.

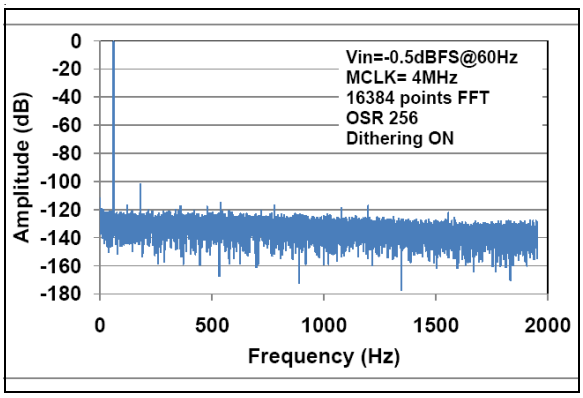


FIGURE 2-1: *Spectral Response.*

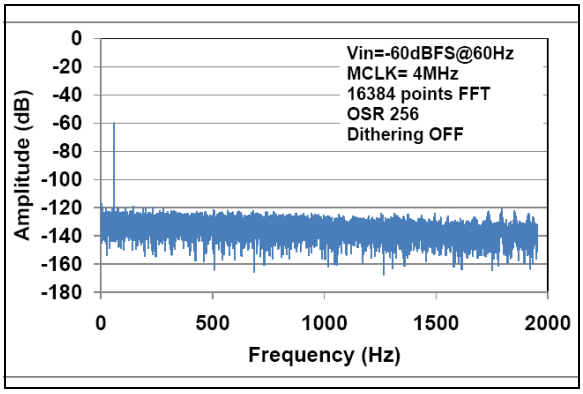


FIGURE 2-4: *Spectral Response.*

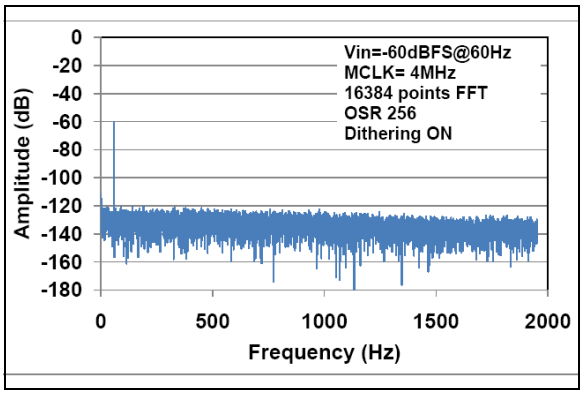


FIGURE 2-2: *Spectral Response.*

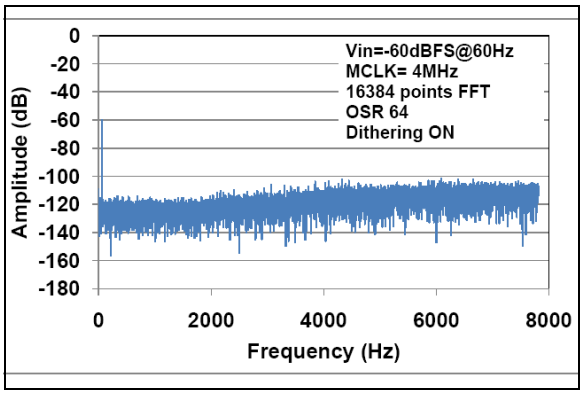


FIGURE 2-5: *Spectral Response.*

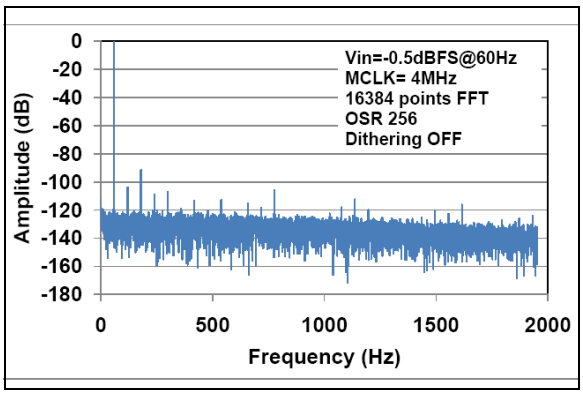


FIGURE 2-3: *Spectral Response.*

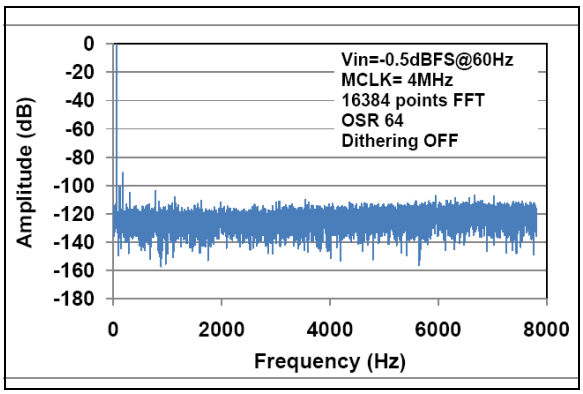


FIGURE 2-6: *Spectral Response.*

Note: Unless otherwise indicated, AV_{DD} = 5.0V, DV_{DD} = 3.3 V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; V_{IN} = -0.5 dBFS @ 60 Hz.

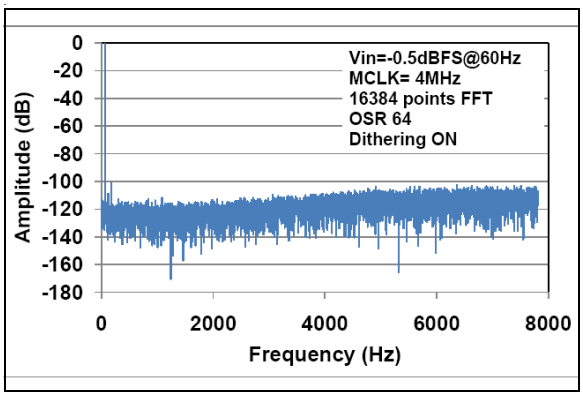


FIGURE 2-7: *Spectral Response.*

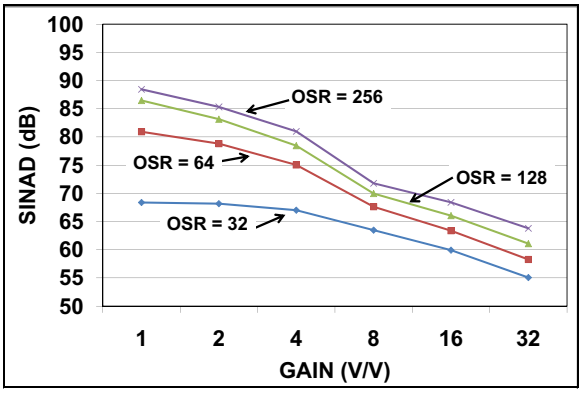


FIGURE 2-10: *Signal-to-Noise and Distortion vs. Gain (Dithering OFF).*

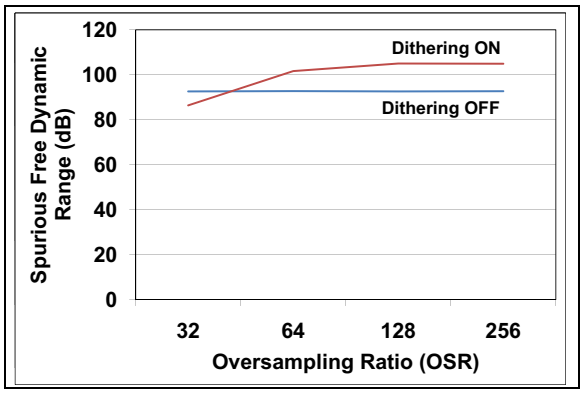


FIGURE 2-8: *Spurious Free Dynamic Range vs Oversampling Ratio.*

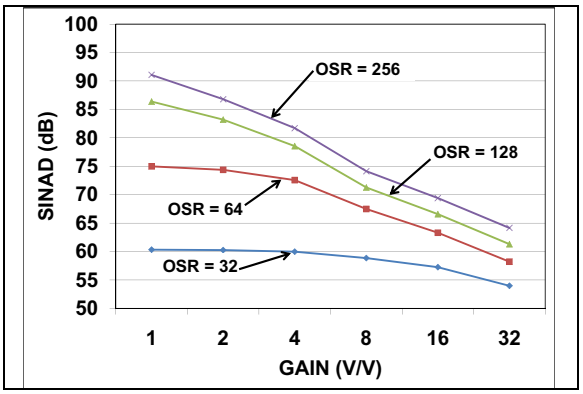


FIGURE 2-11: *Signal-to-Noise and Distortion vs. Gain (Dithering ON).*

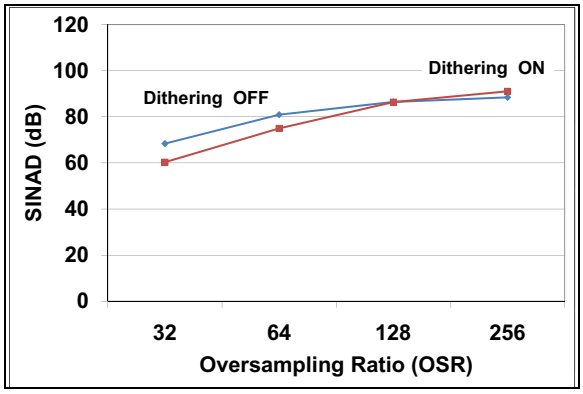


FIGURE 2-9: *Signal-to-Noise and Distortion vs. Oversampling Ratio.*

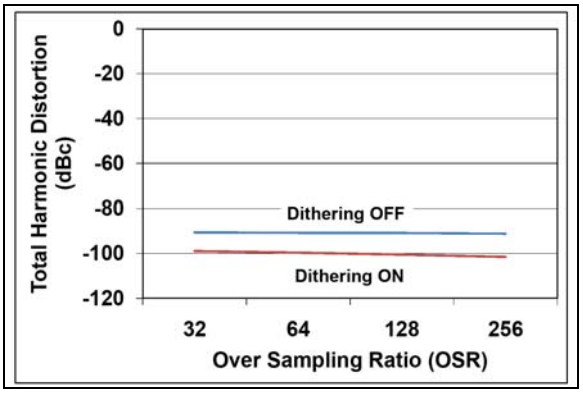


FIGURE 2-12: *Total Harmonic Distortion vs. Oversampling Ratio.*

Note: Unless otherwise indicated, AV_{DD} = 5.0V, DV_{DD} = 3.3 V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; V_{IN} = -0.5 dBFS @ 60 Hz.

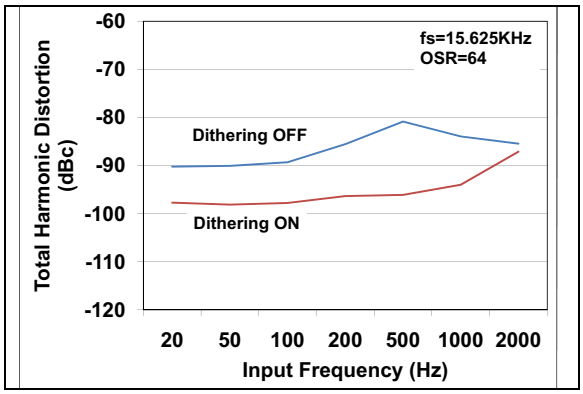


FIGURE 2-13: *Total Harmonic Distortion vs. Input Signal Frequency.*

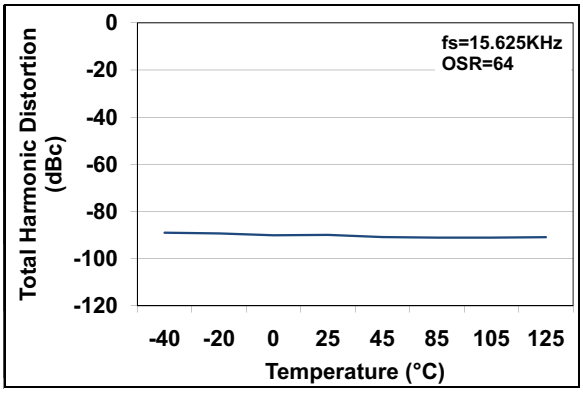


FIGURE 2-14: *Total Harmonic Distortion vs. Temperature.*

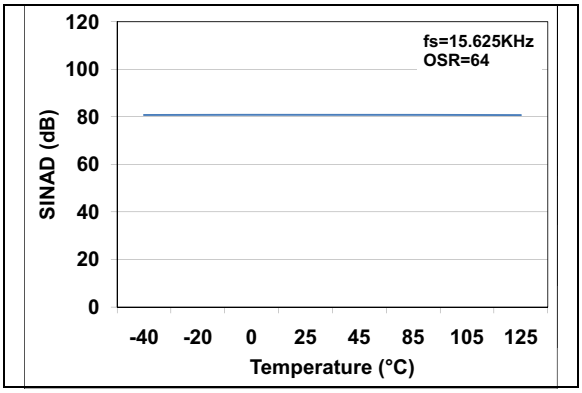


FIGURE 2-16: *Signal-to-Noise and Distortion vs. Temperature.*

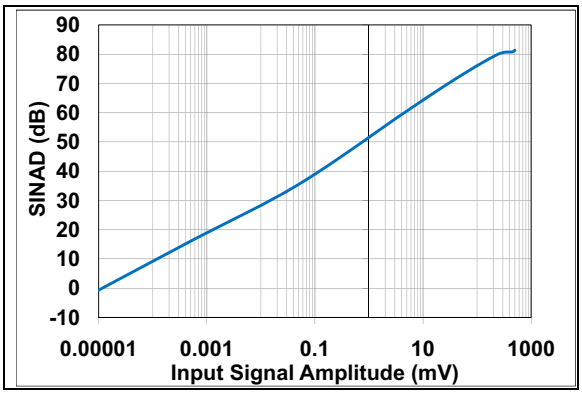


FIGURE 2-17: *Signal-to-Noise and Distortion vs. Input Signal Amplitude.*

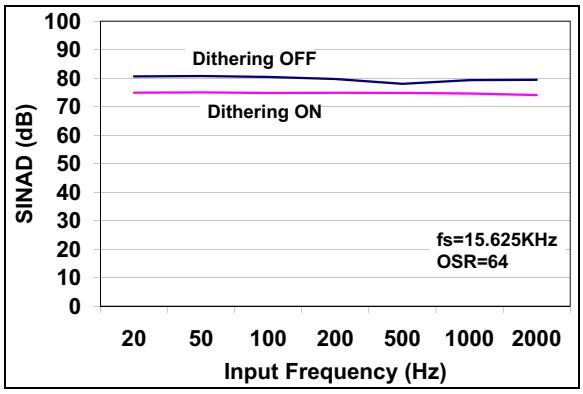


FIGURE 2-15: *Signal-to-Noise and Distortion vs. Input Signal Frequency.*

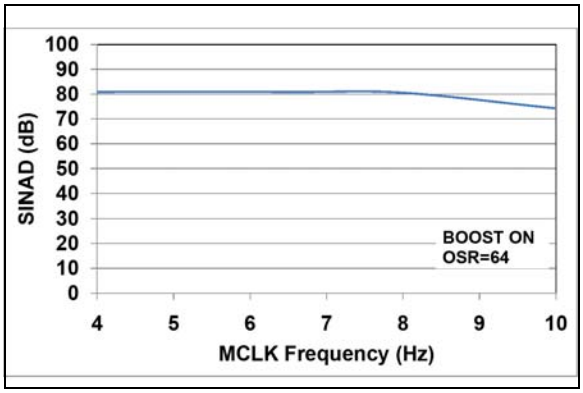


FIGURE 2-18: *Signal-to-Noise and Distortion vs. Master Clock.*

Note: Unless otherwise indicated, AV_{DD} = 5.0V, DV_{DD} = 3.3 V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; V_{IN} = -0.5 dBFS @ 60 Hz.

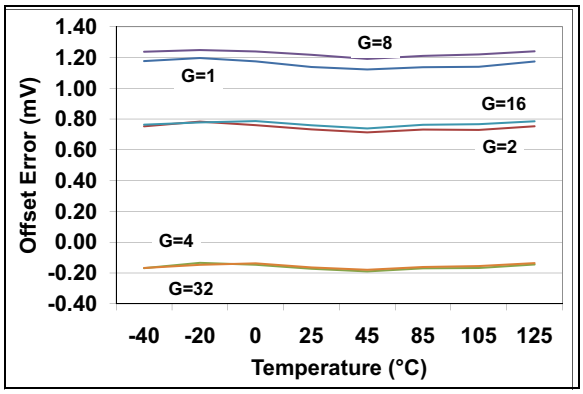


FIGURE 2-19: *Offset Error vs. Temperature (Channel 0).*

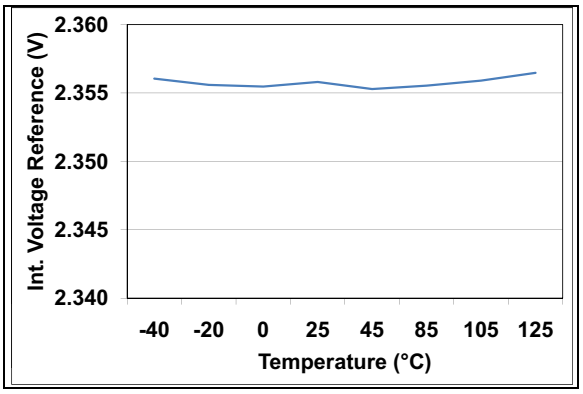


FIGURE 2-22: *Internal Voltage Reference vs. Temperature.*

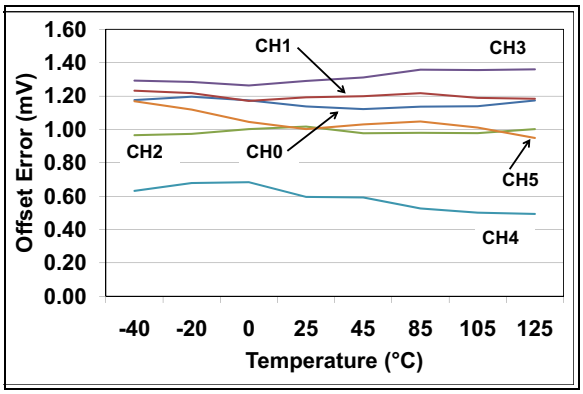


FIGURE 2-20: *Channel-to-Channel Offset Match vs. Temperature.*

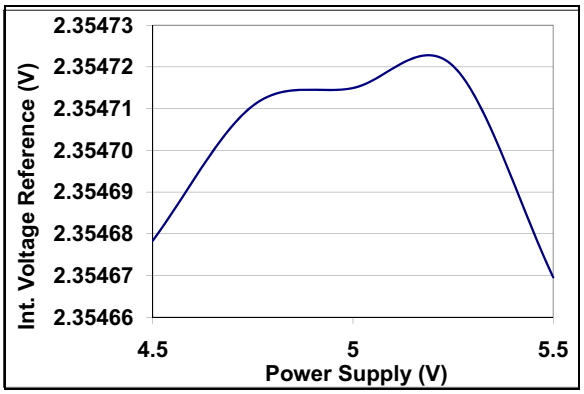


FIGURE 2-23: *Internal Voltage Reference vs. Supply Voltage.*

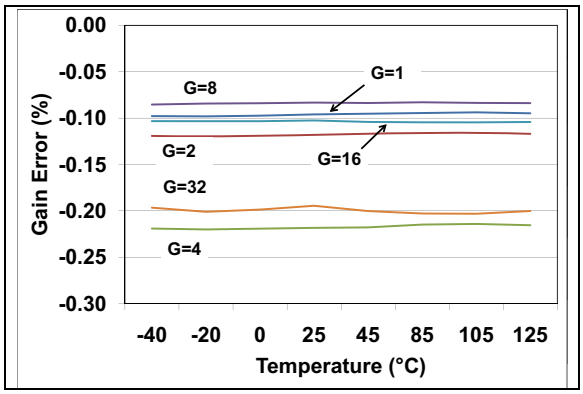


FIGURE 2-21: *Gain Error vs. Temperature.*

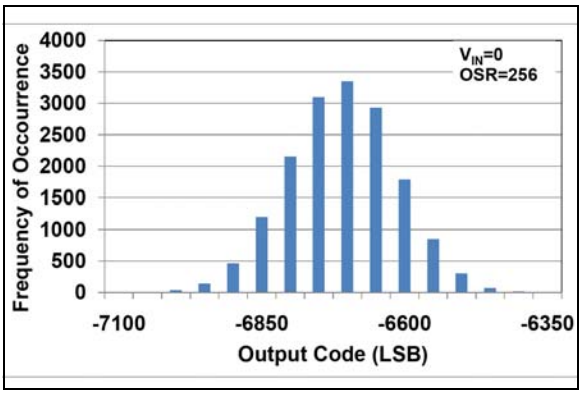


FIGURE 2-24: *Noise Histogram.*

Note: Unless otherwise indicated, AV_{DD} = 5.0V, DV_{DD} = 3.3 V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; V_{IN} = -0.5 dBFS @ 60 Hz.

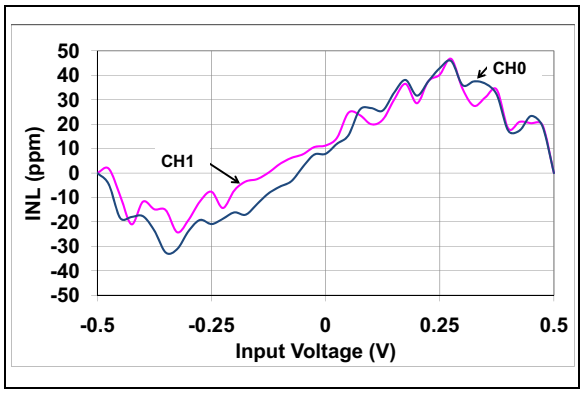


FIGURE 2-25: *Integral Non-Linearity (Dithering OFF).*

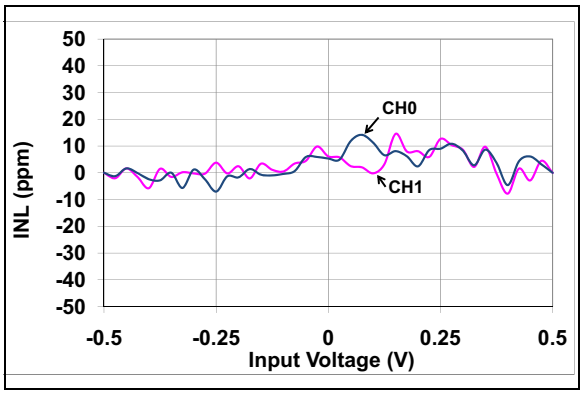


FIGURE 2-26: *Integral Non-Linearity (Dithering ON).*

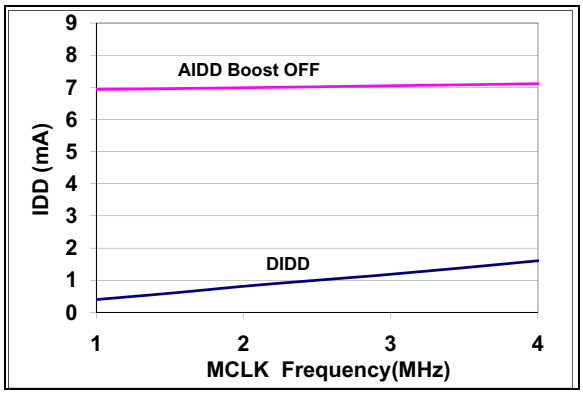


FIGURE 2-27: *Operating Current vs. Master Clock (MCLK).*

3.0 PIN DESCRIPTION

TABLE 3-1: PIN FUNCTION TABLE

Pin No.	Symbol	Function
1	AV_{DD}	Analog Power Supply Pin
2	CH0+	Non-Inverting Analog Input Pin for Channel 0
3	CH0-	Inverting Analog Input Pin for Channel 0
4	CH1-	Inverting Analog Input Pin for Channel 1
5	CH1+	Non-Inverting Analog Input Pin for Channel 1
6	CH2+	Non-Inverting Analog Input Pin for Channel 2
7	CH2-	Inverting Analog Input Pin for Channel 2
8	CH3-	Inverting Analog Input Pin for Channel 3
9	CH3+	Non-Inverting Analog Input Pin for Channel 3
10	CH4+	Non-Inverting Analog Input Pin for Channel 4
11	CH4-	Inverting Analog Input Pin for Channel 4
12	CH5-	Inverting Analog Input Pin for Channel 5
13	CH5+	Non-Inverting Analog Input Pin for Channel 5
14	REFIN+/OUT	Non-Inverting Voltage Reference Input and Internal Reference Output Pin
15	REFIN-	Inverting Voltage Reference Input Pin
16	A_{GND}	Analog Ground Pin, Return Path for internal analog circuitry
17	D_{GND}	Digital Ground Pin, Return Path for internal digital circuitry
18	$\overline{DRA}$	Data Ready Signal Output for channels pair A
19	$\overline{DRB}$	Data Ready Signal Output for channels pair B
20	$\overline{DRC}$	Data Ready Signal Output for channels pair C
21	OSC1	Oscillator Crystal Connection Pin or Clock Input Pin
22	OSC2	Oscillator Crystal Connection Pin
23	$\overline{CS}$	Chip Select for Serial Interface
24	SCK	Serial Interface Clock Pin
25	SDO	Serial Interface Data Output Pin
26	SDI	Serial Interface Data Input Pin
27	$\overline{RESET}$	Master Reset Logic Input Pin
28	DV_{DD}	Digital Power Supply Pin

3.1 $\overline{RESET}$

This pin is active low and places the entire chip in a reset state when active.

When $\overline{RESET}$=0, all registers are reset to their default value, no communication can take place, no clock is distributed inside the part. This state is equivalent to a POR state.

Since the default state of the ADCs is on, the analog power consumption when $\overline{RESET}$ = 0 is equivalent to when $\overline{RESET}$ = 1. Only the digital power consumption is largely reduced because this current consumption is essentially dynamic and is reduced drastically when there is no clock running. All the analog biases are enabled during a reset so that the part is fully operational just after a $\overline{RESET}$ rising edge. This input is Schmitt triggered.

3.2 Digital V_{DD} (DV_{DD})

DV_{DD} is the power supply pin for the digital circuitry within the MCP3903. This pin requires appropriate bypass capacitors and should be maintained between 2.7V and 3.6V for specified operation.

3.3 Analog V_{DD} (AV_{DD})

AV_{DD} is the power supply pin for the analog circuitry within the MCP3903.

This pin requires appropriate bypass capacitors and should be maintained to 5V ±10% for specified operation.

3.4 ADC Differential Analog Inputs(CHn+/CHn-)

CHn- and CHn+, are the two fully-differential analog voltage inputs for the Delta-Sigma ADCs. There are six channels in total grouped in three channel pairs.

The linear and specified region of the channels are dependent on the PGA gain. This region corresponds to a differential voltage range of ±500 mV/GAIN with V_{REF} = 2.4V. The maximum absolute voltage, with respect to AGND, for each CHn+/- input pin is +/-1V with no distortion and ±6V with no breaking after continuous voltage.

3.5 Analog Ground (AGND)

AGND is the ground connection to internal analog circuitry (ADCs, PGA, voltage reference, POR). To ensure accuracy and noise cancellation, this pin must be connected to the same ground as DGND, preferably with a star connection. If an analog ground plane is available, it is recommended that this pin be tied to this plane of the PCB. This plane should also reference all other analog circuitry in the system.

3.6 Non-Inverting Reference Input, Internal Reference Output (REFIN+/OUT)

This pin is the non-inverting side of the differential voltage reference input for all ADCs or the internal voltage reference output. When VREFEXT = 1, and an external voltage reference source can be used, the internal voltage reference is disabled. When using an external differential voltage reference, it should be connected to its V_{REF+} pin.

When using an external single-ended reference, it should be connected to this pin.

When VREFEXT = 0, the internal voltage reference is enabled and connected to this pin through a switch. This voltage reference has minimal drive capability and thus needs proper buffering and bypass capacitances (10 µF tantalum in parallel with 0.1 µF ceramic) if used as a voltage source.

For optimal performance, bypass capacitances should be connected between this pin and AGND at all times even when the internal voltage reference is used.

3.7 Inverting Reference Input (REFIN-)

This pin is the inverting side of the differential voltage reference input for both ADCs. When using an external differential voltage reference, it should be connected to its V_{REF-} pin. When using an external single-ended voltage reference, or when VREFEXT = 0 (Default) and using the internal voltage reference, this pin should be directly connected to AGND.

3.8 Digital Ground Connection (DGND)

DGND is the ground connection to internal digital circuitry (SINC filters, oscillator, serial interface). To ensure accuracy and noise cancellation, DGND must be connected to the same ground as AGND, preferably with a star connection. If a digital ground plane is available, it is recommended that this pin be tied to this plane of the Printed Circuit Board (PCB). This plane should also reference all other digital circuitry in the system.

3.9 $\overline{DR}$n (Data Ready Pins)

The Data Ready pins indicate if a new conversion result is ready to be read on each of the A, B and C pairs of ADCs. The default state of this pin is high when DR_HIZN=1 and is high impedance when DR_HIZN=0 (Default). After each conversion is finished, a low pulse will take place on the data ready pins to indicate the conversion result is ready as an interrupt. This pulse is synchronous with the master clock and has a defined and constant width.

The Data Ready pins are independent of the SPI interface and act like an interrupt output.The Data Ready pins state is not latched and the pulse width (and period) are both determined by the MCLK frequency, over-sampling rate, and internal clock pre-scale settings. The DR pulse width is equal to one DMCLK period and the frequency of the pulses is equal to DRCLK (see Figure 1-3).

Note:	These pins should not be left floating when $\overline{DR}$_HIZ bit is low; a 100kΩ pull-up resistor connected to DV_{DD} is recommended.

3.10 Oscillator And Master Clock Input Pins (OSC1/CLKI, OSC2)

OSC1/CLKI and OSC2 provide the master clock for the device. When CLKEXT = 0 (Default), a resonant crystal or clock source with a similar sinusoidal waveform must be placed across these pins to ensure proper operation. The typical clock frequency specified is 4 MHz. However, the clock frequency can be 1 MHz to 5 MHz without disturbing ADC accuracy. With the current boost circuit enabled, the master clock can be used up to 8.192 MHz without disturbing ADC accuracy. Appropriate load capacitance should be connected to these pins for proper operation.

Note:	When CLKEXT = 1, the crystal oscillator is disabled, as well as the OSC2 input. The OSC1 becomes the master clock input CLKI, direct path for an external clock source, for example a clock source generated by an MCU.

3.11 $\overline{CS}$ (Chip Select)

This pin is the SPI Chip Select that enables the serial communication. When this pin is high, no communication can take place. A chip select falling edge initiates the serial communication and a chip select rising edge terminates the communication. No communication can take place even when $\overline{CS}$ is low and when $\overline{RESET}$ is low.

This input is Schmitt-triggered.

3.12 SCK (Serial Data Clock)

This is the serial clock pin for SPI communication. Data is clocked into the device on the RISING edge of SCK. Data is clocked out of the device on the FALLING edge of SCK. The MCP3903 interface is compatible with both SPI 0,0 and 1,1 modes. The maximum clock speed specified is 10 MHz. This input is Schmitt triggered.

3.13 SDO (Serial Data Output)

This is the SPI data output pin. Data is clocked out of the device on the FALLING edge of SCK. This pin stays at high impedance during the control byte. It also stays at high impedance during the whole communication for write commands and when the CS pin is high or when the RESET pin is low. This pin is active only when a read command is processed. Each read is processed by a packet of 24 bits (size of each register), except on the ADC output registers when WIDTH=0.

3.14 SDI (Serial Data Input)

This is the SPI data input pin. Data is clocked into the device on the RISING edge of SCK. When CS is low, this pin is used to communicate with a series of 8-bit commands. The interface is half-duplex (inputs and outputs do not happen at the same time). Each communication starts with a chip select falling edge followed by an 8-bit control byte entered through the SDI pin. Each write is processed by packets of 24 bits (size of each register). Each command is either a Read or a Write command. Toggling SDI during a Read command has no effect. This input is Schmitt-triggered.

4.0 TERMINOLOGY AND FORMULAS

This section defines the terms and formulas used throughout this data sheet. The following terms are defined:

MCLK - Master Clock

AMCLK - Analog Master Clock

DMCLK - Digital Master Clock

DRCLK - Data Rate Clock

OSR - Oversampling Ratio

Offset Error

Gain Error

Integral Non-Linearity Error

Signal-To-Noise Ratio (SNR)

Signal-To-Noise Ratio And Distortion (SINAD)

Total Harmonic Distortion (THD)

Spurious-Free Dynamic Range (SFDR)

MCP3903 Delta-Sigma Architecture

Idle Tones

Dithering

Crosstalk

PSRR

CMRR

ADC Reset Mode

Hard Reset Mode (RESET = 0)

ADC Shutdown Mode

Full Shutdown Mode

4.1 MCLK - Master Clock

This is the fastest clock present in the device. This is the frequency of the crystal placed at the OSC1/OSC2 inputs when CLKEXT = 0 or the frequency of the clock input at the OSC1/CLKI when CLKEXT = 1.

4.2 AMCLK - Analog Master Clock

This is the clock frequency that is present on the analog portion of the device, after prescaling has occurred via the CONFIG PRESCALE<1:0> register bits. The analog portion includes the PGAs and the two sigma-delta modulators.

EQUATION 4-1:

$$AMCLK = \frac{MCLK}{PRESCALE}$$

TABLE 4-1: MCP3903 OVERSAMPLING RATIO SETTINGS

Config PRE<1:0>		Analog Master Clock Prescale
0	0	AMCLK = MCLK/ 1 (default)
0	1	AMCLK = MCLK/ 2
1	0	AMCLK = MCLK/ 4
1	1	AMCLK = MCLK/ 8

4.3 DMCLK - Digital Master Clock

This is the clock frequency that is present on the digital portion of the device, after prescaling and division by 4. This is also the sampling frequency, that is the rate at which the modulator outputs are refreshed. Each period of this clock corresponds to one sample and one modulator output.

EQUATION 4-2:

$$DMCLK = \frac{AMCLK}{4} = \frac{MCLK}{4 \times PRESCALE}$$

4.4 DRCLK - Data Rate Clock

This is the output data rate i.e. the rate at which the ADCs output new data. Each new data is signaled by a data ready pulse on the $\overline{DR}$ pin.

This data rate is depending on the OSR and the prescaler with the following formula:

EQUATION 4-3:

$$DRCLK = \frac{DMCLK}{OSR} = \frac{AMCLK}{4 \times OSR} = \frac{MCLK}{4 \times OSR \times PRESCALE}$$

Since this is the output data rate, and since the decimation filter is a SINC (or notch) filter, there is a notch in the filter transfer function at each integer multiple of this rate.

The following table describes the various combinations of OSR and PRESCALE and their associated AMCLK, DMCLK and DRCLK rates.

TABLE 4-2: DEVICE DATA RATES IN FUNCTION OF MCLK, OSR, AND PRESCALE

PRE <1:0>		OSR <1:0>		OSR	AMCLK	DMCLK	DRCLK	DRCLK (ksps)
1	1	1	1	256	MCLK/8	MCLK/32	MCLK/8192	0.4882
1	1	1	0	128	MCLK/8	MCLK/32	MCLK/4096	0.976
1	1	0	1	64	MCLK/8	MCLK/32	MCLK/2048	1.95
1	1	0	0	32	MCLK/8	MCLK/32	MCLK/1024	3.9
1	0	1	1	256	MCLK/4	MCLK/16	MCLK/4096	0.976
1	0	1	0	128	MCLK/4	MCLK/16	MCLK/2048	1.95
1	0	0	1	64	MCLK/4	MCLK/16	MCLK/1024	3.9
1	0	0	0	32	MCLK/4	MCLK/16	MCLK/512	7.8125
0	1	1	1	256	MCLK/2	MCLK/8	MCLK/2048	1.95
0	1	1	0	128	MCLK/2	MCLK/8	MCLK/1024	3.9
0	1	0	1	64	MCLK/2	MCLK/8	MCLK/512	7.8125
0	1	0	0	32	MCLK/2	MCLK/8	MCLK/256	15.625
0	0	1	1	256	MCLK	MCLK/4	MCLK/1024	3.9
0	0	1	0	128	MCLK	MCLK/4	MCLK/512	7.8125
0	**0**	**0**	**1**	**64**	**MCLK**	MCLK/4	MCLK/256	**15.625**
0	0	0	0	32	MCLK	MCLK/4	MCLK/128	31.25

Note: For OSR = 32 and 64, DITHER = 0. For OSR = 128 and 256, DITHER = 1.

4.5 OSR - Oversampling Ratio

The ratio of the sampling frequency to the output data rate is OSR = DMCLK/DRCLK. The default OSR is 64, or with MCLK = 4 MHz, PRESCALE = 1, AMCLK = 4 MHz, f_S = 1 MHz, f_D = 15.625 ksps. The following bits in the CONFIG1 register are used to change the oversampling ratio (OSR).

TABLE 4-3: MCP3903 OVERSAMPLING RATIO SETTINGS

CONFIG OSR<1:0>		OVER SAMPLING RATIO (OSR)
0	0	32
0	1	64 (DEFAULT)
1	0	128
1	1	256

4.6 Offset Error

This is the error induced by the ADC when the inputs are shorted together (V_{IN} = 0V). The specification incorporates both PGA and ADC offset contributions. This error varies with PGA and OSR settings. The offset is different on each channel and varies from chip to chip. This offset error can easily be calibrated out by a MCU with a subtraction. The offset is specified in mV.

The offset on the MCP3903 has a low temperature coefficient, see **Section 2.0 "Typical Performance Curves"**.

4.7 Gain Error

This is the error induced by the ADC on the slope of the transfer function. It is the deviation expressed in % compared to the ideal transfer function defined by Equation 5-3. The specification incorporates both PGA and ADC gain error contributions, but not the V_{REF} contribution (it is measured with an external V_{REF}).This error varies with PGA and OSR settings.

The gain error on the MCP3903 has a low temperature coefficient. See the typical performance curves for more information.

4.8 Integral Non-Linearity Error

Integral non-linearity error is the maximum deviation of an ADC transition point from the corresponding point of an ideal transfer function, with the offset and gain errors removed, or with the end points equal to zero.

It is the maximum remaining error after calibration of offset and gain errors for a DC input signal.

4.9 Signal-To-Noise Ratio (SNR)

For the MCP3903 ADC, the signal-to-noise ratio is a ratio of the output fundamental signal power to the noise power (not including the harmonics of the signal), when the input is a sinewave at a predetermined frequency. It is measured in dB. Usually, only the maximum signal to noise ratio is specified. The SNR figure depends mainly on the OSR and DITHER settings of the device.

EQUATION 4-4: SIGNAL-TO-NOISE RATIO

$$SNR(dB) = 10log\left(\frac{SignalPower}{NoisePower}\right)$$

4.10 Signal-To-Noise Ratio And Distortion (SINAD)

The most important figure of merit for the analog performance of the ADCs present on the MCP3903 is the Signal-to-Noise And Distortion (SINAD) specification.

Signal-to-noise and distortion ratio is similar to signal-to-noise ratio, with the exception that you must include the harmonics power in the noise power calculation. The SINAD specification depends mainly on the OSR and DITHER settings.

EQUATION 4-5: SINAD EQUATION

$$SINAD(dB) = 10\log\left(\frac{SignalPower}{Noise + HarmonicsPower}\right)$$

The calculated combination of SNR and THD per the following formula also yields SINAD:

EQUATION 4-6: SINAD, THD, AND SNR RELATIONSHIP

$$SINAD(dB) = 10log\left[10^{\left(\frac{SNR}{10}\right)} + 10^{\left(\frac{-THD}{10}\right)}\right]$$

4.11 Total Harmonic Distortion (THD)

The total harmonic distortion is the ratio of the output harmonics power to the fundamental signal power for a sinewave input and is defined by the following equation.

EQUATION 4-7:

$$THD(dB) = 10log\left(\frac{HarmonicsPower}{FundamentalPower}\right)$$

The THD calculation includes the first 35 harmonics for the MCP3903 specifications. The THD is usually only measured with respect to the 10 first harmonics. THD is sometimes expressed in %. For converting the THD in %, here is the formula:

EQUATION 4-8:

$$THD(\%) = 100 \times 10^{\frac{THD(dB)}{20}}$$

This specification depends mainly on the DITHER setting.

4.12 Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio between the output power of the fundamental and the highest spur in the frequency spectrum. The spur frequency is not necessarily a harmonic of the fundamental even though it is usually the case. This figure represents the dynamic range of the ADC when a full-scale signal is used at the input. This specification depends mainly on the DITHER setting.

EQUATION 4-9:

$$SFDR(dB) = 10log\left(\frac{FundamentalPower}{HighestSpurPower}\right)$$

4.13 MCP3903 Delta-Sigma Architecture

The MCP3903 incorporates six Delta-Sigma ADCs with a multi-bit digital to analog converter as quantizer. A Delta-Sigma ADC is an oversampling converter that incorporates a built-in modulator which is digitizing the quantity of charge integrated by the modulator loop (see Figure 5-1). The quantizer is the block that is performing the analog-to-digital conversion. The quantizer is typically 1-bit, or a simple comparator which helps to maintain the linearity performance of the ADC (the DAC structure is inherently linear in this case).

Multi-bit quantizers help to lower the quantization error (the error fed back in the loop can be very large with 1-bit quantizers) without changing the order of the modulator or the OSR, which leads to better SNR figures. However, typically, the linearity of such architectures is more difficult to achieve since the DAC is no more simple to realize and its linearity limits the THD of such ADCs.

The MCP3903's 5-level quantizer is a flash ADC composed of 4 comparators arranged with equally spaced thresholds and a thermometer coding. The MCP3903 also includes proprietary 5-level DAC architecture that is inherently linear for improved THD figures.

4.14 Idle Tones

A Delta-Sigma converter is an integrating converter. It also has a finite quantization step (LSB) which can be detected by its quantizer. A DC input voltage that is below the quantization step should only provide an all zeros result since the input is not large enough to be detected. As an integrating device, any Delta-Sigma will show, in this case, idle tones. This means that the output will have spurs in the frequency content that are depending on the ratio between quantization step voltage and the input voltage. These spurs are the result of the integrated sub-quantization step inputs that will eventually cross the quantization steps after a long enough integration. This will induce an AC frequency at the output of the ADC and can be shown in the ADC output spectrum.

These idle tones are residues that are inherent to the quantization process and the fact that the converter is integrating at all times without being reset. They are residues of the finite resolution of the conversion process. They are very difficult to attenuate and they are heavily signal dependent. They can degrade both SFDR and THD of the converter, even for DC inputs. They can be localized in the baseband of the converter and thus difficult to filter from the actual input signal.

For power metering applications, idle tones can be very disturbing because energy can be detected even at the 50 or 60 Hz frequency, depending on the DC offset of the ADCs, while no power is really present at the inputs. The only practical way to suppress or attenuate idle tones phenomenon is to apply dithering to the ADC. The idle tones amplitudes are a function of the order of the modulator, the OSR and the number of levels in the quantizer of the modulator. A higher order, a higher OSR, or a higher number of levels for the quantizer will attenuate the idle tones amplitude.

4.15 Dithering

In order to suppress or attenuate the idle tones present in any Delta-Sigma ADCs, dithering can be applied to the ADC. Dithering is the process of adding an error to the ADC feedback loop in order to "decorrelate" the outputs and "break" the idle tone's behavior. Usually a random or pseudo-random generator adds an analog or digital error to the feedback loop of the delta-sigma ADC in order to ensure that no tonal behavior can happen at its outputs. This error is filter by the feedback loop and typically has a zero average value so that the converter static transfer function is not disturbed by the dithering process. However, the dithering process slightly increases the noise floor (it adds noise to the part) while reducing its tonal behavior and thus improving SFDR and THD. The dithering process scrambles the idle tones into baseband white noise and ensures that dynamic specs (SNR, SINAD, THD, SFDR) are less signal dependent. The MCP3903 incorporates a proprietary dithering algorithm on all ADCs in order to remove idle tones and improve THD, which is crucial for power metering applications.

4.16 Crosstalk

The crosstalk is defined as the perturbation caused by one ADC channel on the other ADC channel. It is a measurement of the isolation between the six ADCs present in the chip.

This measurement is a two-step procedure:

1. Measure one ADC input with no perturbation on any other ADC (ADC inputs shorted).
2. Measure the same ADC input with a perturbation sine wave signal on the other ADC at a certain predefined frequency.

The crosstalk is then the ratio between the output power of the ADC when the perturbation is present and when it is not divided by the power of the perturbation signal.

A lower crosstalk value implies more independence and isolation between the six channels.

The measurement of this signal is performed under the following conditions:

- GAIN = 1,
- PRESCALE = 1,
- OSR = 256,
- MCLK = 4 MHz

Step 1

- CH0+=CH0-=AGND
- CHn+=CHn-=AGND, n different than 0

Step 2

- CH0+=CH0-=AGND
- CHn+ - CHn-=1V_{P-P} @ 50/60 Hz (Full-scale sine wave)

The crosstalk is then calculated with the following formula:

EQUATION 4-10:

$$CTalk(dB) = 10log\left(\frac{\Delta CH0Power}{\Delta CHnPower}\right)$$

4.17 PSRR

This is the ratio between a change in the power supply voltage and the ADC output codes. It measures the influence of the power supply voltage on the ADC outputs.

The PSRR specification can be DC (the power supply is taking multiple DC values) or AC (the power supply is a sinewave at a certain frequency with a certain common mode). In AC, the amplitude of the sinewave is representing the change in the power supply.

It is defined as:

EQUATION 4-11:

$$PSRR(dB) = 20log\left(\frac{\Delta V_{OUT}}{\Delta AV_{DD}}\right)$$

Where V_{OUT} is the equivalent input voltage that the output code translates to with the ADC transfer function. In the MCP3903 specification, AV_{DD} varies from 4.5V to 5.5V, and for AC PSRR a 50/60 Hz sinewave is chosen, centered around 5V with a maximum 500 mV amplitude. The PSRR specification is measured with DV_{DD} = 3.3V.

4.18 CMRR

This is the ratio between a change in the Common-Mode input voltage and the ADC output codes. It measures the influence of the Common-Mode input voltage on the ADC outputs.

The CMRR specification can be DC (the common-mode input voltage is taking multiple DC values) or AC (the common-mode input voltage is a sinewave at a certain frequency with a certain common mode). In AC, the amplitude of the sinewave is representing the change in the power supply.

It is defined as:

EQUATION 4-12:

$$CMRR(dB) = 20log\left(\frac{\Delta V_{OUT}}{\Delta V_{CM}}\right)$$

Where V_{CM}= (CHn+ + CHn-)/2 is the Common-Mode input voltage and V_{OUT} is the equivalent input voltage that the output code translates to with the ADC transfer function. In the MCP3903 specification, VCM varies from -1V to +1V, and for AC specification a 50/60 Hz sinewave is chosen centered around 0V with a 500 mV amplitude.

4.19 ADC Reset Mode

ADC Reset mode (called also soft reset mode) can only be entered through setting high the RESET<5:0> bits in the configuration register. This mode is defined as the condition where the converters are active but their output is forced to 0.

The registers are not affected in this reset mode and retain their values.

The ADCs can immediately output meaningful codes after leaving reset mode (and after the sinc filter settling time of 3/DRCLK). This mode is both entered and exited through setting of bits in the configuration register.

Each converter can be placed in soft reset mode independently. The configuration registers are not modified by the soft reset mode.

A data ready pulse will not be generated by any ADC while in reset mode.

When an ADC exists ADC reset mode, any phase delay present before reset was entered will still be present. If one ADC was not in reset, the ADC leaving reset mode will automatically resynchronize the phase delay relative to the other ADC channel, per the phase delay register block and give data ready pulses accordingly.

If an ADC is placed in Reset mode while the other is converting, it is not shutting down the internal clock. When going back out of reset, it will be resynchronized automatically with the clock that did not stop during reset.

If all ADCs are in soft reset or shutdown modes, the clock is no longer distributed to the digital core for low power operation. Once the ADC is back to normal operation, the clock is automatically distributed again.

4.20 Hard Reset Mode ($\overline{\text{RESET}}$ = 0)

This mode is only available during a POR or when the $\overline{\text{RESET}}$ pin is pulled low. The $\overline{\text{RESET}}$ pin low state places the device in a hard reset mode.

In this mode, all internal registers are reset to their default state.

The DC biases for the analog blocks are still active, i.e. the MCP3903 is ready to convert. However, this pin clears all conversion data in the ADCs. The comparator outputs of all ADCs are forced to their reset state (0011). The SINC filters are all reset, as well as their double output buffers. See serial timing for minimum pulse low time, in **Section 1.0 "Electrical Characteristics"**.

During a hard reset, no communication with the part is possible. The digital interface is maintained in a reset state.

4.21 ADC Shutdown Mode

ADC shutdown mode is defined as a state where the converters and their biases are off, consuming only leakage current. After this is removed, start-up delay time (SINC filter settling time) will occur before outputting meaningful codes. The start-up delay is needed to power-up all DC biases in the channel that was in shutdown. This delay is the same than t_{POR} and any $\overline{\text{DR}}$ pulse coming within this delay should be discarded.

Each converter can be placed in shutdown mode independently. The CONFIG registers are not modified by the shutdown mode. This mode is only available through programming of the SHUTDOWN<5:0> bits in the CONFIG register.

The output data is flushed to all zeros while in ADC shutdown. No data ready pulses are generated by any ADC while in ADC shutdown mode.

When an ADC exits ADC shutdown mode, any phase delay present before shutdown was entered will still be present. If one ADC was not in shutdown, the ADC leaving shutdown mode will automatically resynchronize the phase delay relative to the other ADC channel, per the phase delay register block and give data ready pulses accordingly.

If an ADC is placed in shutdown while others are converting, then the internal clock will not shut down. When going back out of shutdown, it will be automatically resynchronized with the clock that did not stop during reset.

If all ADCs are in ADC reset or ADC shutdown modes, the clock is not distributed to the digital core for low power operation. Once any of the ADC is back to normal operation, the clock is automatically distributed again.

4.22 Full Shutdown Mode

The lowest power consumption can be achieved when SHUTDOWN<5:0>=111111, VREFEXT=CLKEXT= 1. This mode is called "Full shutdown mode", and no analog circuitry is enabled. In this mode, the POR A_{VDD} monitoring circuit is also disabled. When the clock is idle (OSC1 = high or low continuously), no clock is propagated throughout the chip. All ADCs are in shutdown, the internal voltage reference is disabled and the internal oscillator is disabled.

The only circuit that remains active is the SPI interface but this circuit does not induce any static power consumption. If SCK is idle, the only current consumption comes from the leakage currents induced by the transistors and is less than 1 µA on each power supply, for temperatures lower than 85°C.

This mode can be used to power down the chip completely and avoid power consumption when there is no data to convert at the analog inputs. Any SCK or MCLK edge coming while in this mode will induce dynamic power consumption.

Once any of the SHUTDOWN, CLKEXT and VREFEXT bits returns to 0, the POR AV_{DD} monitoring block is back to operation and AV_{DD} monitoring can take place.

5.0 DEVICE OVERVIEW

5.1 Analog Inputs (CHn+/-)

The MCP3903 analog inputs can be connected directly to current and voltage transducers (such as shunts, current transformers, or Rogowski coils). Each input pin is protected by specialized ESD structures that are certified to pass 5 kV HBM and 500V MM contact charge. These structures allow bipolar ±6V continuous voltage with respect to AGND, to be present at their inputs without the risk of permanent damage.

All channels have fully differential voltage inputs for better noise performance. The absolute voltage at each pin relative to AGND should be maintained in the ±1V range during operation in order to ensure the specified ADC accuracy. The Common-Mode signals should be adapted to respect both the previous conditions and the differential input voltage range. For best performance, the Common-Mode signals should be maintained to AGND.

5.2 Programmable Gain Amplifiers (PGA)

The six Programmable Gain Amplifiers (PGAs) reside at the front-end of each Delta-Sigma ADC. They have two functions: translate the common-mode of the input from AGND to an internal level between AGND and A_{VDD}, and amplify the input differential signal. The translation of the common mode does not change the differential signal but recenters the common-mode so that the input signal can be properly amplified.

The PGA block can be used to amplify very low signals, but the differential input range of the delta-sigma modulator must not be exceeded. The PGA is controlled by the PGA_CHn<2:0> bits in the GAIN register. The following table represents the gain settings for the PGA:

TABLE 5-1: PGA CONFIGURATION SETTING

Gain PGA_CHn<2:0>			Gain (V/V)	Gain (dB)	V_{IN} Range (V)
0	0	0	1	0	±0.5
0	0	1	2	6	±0.25
0	1	0	4	12	±0.125
0	1	1	8	18	±0.0625
1	0	0	16	24	±0.03125
1	0	1	32	30	±0.015625

5.3 Delta-Sigma Modulator

5.3.1 ARCHITECTURE

All ADCs are identical in the MCP3903 and they include a second-order modulator with a multi-bit DAC architecture (see Figure 5-1). The quantizer is a flash ADC composed of 4 comparators with equally spaced thresholds and a thermometer output coding. The proprietary 5-level architecture ensures minimum quantization noise at the outputs of the modulators without disturbing linearity or inducing additional distortion. The sampling frequency is DMCLK (typically 1 MHz with MCLK=4 MHz) so the modulator outputs are refreshed at a DMCLK rate. The modulator outputs are available in the MOD register.

Each modulator also includes a dithering algorithm that can be enabled through the DITHER<5:0> bits in the configuration register. This dithering process improves THD and SFDR (for high OSR settings) while increasing slightly the noise floor of the ADCs. For power metering applications and applications that are distortion-sensitive, it is recommended to keep DITHER enabled for all ADCs. In the case of power metering applications, THD and SFDR are critical specifications to optimize SNR (noise floor). This is not really problematic due to large averaging factor at the output of the ADCs, therefore even for low OSR settings, the dithering algorithm will show a positive impact on the performance of the application.

Figure 5-1 represents a simplified block diagram of the Delta-Sigma ADC present on MCP3903.

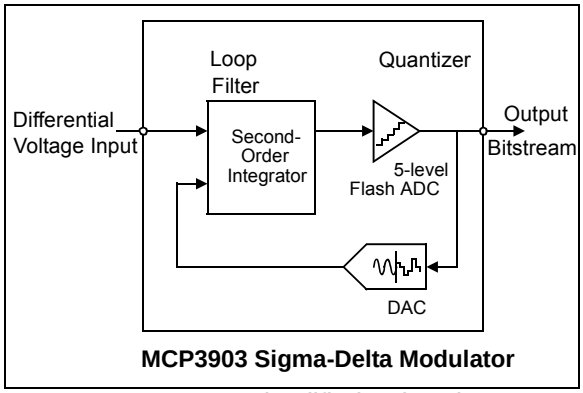


FIGURE 5-1: *Simplified Delta-Sigma ADC Block Diagram.*

5.3.2 MODULATOR INPUT RANGE AND SATURATION POINT

For a specified voltage reference value of 2.4V, the modulator specified differential input range is ±500 mV. The input range is proportional to V_{REF} and scales according to the V_{REF} voltage. This range ensures the stability of the modulator over amplitude and frequency. Outside of this range, the modulator is still functional, however its stability is no longer guaranteed and therefore it is not recommended to exceed this limit. The saturation point for the modulator is $V_{REF}/3$ since the transfer function of the ADC includes a gain of 3 by default (independent from the PGA setting. See **Section 5.5 "ADC OUTPUT CODING"**).

5.3.3 BOOST MODE

The Delta-Sigma modulators also include an independent BOOST mode for each channel. If the corresponding BOOST<1:0> bit is enabled, the power consumption of the modulator is multiplied by 2 and its bandwidth is increased to be able to sustain AMCLK clock frequencies up to 8.192 MHz while keeping the ADC accuracy. When disabled, the power consumption returns back to normal and the AMCLK clock frequencies can only reach up to 5 MHz without affecting ADC accuracy.

5.4 SINC^3 Filter

All ADCs present in the MCP3903 include a decimation filter that is a third-order sinc (or notch) filter. This filter processes the multi-bit bitstream into 16 or 24 bits words (depending on the WIDTH configuration bit). The settling time of the filter is 3 DMCLK periods. It is recommended to discard unsettled data to avoid data corruption which can be done easily by setting the DR_LTY bit high in the STATUS/COM register.

The resolution achievable at the output of the sinc filter (the output of the ADC) is dependant on the OSR and is summarized in the following table:

TABLE 5-2: ADC RESOLUTION VS. OSR

OSR<1:0>		OSR	ADC Resolution (bits) No Missing Codes
0	0	32	17
0	1	64	20
1	0	128	23
1	1	256	24

For 24 -bit output mode (WIDTH = 1), the output of the sinc filter is padded with least significant zeros for any resolution less than 24 bits.

For 16-bit output modes, the output of the sinc filter is rounded to the closest 16-bit number in order to conserve only 16-bit words and to minimize truncation error.

The gain of the transfer function of this filter is 1 at each multiple of DMCLK (typically 1 MHz) so a proper anti-aliasing filter must be placed at the inputs to attenuate the frequency content around DMCLK, and keep the desired accuracy over the baseband of the converter. This anti-aliasing filter can be a simple first-order RC network, with a sufficiently low time constant to generate high rejection at DMCLK frequency.

EQUATION 5-1: SINC FILTER TRANSFER FUNCTION H(Z)

$$H(z) = \left(\frac{1 - z^{-OSR}}{OSR(1 - z^{-1})}\right)^3$$

Where:

$$z = \exp\left(\frac{2\pi fj}{DMCLK}\right)$$

The Normal-Mode Rejection Ratio (NMRR), or gain of the transfer function, is shown in the following equation:

EQUATION 5-2: MAGNITUDE OF FREQUENCY RESPONSE H(f)

$$NMRR(f) = \left|\frac{sinc\left(\pi \cdot \frac{f}{DRCLK}\right)}{sinc\left(\pi \cdot \frac{f}{DMCLK}\right)}\right|^3$$

or:

$$NMRR(f) = \left|\frac{\sin c\left(\pi \cdot \frac{f}{f_D}\right)}{\sin c\left(\pi \cdot \frac{f}{f_S}\right)}\right|^3$$

where:

$$\sin c(x) = \frac{\sin(x)}{x}$$

Figure 5-2 shows the sinc filter frequency response:

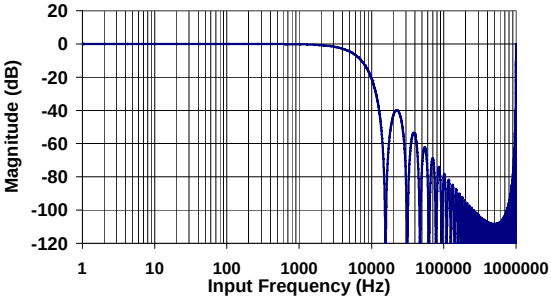


FIGURE 5-2: *SINC Filter Response with MCLK = 4 MHz, OSR = 64, PRESCALE = 1.*

5.5 ADC OUTPUT CODING

The second order modulator, SINC^3 filter, PGA, V_{REF} and analog input structure all work together to produce the device transfer function for the analog to digital conversion, shown in Equation 5-3.

The channel data is either a 16-bit or 24-bit word, presented in 23-bit or 15-bit plus sign, two's complement format and is MSB (left) justified.

The ADC data is two or three bytes wide depending on the WIDTH bit of the associated channel. The 16-bit mode includes a round to the closest 16-bit word (instead of truncation) in order to improve the accuracy of the ADC data.

In case of positive saturation (CHn+ - CHn- > $V_{REF}/3$), the output is locked to 7FFFFF for 24 bit mode (7FFF for 16 bit mode). In case of negative saturation (CHn+ - CHn- <-$V_{REF}/3$), the output code is locked to 800000 for 24-bit mode (8000 for 16 bit mode).

Equation 5-3 is only true for DC inputs. For AC inputs, this transfer function needs to be multiplied by the transfer function of the SINC^3 filter (see Equation 5-1 and Equation 5-2).

EQUATION 5-3:

$$DATA\_CHn = \left(\frac{(CH_{n+} - CH_{n-})}{V_{REF+} - V_{REF-}}\right) \times 8{,}388{,}608 \times G \times 3 \quad \textbf{(For 24-bit Mode Or WIDTH\_CHn = 1)}$$

$$DATA\_CHn = \left(\frac{(CH_{n+} - CH_{n-})}{V_{REF+} - V_{REF-}}\right) \times 32{,}768 \times G \times 3 \quad \textbf{(For 16-bit Mode Or WIDTH\_CHn = 0)}$$

5.5.1 ADC RESOLUTION AS A FUNCTION OF OSR

The ADC resolution is a function of the OSR (**Section 5.4 "SINC3 Filter"**). The resolution is the same for both channels. No matter what the resolution is, the ADC output data is always presented in 24-bit words, with added zeros at the end if the OSR is not large enough to produce 24-bit resolution (left justification).

TABLE 5-3: OSR = 256 OUTPUT CODE EXAMPLES

ADC Output Code (MSB First)	Hexadecimal	Decimal
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0x7FFFFF	+ 8,388,607
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	0x7FFFFE	+ 8,388,606
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x000000	0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0xFFFFFF	-1
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	0x800001	- 8,388,607
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x800000	- 8,388,608

TABLE 5-4: OSR = 128 OUTPUT CODE EXAMPLES

ADC Output Code (MSB First)	Hexadecimal	Decimal 23-bit Resolution
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	0x7FFFFE	+ 4,194,303
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 0 0	0x7FFFFC	+ 4,194,302
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x000000	0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	0xFFFFFE	-1
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0	0x800002	- 4,194,303
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x800000	- 4,194,304

TABLE 5-5: OSR = 64 OUTPUT CODE EXAMPLES

ADC Output code (MSB First)	Hexadecimal	Decimal 20-bit resolution
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0	0x7FFFF0	+ 524, 287
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0	0x7FFFE0	+ 524, 286
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x000000	0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0	0xFFFFF0	-1
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0	0x800010	- 524,287
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x800000	- 524, 288

TABLE 5-6: OSR = 32 OUTPUT CODE EXAMPLES

ADC Output code (MSB First)	Hexadecimal	Decimal 17-bit resolution
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0	0x7FFF80	+ 65, 535
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0	0x7FFF00	+ 65, 534
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x000000	0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0	0xFFFF80	-1
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0	0x800080	- 65,535
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x800000	- 65, 536

5.6 Voltage Reference

5.6.1 INTERNAL VOLTAGE REFERENCE

The MCP3903 contains an internal voltage reference source specially designed to minimize drift over temperature. In order to enable the internal voltage reference, the VREFEXT bit in the configuration register must be set to 0 (default mode). This internal V_{REF} supplies reference voltage to both channels. The typical value of this voltage reference is 2.35V ±2%. The internal reference has a very low typical temperature coefficient of ±5 ppm/°C, allowing the output codes to have minimal variation with respect to temperature since they are proportional to ($1/V_{REF}$).

The noise of the internal voltage reference is low enough not to significantly degrade the SNR of the ADC if compared to a precision external low-noise voltage reference.

The output pin for the internal voltage reference is REFIN+/OUT.

When the internal voltage reference is enabled, REFIN- pin should always be connected to AGND.

For optimal ADC accuracy, appropriate bypass capacitors should be placed between REFIN+/OUT and AGND. De-coupling at the sampling frequency, around 1 MHz, is important for any noise around this frequency will be aliased back into the conversion data. 0.1 µF ceramic and 10 µF tantalum capacitors are recommended.

These bypass capacitors are not mandatory for correct ADC operation, but removing these capacitors may degrade accuracy of the ADC. The bypass capacitors also help for applications where the voltage reference output is connected to other circuits. In this case, additional buffering may be needed as the output drive capability of this output is low.

5.6.2 DIFFERENTIAL EXTERNAL VOLTAGE INPUTS

When the VREFEXT bit is high, the two reference pins (REFIN+/OUT, REFIN-) become a differential voltage reference input. The voltage at the REFIN+/OUT is noted V_{REF}+ and the voltage at the REFIN- pin is noted V_{REF}-. The differential voltage input value is shown in the following equation:

EQUATION 5-4:

$$V_{REF}=V_{REF}+ - V_{REF}-$$

The specified V_{REF} range is from 2.2V to 2.6V. The REFIN- pin voltage (V_{REF}-) should be limited to ±0.3V. Typically, for single-ended reference applications, the REFIN- pin should be directly connected to AGND.

5.7 Power-on Reset

The MCP3903 contains an internal POR circuit that monitors analog supply voltage AV_{DD} during operation. The typical threshold for a power-up event detection is 4.2V ±5%. The POR circuit has a built-in hysteresis for improved transient spikes immunity that has a typical value of 200 mV. Proper decoupling capacitors (0.1 µF ceramic and 10 µF tantalum) should be mounted as close as possible to the AV_{DD} pin, providing additional transient immunity.

Figure 5-3 illustrates the different conditions at power-up and a power-down event, in typical conditions. All internal DC biases are not settled until at least 50 µs after system POR. Any data ready pulses during this time after system reset should be ignored. After POR, data ready pulses are present at the pin with all the default conditions in the configuration registers.

Both AV_{DD} and DV_{DD} power supplies are independent. Since AV_{DD} is the only power supply that is monitored, it is highly recommended to power up DV_{DD} first as a power-up sequence. If AV_{DD} is powered up first, it is highly recommended to keep the $\overline{\text{RESET}}$ pin low during the whole power-up sequence.

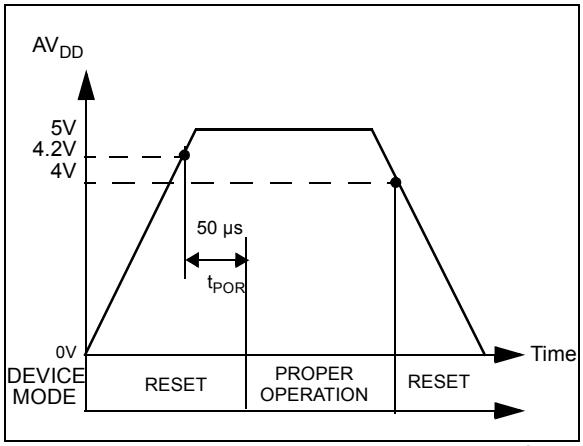


FIGURE 5-3: *Power-on Reset Operation.*

5.8 $\overline{\text{RESET}}$ Effect On Delta Sigma Modulator/SINC Filter

When the $\overline{\text{RESET}}$ pin is low, both ADCs will be in Reset and output code 0x0000h. The $\overline{\text{RESET}}$ pin performs a hard reset (DC biases still on, part ready to convert) and clears all charges contained in the sigma delta modulators. The comparator outputs are `0011` for each ADC.

The SINC filters are all reset, as well as their double output buffers. This pin is independent of the serial interface. It brings the CONFIG registers to the default state. When $\overline{\text{RESET}}$ is low, any write with the SPI interface will be disabled and will have no effect. All output pins (SDO, $\overline{\text{DR}}$, MDAT0/1) are high impedance, and no clock is propagated through the chip.

5.9 Phase Delay Block

The MCP3903 incorporates a phase delay generator which ensures that the six ADCs are converting the inputs with a fixed delay between them. The six ADCs are synchronously sampling but the averaging of modulator outputs is delayed so that the SINC filter outputs (thus the ADC outputs) show a fixed phase delay, as determined by the PHASE register setting. The phase register is composed of three bytes: PHASEC<7:0>, PHASEB<7:0>, PHASEA<7:0>. Each byte is a 7 bit + sign MSB first, two's complement code that represents the amount of delay between each pair of ADCs. The PHASEC byte represents the delay between Channel 4 and channel 5 (pair C). The PHASEB byte represents the delay between Channel 2 and channel 3 (pair B). The PHASEA byte represents the delay between Channel 0 and channel 1 (pair A). The reference channel is the odd channel (channel 1/3/5). When PHASEn<7:0> is positive, Channel 0/2/4 is lagging versus channel 1/3/5 otherwise it is leading. The amount of delay between two ADC conversions is given by the following formula:

EQUATION 5-5:

$$Delay = \frac{Phase\ Register\ Code}{DMCLK}$$

The timing resolution of the phase delay is 1/DMCLK or 1 µs in the default configuration with MCLK = 4 MHz.

The data ready signals are affected by the phase delay settings. Typically, the time difference between the data ready pulses of channel 0 and channel 1 is equal to the phase delay setting.

Note: A detailed explanation of the Data Ready pins ($\overline{\text{DRn}}$) with phase delay is present in **Section 6.10 "Data Ready Pulses (DRn)"**.

5.9.1 PHASE DELAY LIMITS

The Phase delay can only go from -OSR/2 to +OSR/2 - 1. This sets the fine phase resolution. The phase register is coded with 2's complement.

If larger delays between the two channels from the same pair are needed, they can be implemented externally to the chip with an MCU. A FIFO in the MCU can save incoming data from the leading channel for a number N of DRCLK clocks. In this case, DRCLK would represent the coarse timing resolution, and DMCLK the fine timing resolution. The total delay will then be equal to:

Delay = N/DRCLK + PHASE/DMCLK

The Phase Delay register can be programmed once with the OSR=256 setting and will adjust to the OSR automatically afterward without the need to change the value of the PHASE register.

- **OSR=256**: the delay can go from -128 to +127. PHASEn<7> is the sign bit. PHASEn<6> is the MSB and PHASEn<0> the LSB.
- **OSR=128:** the delay can go from -64 to +63. PHASEn<6> is the sign bit. PHASEn<5> is the MSB and PHASEn<0> the LSB.
- **OSR=64**: the delay can go from -32 to +31. PHASEn<5> is the sign bit. PHASEn<4> is the MSB and PHASEn<0> the LSB.
- **OSR=32:** the delay can go from -16 to +15. PHASEn<4> is the sign bit. PHASEn<3> is the MSB and PHASEn<0> the LSB.

TABLE 5-7: PHASE VALUES WITH MCLK = 4 MHZ, OSR = 256

Phase Register Value								Hex	Delay (CH0/2/4 relative to CH1/3/5)
0	1	1	1	1	1	1	1	0x7F	+ 127 µs
0	1	1	1	1	1	1	0	0x7E	+ 126 µs
0	0	0	0	0	0	0	1	0x01	+ 1 µs
0	0	0	0	0	0	0	0	0x00	0 µs
1	1	1	1	1	1	1	1	0xFF	- 1 µs
1	0	0	0	0	0	0	1	0x81	- 127 µs
1	0	0	0	0	0	0	0	0x80	-128 µs

5.10 Crystal Oscillator

The MCP3903 includes a Pierce-type crystal oscillator with very high stability and ensures very low tempco and jitter for the clock generation. This oscillator can handle up to 16.384 MHz crystal frequencies, provided that proper load capacitances and quartz quality factor are used.

For keeping specified ADC accuracy, AMCLK should be kept between 1 and 5 MHz with BOOST off or 1 and 8.192 MHz with BOOST on. Larger MCLK frequencies can be used, provided the prescaler clock settings allow the AMCLK to respect these ranges.

For a proper start-up, the load capacitors of the crystal should be connected between OSC1 and DGND and between OSC2 and DGND. They should also respect the following equation:

EQUATION 5-6:

$$R_M < 1.6 \times 10^6 \times \left(\frac{1}{f \times C_{LOAD}}\right)^2$$

Where:

f	=	crystal frequency in MHz
C_{LOAD}	=	load capacitance in pF including parasitics from the PCB
R_M	=	motional resistance in ohms of the quartz

When CLKEXT=1, the crystal oscillator is bypassed by a digital buffer to allow direct clock input for an external clock.

6.0 SERIAL INTERFACE DESCRIPTION

6.1 OVERVIEW

The MCP3903 device is compatible with SPI modes 0,0 and 1,1. Data is clocked *out* of the MCP3903 on the *falling* edge of SCK, and data is clocked *into* the MCP3903 on the *rising* edge of SCK. In these modes, SCK can idle either high or low. Each SPI communication starts with a CS falling edge and stops with the CS rising edge. Each SPI communication is independent. When CS is high, SDO is in high impedance, and transitions on SCK and SDI have no effect. Additional controls: $\overline{\text{RESET}}$, $\overline{\text{DR}}$ are also provided on separate pins for advanced communication. The MCP3903 interface has a simple command structure. The first byte transmitted is always the CONTROL byte that is 8 bits wide and is followed by data bytes that are 24 bits wide. Both ADCs are continuously converting data by default and can be reset or shutdown through a CONFIG register setting.

Since each ADC data is either 16 or 24 bits (depending on the WIDTH bits), the internal registers can be grouped together with various configurations (through the READ bits) in order to allow easy data retrieval within only one communication. For device reads, the internal address counter can be automatically incremented in order to loop through groups of data within the register map. The SDO will then output the data located at the ADDRESS (A<4:0>) defined in the control byte and then ADDRESS+1 depending on the READ<1:0> bits which select the groups of registers. These groups are defined in **Section 7.1 "ADC Channel Data Output Registers"** (Register Map). The Data Ready pins (DRn) can be used as an interrupt for an MCU and outputs pulses when new ADC channel data is available. The $\overline{\text{RESET}}$ pin acts like a hard reset and can reset the part to its default power-up configuration.

6.2 CONTROL BYTE

The control byte of the MCP3903 contains two device address bits A<6:5>, 5 register address bits A<4:0>, and a read/write bit (R/W). The first byte transmitted to the MCP3903 is always the control byte.

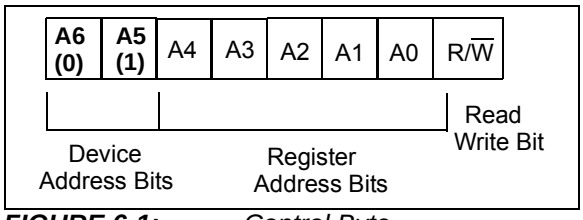


FIGURE 6-1: *Control Byte.*

The default device address bits are 01. A read on undefined addresses will give an all zeros output on the first and all subsequent transmitted bytes. A write on an undefined address will have no effect and will not increment the address counter either.

The register map is defined in **Section 7.1 "ADC Channel Data Output Registers"**.

6.3 Reading from the Device

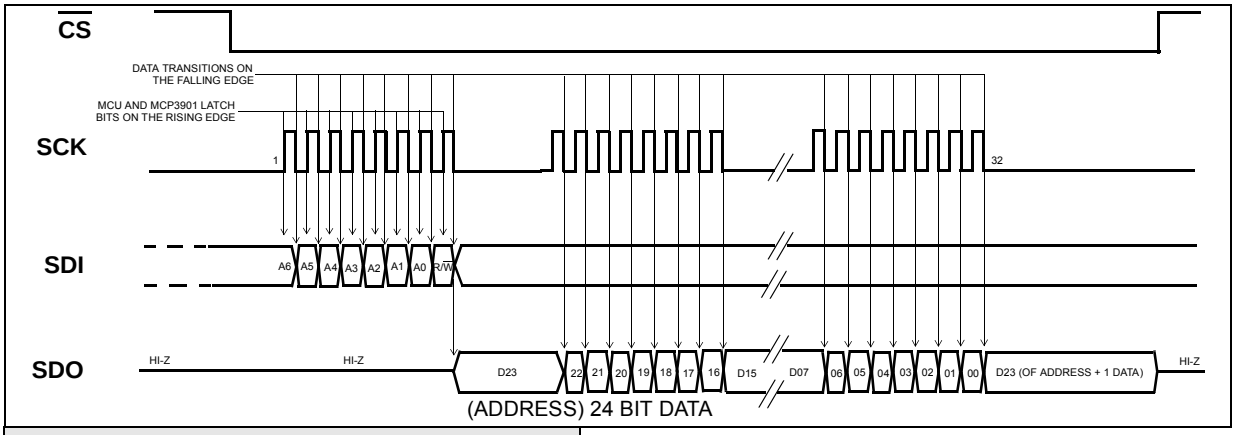
The first data byte read is the one defined by the address given in the CONTROL byte. After this first byte is transmitted, if $\overline{\text{CS}}$ pin is maintained low, the communication continues and the address of the next transmitted byte is determined by the status of the READ bits in the STATUS/COM register. Multiple looping configurations can be defined through the READ<1:0> bits for the address increment (see **6.6 "SPI MODE 1,1 - Clock Idle High, Read/Write Examples""**).

6.4 Writing to the Device

The first data byte written is the one defined by the address given in the control byte. The write communication automatically increments the address for subsequent bytes. The address of the next transmitted byte within the same communication (CS stays low) is the next address defined on the register map. At the end of the register map, the address loops to the beginning of the register map. Writing a non-writable register has no effect. SDO pin stays high impedance during a write communication.

6.5 SPI MODE 0,0 - Clock Idle Low, Read/Write Examples

In this SPI mode, the clock idles low. For the MCP3903, this means that there will be a rising edge before there is a falling edge.



Note:

FIGURE 6-2: *Device Read (SPI MODE 0,0 - Clock Idles Low).*

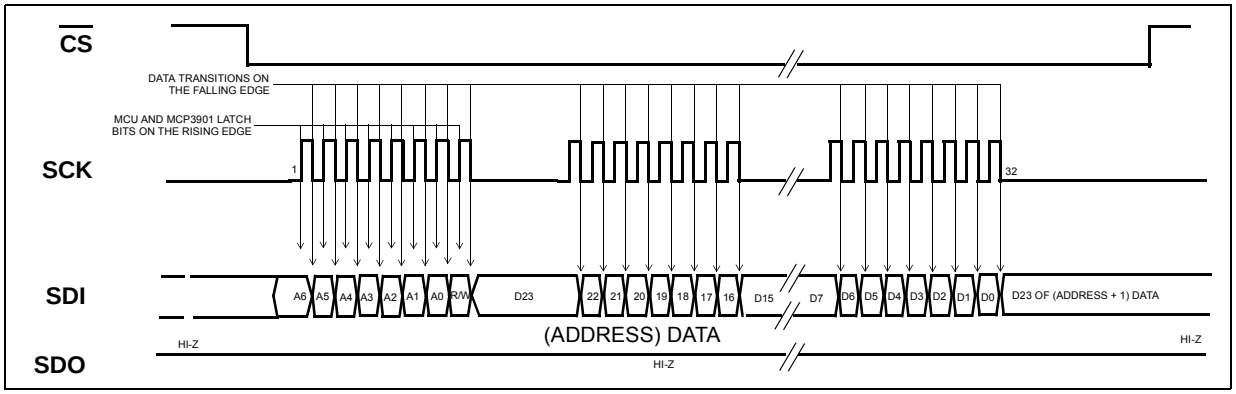


FIGURE 6-3: *Device Write (SPI Mode 0,0 - Clock Idles Low).*

6.6 SPI MODE 1,1 - Clock Idle High, Read/Write Examples

In this SPI mode, the clock idles High. For the MCP3903, this means that there will be a falling edge before there is a rising edge.

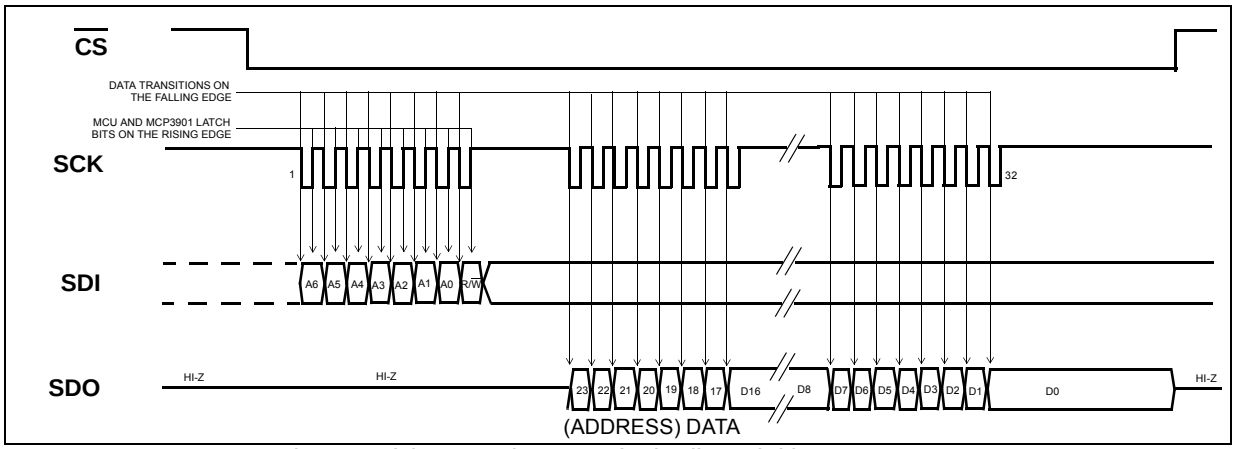


FIGURE 6-4: *Device Read (SPI Mode 1,1 - Clock Idles High).*

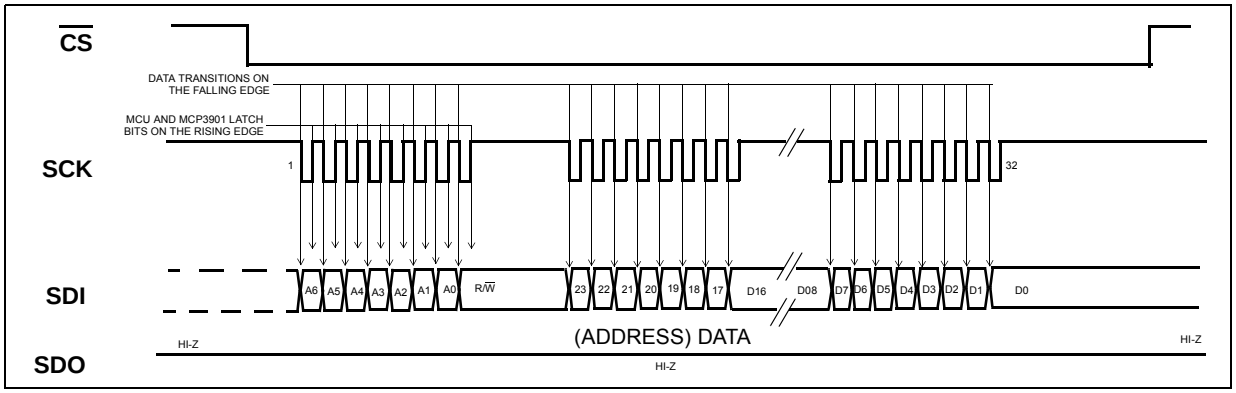


FIGURE 6-5: *Device Write (SPI Mode 1,1 - Clock Idles High).*

6.7 Read Continuously Channel Data, LOOPING ON ADDRESS SETS

If the user wishes to read back any of the ADC channels continuously, or all channels continuously, the internal address counter of the MCP3903 can be set to loop on specific register sets. In this case, there is only one control byte on SDI to start the communication. The part stays within the same loop until $\overline{CS}$ returns high.

This internal address counter allows the following functionality:

- Read one ADC channel data continuously
- Read all ADC channel data continuously (all ADC data can be independent or linked with DRn_MODE settings)
- Read continuously the entire register map
- Read continuously each separate register
- Read continuously all configuration registers
- Write all configuration registers in one communication (see Figure 6-6)

The STATUS/COM register contains the loop settings for the internal address counter (READ<1:0>). The internal address counter can either stay constant (READ<1:0>=00) and continuously read the same byte, or it can auto-increment and loop through the register groups defined below (READ<1:0>=01), register types (READ<1:0>=10) or the entire register map (READ<1:0>=11).

Each channel is configured independently as either a 16-bit or 24-bit data word, depending on the setting of the corresponding WIDTH bit in the CONFIG register.

For continuous reading, in the case of WIDTH=0 (16-bit), the lower byte of the ADC data is not accessed and the part jumps automatically to the following address (the user does not have to clock out the lower byte since it becomes undefined for WIDTH=0).

The following figure represents a typical continuous read communication with the default settings (DRMODE<1:0>=00, READ<1:0>=10) for both WIDTH settings. This configuration is typically used for power metering applications.

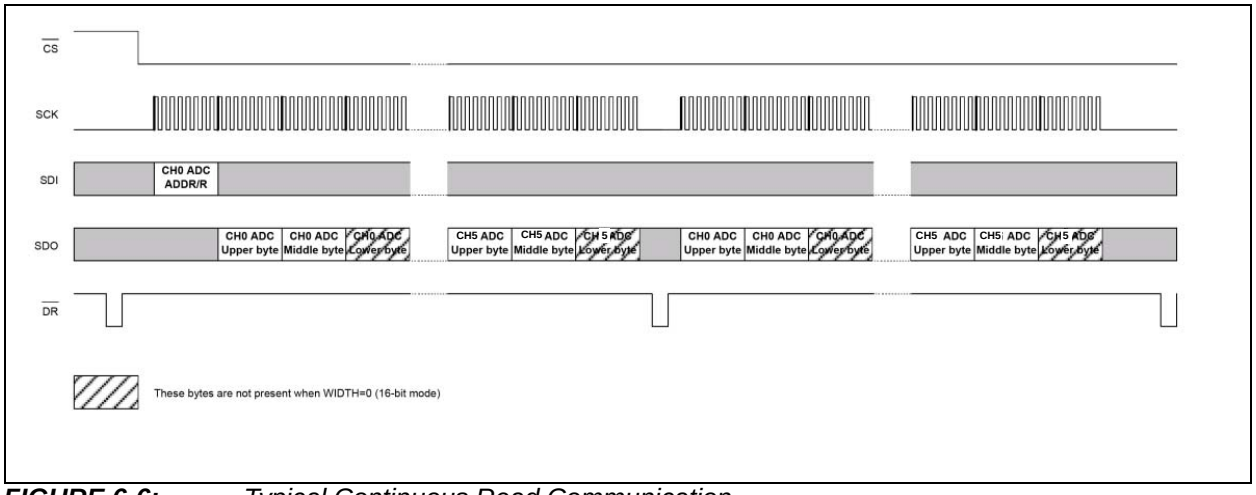


FIGURE 6-6: *Typical Continuous Read Communication.*

6.7.1 CONTINUOUS READ

All ADCs are powered up with their default configurations, and begin to output data ready pulses immediately (RESET<5:0> and SHUTDOWN<5:0> bits are off by default). The default output codes for both ADCs are all zeros.The default modulator output for both ADCs is 0011 (corresponding to a theoretical zero voltage at the inputs). The default phase is zero between the two channels. It is recommended to enter into ADC reset mode for both ADCs just after power-up because the desired MCP3903 register configuration may not be the default one and in this case, the ADC would output undesired data. Within the ADC reset mode (RESET<5:0>=111111), the user can configure the whole part with a single communication. The write commands automatically increment the address so the user can start writing the PHASE register and finish with the CONFIG register in only one communication (see Figure 6-6). The RESET<5:0> bits are in the CONFIG register to allow it to exit soft reset mode and have the whole part configured and ready to run in only one command.

TABLE 6-1: REGISTER GROUPS

GROUP	ADDRESSES
Pair A, CHANNEL 0/1	0x00 - 0x01
Pair B, CHANNEL 2/3	0x02 - 0x03
Pair C, CHANNEL 4/5	0x04 - 0x05
MOD, PHASE, GAIN	0x06 - 0x08
STATUS, CONFIG	0x09 - 0x0A

The following internal registers are defined as types:

TABLE 6-2: REGISTER TYPES

TYPE	ADDRESSES
ADC DATA	0x00 - 0x05
CONTROL	0x06 - 0x0A

6.8 Situations that Reset ADC Data

Immediately after the following actions, the ADCs are reset and automatically restarted in order to provide proper operations:

1: Change in phase register

2: Change in the OSR setting

3: Change in the PRESCALER setting

4: Overwrite of identical PHASE register value

5: Change in EXTCLK bit in the CONFIG register modifying internal oscillator state.

After these temporary resets, the ADCs go back to normal operation with no need for an additional command. These are also the settings where the DR position is affected. The phase register can be used to soft reset the ADC without using the RESET bits in the configuration register.

6.9 Line Cycle Sampling Options

Since the AMCLK range can go up to 5 MHz, the MCP3903 is able to accommodate 256 output samples per line cycles with line frequencies up to 76.2Hz at OSR=64.

TABLE 6-1: MCLK FREQUENCIES FOR LINE SAMPLING

OUTPUT SAMPLES / LINE CYCLE	F_{LINE} = 45 HZ OSR = 64		F_{LINE} = 65 HZ OSR = 64	
	F_D	MCLK	F_D	MCLK
64	2.8 ksps	737.28 kHz	4.2 ksps	1.075 MHz
128	5.76 ksps	1.475 MHz	8.4 ksps	2.15 MHz
256	11.5 ksps	2.949 MHz	16.7 ksps	4.3 MHz

Figure 6-7 illustrates operating the part in this manner (timings not to scale, functional description only).

All channels are continuously converting during normal operation of the device except when it is in Sleep Mode by using the RESET bit, or if $\overline{\text{RESET}}$ is low. The following figure represents the clocking scheme and how the CONFIG PRESCALE<1:0> bits and OSR<1:0> bits registers is used to modify the clock prescale and oversampling ratio.

For example, if a data ready pulse occurs while ADC data (a) is being transmitted on SPI, this data will not be corrupt in any way. After $\overline{\text{CS}}$ is toggled low to begin another transmission, the next data (b) would be present in the output buffer ready for transmission.

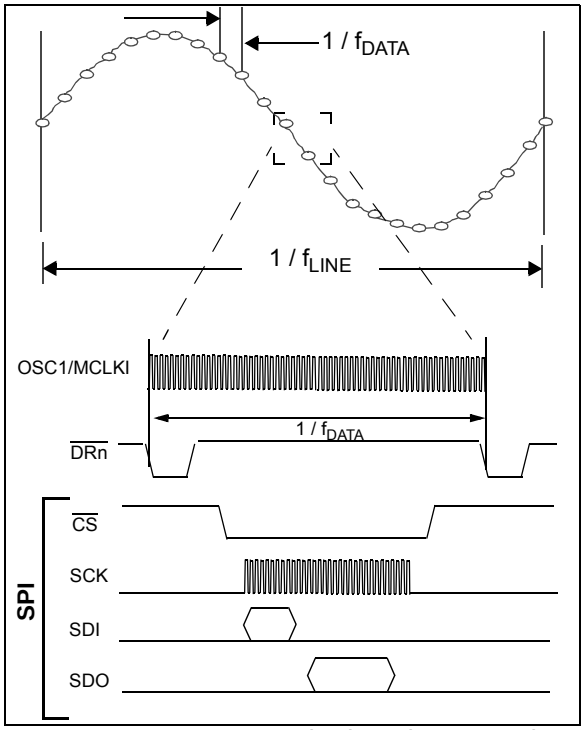


FIGURE 6-7: *Standard Device Operation.*

6.10 Data Ready Pulses ($\overline{DRn}$)

To ensure that all channel ADC data are present at the same time for SPI read, regardless of phase delay settings for either or both channels, there are two sets of latches in series with both the data ready and the 'read start' triggers.

The first set of latches holds each output when data is ready and latches both outputs together when DRMODE<1:0>=00. When this mode is on, both ADCs work together and produce one set of available data after each data ready pulse (that corresponds to the lagging ADC data ready). The second set of latches ensures that when reading starts on an ADC output, the corresponding data is latched so that no data corruption can occur.

If an ADC read has started, in order to read the following ADC output, the current reading needs to be completed (all bits must be read from the ADC output data registers).

6.10.1 DATA READY PINS ($\overline{DRn}$) CONTROL USING DRn_MODE BITS

There are four modes that control the data ready pulses, and these modes are set with the DRn_MODE<1:0> bits in the STATUS/COM register. For power metering applications, DRn_MODE<1:0>=00 is recommended (default mode).

The position of data ready pulses vary with respect to this mode, to the OSR and to the PHASE settings:

- **DRn_MODE<1:0> = 11:** Both Data Ready pulses from ADC Channel 0/2/4 and ADC Channel 1/3/5 are output on DR pin.
- **DRn_MODE<1:0> = 10:** Data Ready pulses from ADC Channel 1/3/5 are output on the corresponding DRn pin. Data Ready pulses from ADC Channel 0/2/4 are not present on the pin.
- **DRn_MODE<1:0> = 01:** Data Ready pulses from ADC Channel 0/2/4 are output on the corresponding DRn pin. Data Ready pulses from ADC Channel 1/3/5 are not present on the pin.
- **DRn_MODE<1:0> = 00:** (Recommended, and Default Mode). Data Ready pulses from the lagging ADC between the two are output on DR pin. The lagging ADC depends on the phase register and on the OSR. In this mode the two ADCs are linked together so their data is latched together when the lagging ADC output is ready.

6.10.2 DR PULSES WITH SHUTDOWN OR RESET CONDITIONS

There will be no data ready pulses if DRn_MODE<1:0>=00 when either one or both of the ADCs of the corresponding pair are in reset or shutdown. In Mode 00, a data ready pulse only happens when both ADCs of the corresponding pair are ready. Any data ready pulse will correspond to one data on both ADCs. The two ADCs are linked together and act as if there was only one channel with the combined data of both ADCs. This mode is very practical when both ADC channel data retrieval and processing need to be synchronized, as in power metering applications.

Figure 6-8 represents the behavior of the data ready pin with the different DRn_MODE and DR_LTY configurations, while shutdown or resets are applied.

Note:	If DRn_MODE<1:0>=11, the user will still be able to retrieve the data ready pulse for the ADC not in shutdown or reset, i.e. only 1 ADC channel needs to be awake.

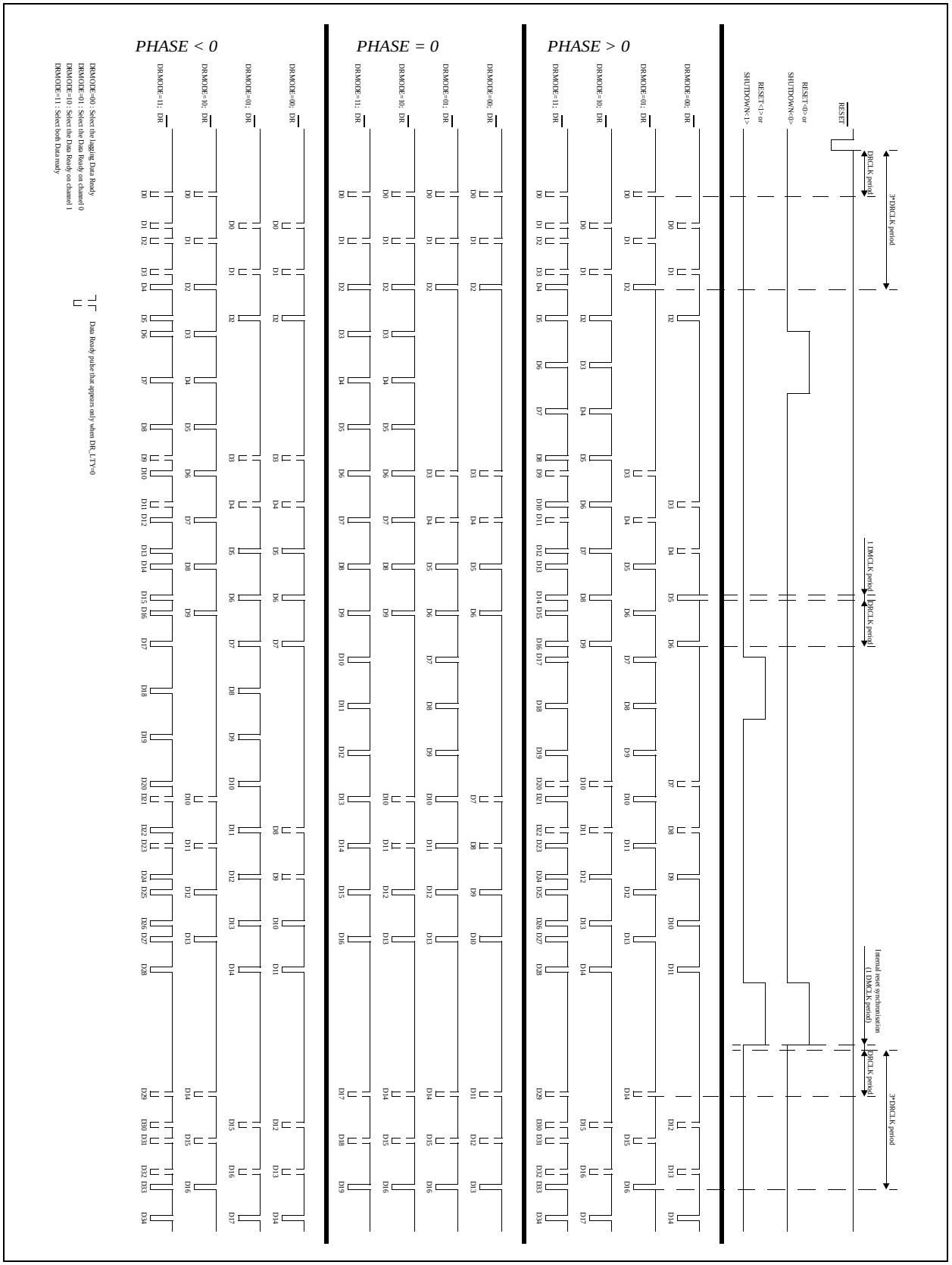


FIGURE 6-8: *Data Ready Behavior.*

6.11 DATA READY PULSE WITH PHASE DELAY

To ensure that both channel ADC data from the same pair are present at the same time for SPI read, regardless of phase delay settings for either or both channels, there are two sets of latches in series with both the data ready and the reading start triggers. The first latch is set on whichever channel is the lagging channel (relative to the other channel, in a single channel pair). The second latch is set when an ADC output read command is issued, ensuring synchronized data ready pulses.

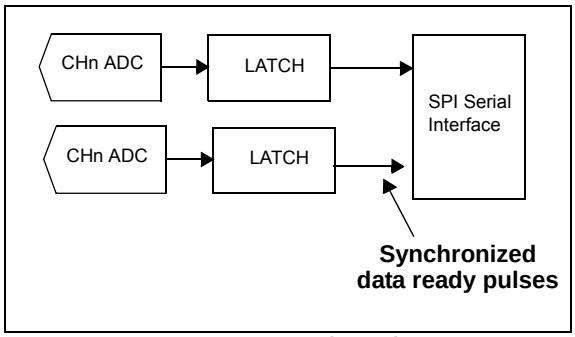


FIGURE 6-9: *Internal Latches Synchronizing Data Ready Pulses with Phase Delay Present (Single Channel Pair Shown).*

6.11.1 DATA READY LINK

When DRLINK=0, the three pairs of ADCs are independent from each other. The data readys and the latches for the output data only depend on both ADCs in the pair. When another ADC (not in the pair) is put in SHUTDOWN or RESET, it has no effect.

When DRLINK=1, all ADCs are linked together. The DRn_MODE<1:0> are all set internally to 00. All DRn_MODE<1:0> bits are not taken into account.

All six channel ADC data are latched synchronously with the most lagging ADC channel of the six.

All three $\overline{\text{DRA}}$, $\overline{\text{DRB}}$ and $\overline{\text{DRC}}$ data ready pins are giving the same output that is synchronized with the most lagging ADC of the six channels. Only one pin can be connected to the MCU in this mode, which saves two connection ports on the MCU.

In this mode, if any channel is in SHUTDOWN or RESET mode, no data ready is present on any of the $\overline{\text{DRA}}$/$\overline{\text{DRB}}$/$\overline{\text{DRC}}$ pins. The part acts as if there was only one ADC channel with 6x24 bits.

Depending on the read modes, the ADC data can be retrieved by pair (Read by GROUP) or all together (Read by TYPE). Any time a new read command is performed, the ADC outputs are re-latched. In order to avoid loss of data or bad synchronization, the read mode by TYPES is recommended (READ<1:0>=10) so that all data can be latched once at the beginning of the read. In the read mode by GROUP (READ<1:0>=01) mode, the data will be relatched every time the part accesses to each group or pair of ADCs.

7.0 INTERNAL REGISTERS

The addresses associated with the internal registers are listed below. All registers are 24 bits long and can be addressed separately. A detailed description of the registers follows.

TABLE 7-1: INTERNAL REGISTER SUMMARY

Address	Name	Bits	R/W	Description
0x00	CHANNEL 0	24	R	Channel 0 ADC Data <23:0>, MSB first, left justified
0x01	CHANNEL 1	24	R	Channel 1 ADC Data <23:0>, MSB first, left justified
0x02	CHANNEL 2	24	R	Channel 2 ADC Data <23:0>, MSB first, left justified
0x03	CHANNEL 3	24	R	Channel 3 ADC Data <23:0>, MSB first, left justified
0x04	CHANNEL 4	24	R	Channel 4 ADC Data <23:0>, MSB first, left justified
0x05	CHANNEL 5	24	R	Channel 5 ADC Data <23:0>, MSB first, left justified
0x06	MOD	24	R/W	Delta Sigma Modulators Output Value
0x07	PHASE	24	R/W	Phase Delay Configuration Register
0x08	GAIN	24	R/W	Gain Configuration Register
0x09	STATUS/COM	24	R/W	Status/Communication Register
0x0A	CONFIG	24	R/W	Configuration Register

The following table shows how the internal address counter will loop on specific register groups and types.

TABLE 7-2: CONTINUOUS READ OPTIONS, LOOPING ON INTERNAL ADDRESSES

Function	Address	READ<1:0>		
		= "01"	= "10"	="11"
CHANNEL 0	0x00	GROUP	TYPE	LOOP ENTIRE REGISTER MAP
CHANNEL 1	0x01			
CHANNEL 2	0x02	GROUP		
CHANNEL 3	0x03			
CHANNEL 4	0x04	GROUP		
CHANNEL 5	0x05			
MOD	0x06	GROUP	TYPE	
PHASE	0x07			
GAIN	0x08			
STATUS/ COM	0x09	GROUP		
CONFIG	0x0A			

7.1 Channel Output Registers

TABLE 7-3: ADC OUTPUT REGISTERS

Name	Bits	Address	Cof
CHANNEL 0	24	0x00	R
CHANNEL 1	24	0x01	R
CHANNEL 2	24	0x02	R
CHANNEL 3	24	0x03	R
CHANNEL 4	24	0x04	R
CHANNEL 5	24	0x05	R

The ADC Channel data output registers always contain the most recent A/D conversion data for each channel. These registers are read-only. They can be accessed independently or linked together (with READ<1:0> bits). These registers are latched when an ADC read communication occurs. When a data ready event occurs during a read communication, the most current ADC data is also latched to avoid data corruption issues. The three bytes of each channel are updated synchronously at a DRCLK rate. The three bytes can be accessed separately if needed, but are refreshed synchronously. The coding is 23-bit + sign two's complement (see Section 5.5).

REGISTER 7-1: CHANNEL REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
D23 (MSB)	D22	D21	D20	D19	D18	D17	D16
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
D15	D14	D13	D12	D11	D10	D9	D8
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
D7	D6	D5	D4	D3	D2	D1	D0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23:0 24-bit ADC output data of the corresponding channel

7.2 Mod Register

TABLE 7-4: MODULATOR OUTPUT REGISTER

Name	Bits	Address	Cof
MOD	24	0x06	R/W

The MOD register contains the most recent modulator data output. The default value corresponds to an equivalent input of 0V on each ADC. Each bit in this register corresponds to one comparator output on one of the channels.

This register should be used as a read-only register.

(Note 1). This register is updated at the refresh rate of DMCLK (typically 1 MHz with MCLK = 4 MHz). The default state for this register is 001100110011001100110011.

REGISTER 7-2: MOD REGISTER

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1
COMP3_CH5	COMP2_CH5	COMP1_CH5	COMP0_CH5	COMP3_CH4	COMP2_CH4	COMP1_CH4	COMP0_CH4
bit 23							bit 16

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1
COMP3_CH3	COMP2_CH3	COMP1_CH3	COMP0_CH3	COMP3_CH2	COMP2_CH2	COMP1_CH2	COMP0_CH2
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1
COMP3_CH1	COMP2_CH1	COMP1_CH1	COMP0_CH1	COMP3_CH1	COMP2_CH0	COMP1_CH0	COMP0_CH0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23:20 **COMPn_CH5:** Comparator Outputs from ADC Channel 5

bit 19:16 **COMPn_CH4:** Comparator Outputs from ADC Channel 4

bit 15:12 **COMPn_CH3:** Comparator Outputs from ADC Channel 3

bit 11:8 **COMPn_CH2:** Comparator Outputs from ADC Channel 2

bit 7:4 **COMPn_CH1:** Comparator Outputs from ADC Channel 1

bit 3:0 **COMPn_CH0:** Comparator Outputs from ADC Channel 0

7.3 Phase Register

TABLE 7-5: PHASE REGISTER

Name	Bits	Address	Cof
PHASE	24	0x07	R/W

The phase register is composed of three bytes: PHASEC<7:0>, PHASEB<7:0>, PHASEA<7:0>. Each byte is a 7 bit + sign MSB first, two's complement code that represents the amount of delay between each pair of ADCs. The PHASEC byte represents the delay between Channel 4 and Channel 5 (pair C). The PHASEB byte represents the delay between Channel 2 and Channel 3 (pair B). The PHASEA byte represents the delay between Channel 0 and Channel 1 (pair A).

The reference channel is the odd channel (Channel 1/3/5). When PHASEn<7:0> is positive, Channel 0/2/4 is lagging versus channel 1/3/5 otherwise it is leading.

The delay is calculated by the following formula:

Delay = PHASE Register Code / DMCLK.

REGISTER 7-3: PHASE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEC7	PHASEC6	PHASEC5	PHASEC4	PHASEC3	PHASEC2	PHASEC1	PHASEC0
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEB7	PHASEB6	PHASEB5	PHASEB4	PHASEB3	PHASEB2	PHASEB1	PHASEB0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEA7	PHASEA6	PHASEA5	PHASEA4	PHASEA3	PHASEA2	PHASEA1	PHASEA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23:16 **PHASECn:** CH4 relative to CH5 phase delay

bit 15:8 **PHASEBn:** CH2 relative to CH3 phase delay

bit 7:0 **PHASEAn:** CH0 relative to CH1 phase delay

7.4 Gain Configuration Register

TABLE 7-6: GAIN REGISTER

Name	Bits	Address	Cof
GAIN	24	0x08	R/W

This register contains the gain register

REGISTER 7-4: GAIN REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PGA2_CH5	PGA1_CH5	PGA0_CH5	BOOST_ CH5	BOOST_ CH4	PGA2_CH4	PGA1_CH4	PGA0_CH4
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PGA2_CH3	PGA1_CH3	PGA0_CH3	BOOST_ CH3	BOOST_ CH2	PGA2_CH2	PGA1_CH2	PGA0_CH2
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PGA2_CH1	PGA1_CH1	PGA0_CH1	BOOST_ CH1	BOOST_ CH0	PGA2_CH0	PGA1_CH0	PGA0_CH0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit **PGA_CHn:** PGA Setting for Channel n

111 = Reserved (Gain = 1)
110 = Reserved (Gain = 1)
101 = Gain is 32
100 = Gain is 16
011 = Gain is 8
010 = Gain is 4
001 = Gain is 2
000 = Gain is 1

bit **BOOST_CHn** Current Scaling for high speed operation for channel n

1 = Channel has current x 2
0 = Channel has normal current

7.5 STATUS/COM Register - Status and Communication Register

TABLE 7-7: STATUS/COM Register

Name	Bits	Address	Cof
STATUS/COM	24	0x09	R/W

7.5.1 DATA READY LATENCY - DR_LTY

This bit determines if the data ready pulses correspond to settled data or unsettled data from each $SINC^3$ filter. Unsettled data will provide data ready pulses every DRCLK period. Settled data will wait for 3 DRCLK periods before giving data ready pulses and will then give data ready pulses every DRCLK period.

7.5.2 DATA READY HIGH Z MODE - $\overline{DR\_HIZ}$

Using this bit, the user can connect multiple chips with the same data ready pin with a pull up resistor ($\overline{DR\_HIZ}$=0) or a single chip with no external component ($\overline{DR\_HIZ}$=1)

7.5.3 DATA READY MODE - DRN_MODE

These bits control which ADC data ready is present on the data ready pin. When the bits are set to 00, the output of the two ADCs are latched synchronously at the moment of the data ready event. This prevents bad synchronization between the two ADCs. The output is also latched at the beginning of a reading, in order not to be updated during a read, and not to give erroneous data.

If one of the channels is in reset or shutdown, only one of the data ready pulses is present and the situation is similar to DRn_MODE<1:0> = 01 or 10. In the 01,10 and 11 modes, the data is latched at the beginning of a reading, in order to prevent the case of erroneous data when a data ready pulse happens when reading.

7.5.4 DATA READY STATUS FLAG - DRSTATUS_CHN

These bits indicate the data ready status of each channel. These flags are set to logic high after being the STATUS/COM register has been read. These bits are cleared when a data ready event has happened on its respective ADC. Writing these bits has no effect.

Note: These bits are useful if multiple devices share the same $\overline{DRn}$ output pin ($\overline{DR\_HIZ}$=0) in order to understand which device the data ready event occured from. In case the DRn_MODE=00 (Linked ADCs), these data ready status bits will be updated synchronously upon the same event (lagging ADC is ready). These bits are also useful in systems where the $\overline{DRn}$ pins are not used to save MCU I/O.

REGISTER 7-5: STATUS/COM REGISTER

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
READ1	READ0	WMODE	WIDTH_CH5	WIDTH_CH4	WIDTH_CH3	WIDTH_CH2	WIDTH_CH1
bit 23							bit 16

R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WIDTH_CH0	DR_LTY	$\overline{DR\_HIZ}$	DR_LINK	DRC_MODE1	DRC_MODE0	DRB_MODE1	DRB_MODE0
bit 15							bit 8

R/W-0	R/W-0	R-1	R-1	R-1	R-1	R-1	R-1
DRA_MODE1	DRA_MODE0	DRSTATUS_CH5	DRSTATUS_CH4	DRSTATUS_CH3	DRSTATUS_CH2	DRSTATUS_CH1	DRSTATUS_CH0
bit 7							bit 0

bit 23:22 **READ[1:0]:** Address Loop Setting
- 11 = Address counter incremented, cycle through entire register map
- 10 = Address counter loops on register TYPES **(DEFAULT)**
- 01 = Address counter loops on register GROUPS
- 00 = Address not incremented, continually read single register

bit 21 **WMODE:** Write Mode Bit (internal use only)
- 1 = Static addressing Write Mode
- 0 = Incremental addressing Write Mode (**DEFAULT)**

REGISTER 7-5: STATUS/COM REGISTER (CONTINUED)

bit 20:15 **WIDTH_CHn** ADC Channels output data word width control
1 = 24-bit mode for the corresponding channel
0 = 16-bit mode for the corresponding channel (default)

bit 14 **DR_LTY:** Data Ready Latency Control for $\overline{DRA}$, $\overline{DRB}$, and $\overline{DRC}$ pins
1 = True "No Latency" Conversion, data ready pulses after 3 DRCLK periods **(DEFAULT)**
0 = Unsettled Data is available after every DRCLK period

bit 13 **DR_HIZ:** Data Ready Pin Inactive State Control for $\overline{DRA}$, $\overline{DRB}$, and $\overline{DRC}$ pins
1 = The Default state is a logic high when data is NOT ready
0 = The Default state is high impedance when data is NOT ready **(DEFAULT)**

bit 12 **DR_LINK** Data Ready Link Control
1 = Data Ready Link turned ON, all channels linked and data ready pulses from the most lagging ADC are present on each $\overline{DRn}$ pin
0 = Data Ready Link tunred OFF **(DEFAULT)**

bit 11:10 **DRC_MODE[1:0]**
11 = Both Data Ready pulses from CH4 and CH5 are output on $\overline{DRC}$ pin.
10 = Data Ready pulses from CH5 are output on $\overline{DRC}$ pin. Data Ready pulses R from CH4 are not present on the pin.
01 = Data Ready pulses from CH4 are output on $\overline{DRC}$ pin. Data Ready pulses from CH5 are not present on the pin.
00 = Data Ready pulses from the lagging ADC channel between the two are output on $\overline{DRC}$ pin. The lagging ADC channel depends on the phase register and on the OSR. **(DEFAULT)**

bit 9:8 **DRB_MODE[1:0]**
11 = Both Data Ready pulses from CH2 and CH3 are output on $\overline{DRB}$ pin.
10 = Data Ready pulses from CH3 are output on $\overline{DRB}$ pin. Data Ready pulses from CH2 are not present on the pin.
01 = Data Ready pulses from CH2 are output on $\overline{DRB}$ pin. Data Ready pulses from CH3 are not present on the pin.
00 = Data Ready pulses from the lagging ADC channel between the two are output on $\overline{DRB}$ pin. The lagging ADC channel depends on the phase register and on the OSR. **(DEFAULT)**

bit 7:6 **DRA_MODE[1:0]**
11 = Both Data Ready pulses from CH0 and CH1 are output on $\overline{DRA}$ pin.
10 = Data Ready pulses from CH1 are output on $\overline{DRA}$ pin. Data Ready pulses from CH0 are not present on the pin.
01 = Data Ready pulses from CH0 are output on $\overline{DRA}$ pin. Data Ready pulses from CH1 are not present on the pin.
00 = Data Ready pulses from the lagging ADC channel between the two are output on $\overline{DRA}$ pin. The lagging ADC channel depends on the phase register and on the OSR. **(DEFAULT)**

bit 5:0 **DRSTATUS_CHn: Data Ready Status**
1 = Data Not Ready (default)
0 = Data Ready

7.6 Config Register - Configuration Register

TABLE 7-8: CONFIG Register

Name	Bits	Address	Cof
CONFIG	24	0x0A	R/W

REGISTER 7-6: CONFIG REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RESET_CH5	RESET_CH4	RESET_CH3	RESET_CH2	RESET_CH1	RESET_CH0	SHUTDOWN_CH5	SHUTDOWN_CH4
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1
SHUTDOWN_ CH3	SHUTDOWN_ CH2	SHUTDOWN_CH1	SHUTDOWN_CH0	DITHER_CH5	DITHER_CH4	DITHER_CH3	DITHER_CH2
bit 15							bit 8

R/W-1	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
DITHER_CH1	DITHER_CH0	OSR1	OSR0	PRESCALE1	PRESCALE0	EXTVREF	EXTCLK
bit 7							bit 0

bit 23:18 **RESET_CHn:** Reset mode setting for ADCs

1 = Reset mode for the corresponding ADC channel ON
0 = Reset mode for the corresponding ADC chnnel OFF **(default)**

bit 17:12 **SHUTDOWN_CHn:** Shutdown mode setting for ADCs

1 = Shutdown mode for the corresponding ADC channel ON
0 = Shutdown mode for the corresponding ADC channel OFF**(default)**

bit 11:6 **DITHER_CHn:** Control for dithering circuit for idle tones cancellation

1 = Dithering circuit for the corresponding ADC channel ON **(default)**
0 = Dithering circuit for the corresponding ADC channel OFF

bit 5:4 **OSR[1:0]** Oversampling Ratio for Delta Sigma A/D Conversion (ALL CHANNELS, f_d / f_S)

11 = 256
10 = 128
01 = 64 **(default)**
00 = 32

bit 3:2 **PRESCALE[1:0]** Internal Master Clock (AMCLK) Prescaler Value

11 = AMCLK = MCLK/ 8
10 = AMCLK = MCLK/ 4
01 = AMCLK = MCLK/ 2
00 = AMCLK = MCLK (DEFAULT)

bit 1 **EXTVREF** Internal Voltage Reference Shutdown Control

1 = Internal Voltage Reference Disabled
0 = Internal Voltage Reference Enabled **(default)**

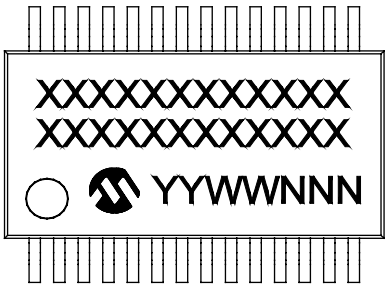
bit 0 **EXTCLK** Clock Mode

1 = CLOCK Mode (Internal Oscillator Disabled - Lower Power)
0 = XT Mode - A crystal must be placed between OSC1/OSC2 **(default)**

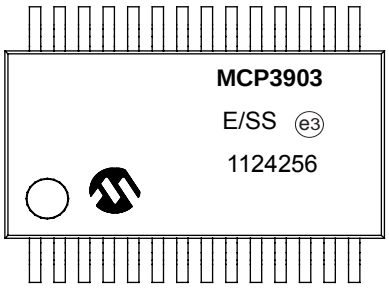
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

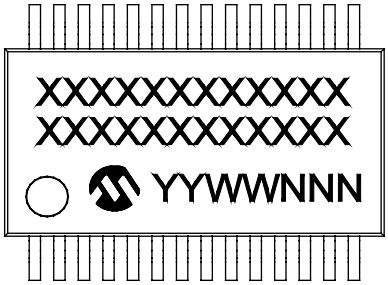
28-Lead SSOP (5.30 mm)



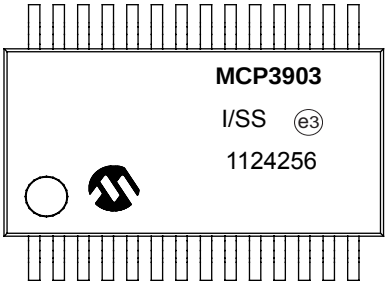
Example



28-Lead SSOP (5.30 mm)



Example

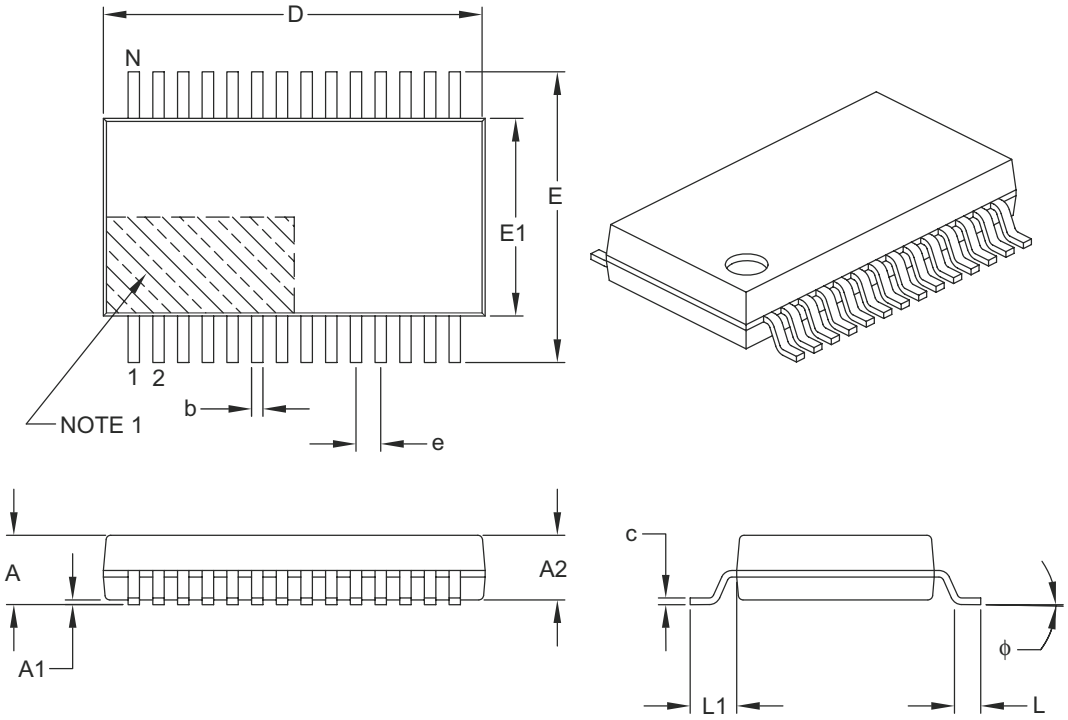


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

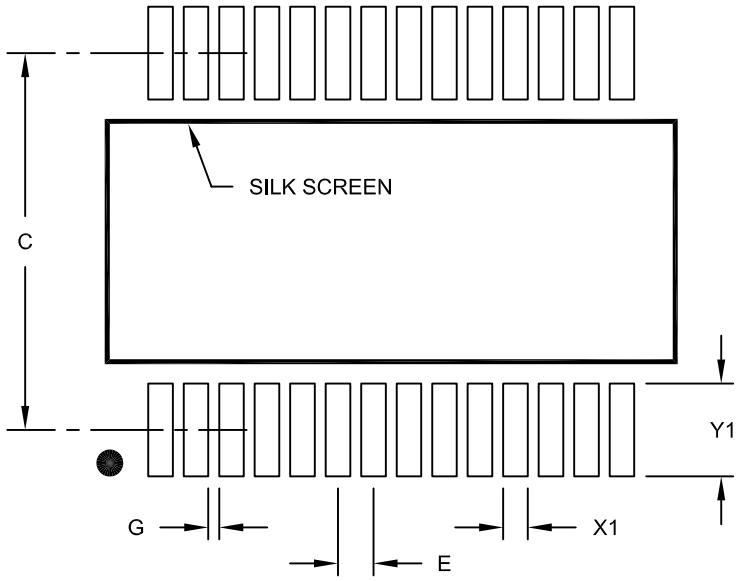
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

APPENDIX A: REVISION HISTORY

Revision B (July 2011)

- Added **Section 2.0, Typical Performance Curves**, with characterization graphs.

Revision A (June 2011)

- Original data sheet for the MCP3903 device.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	X	/XX
Device	Tape and Reel	Temperature Range	Package

Device:	MCP3903:	Six Channel ΔΣ A/D Converter
	* Default option. Contact Microchip factory for other address options	
Tape and Reel:	T =	Tape and Reel
Temperature Range:	I =	-40°C to +85°C
	E =	-40°C to +125°C
Package:	SS =	Small Shrink Output Package (SSOP-28)

Examples:

a) MCP3903T-E/SS: Tape and Reel, Six Channel ΔΣ A/D Converter, SSOP-28 package

b) MCP3903T-I/SS: Tape and Reel, Six Channel ΔΣ A/D Converter, SSOP-28 package

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