

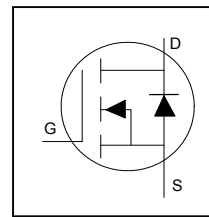
IR MOSFET - StrongIRFET™

Applications

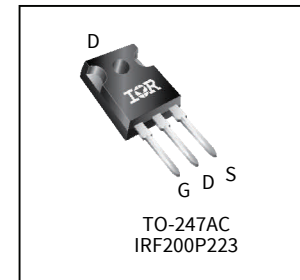
- UPS and Inverter applications
- Half-bridge and full-bridge topologies
- Resonant mode power supplies
- DC/DC and AC/DC converters
- OR-ing and redundant power switches
- Brushed and BLDC Motor drive applications
- Battery powered circuits

Benefits

- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dv/dt and di/dt Capability
- Pb-Free ; RoHS Compliant ; Halogen-Free



V_{DSS}	200V
R_{DS(on) typ.}	9.5mΩ
	max
I_D	100A



G	D	S
Gate	Drain	Source



Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF200P223	TO-247AC	Tube	25	IRF200P223

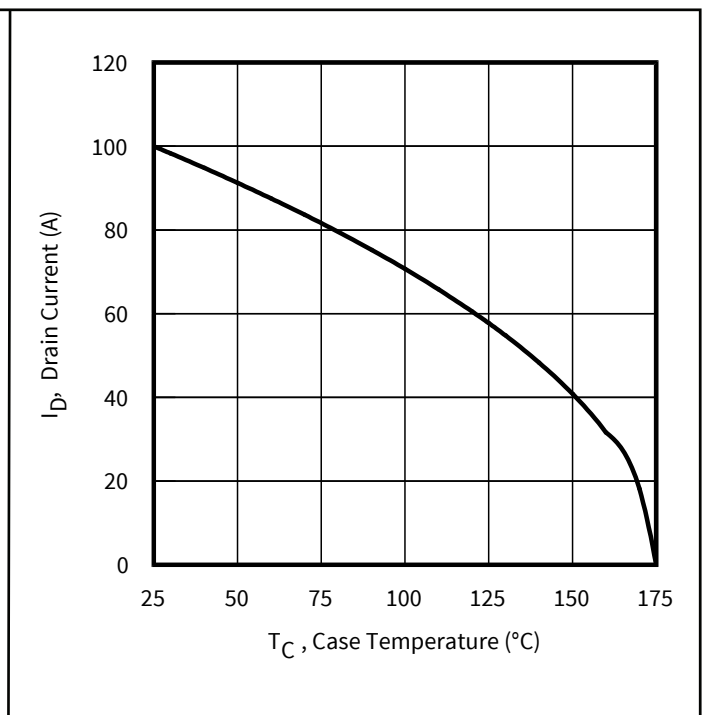
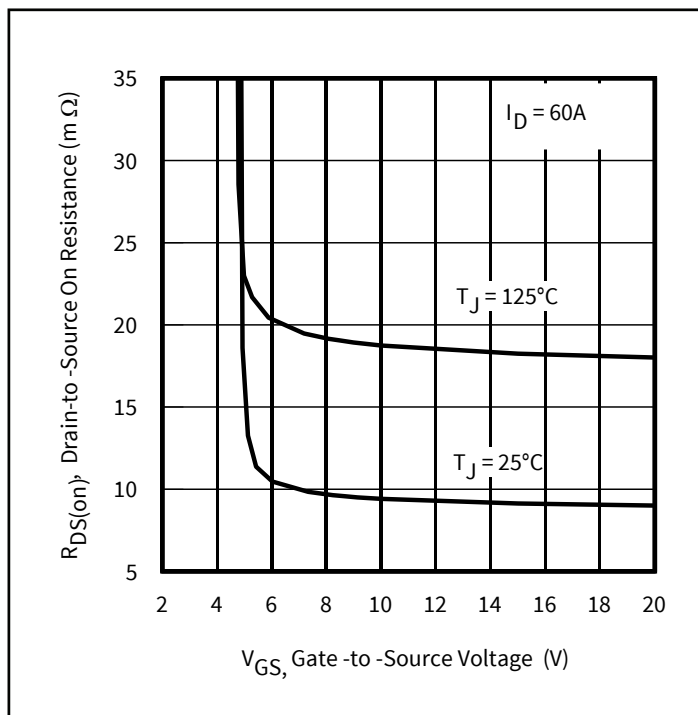


Figure 1 Typical On-Resistance vs. Gate Voltage

Figure 2 Maximum Drain Current vs. Case Temperature

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1 Parameters

Table1 Key performance parameters

Parameter	Values	Units
V_{DS}	200	V
$R_{DS(on) \max}$	11.5	m Ω
I_D	100	A

2 Maximum ratings and thermal characteristics

Table 2 Maximum ratings (at $T_J=25^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Conditions	Values	Unit
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$, $V_{GS} @ 10\text{V}$	100	A
Continuous Drain Current	I_D	$T_C = 100^\circ\text{C}$, $V_{GS} @ 10\text{V}$	71	
Pulsed Drain Current ①	I_{DM}	$T_C = 25^\circ\text{C}$	400	
Maximum Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	313	W
Linear Derating Factor		$T_C = 25^\circ\text{C}$	2.1	W/ $^\circ\text{C}$
Gate-to-Source Voltage	V_{GS}	-	± 20	V
Operating Junction and Storage Temperature Range	T_J T_{STG}	-	-55 to +175	$^\circ\text{C}$
Soldering Temperature, for 10 seconds (1.6mm from case)	-	-	300	
Mounting Torque, 6-32 or M3 Screw	-	-	10 lbf·in (1.1 N·m)	

Table 3 Thermal characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Junction-to-Case ⑦	$R_{\theta JC}$	T_J approximately 90°C	-	-	0.48	$^\circ\text{C}/\text{W}$
Case-to-Sink, Flat Greased Surface	$R_{\theta CS}$	-	-	0.24	-	
Junction-to-Ambient	$R_{\theta JA}$	-	-	-	40	

Table 4 Avalanche characteristics

Parameter	Symbol	Values	Unit
Single Pulse Avalanche Energy ②	E_{AS} (Thermally limited)	429	mJ
Single Pulse Avalanche Energy ⑧	E_{AS} (Thermally limited)	541	
Avalanche Current ①	I_{AR}	See Fig 16, 17, 23a, 23b	A
Repetitive Avalanche Energy ①	E_{AR}		mJ

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.24\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 60\text{A}$, $V_{GS} = 10\text{V}$.
- ③ $I_{SD} \leq 60\text{A}$, $di/dt \leq 2330\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ R_θ is measured at T_J approximately 90°C .
- ⑧ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 1\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 33\text{A}$, $V_{GS} = 10\text{V}$.

3 Electrical characteristics

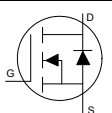
Table 5 Static characteristics

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 1mA$	200	-	-	V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to 25°C, $I_D = 1mA$ ①	-	0.10	-	V/°C
Static Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 60A$	-	9.5	11.5	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 270\mu A$	2.0	-	4.0	V
Drain-to-Source Leakage Current	I_{DSS}	$V_{DS} = 160V, V_{GS} = 0V$	-	-	1.0	μA
		$V_{DS} = 160V, V_{GS} = 0V, T_J = 125^\circ C$	-	-	100	
Gate-to-Source Forward Leakage	I_{GSS}	$V_{GS} = 20V$	-	-	100	nA
Gate Resistance	R_G		-	2.7	-	Ω

Table 6 Dynamic characteristics

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Forward Trans conductance	gfs	$V_{DS} = 50V, I_D = 60A$	93	-	-	S
Total Gate Charge	Q_g	$I_D = 60A$ $V_{DS} = 100V$ $V_{GS} = 10V$	-	68	102	nC
Gate-to-Source Charge	Q_{gs}		-	25	-	
Gate-to-Drain Charge	Q_{gd}		-	13	-	
Total Gate Charge Sync. ($Q_g - Q_{gd}$)	Q_{sync}		-	55	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 130V$	-	16	-	ns
Rise Time	t_r	$I_D = 60A$	-	66	-	
Turn-Off Delay Time	$t_{d(off)}$	$R_G = 2.7\Omega$	-	55	-	
Fall Time	t_f	$V_{GS} = 10V$	-	62	-	
Input Capacitance	C_{iss}	$V_{GS} = 0V$	-	5094	-	pF
Output Capacitance	C_{oss}	$V_{DS} = 50V$	-	628	-	
Reverse Transfer Capacitance	C_{rss}	$f = 1.0MHz$, See Fig.7	-	8.7	-	
Effective Output Capacitance (Energy Related)	$C_{oss\ eff.(ER)}$	$V_{GS} = 0V, V_{DS} = 0V$ to 160V ⑥	-	537	-	
Output Capacitance (Time Related)	$C_{oss\ eff.(TR)}$	$V_{GS} = 0V, V_{DS} = 0V$ to 160V ⑤	-	783	-	

Table 7 Reverse Diode

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode. 	-	-	100	A
Pulsed Source Current (Body Diode) ①	I_{SM}		-	-	400	
Diode Forward Voltage	V_{SD}	$T_J = 25^\circ C, I_S = 60A, V_{GS} = 0V$ ④	-	-	1.2	V
Peak Diode Recovery dv/dt ③	dv/dt	$T_J = 175^\circ C, I_S = 60A, V_{DS} = 200V$	-	15	-	V/ns
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ C$ $V_{DD} = 170V$	-	105	-	ns
		$T_J = 125^\circ C$ $I_F = 60A,$	-	150	-	
Reverse Recovery Charge	Q_{rr}	$T_J = 25^\circ C$ $di/dt = 100A/\mu s$ ④	-	283	-	nC
		$T_J = 125^\circ C$	-	580	-	
Reverse Recovery Current	I_{RRM}	$T_J = 25^\circ C$	-	4.1	-	A

4 Electrical characteristic diagrams

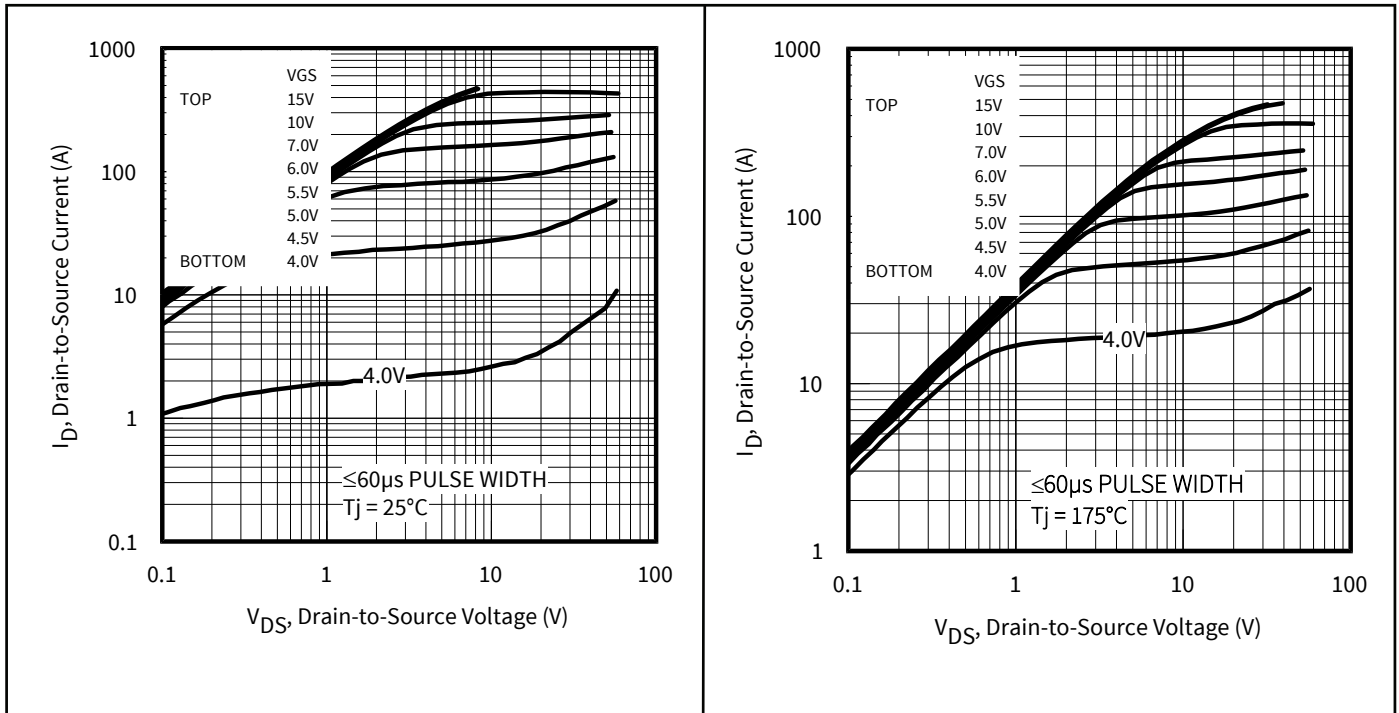


Figure 3 Typical Output Characteristics

Figure 4 Typical Output Characteristics

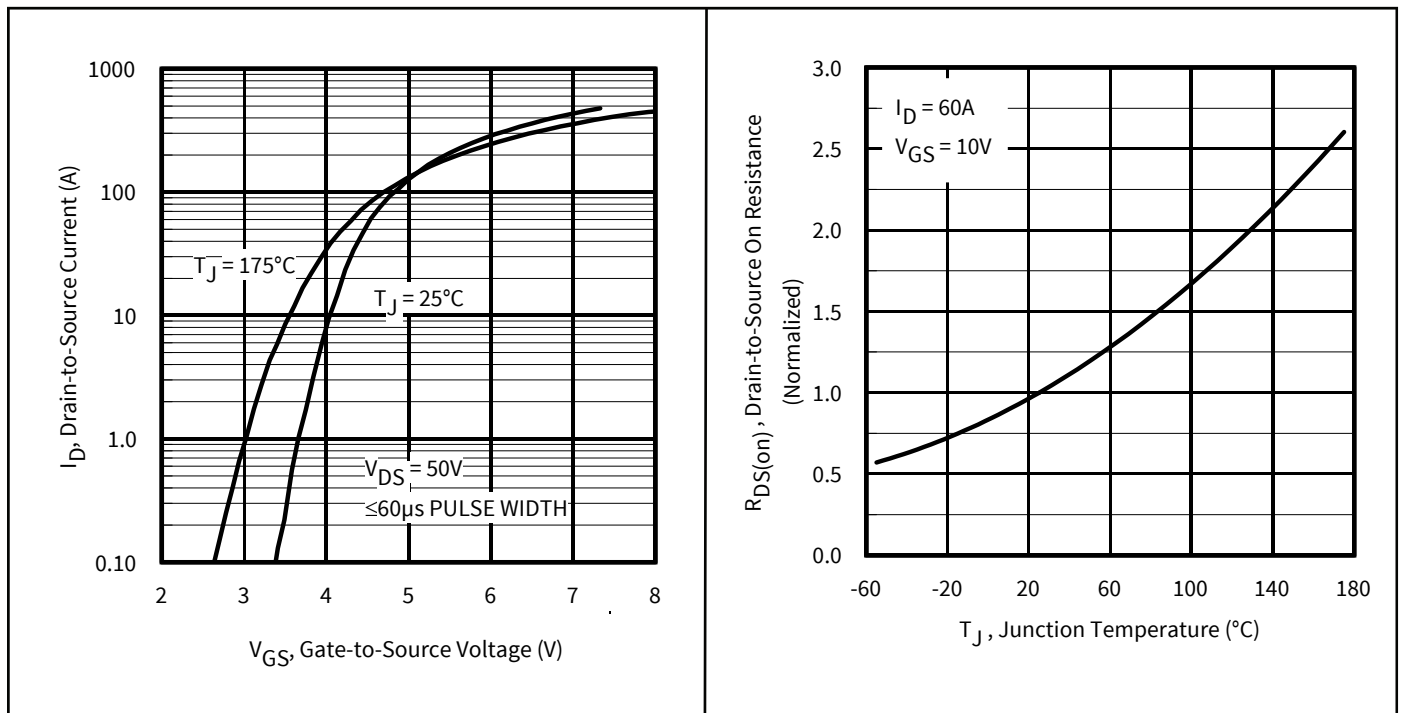


Figure 5 Typical Transfer Characteristics

Figure 6 Normalized On-Resistance vs. Temperature

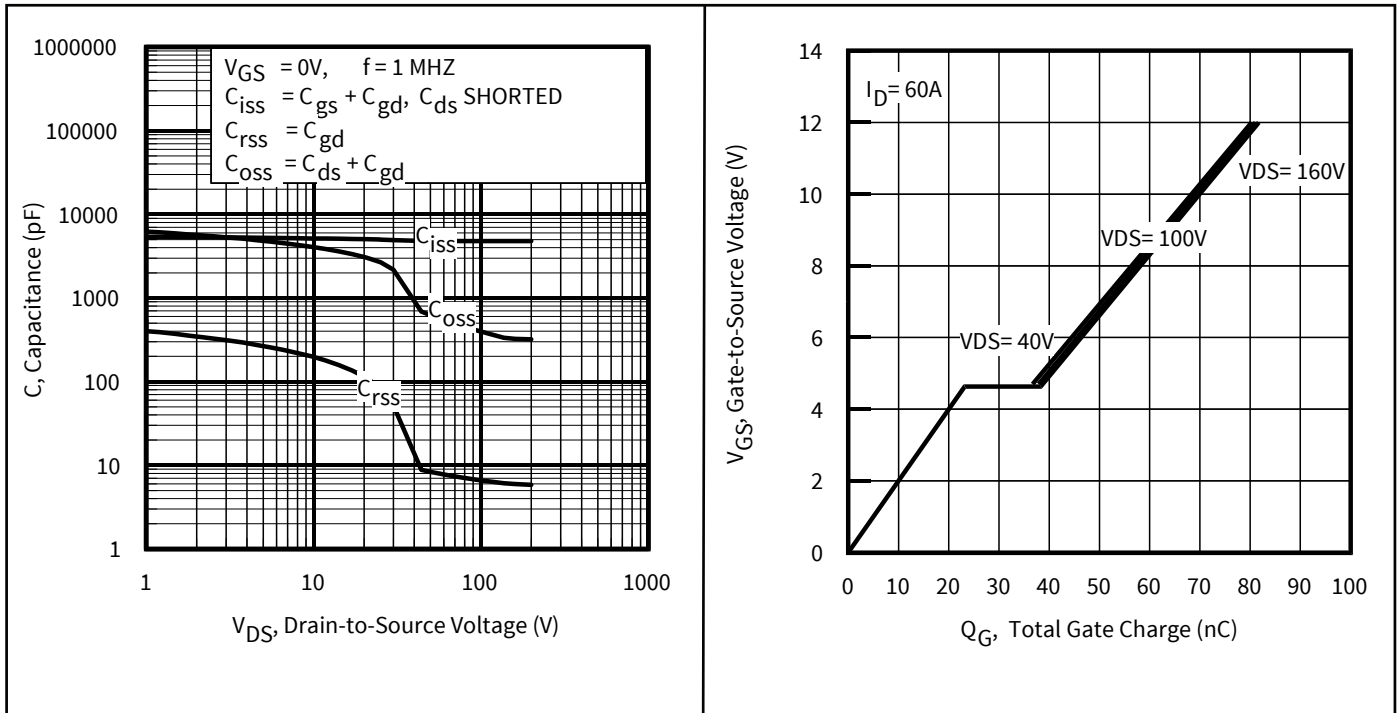


Figure 7 Typical Capacitance vs. Drain-to-Source Voltage

Figure 8 Typical Gate Charge vs. Gate-to-Source Voltage

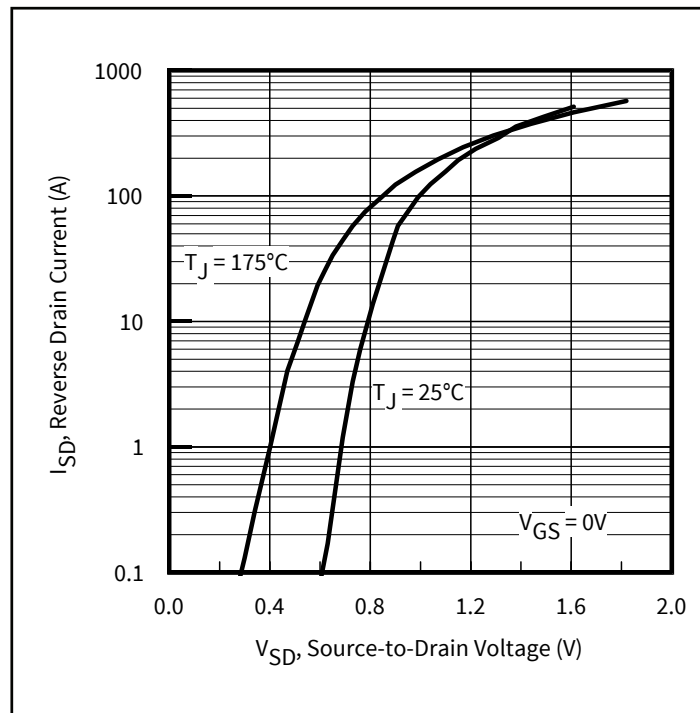


Figure 9 Typical Source-Drain Diode Forward Voltage

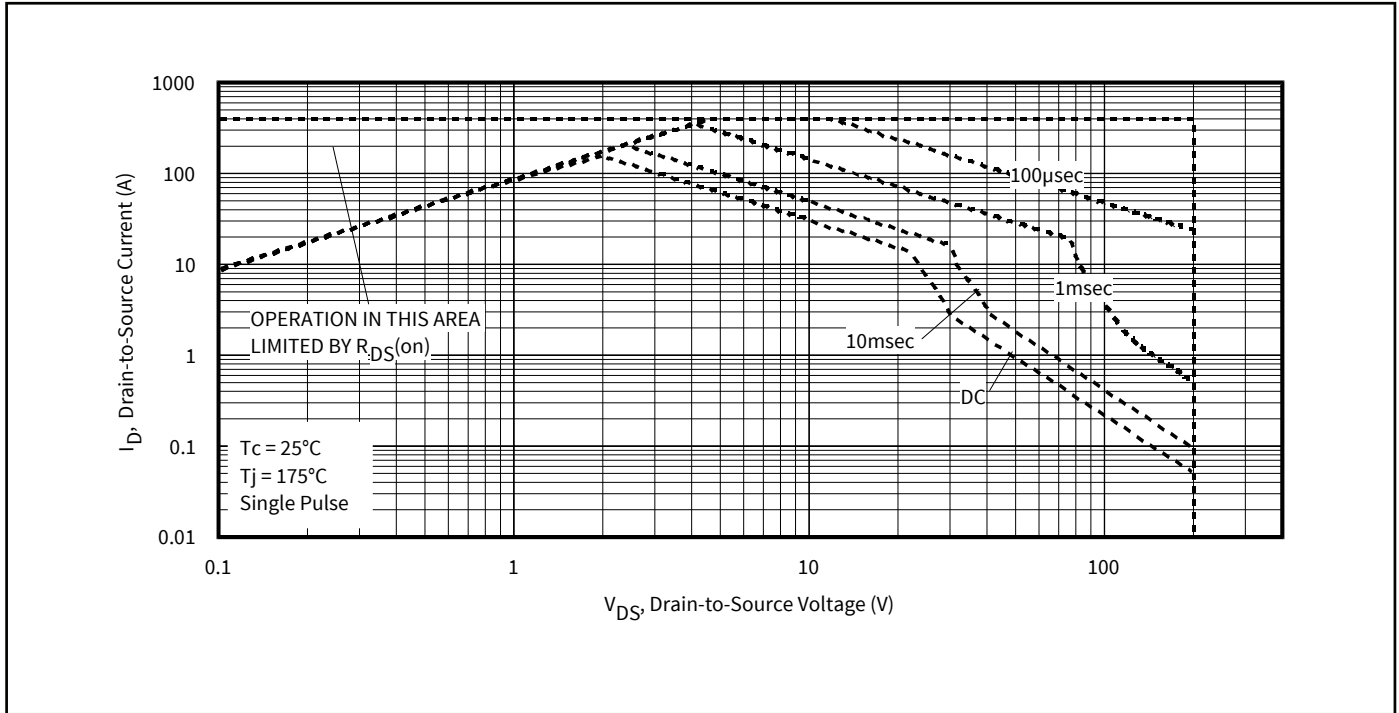


Figure 10 Maximum Safe Operating Area

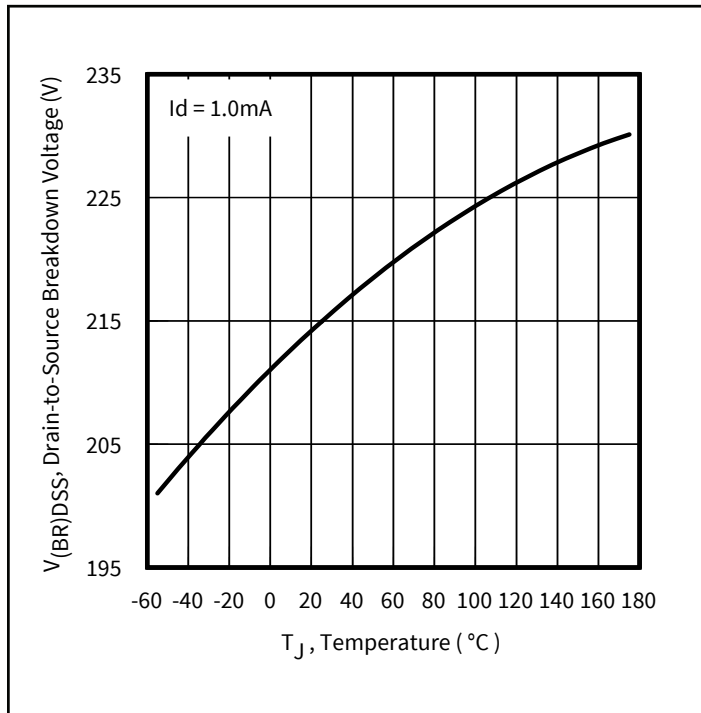


Figure 11 Drain-to-Source Breakdown Voltage

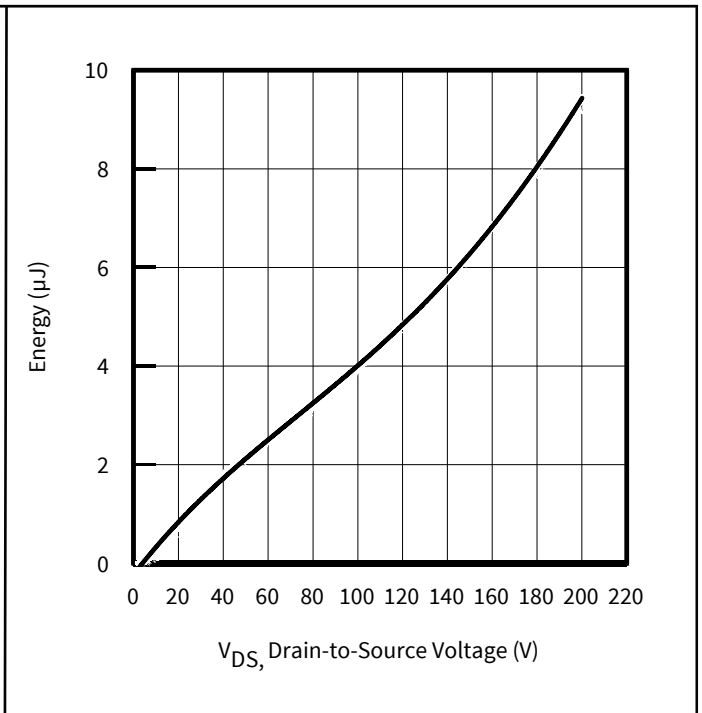


Figure 12 Typical Coss Stored Energy

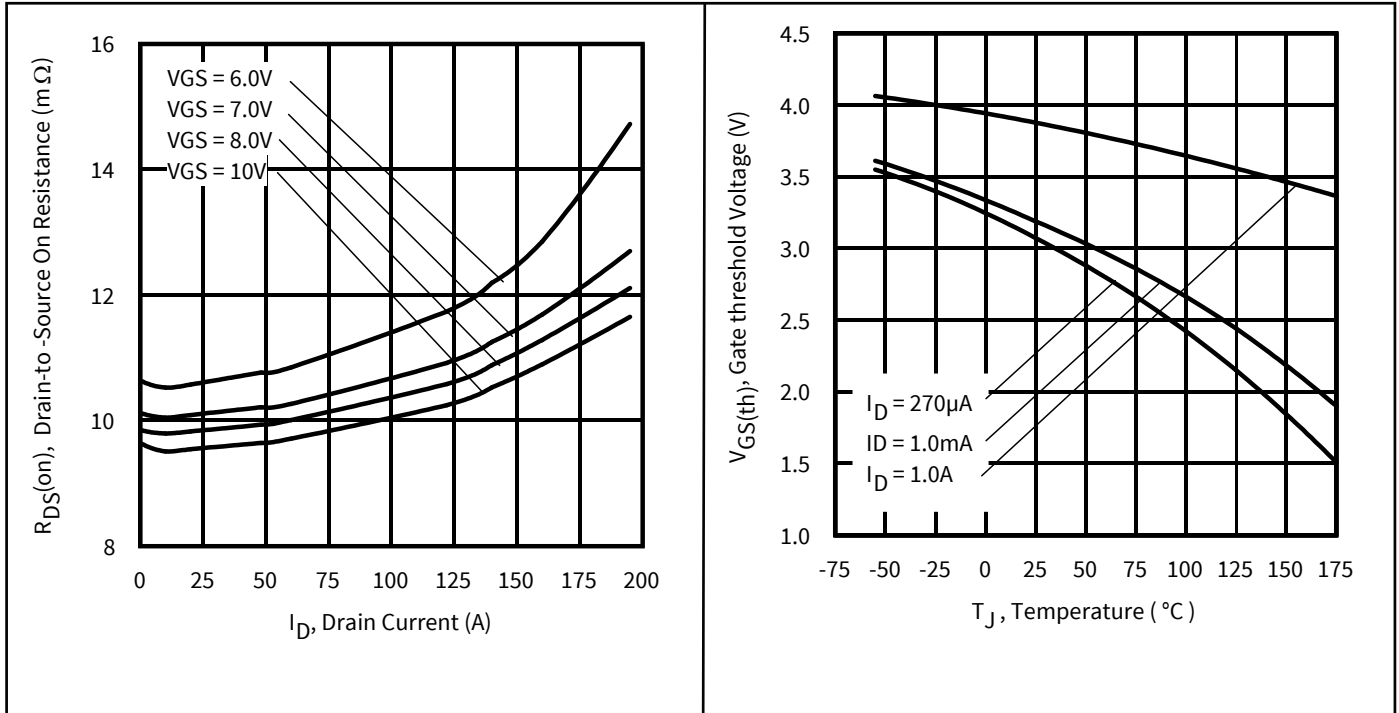


Figure 13 Typical On-Resistance vs. Drain Current

Figure 14 Threshold Voltage vs. Temperature

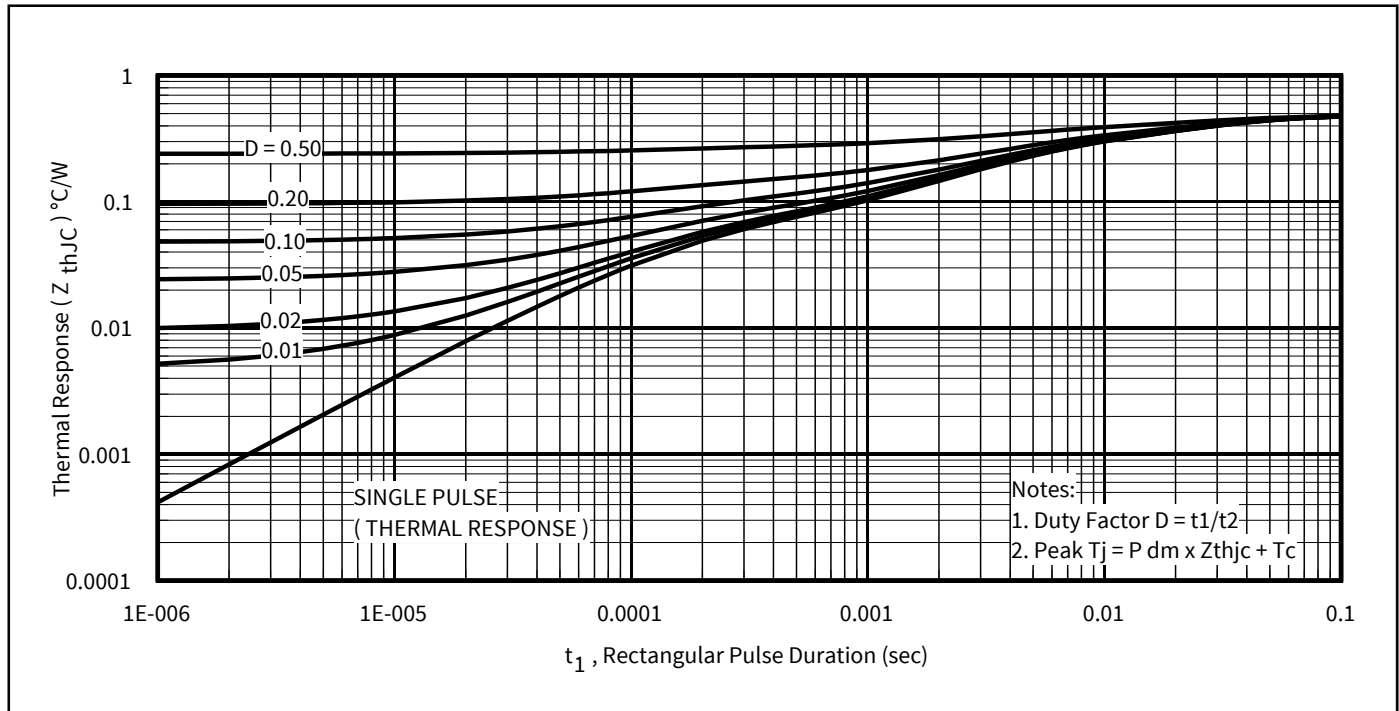


Figure 15 Maximum Effective Transient Thermal Impedance, Junction-to-Case

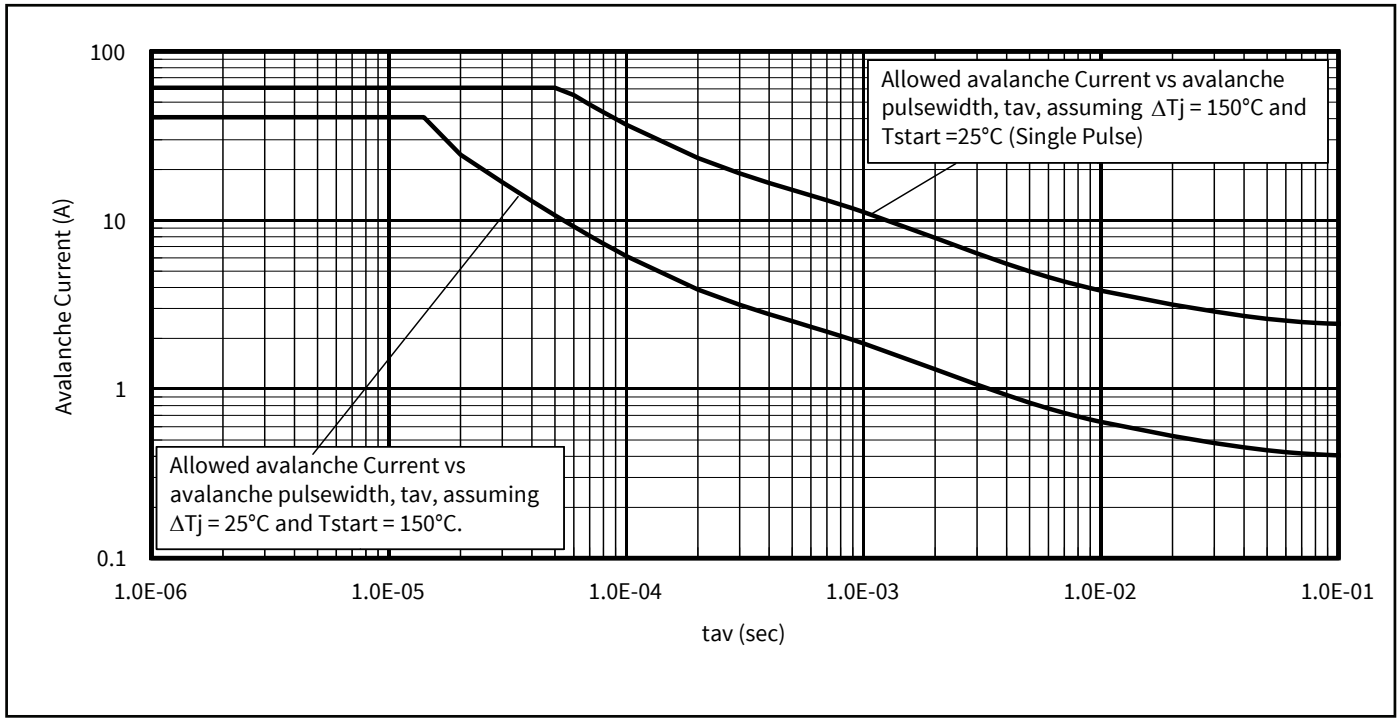
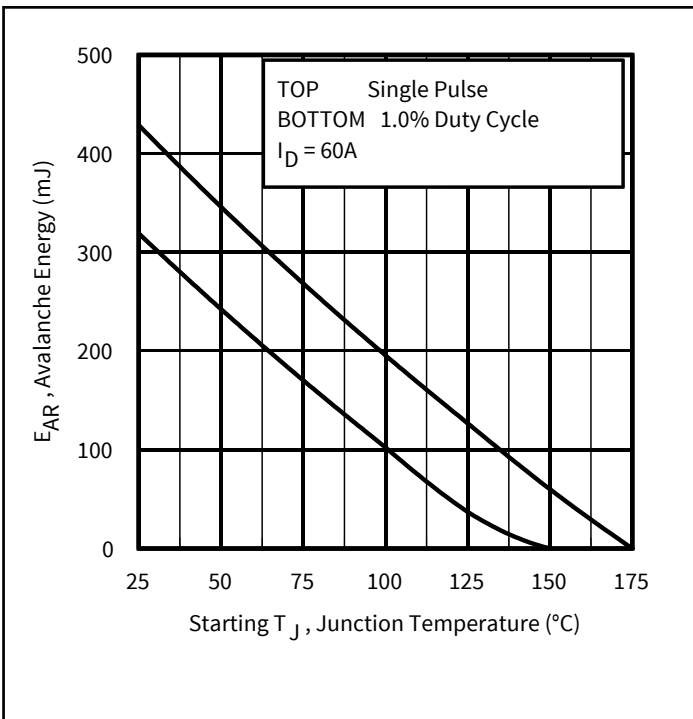


Figure 16 Avalanche Current vs. Pulse Width



Notes on Repetitive Avalanche Curves , Figures 16, 17:
(For further info, see AN-1005 at www.infineon.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. DT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 14)
 $P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$

Figure 17 Maximum Avalanche Energy vs. Temperature

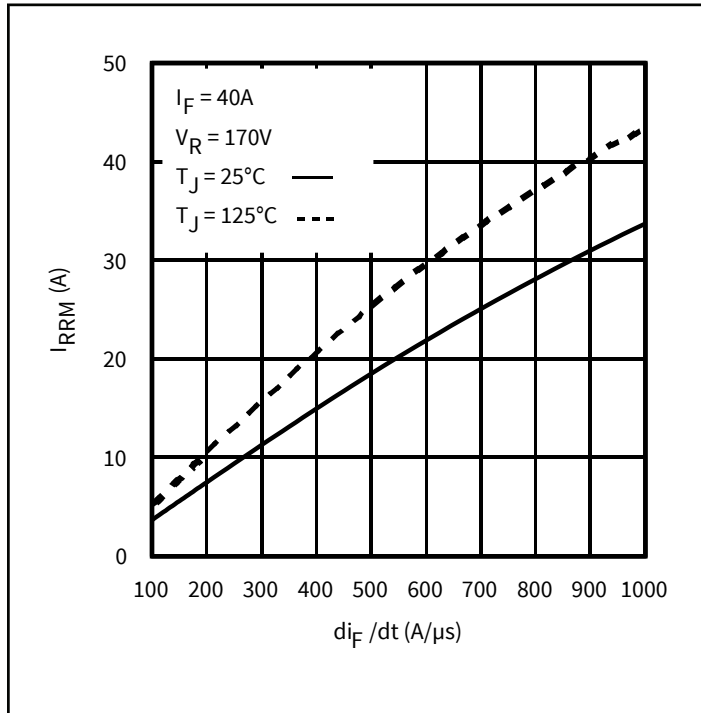


Figure 18 Typical Recovery Current vs. di_F/dt

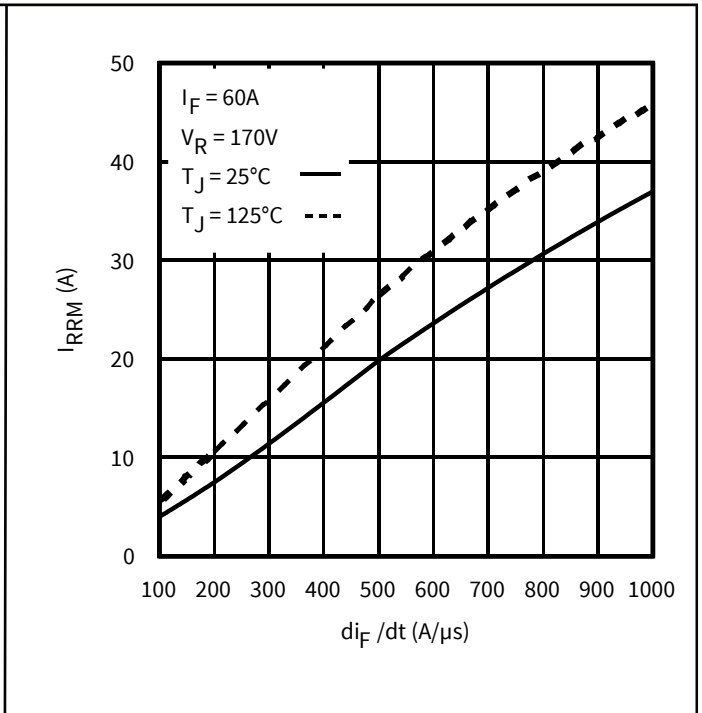


Figure 19 Typical Recovery Current vs. di_F/dt

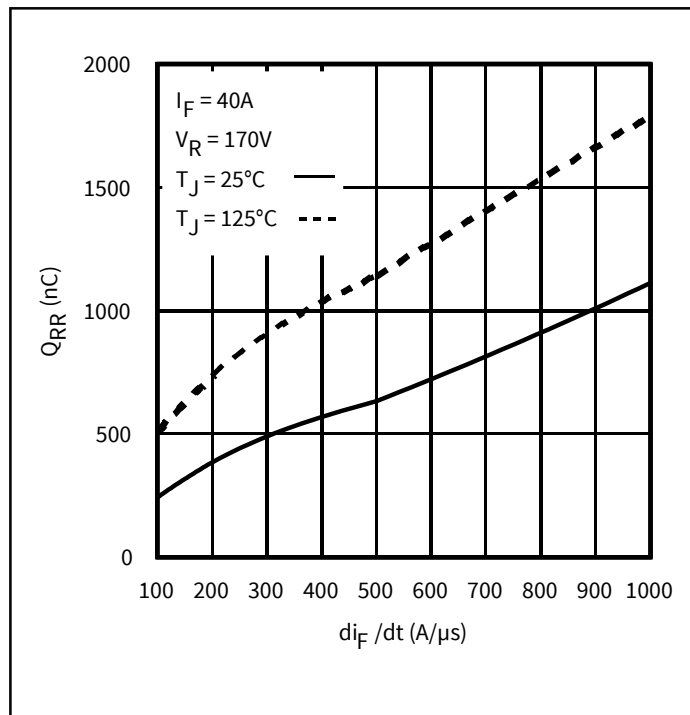


Figure 20 Typical Stored Charge vs. di_F/dt

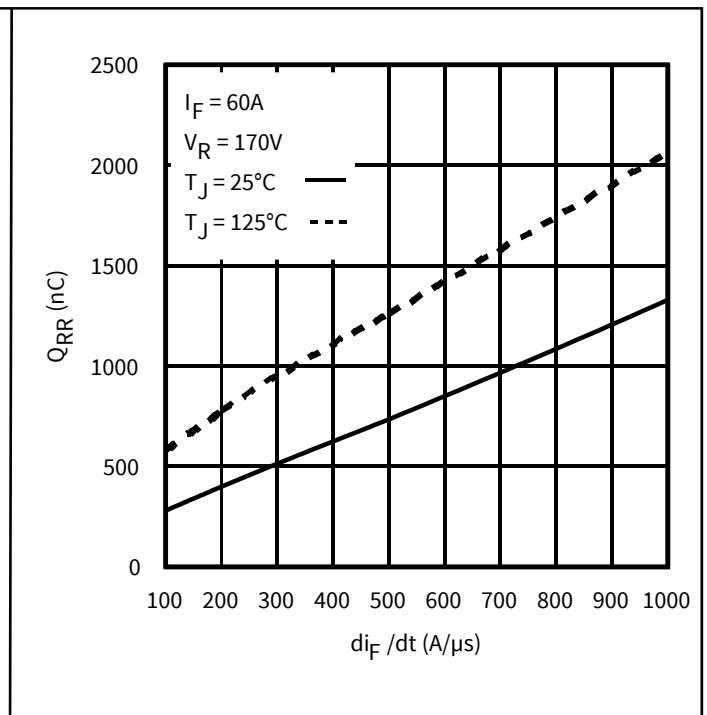


Figure 21 Typical Stored Charge vs. di_F/dt

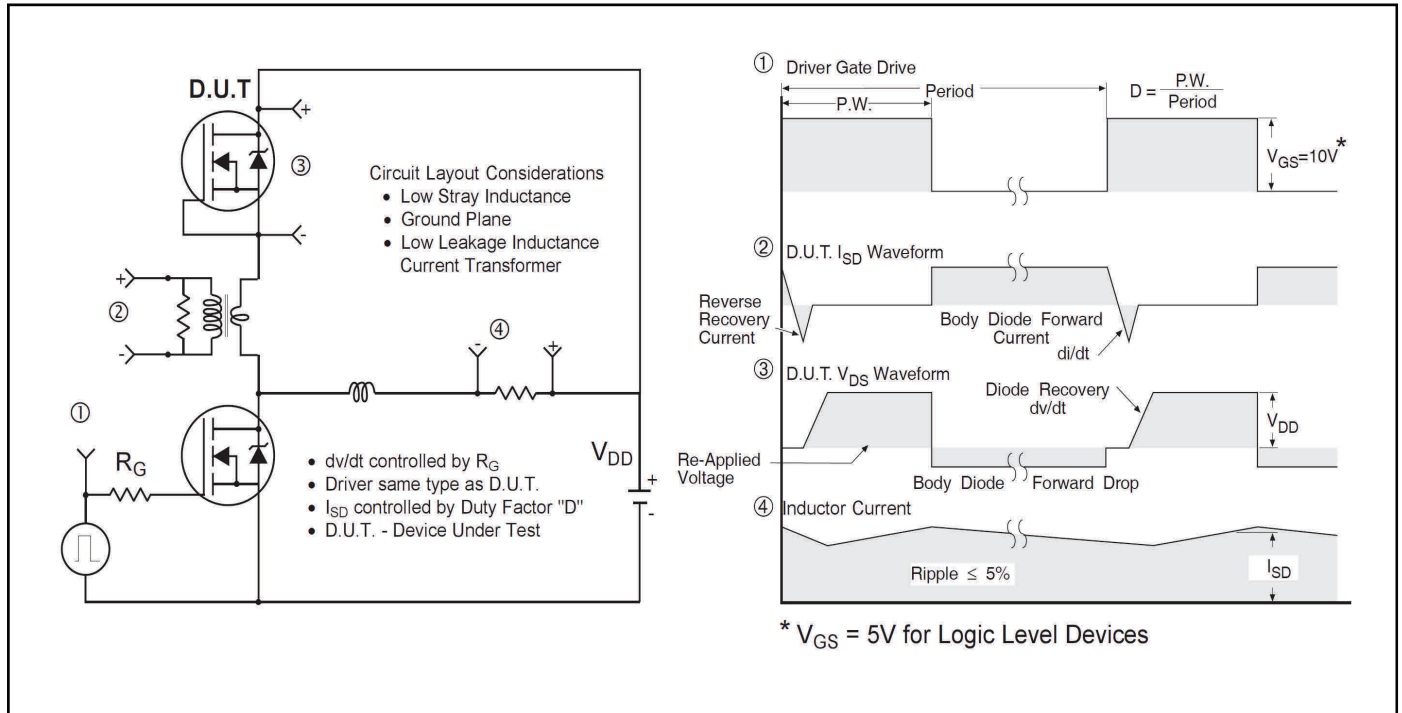


Figure 22 Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET™ Power MOSFETs

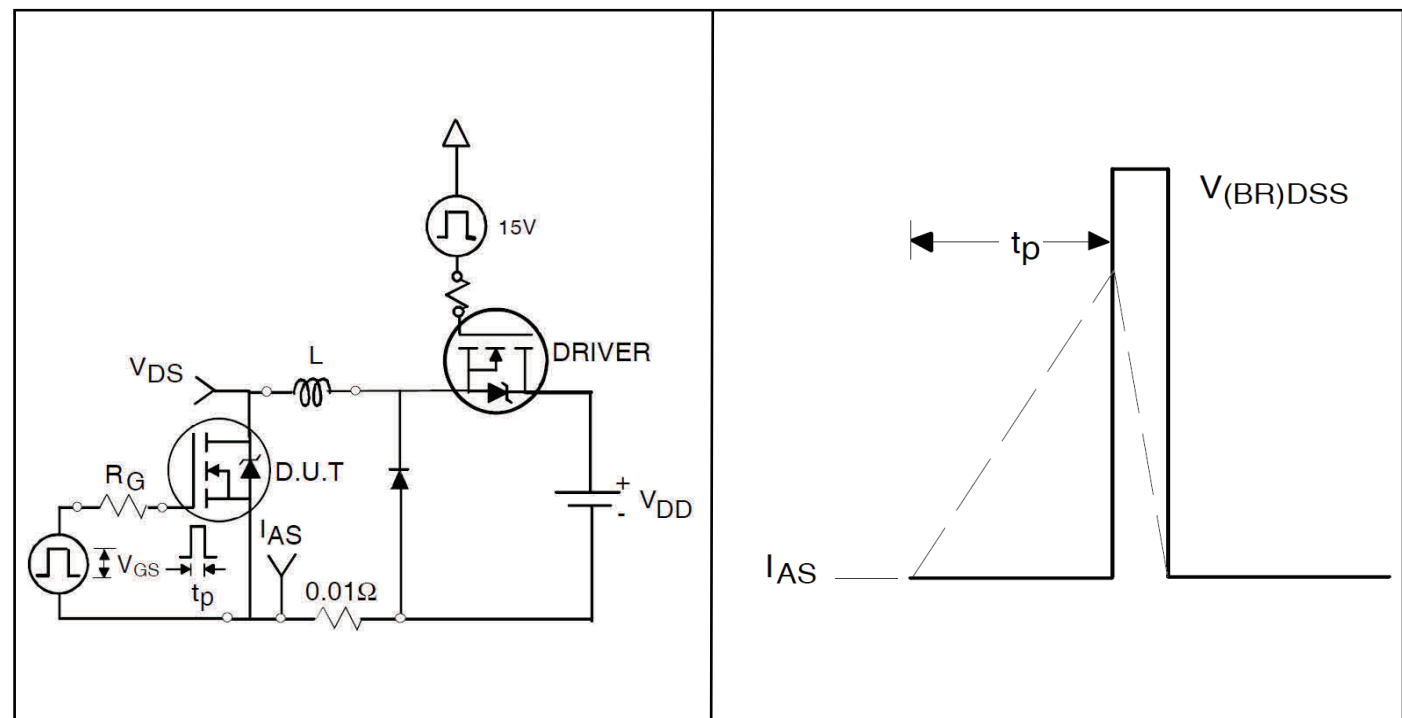


Figure 23a Unclamped Inductive Test Circuit

Figure 23b Unclamped Inductive Waveforms

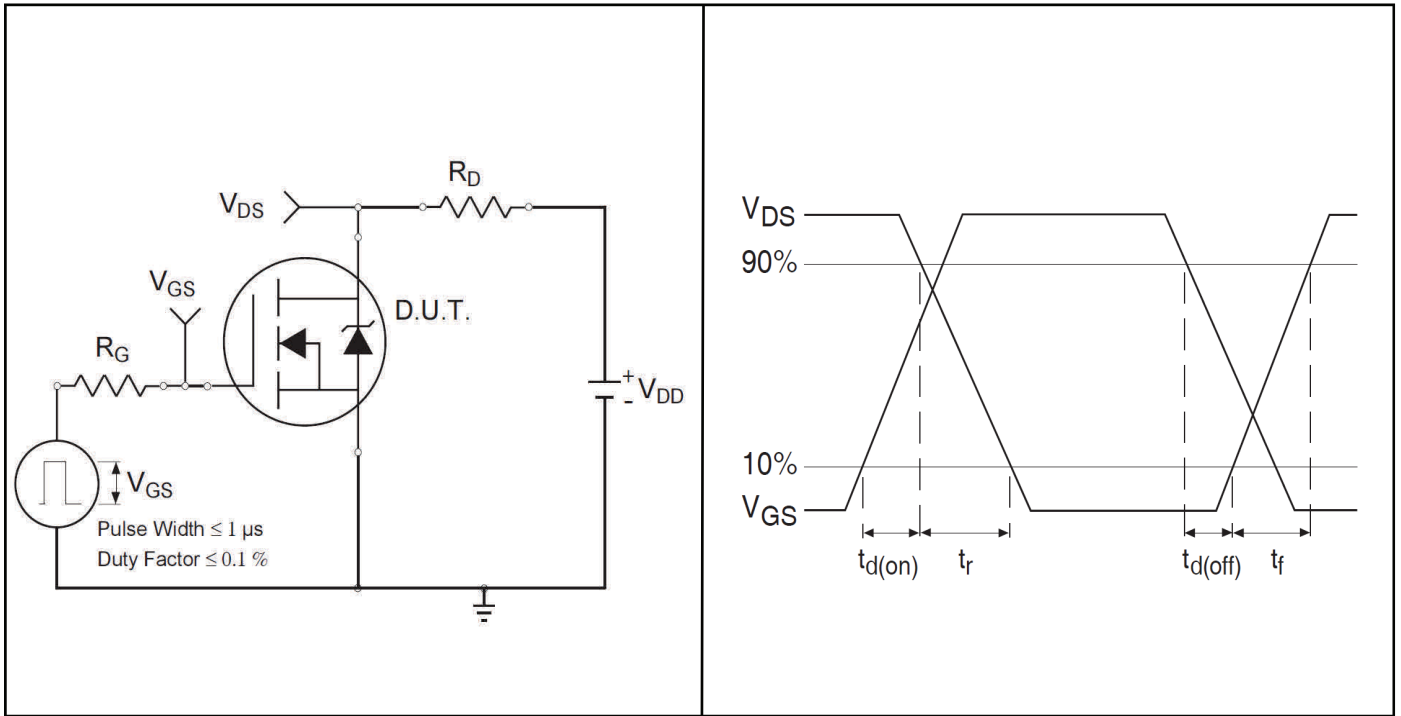
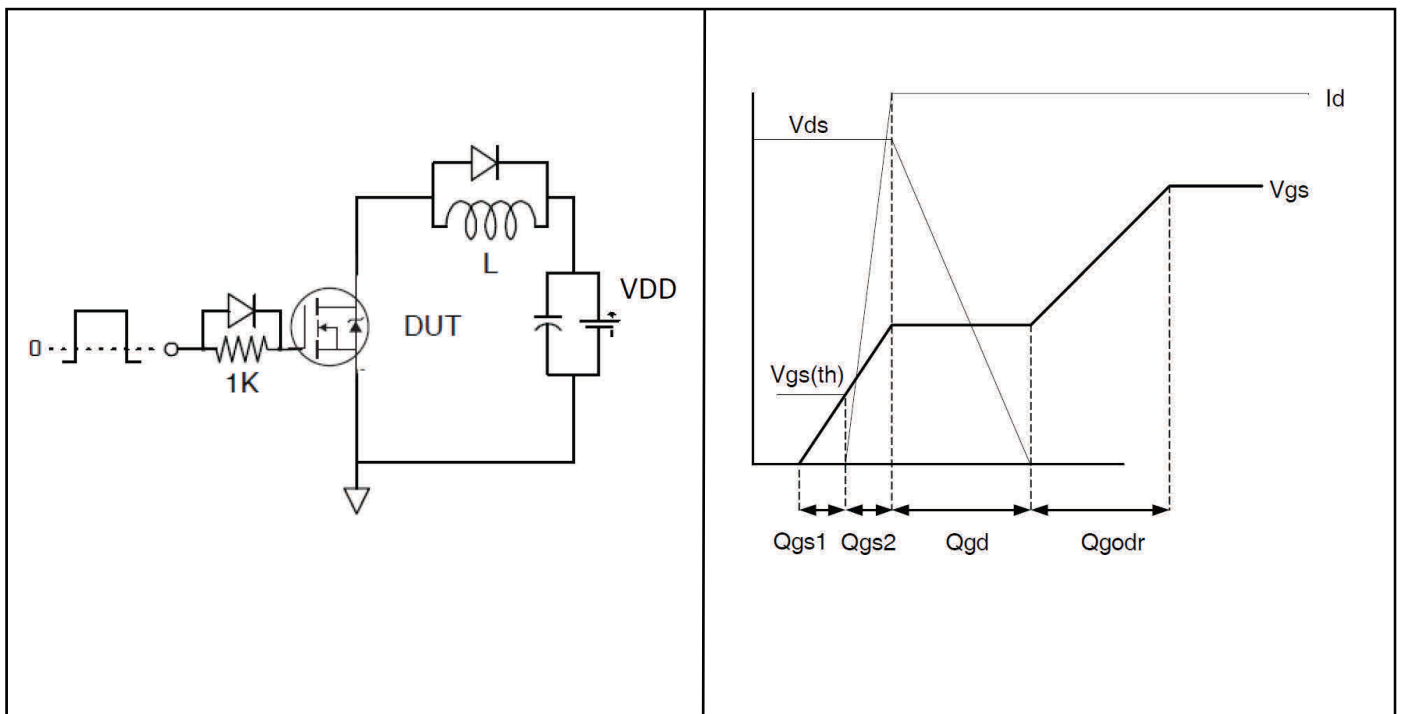


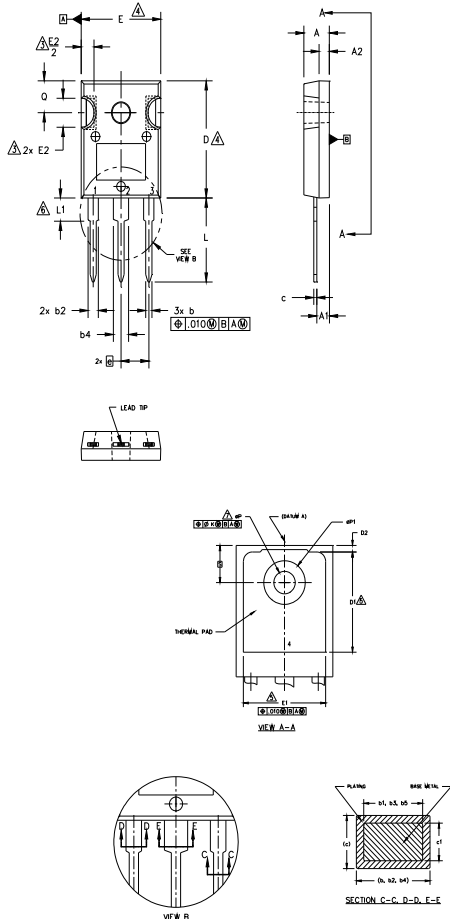
Figure 24a Switching Time Test Circuit

Figure 24b Switching Time Waveforms



5 Package Information

TO-247AC Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ϕP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
ϕk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
ϕP	.140	.144	3.56	3.66	
$\phi P1$	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

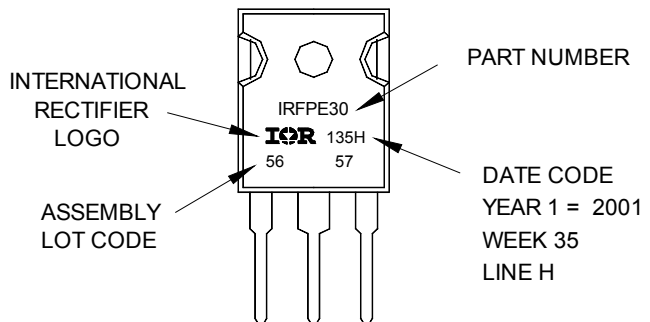
DIODES

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2001
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-247AC package is not recommended for Surface Mount Application.

6 Qualification Information

Qualification Information

Qualification Level	Industrial (per JEDEC JESD47F) †	
Moisture Sensitivity Level	TO-247AC	N/A
RoHS Compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Revision History

Major changes since the last revision

Page or Reference	Revision	Date	Description of changes
All pages	1.0	2017-03-16	• First release data sheet.

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<http://moschip.ru/get-element>

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

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