

BUK9K32-100E

Dual N-channel 100 V, 33 m Ω logic level MOSFET

10 December 2013

Product data sheet

1. General description

Dual logic level N-channel MOSFET in an LFPAK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Dual MOSFET
- Q101 Compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with V_{GS(th)} rating of greater than 0.5 V at 175 °C

3. Applications

- 12 V, 24 V and 48 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	100	V
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; <u>Fig. 1</u>		-	-	26	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>		-	-	64	W
Static characte	Static characteristics FET1 and FET2						
R _{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ °C}; Fig. 11$		-	26.6	33	mΩ
Dynamic characteristics FET1 and FET2							
Q_{GD}	gate-drain charge	$I_D = 5 \text{ A}; V_{DS} = 80 \text{ V}; V_{GS} = 5 \text{ V};$ $T_j = 25 \text{ °C}; \underline{\text{Fig. 13}}; \underline{\text{Fig. 14}}$		-	11	-	nC



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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	8 7 6 5	D1 D1 D2 D2
2	G1	gate1	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2	l l l l l	mbk725
7	D1	drain1	1 2 3 4 LFPAK56D (SOT1205)	
8	D1	drain1	2.17.11.005 (0011200)	

6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
BUK9K32-100E	LFPAK56D	Plastic single ended surface mounted package (LFPAK56D); 8 leads	SOT1205		

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9K32-100E	93210E

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

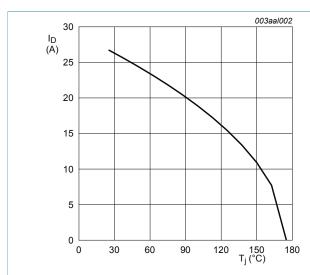
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	100	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 k Ω		-	100	V
V_{GS}	gate-source voltage	T _j ≤ 175 °C; DC		-10	10	V
		T _j ≤ 175 °C; Pulsed	[1][2]	-15	15	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 5 V; <u>Fig. 1</u>		-	26	Α
		T _{mb} = 100 °C; V _{GS} = 5 V; <u>Fig. 1</u>		-	19	Α
I _{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \mu s$; Fig. 4		-	106	Α

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Symbol	Parameter	Conditions		Min	Max	Unit
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>		-	64	W
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
Source-drai	n diode FET1 and FET2		'			'
I _S	source current			-	26	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	106	Α
Avalanche Ruggedness FET1 and FET2						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	$I_D = 26 \text{ A}; V_{sup} \le 100 \text{ V}; V_{GS} = 10 \text{ V};$ $T_{j(init)} = 25 \text{ °C}; Fig. 3$	[3][4]	-	74	mJ

- Accumulated Pulse duration up to 50 hours delivers zero defect ppm
- Significantly longer life times are achieved by lowering T_i and or V_{GS} . [2]
- [3] [4] Refer to application note AN10273 for further information
- Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



Continuous drain current as a function of mounting base temperature

$$V_{GS} \ge 5V$$

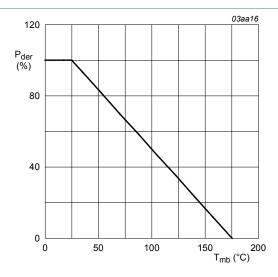


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

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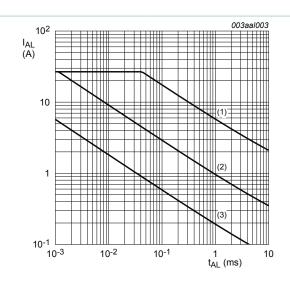
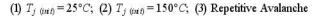


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time



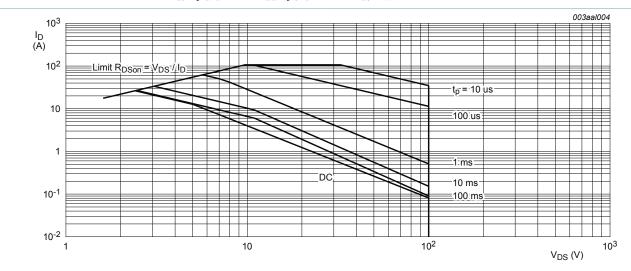


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

 $T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

9. Thermal characteristics

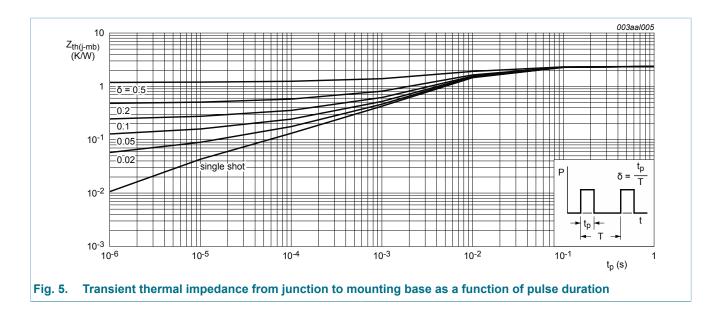
Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 5	-	-	2.36	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics FET1 and FET2		'			
V _{(BR)DSS}	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	90	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	100) -	-	V
$V_{GS(th)}$	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; Fig. 9; Fig. 10	1.4	1.7	2.1	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; Fig. 9; Fig. 10	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 9; Fig. 10	-	-	2.45	V
I _{DSS} drain leakag	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C	-	0.02	1	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μΑ
I _{GSS}	gate leakage current	V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 5 A; T _j = 175 °C; Fig. 11; Fig. 12	-	73.4	91	mΩ
		V _{GS} = 10 V; I _D = 5 A; T _j = 25 °C; <u>Fig. 11</u>	-	25.6	31	mΩ
R _{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ °C}; Fig. 11$	-	26.6	33	mΩ
Dynamic ch	naracteristics FET1 and FE	T2			1	
Q _{G(tot)}	total gate charge	I _D = 5 A; V _{DS} = 80 V; V _{GS} = 5 V;	-	27.3	-	nC
Q _{GS}	gate-source charge	T _j = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>	-	4.7	-	nC

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Q_{GD}	gate-drain charge		-	11	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz;	-	2377	3168	pF
C _{oss}	output capacitance	T _j = 25 °C; <u>Fig. 15</u>	-	153	184	pF
C _{rss}	reverse transfer capacitance		-	101	139	pF
t _{d(on)}	turn-on delay time	V_{DS} = 80 V; R_{L} = 15 Ω ; V_{GS} = 5 V; $R_{G(ext)}$ = 5 Ω ; I_{D} = 5 A; T_{j} = 25 °C	-	12.6	-	ns
t _r	rise time		-	22	-	ns
t _{d(off)}	turn-off delay time		-	39.5	-	ns
t _f	fall time		-	23.1	-	ns
Source-dra	in diode FET1 and FET2		, , , , , , , , , , , , , , , , , , ,			
V_{SD}	source-drain voltage	I _S = 5 A; V _{GS} = 0 V; T _j = 25 °C; <u>Fig. 16</u>	-	0.78	1.2	V
t _{rr}	reverse recovery time	$I_S = 10 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$	-	35.6	-	ns
Q _r	recovered charge	V _{DS} = 50 V; T _j = 25 °C	-	47.3	-	nC

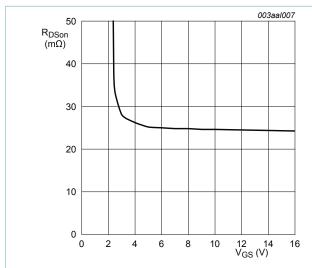


Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25$$
°C; $I_D = 5A$

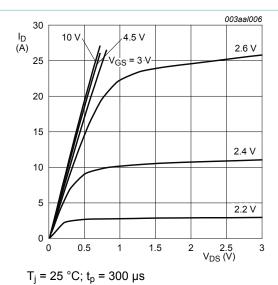


Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values

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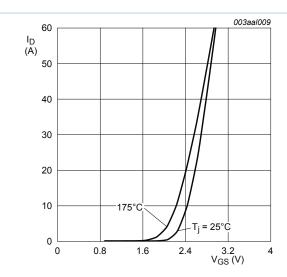


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values



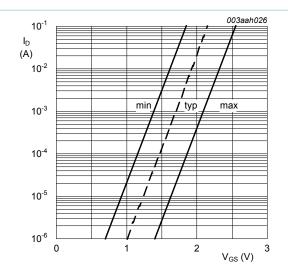


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25$$
°C; $V_{DS} = 5V$

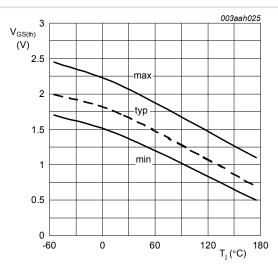
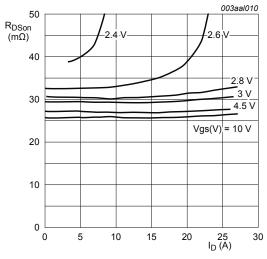


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; \ V_{DS} = V_{GS}$$



 $T_i = 25 \,^{\circ}\text{C}; t_p = 300 \,\mu\text{s}$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

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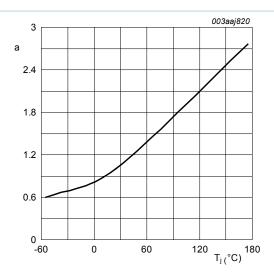


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon (25^{\circ}C)}}$$

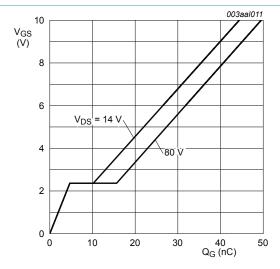


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25$$
°C; $I_D = 5A$

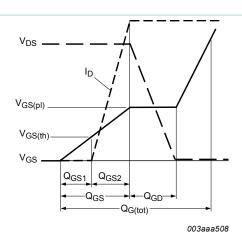


Fig. 13. Gate charge waveform definitions

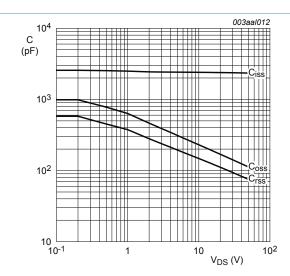


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = \mathbf{0}V; f = \mathbf{1}MHz$$

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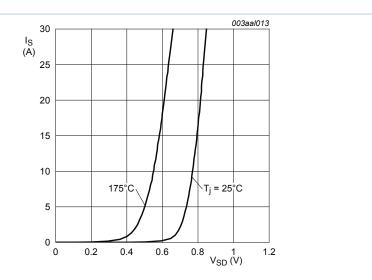


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

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11. Package outline

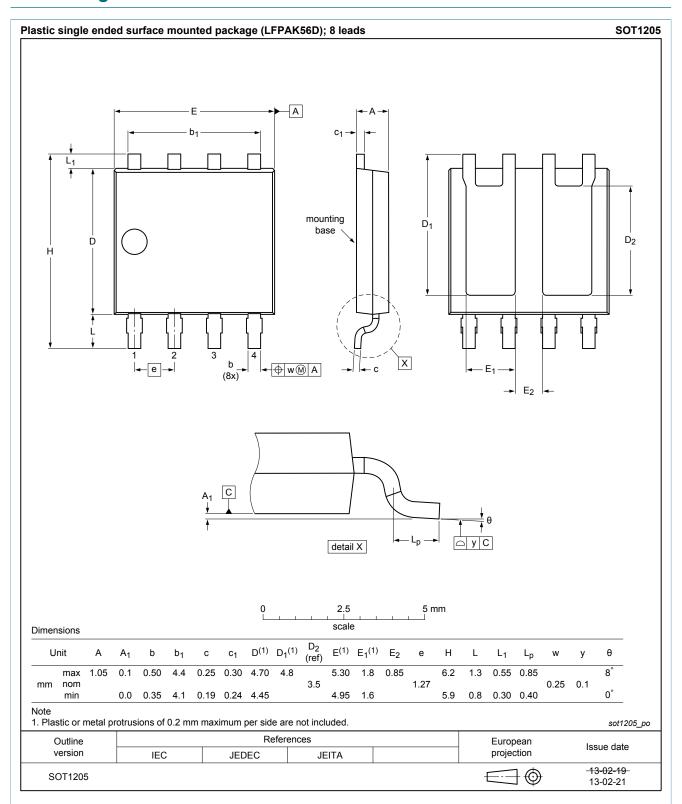


Fig. 17. Package outline LFPAK56D (SOT1205)

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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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