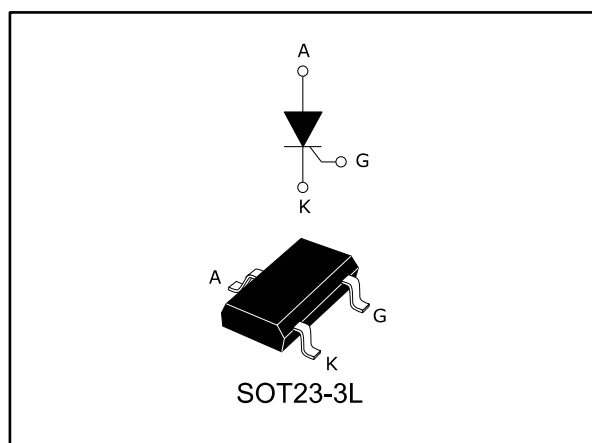


## Sensitive high immunity 0.25 A SCR Thyristor

Datasheet - production data



### Description

Thanks to highly sensitive triggering levels, the 0.25 A P0109AL SCR Thyristor is suitable for all applications where available gate current is limited. Its high immunity makes it ideal for high electric noise circuits.

The surface mount SOT23-3L package allows compact SMD based designs for automated manufacturing.

**Table 1: Device summary**

Symbol	Value	Unit
$I_{T(RMS)}$	0.25	A
$V_{DRM}/V_{RRM}$	100	V
$I_{GT}$	1	$\mu A$
$T_j \text{ max.}$	125	$^{\circ}C$

### Features

- $I_{T(RMS)}$  0.25 A
- Low 1  $\mu A$  gate current
- High noise immunity 100 V/ $\mu s$
- ECOPACK<sup>®</sup>2 compliant component

### Applications

- Standby mode power supplies
- Smoke detectors
- DC 24/48 V proximity sensors
- Gate driver for large Thyristors
- Overvoltage crowbar protection
- Capacitive ignition circuit

# 1 Characteristics

**Table 2: Absolute maximum ratings (limiting values), T<sub>j</sub> = 25 °C unless otherwise specified**

Symbol	Parameter		Value	Unit	
I <sub>T(RMS)</sub>	RMS on-state current (180 ° conduction angle)		0.25	A	
I <sub>T(AV)</sub>	Average on-state current (180 ° conduction angle)				
I <sub>TSM</sub>	Non repetitive surge peak on-state current (T <sub>j</sub> initial = 25 °C)		t <sub>p</sub> = 8.3 ms	7	
			t <sub>p</sub> = 10 ms	6	
I <sup>2</sup> t	I <sup>2</sup> t value for fusing		t <sub>p</sub> = 10 ms	0.18	A <sup>2</sup> s
di/dt	Critical rate of rise of on-state current I <sub>G</sub> = 2 x I <sub>GT</sub> , t <sub>r</sub> ≤ 100 ns	f = 60 Hz	T <sub>j</sub> = 125 °C	50	A/μs
V <sub>DRM</sub> /V <sub>RRM</sub>	Repetitive peak off-state voltage		T <sub>j</sub> = 125 °C	100	V
I <sub>GM</sub>	Peak gate current	t <sub>p</sub> = 20 μs	T <sub>j</sub> = 125 °C	0.5	A
P <sub>G(AV)</sub>	Average gate power dissipation		T <sub>j</sub> = 125 °C	0.02	W
T <sub>stg</sub>	Storage junction temperature range			-40 to +150	°C
T <sub>j</sub>	Operating junction temperature			-40 to +125	°C

**Table 3: Electrical characteristics (T<sub>j</sub> = 25 °C unless otherwise specified)**

Symbol	Test conditions		Value	Unit	
I <sub>GT</sub>	V <sub>D</sub> = 12 V, R <sub>L</sub> = 140 Ω		Max.	1	μA
V <sub>GT</sub>			Max.	0.8	V
V <sub>GD</sub>	V <sub>D</sub> = V <sub>DRM</sub> , R <sub>L</sub> = 3.3 kΩ, R <sub>GK</sub> = 1000 Ω	T <sub>j</sub> = 125 °C	Min.	0.1	V
V <sub>RG</sub>	I <sub>RG</sub> = 10 μA		Min.	8	V
I <sub>H</sub>	I <sub>T</sub> = 50 mA, R <sub>GK</sub> = 1000 Ω		Max.	6	mA
I <sub>L</sub>	I <sub>G</sub> = 1.2 x I <sub>GT</sub> , R <sub>GK</sub> = 1000 Ω		Max.	7	mA
dV/dt	V <sub>D</sub> = 67 % V <sub>DRM</sub> , R <sub>GK</sub> = 1000 Ω	T <sub>j</sub> = 125 °C	Min.	100	V/μs

**Table 4: Static characteristics**

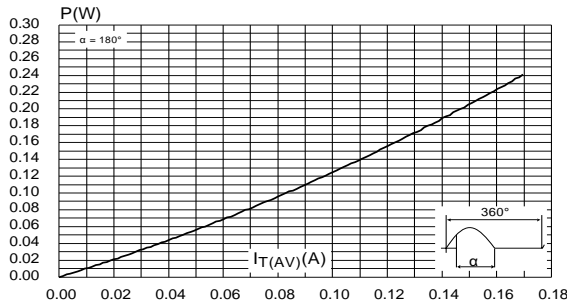
Symbol	Test conditions		Value	Unit		
V <sub>TM</sub>	I <sub>TM</sub> = 0.4 A, t <sub>p</sub> = 380 μs	T <sub>j</sub> = 25 °C	Max.	1.7	V	
V <sub>TO</sub>	Threshold voltage		Max.	1		
R <sub>D</sub>	Dynamic resistance		T <sub>j</sub> = 125 °C	Max.	1000	mΩ
I <sub>DRM</sub> /I <sub>RRM</sub>	V <sub>D</sub> = V <sub>DRM</sub> ; V <sub>R</sub> = V <sub>RRM</sub> , R <sub>GK</sub> = 1000 Ω		T <sub>j</sub> = 25 °C	Max.	1	μA
			T <sub>j</sub> = 125 °C		100	

**Table 5: Thermal parameters**

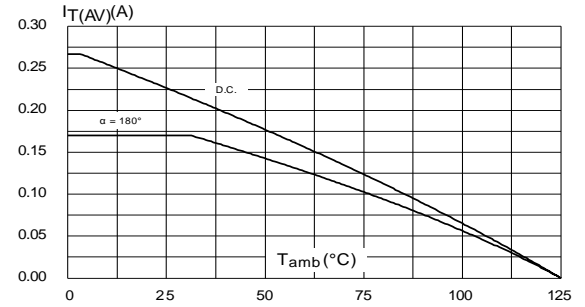
Symbol	Parameter	Value	Unit
R <sub>th(j-a)</sub>	Junction to ambient (Mounted on FR4 with recommended pad layout)	400	°C/W

# 1.1 Characteristics (curves)

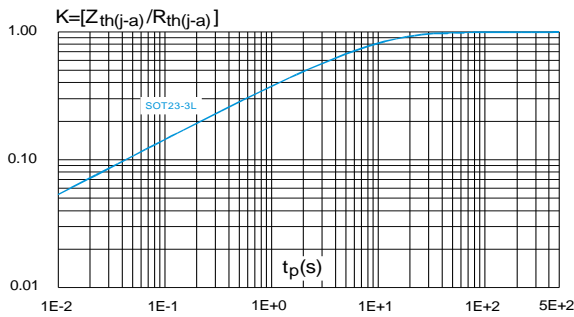
**Figure 1: Maximum average power dissipation versus average on-state current**



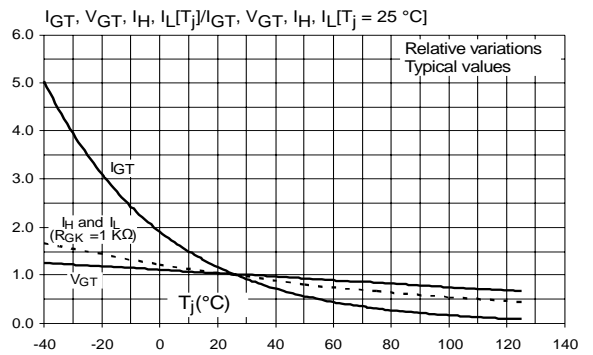
**Figure 2: Average and DC on-state current versus ambient temperature**



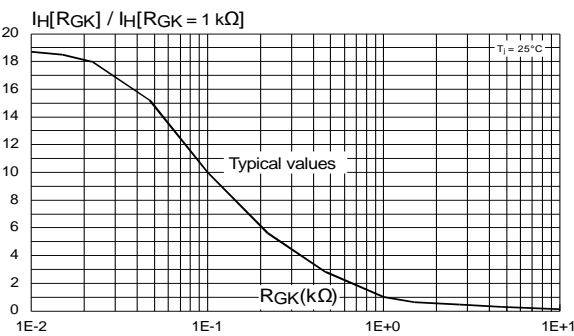
**Figure 3: Relative variation of thermal impedance junction to ambient versus pulse duration**



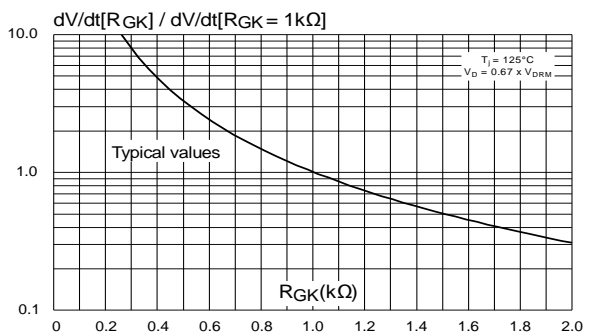
**Figure 4: Gate trigger, holding, and latching currents with gate trigger voltage versus junction temperature**



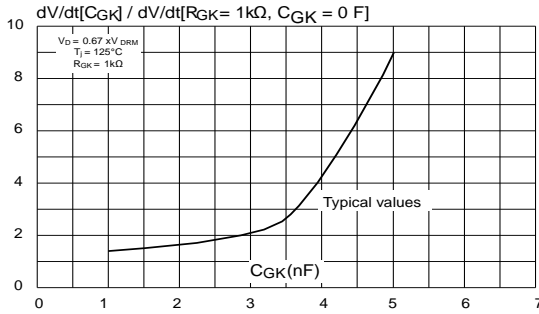
**Figure 5: Relative variation of holding current versus gate-cathode resistance**



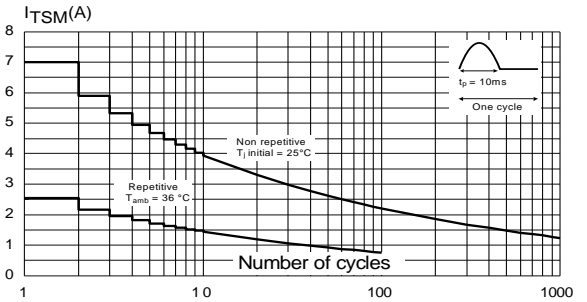
**Figure 6: Relative variation of dV/dt immunity versus gate-cathode resistance**



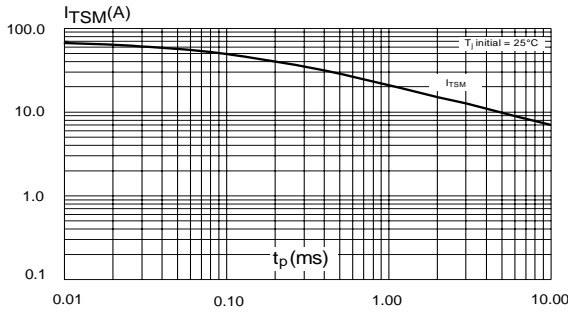
**Figure 7: Relative variation of dV/dt immunity versus gate-cathode capacitance**



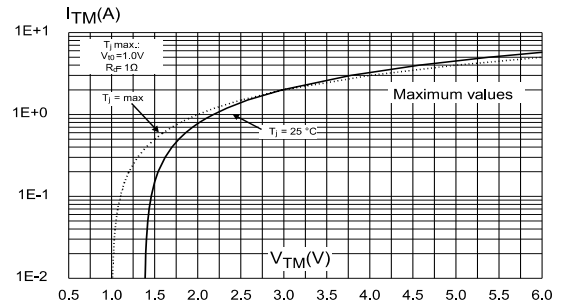
**Figure 8: Surge peak on-state current versus number of cycles**



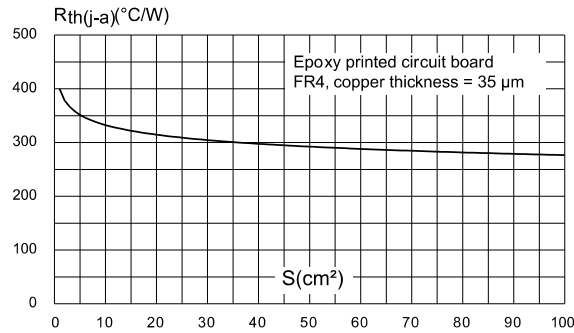
**Figure 9: Non-repetitive surge peak on-state current for sinusoidal pulse ( $t_p < 10 \text{ ms}$ )**



**Figure 10: On-state characteristics**



**Figure 11: Thermal resistance junction to ambient versus copper surface under tab**



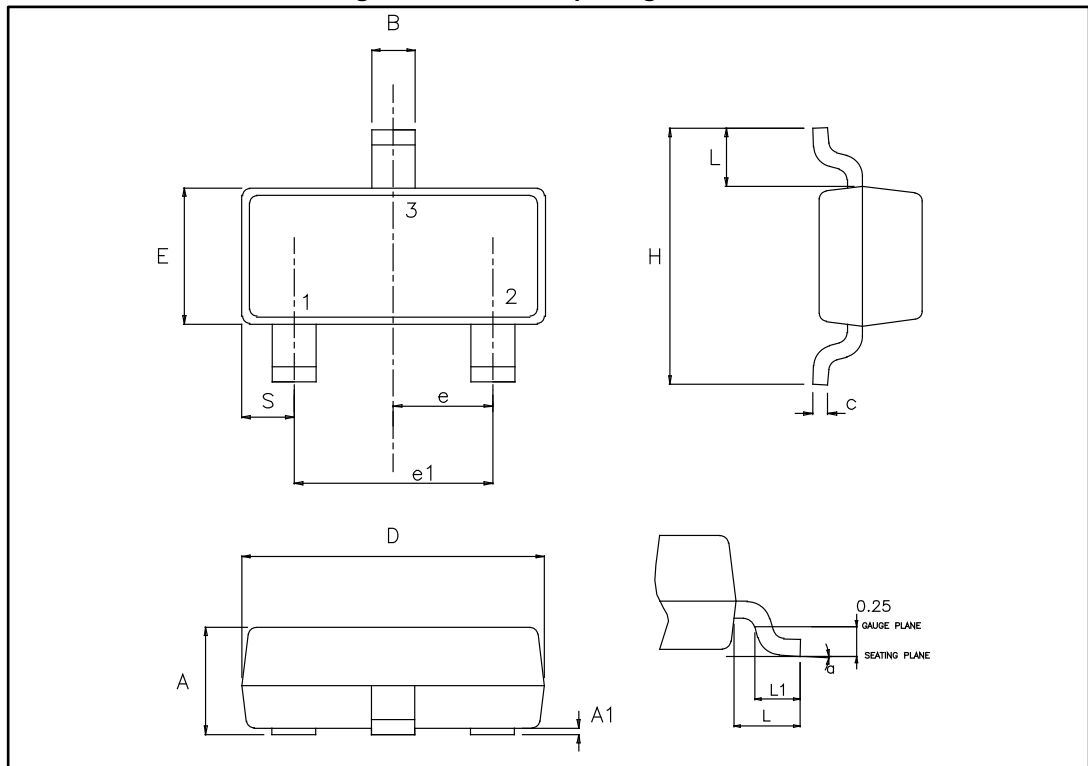
## 2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

- Lead-free package
- Halogen free molding resin
- Epoxy meets UL94, V0

### 2.1 SOT23-3L package information

Figure 12: SOT23-3L package outline



This package drawing may slightly differ from the physical package. However, all the specified dimensions in the following table are guaranteed.

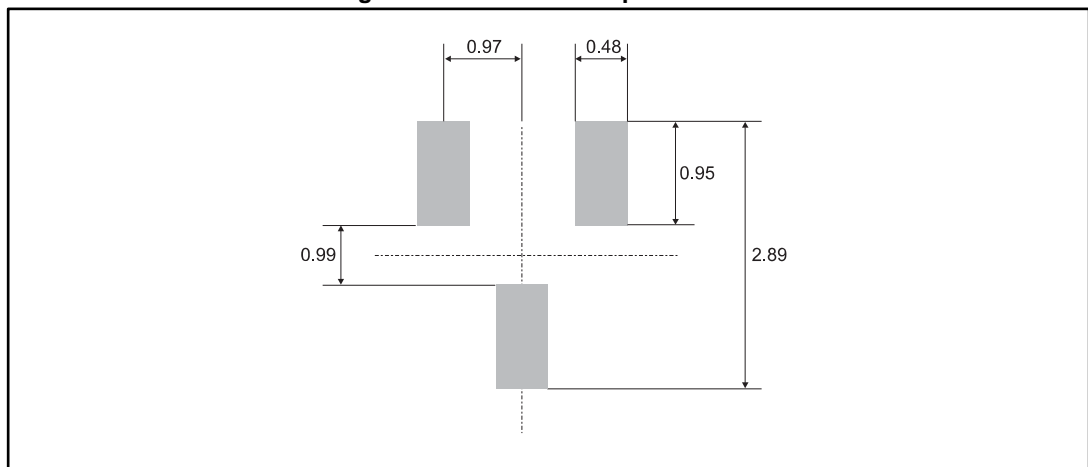
Table 6: SOT23-3L package mechanical data

Ref.	Dimensions					
	Millimeters			Inches <sup>(1)</sup>		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.89		1.40	0.0350		0.0551
A1	0.00		0.10	0.0000		0.0039
B	0.30		0.51	0.0118		0.0201
C	0.085		0.18	0.0033		0.0071
D	2.75		3.04	0.1083		0.1197
e	0.85		1.05	0.0335		0.0413
e1	1.70		2.10	0.0669		0.0827
E	1.20		1.75	0.0472		0.0689
H	2.10		3.00	0.0827		0.1181
L		0.60			0.0236	
S	0.35		0.65	0.0138		0.256
L1	0.25		0.55	0.0098		0.0217
a	0°		8°	0°		8°

**Notes:**

<sup>(1)</sup>Dimension in inches are given for reference only.

Figure 13: SOT23-3L footprint in mm



This drawing may not be in scale; however, all the specified dimensions are guaranteed.

### 3 Ordering information

Figure 14: Ordering information scheme

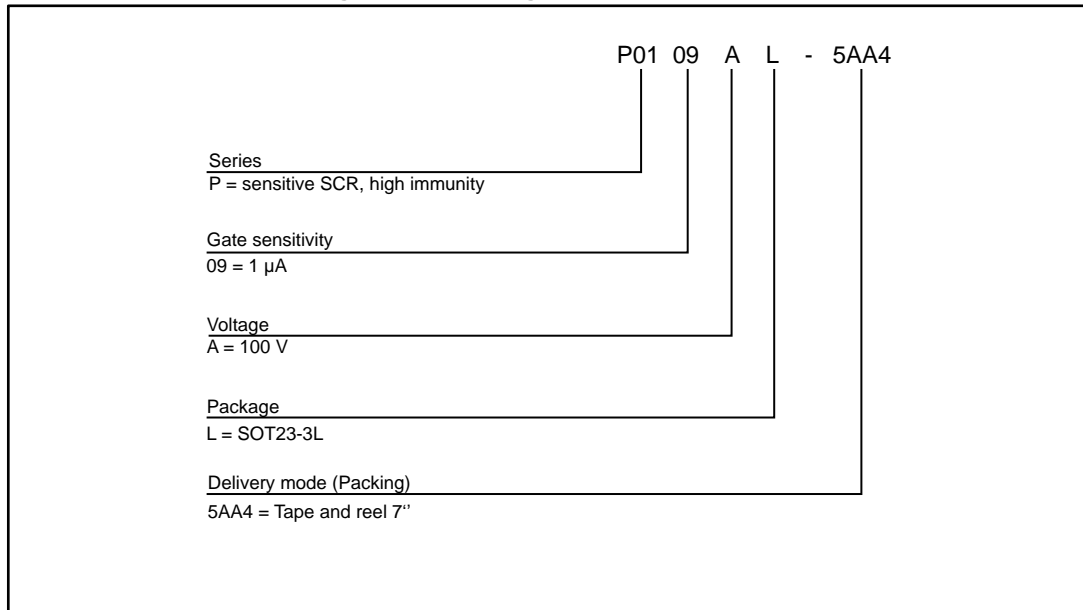


Table 7: Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
P0109AL 5AA4	P9A	SOT23-3L	0.01 g	3000	Tape and reel 7"

### 4 Revision history

Table 8: Document revision history

Date	Revision	Changes
05-Jun-2017	1	Initial release.
09-Aug-2017	2	Updated drawing in cover page.

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