# PIC32MX1XX/2XX/5XX 64/100-PIN

## 32-bit Microcontrollers (up to 512 KB Flash and 64 KB SRAM) with Audio/Graphics/Touch (HMI), CAN, USB, and Advanced Analog

### Operating Conditions

- 2.3V to 3.6V, -40ºC to +105ºC (DC to 40 MHz), -40ºC to +85ºC (DC to 50 MHz)

### Core: 50 MHz/83 DMIPS MIPS32® M4K®

- MIPS16e® mode for up to 40% smaller code size
- Code-efficient (C and Assembly) architecture
- Single-cycle (MAC) 32x16 and two-cycle 32x32 multiply

### Clock Management

- 0.9% internal oscillator
- Programmable PLLs and oscillator clock sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timer
- Fast wake-up and start-up

### Power Management

- Low-power management modes (Sleep and Idle)
- Integrated Power-on Reset, Brown-out Reset, and High Voltage Detect
- 0.5 mA/MHz dynamic current (typical)
- 44 µA $I_{PD}$ current (typical)

### Audio/Graphics/Touch HMI Features

- External graphics interface with up to 34 PMP pins
- Audio data communication: $I^2S$, LJ, RJ, USB
- Audio data control interface: SPI and $I^2C$
- Audio data master clock:
  - Generation of fractional clock frequencies
  - Can be synchronized with USB clock
  - Can be tuned in run-time
- Charge Time Measurement Unit (CTMU):
  - Supports mTouch® capacitive touch sensing
  - Provides high-resolution time measurement (1 ns)

### Advanced Analog Features

- ADC Module:
  - 10-bit 1 Msps rate with one Sample and Hold (S&H)
  - Up to 48 analog inputs
  - Can operate during Sleep mode
- Flexible and independent ADC trigger sources
- On-chip temperature measurement capability
- Comparators:
  - Three dual-input Comparator modules
  - Programmable reference with 32 voltage points

### Timers/Output Compare/Input Capture

- Five General Purpose Timers:
  - Five 16-bit and up to two 32-bit Timers/Counters
- Five Output Compare (OC) modules
- Five Input Capture (IC) modules
- Peripheral Pin Select (PPS) to allow function remap
- Real-Time Clock and Calendar (RTCC) module

### Communication Interfaces

- USB 2.0-compliant Full-speed OTG controller
- Up to five UART modules (12.5 Mbps):
  - LIN 1.2 protocols and IrDA® support
- Four 4-wire SPI modules (25 Mbps)
- Two $I^2C$ modules (up to 1 Mbaud) with SMBus support
- PPS to allow function remap
- Parallel Master Port (PMP) with dual read/write buffers
- Controller Area Network (CAN) 2.0B Compliant with DeviceNet™ addressing support

### Direct Memory Access (DMA)

- Four channels of hardware DMA with automatic data size detection
- 32-bit Programmable Cyclic Redundancy Check (CRC)
- Two additional channels dedicated to USB
- Two additional channels dedicated to CAN

### Input/Output

- 10 mA or 15 mA source/sink for standard $V_{OH}/V_{OL}$ and up to 22 mA for non-standard $V_{OH1}$
- 5V-tolerant pins
- Selectable open drain, pull-ups, and pull-downs
- External interrupts on all I/O pins

### Qualification and Class B Support

- AEC-Q100 REVG (Grade 2 -40ºC to +105ºC)
- Class B Safety Library, IEC 60730

### Debugger Development Support

- In-circuit and in-application programming
- 4-wire MIPS® Enhanced JTAG interface
- Unlimited program and six complex data breakpoints
- IEEE 1149.2-compatible (JTAG) boundary scan

### Packages

| Type | QFN | TQFP | | | TFBGA (see Note 1) |
|---|---|---|---|---|---|
| Pin Count | 64 | 64 | 100 | 100 | 100 |
| I/O Pins (up to) | 53 | 53 | 85 | 85 | 85 |
| Contact/Lead Pitch | 0.50 mm | 0.50 mm | 0.40 mm | 0.50 mm | 0.65 mm |
| Dimensions | 9x9x0.9 mm | 10x10x1 mm | 12x12x1 mm | 14x14x1 mm | 7x7x1.2 mm |

**Note 1:** Please contact your local Microchip Sales Office for information regarding the availability of devices in the 100-pin TFBGA package.

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**TABLE 1: PIC32MX1XX/2XX/5XX 64/100-PIN CONTROLLER FAMILY FEATURES**

| Device | Pins | Packages(4) | Program Memory (KB)(1) | Data Memory (KB) | Remappable Peripherals | | | | | 10-bit 1 Msps ADC (Channels) | Analog Comparators | USB On-The-Go (OTG) | CAN | CTMU | $I^2C$ | PMP | RTCC | DMA Channels (Programmable/Dedicated) | I/O Pins | JTAG |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Remappable Pins | Timers/Capture/Compare(2) | UART | SPI/$I^2S$ | External Interrupts(3) | | | | | | | | | | | |
| PIC32MX120F064H | 64 | QFN, TQFP | 64+3 | 8 | 37 | 5/5/5 | 4 | 3 | 5 | 28 | 3 | N | 0 | Y | 2 | Y | Y | 4/0 | 53 | Y |
| PIC32MX130F128H | 64 | QFN, TQFP | 128+3 | 16 | 37 | 5/5/5 | 4 | 3 | 5 | 28 | 3 | N | 0 | Y | 2 | Y | Y | 4/0 | 53 | Y |
| PIC32MX130F128L | 100 | TQFP | 128+3 | 16 | 54 | 5/5/5 | 5 | 4 | 5 | 48 | 3 | N | 0 | Y | 2 | Y | Y | 4/0 | 85 | Y |
| | 100 | TFBGA | | | | | | | | | | | | | | | | | | |
| PIC32MX230F128H | 64 | QFN, TQFP | 128+3 | 16 | 37 | 5/5/5 | 4 | 3 | 5 | 28 | 3 | Y | 0 | Y | 2 | Y | Y | 4/2 | 49 | Y |
| PIC32MX230F128L | 100 | TQFP | 128+3 | 16 | 54 | 5/5/5 | 5 | 4 | 5 | 48 | 3 | Y | 0 | Y | 2 | Y | Y | 4/2 | 81 | Y |
| | 100 | TFBGA | | | | | | | | | | | | | | | | | | |
| PIC32MX530F128H | 64 | QFN, TQFP | 128+3 | 16 | 37 | 5/5/5 | 4 | 3 | 5 | 28 | 3 | Y | 1 | Y | 2 | Y | Y | 4/4 | 49 | Y |
| PIC32MX530F128L | 100 | TQFP | 128+3 | 16 | 54 | 5/5/5 | 5 | 4 | 5 | 48 | 3 | Y | 1 | Y | 2 | Y | Y | 4/4 | 81 | Y |
| | 100 | TFBGA | | | | | | | | | | | | | | | | | | |
| PIC32MX150F256H | 64 | QFN, TQFP | 256+3 | 32 | 37 | 5/5/5 | 4 | 3 | 5 | 28 | 3 | N | 0 | Y | 2 | Y | Y | 4/0 | 53 | Y |
| PIC32MX150F256L | 100 | TQFP | 256+3 | 32 | 54 | 5/5/5 | 5 | 4 | 5 | 48 | 3 | N | 0 | Y | 2 | Y | Y | 4/0 | 85 | Y |
| | 100 | TFBGA | | | | | | | | | | | | | | | | | | |
| PIC32MX250F256H | 64 | QFN, TQFP | 256+3 | 32 | 37 | 5/5/5 | 4 | 3 | 5 | 28 | 3 | Y | 0 | Y | 2 | Y | Y | 4/2 | 49 | Y |
| PIC32MX250F256L | 100 | TQFP | 256+3 | 32 | 54 | 5/5/5 | 5 | 4 | 5 | 48 | 3 | Y | 0 | Y | 2 | Y | Y | 4/2 | 81 | Y |
| | 100 | TFBGA | | | | | | | | | | | | | | | | | | |
| PIC32MX550F256H | 64 | QFN, TQFP | 256+3 | 32 | 37 | 5/5/5 | 4 | 3 | 5 | 28 | 3 | Y | 1 | Y | 2 | Y | Y | 4/4 | 49 | Y |
| PIC32MX550F256L | 100 | TQFP | 256+3 | 32 | 54 | 5/5/5 | 5 | 4 | 5 | 48 | 3 | Y | 1 | Y | 2 | Y | Y | 4/4 | 81 | Y |
| | 100 | TFBGA | | | | | | | | | | | | | | | | | | |
| PIC32MX170F512H | 64 | QFN, TQFP | 512+3 | 64 | 37 | 5/5/5 | 4 | 3 | 5 | 28 | 3 | N | 0 | Y | 2 | Y | Y | 4/0 | 53 | Y |
| PIC32MX170F512L | 100 | TQFP | 512+3 | 64 | 54 | 5/5/5 | 5 | 4 | 5 | 48 | 3 | N | 0 | Y | 2 | Y | Y | 4/0 | 85 | Y |
| | 100 | TFBGA | | | | | | | | | | | | | | | | | | |
| PIC32MX270F512H | 64 | QFN, TQFP | 512+3 | 64 | 37 | 5/5/5 | 4 | 3 | 5 | 28 | 3 | Y | 0 | Y | 2 | Y | Y | 4/2 | 49 | Y |
| PIC32MX270F512L | 100 | TQFP | 512+3 | 64 | 54 | 5/5/5 | 5 | 4 | 5 | 48 | 3 | Y | 0 | Y | 2 | Y | Y | 4/2 | 81 | Y |
| | 100 | TFBGA | | | | | | | | | | | | | | | | | | |
| PIC32MX570F512H | 64 | QFN, TQFP | 512+3 | 64 | 37 | 5/5/5 | 4 | 3 | 5 | 28 | 3 | Y | 1 | Y | 2 | Y | Y | 4/4 | 49 | Y |
| PIC32MX570F512L | 100 | TQFP | 512+3 | 64 | 54 | 5/5/5 | 5 | 4 | 5 | 48 | 3 | Y | 1 | Y | 2 | Y | Y | 4/4 | 81 | Y |
| | 100 | TFBGA | | | | | | | | | | | | | | | | | | |

**Note 1:** All devices feature 3 KB of Boot Flash memory.
**2:** Four out of five timers are remappable.
**3:** Four out of five external interrupts are remappable.
**4:** Please contact your local Microchip Sales Office for information regarding the availability of devices in the 100-pin TFBGA package.


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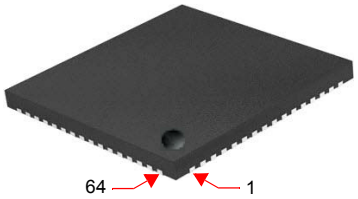
## Device Pin Tables

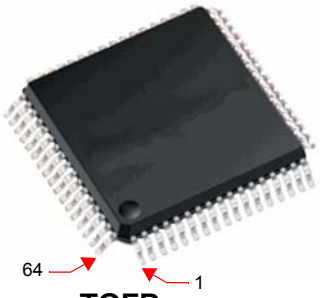
### TABLE 2: PIN NAMES FOR 64-PIN GENERAL PURPOSE DEVICES

**64-PIN QFN(4) AND TQFP (TOP VIEW)**

**PIC32MX120F064H**
**PIC32MX130F128H**
**PIC32MX150F256H**
**PIC32MX170F512H**




QFN(4)




TQFP

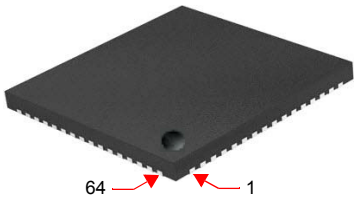
| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | AN22/RPE5/PMD5/RE5 | 33 | RPF3/RF3 |
| 2 | AN23/PMD6/RE6 | 34 | RPF2/RF2 |
| 3 | AN27/PMD7/RE7 | 35 | RPF6/SCK1/INT0/RF6 |
| 4 | AN16/C1IND/RPG6/SCK2/PMA5/RG6 | 36 | SDA1/RG3 |
| 5 | AN17/C1INC/RPG7/PMA4/RG7 | 37 | SCL1/RG2 |
| 6 | AN18/C2IND/RPG8/PMA3/RG8 | 38 | VDD |
| 7 | $\overline{\text{MCLR}}$ | 39 | OSC1/CLKI/RC12 |
| 8 | AN19/C2INC/RPG9/PMA2/RG9 | 40 | OSC2/CLKO/RC15 |
| 9 | VSS | 41 | VSS |
| 10 | VDD | 42 | RPD8/RTCC/RD8 |
| 11 | AN5/C1INA/RPB5/RB5 | 43 | RPD9/RD9 |
| 12 | AN4/C1INB/RB4 | 44 | RPD10/PMA15/RD10 |
| 13 | PGED3/AN3/C2INA/RPB3/RB3 | 45 | RPD11/PMA14/RD11 |
| 14 | PGEC3/AN2/CTCMP/C2INB/RPB2/CTED13/RB2 | 46 | RPD0/RD0 |
| 15 | PGEC1/VREF-/AN1/RPB1/CTED12/RB1 | 47 | SOSCI/RPC13/RC13 |
| 16 | PGED1/VREF+/AN0/RPB0/PMA6/RB0 | 48 | SOSCO/RPC14/T1CK/RC14 |
| 17 | PGEC2/AN6/RPB6/RB6 | 49 | AN24/RPD1/RD1 |
| 18 | PGED2/AN7/RPB7/CTED3/RB7 | 50 | AN25/RPD2/RD2 |
| 19 | AVDD | 51 | AN26/C3IND/RPD3/RD3 |
| 20 | AVSS | 52 | RPD4/PMWR/RD4 |
| 21 | AN8/RPB8/CTED10/RB8 | 53 | RPD5/PMRD/RD5 |
| 22 | AN9/RPB9/CTED4/PMA7/RB9 | 54 | C3INC/RD6 |
| 23 | TMS/CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10 | 55 | C3INB/RD7 |
| 24 | TDO/AN11/PMA12/RB11 | 56 | VCAP |
| 25 | VSS | 57 | VDD |
| 26 | VDD | 58 | C3INA/RPF0/RF0 |
| 27 | TCK/AN12/PMA11/RB12 | 59 | RPF1/RF1 |
| 28 | TDI/AN13/PMA10/RB13 | 60 | PMD0/RE0 |
| 29 | AN14/RPB14/SCK3/CTED5/PMA1/RB14 | 61 | PMD1/RE1 |
| 30 | AN15/RPB15/OCFB/CTED6/PMA0/RB15 | 62 | AN20/PMD2/RE2 |
| 31 | RPF4/SDA2/PMA9/RF4 | 63 | RPE3/CTPLS/PMD3/RE3 |
| 32 | RPF5/SCL2/PMA8/RF5 | 64 | AN21/PMD4/RE4 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.
**2:** Every I/O port pin (RBx-RGx) can be used as a change notification pin (CNBx-CNGx). See **Section 11.0 "I/O Ports"** for more information.
**3:** Shaded pins are 5V tolerant.
**4:** The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

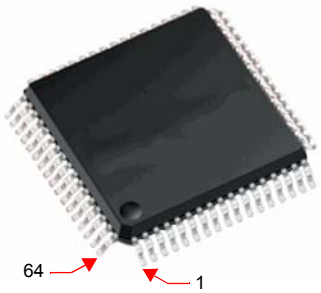
**TABLE 3: PIN NAMES FOR 64-PIN USB DEVICES**

**64-PIN QFN(4) AND TQFP (TOP VIEW)**

**PIC32MX230F128H**
**PIC32MX530F128H**
**PIC32MX250F256H**
**PIC32MX550F256H**
**PIC32MX270F512H**
**PIC32MX570F512H**




**QFN(4)**




**TQFP**

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | AN22/RPE5/PMD5/RE5 | 33 | USBID/RPF3/RF3 |
| 2 | AN23/PMD6/RE6 | 34 | VBUS |
| 3 | AN27/PMD7/RE7 | 35 | VUSB3V3 |
| 4 | AN16/C1IND/RPG6/SCK2/PMA5/RG6 | 36 | D- |
| 5 | AN17/C1INC/RPG7/PMA4/RG7 | 37 | D+ |
| 6 | AN18/C2IND/RPG8/PMA3/RG8 | 38 | VDD |
| 7 | $\overline{\text{MCLR}}$ | 39 | OSC1/CLKI/RC12 |
| 8 | AN19/C2INC/RPG9/PMA2/RG9 | 40 | OSC2/CLKO/RC15 |
| 9 | VSS | 41 | VSS |
| 10 | VDD | 42 | RPD8/RTCC/RD8 |
| 11 | AN5/C1INA/RPB5/VBUSON/RB5 | 43 | RPD9/SDA1/RD9 |
| 12 | AN4/C1INB/RB4 | 44 | RPD10/SCL1/PMA15/RD10 |
| 13 | PGED3/AN3/C2INA/RPB3/RB3 | 45 | RPD11/PMA14/RD11 |
| 14 | PGEC3/AN2/CTCMP/C2INB/RPB2/CTED13/RB2 | 46 | RPD0/INT0/RD0 |
| 15 | PGEC1/VREF-/AN1/RPB1/CTED12/RB1 | 47 | SOSCI/RPC13/RC13 |
| 16 | PGED1/VREF+/AN0/RPB0/PMA6/RB0 | 48 | SOSCO/RPC14/T1CK/RC14 |
| 17 | PGEC2/AN6/RPB6/RB6 | 49 | AN24/RPD1/RD1 |
| 18 | PGED2/AN7/RPB7/CTED3/RB7 | 50 | AN25/RPD2/SCK1/RD2 |
| 19 | AVDD | 51 | AN26/C3IND/RPD3/RD3 |
| 20 | AVSS | 52 | RPD4/PMWR/RD4 |
| 21 | AN8/RPB8/CTED10/RB8 | 53 | RPD5/PMRD/RD5 |
| 22 | AN9/RPB9/CTED4/PMA7/RB9 | 54 | C3INC/RD6 |
| 23 | TMS/CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10 | 55 | C3INB/RD7 |
| 24 | TDO/AN11/PMA12/RB11 | 56 | VCAP |
| 25 | VSS | 57 | VDD |
| 26 | VDD | 58 | C3INA/RPF0/RF0 |
| 27 | TCK/AN12/PMA11/RB12 | 59 | RPF1/RF1 |
| 28 | TDI/AN13/PMA10/RB13 | 60 | PMD0/RE0 |
| 29 | AN14/RPB14/SCK3/CTED5/PMA1/RB14 | 61 | PMD1/RE1 |
| 30 | AN15/RPB15/OCFB/CTED6/PMA0/RB15 | 62 | AN20/PMD2/RE2 |
| 31 | RPF4/SDA2/PMA9/RF4 | 63 | RPE3/CTPLS/PMD3/RE3 |
| 32 | RPF5/SCL2/PMA8/RF5 | 64 | AN21/PMD4/RE4 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.
**2:** Every I/O port pin (RBx-RGx) can be used as a change notification pin (CNBx-CNGx). See **Section 11.0 "I/O Ports"** for more information.
**3:** Shaded pins are 5V tolerant.
**4:** The metal plane at the bottom of the QFN device is not connected to any pins and is recommended to be connected to VSS externally.


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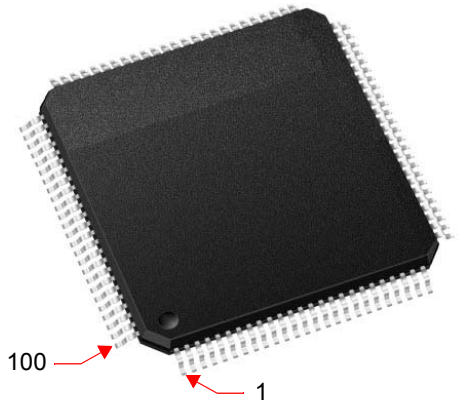
**TABLE 4: PIN NAMES FOR 100-PIN GENERAL PURPOSE DEVICES**

**100-PIN TQFP (TOP VIEW)**

**PIC32MX130F128L**
**PIC32MX150F256L**
**PIC32MX170F512L**




| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | AN28/RG15 | 36 | VSS |
| 2 | VDD | 37 | VDD |
| 3 | AN22/RPE5/PMD5/RE5 | 38 | TCK/CTED2/RA1 |
| 4 | AN23/PMD6/RE6 | 39 | AN34/RPF13/SCK3/RF13 |
| 5 | AN27/PMD7/RE7 | 40 | AN35/RPF12/RF12 |
| 6 | AN29/RPC1/RC1 | 41 | AN12/PMA11/RB12 |
| 7 | AN30/RPC2/RC2 | 42 | AN13/PMA10/RB13 |
| 8 | AN31/RPC3/RC3 | 43 | AN14/RPB14/CTED5/PMA1/RB14 |
| 9 | RPC4/CTED7/RC4 | 44 | AN15/RPB15/OCFB/CTED6/PMA0/RB15 |
| 10 | AN16/C1IND/RPG6/SCK2/PMA5/RG6 | 45 | VSS |
| 11 | AN17/C1INC/RPG7/PMA4/RG7 | 46 | VDD |
| 12 | AN18/C2IND/RPG8/PMA3/RG8 | 47 | AN36/RPD14/RD14 |
| 13 | $\overline{\text{MCLR}}$ | 48 | AN37/RPD15/SCK4/RD15 |
| 14 | AN19/C2INC/RPG9/PMA2/RG9 | 49 | RPF4/PMA9/RF4 |
| 15 | VSS | 50 | RPF5/PMA8/RF5 |
| 16 | VDD | 51 | RPF3/RF3 |
| 17 | TMS/CTED1/RA0 | 52 | AN38/RPF2/RF2 |
| 18 | AN32/RPE8/RE8 | 53 | AN39/RPF8/RF8 |
| 19 | AN33/RPE9/RE9 | 54 | RPF7/RF7 |
| 20 | AN5/C1INA/RPB5/RB5 | 55 | RPF6/SCK1/INT0/RF6 |
| 21 | AN4/C1INB/RB4 | 56 | SDA1/RG3 |
| 22 | PGED3/AN3/C2INA/RPB3/RB3 | 57 | SCL1/RG2 |
| 23 | PGEC3/AN2/CTCMP/C2INB/RPB2/CTED13/RB2 | 58 | SCL2/RA2 |
| 24 | PGEC1/AN1/RPB1/CTED12/RB1 | 59 | SDA2/RA3 |
| 25 | PGED1/AN0/RPB0/RB0 | 60 | TDI/CTED9/RA4 |
| 26 | PGEC2/AN6/RPB6/RB6 | 61 | TDO/RA5 |
| 27 | PGED2/AN7/RPB7/CTED3/RB7 | 62 | VDD |
| 28 | VREF-/PMA7/RA9 | 63 | OSC1/CLKI/RC12 |
| 29 | VREF+/PMA6/RA10 | 64 | OSC2/CLKO/RC15 |
| 30 | AVDD | 65 | VSS |
| 31 | AVSS | 66 | RPA14/RA14 |
| 32 | AN8/RPB8/CTED10/RB8 | 67 | RPA15/RA15 |
| 33 | AN9/RPB9/CTED4/RB9 | 68 | RPD8/RTCC/RD8 |
| 34 | CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10 | 69 | RPD9/RD9 |
| 35 | AN11/PMA12/RB11 | 70 | RPD10/PMA15/RD10 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

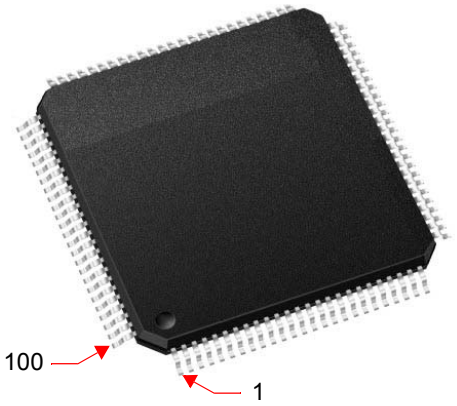
**2:** Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** Shaded pins are 5V tolerant.

**TABLE 4: PIN NAMES FOR 100-PIN GENERAL PURPOSE DEVICES (CONTINUED)**

**100-PIN TQFP (TOP VIEW)**

**PIC32MX130F128L**
**PIC32MX150F256L**
**PIC32MX170F512L**




| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 71 | RPD11/PMA14/RD11 | 86 | VDD |
| 72 | RPD0/RD0 | 87 | AN44/C3INA/RPF0/PMD11/RF0 |
| 73 | SOSCI/RPC13/RC13 | 88 | AN45/RPF1/PMD10/RF1 |
| 74 | SOSCO/RPC14/T1CK/RC14 | 89 | RPG1/PMD9/RG1 |
| 75 | VSS | 90 | RPG0/PMD8/RG0 |
| 76 | AN24/RPD1/RD1 | 91 | RA6 |
| 77 | AN25/RPD2/RD2 | 92 | CTED8/RA7 |
| 78 | AN26/C3IND/RPD3/RD3 | 93 | AN46/PMD0/RE0 |
| 79 | AN40/RPD12/PMD12/RD12 | 94 | AN47/PMD1/RE1 |
| 80 | AN41/PMD13/RD13 | 95 | RG14 |
| 81 | RPD4/PMWR/RD4 | 96 | RG12 |
| 82 | RPD5/PMRD/RD5 | 97 | RG13 |
| 83 | AN42/C3INC/PMD14/RD6 | 98 | AN20/PMD2/RE2 |
| 84 | AN43/C3INB/PMD15/RD7 | 99 | RPE3/CTPLS/PMD3/RE3 |
| 85 | VCAP | 100 | AN21/PMD4/RE4 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

**2:** Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** Shaded pins are 5V tolerant.


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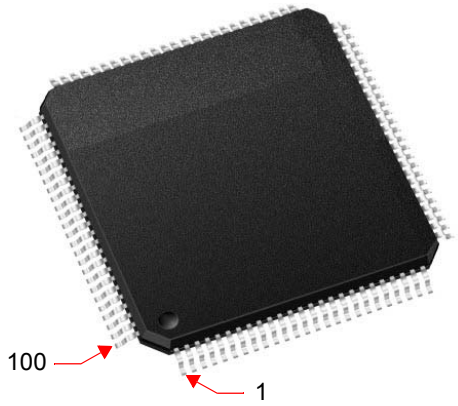
**TABLE 5: PIN NAMES FOR 100-PIN USB DEVICES**

**100-PIN TQFP (TOP VIEW)**

**PIC32MX230F128L**
**PIC32MX530F128L**
**PIC32MX250F256L**
**PIC32MX550F256L**
**PIC32MX270F512L**
**PIC32MX570F512L**




| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | AN28/RG15 | 36 | VSS |
| 2 | VDD | 37 | VDD |
| 3 | AN22/RPE5/PMD5/RE5 | 38 | TCK/CTED2/RA1 |
| 4 | AN23/PMD6/RE6 | 39 | AN34/RPF13/SCK3/RF13 |
| 5 | AN27/PMD7/RE7 | 40 | AN35/RPF12/RF12 |
| 6 | AN29/RPC1/RC1 | 41 | AN12/PMA11/RB12 |
| 7 | AN30/RPC2/RC2 | 42 | AN13/PMA10/RB13 |
| 8 | AN31/RPC3/RC3 | 43 | AN14/RPB14/CTED5/PMA1/RB14 |
| 9 | RPC4/CTED7/RC4 | 44 | AN15/RPB15/OCFB/CTED6/PMA0/RB15 |
| 10 | AN16/C1IND/RPG6/SCK2/PMA5/RG6 | 45 | VSS |
| 11 | AN17/C1INC/RPG7/PMA4/RG7 | 46 | VDD |
| 12 | AN18/C2IND/RPG8/PMA3/RG8 | 47 | AN36/RPD14/RD14 |
| 13 | $\overline{\text{MCLR}}$ | 48 | AN37/RPD15/SCK4/RD15 |
| 14 | AN19/C2INC/RPG9/PMA2/RG9 | 49 | RPF4/PMA9/RF4 |
| 15 | VSS | 50 | RPF5/PMA8/RF5 |
| 16 | VDD | 51 | USBID/RPF3/RF3 |
| 17 | TMS/CTED1/RA0 | 52 | AN38/RPF2/RF2 |
| 18 | AN32/RPE8/RE8 | 53 | AN39/RPF8/RF8 |
| 19 | AN33/RPE9/RE9 | 54 | VBUS |
| 20 | AN5/C1INA/RPB5/VBUSON/RB5 | 55 | VUSB3V3 |
| 21 | AN4/C1INB/RB4 | 56 | D- |
| 22 | PGED3/AN3/C2INA/RPB3/RB3 | 57 | D+ |
| 23 | PGEC3/AN2/CTCMP/C2INB/RPB2/CTED13/RB2 | 58 | SCL2/RA2 |
| 24 | PGEC1/AN1/RPB1/CTED12/RB1 | 59 | SDA2/RA3 |
| 25 | PGED1/AN0/RPB0/RB0 | 60 | TDI/CTED9/RA4 |
| 26 | PGEC2/AN6/RPB6/RB6 | 61 | TDO/RA5 |
| 27 | PGED2/AN7/RPB7/CTED3/RB7 | 62 | VDD |
| 28 | VREF-/PMA7/RA9 | 63 | OSC1/CLKI/RC12 |
| 29 | VREF+/PMA6/RA10 | 64 | OSC2/CLKO/RC15 |
| 30 | AVDD | 65 | VSS |
| 31 | AVSS | 66 | RPA14/SCL1/RA14 |
| 32 | AN8/RPB8/CTED10/RB8 | 67 | RPA15/SDA1/RA15 |
| 33 | AN9/RPB9/CTED4/RB9 | 68 | RPD8/RTCC/RD8 |
| 34 | CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10 | 69 | RPD9/RD9 |
| 35 | AN11/PMA12/RB11 | 70 | RPD10/SCK1/PMA15/RD10 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

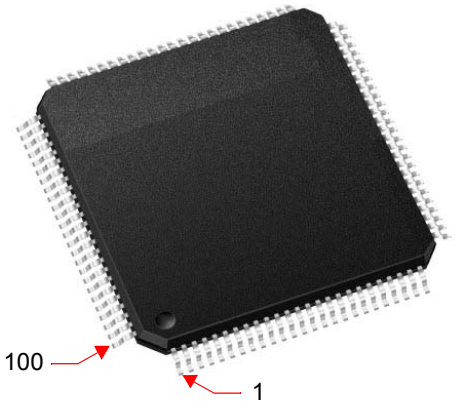
**2:** Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** Shaded pins are 5V tolerant.

**TABLE 5: PIN NAMES FOR 100-PIN USB DEVICES (CONTINUED)**

**100-PIN TQFP (TOP VIEW)**

**PIC32MX230F128L**
**PIC32MX530F128L**
**PIC32MX250F256L**
**PIC32MX550F256L**
**PIC32MX270F512L**
**PIC32MX570F512L**




| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 71 | RPD11/PMA14/RD11 | 86 | VDD |
| 72 | RPD0/INT0/RD0 | 87 | AN44/C3INA/RPF0/PMD11/RF0 |
| 73 | SOSCI/RPC13/RC13 | 88 | AN45/RPF1/PMD10/RF1 |
| 74 | SOSCO/RPC14/T1CK/RC14 | 89 | RPG1/PMD9/RG1 |
| 75 | VSS | 90 | RPG0/PMD8/RG0 |
| 76 | AN24/RPD1/RD1 | 91 | RA6 |
| 77 | AN25/RPD2/RD2 | 92 | CTED8/RA7 |
| 78 | AN26/C3IND/RPD3/RD3 | 93 | AN46/PMD0/RE0 |
| 79 | AN40/RPD12/PMD12/RD12 | 94 | AN47/PMD1/RE1 |
| 80 | AN41/PMD13/RD13 | 95 | RG14 |
| 81 | RPD4/PMWR/RD4 | 96 | RG12 |
| 82 | RPD5/PMRD/RD5 | 97 | RG13 |
| 83 | AN42/C3INC/PMD14/RD6 | 98 | AN20/PMD2/RE2 |
| 84 | AN43/C3INB/PMD15/RD7 | 99 | RPE3/CTPLS/PMD3/RE3 |
| 85 | VCAP | 100 | AN21/PMD4/RE4 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

**2:** Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** Shaded pins are 5V tolerant.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## Referenced Sources

This device data sheet is based on the following individual sections of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

**Note:** To access the documents listed below, browse to the documentation section of the Microchip web site (www.microchip.com).

- **Section 1. "Introduction"** (DS60001127)
- **Section 2. "CPU"** (DS60001113)
- **Section 3. "Memory Organization"** (DS60001115)
- **Section 5. "Flash Program Memory"** (DS60001121)
- **Section 6. "Oscillator Configuration"** (DS60001112)
- **Section 7. "Resets"** (DS60001118)
- **Section 8. "Interrupt Controller"** (DS60001108)
- **Section 9. "Watchdog Timer and Power-up Timer"** (DS60001114)
- **Section 10. "Power-Saving Features"** (DS60001130)
- **Section 12. "I/O Ports"** (DS60001120)
- **Section 13. "Parallel Master Port (PMP)"** (DS60001128)
- **Section 14. "Timers"** (DS60001105)
- **Section 15. "Input Capture"** (DS60001122)
- **Section 16. "Output Compare"** (DS60001111)
- **Section 17. "10-bit Analog-to-Digital Converter (ADC)"** (DS60001104)
- **Section 19. "Comparator"** (DS60001110)
- **Section 20. "Comparator Voltage Reference (CVREF)"** (DS60001109)
- **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS60001107)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106)
- **Section 24. "Inter-Integrated Circuit ($I^2C$)"** (DS60001116)
- **Section 27. "USB On-The-Go (OTG)"** (DS60001126)
- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125)
- **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117)
- **Section 32. "Configuration"** (DS60001124)
- **Section 33. "Programming and Diagnostics"** (DS60001129)
- **Section 34. "Controller Area Network (CAN)"** (DS60001123)
- **Section 37. "Charge Time Measurement Unit (CTMU)"** (DS60001167)

**NOTES:**


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## 1.0 DEVICE OVERVIEW

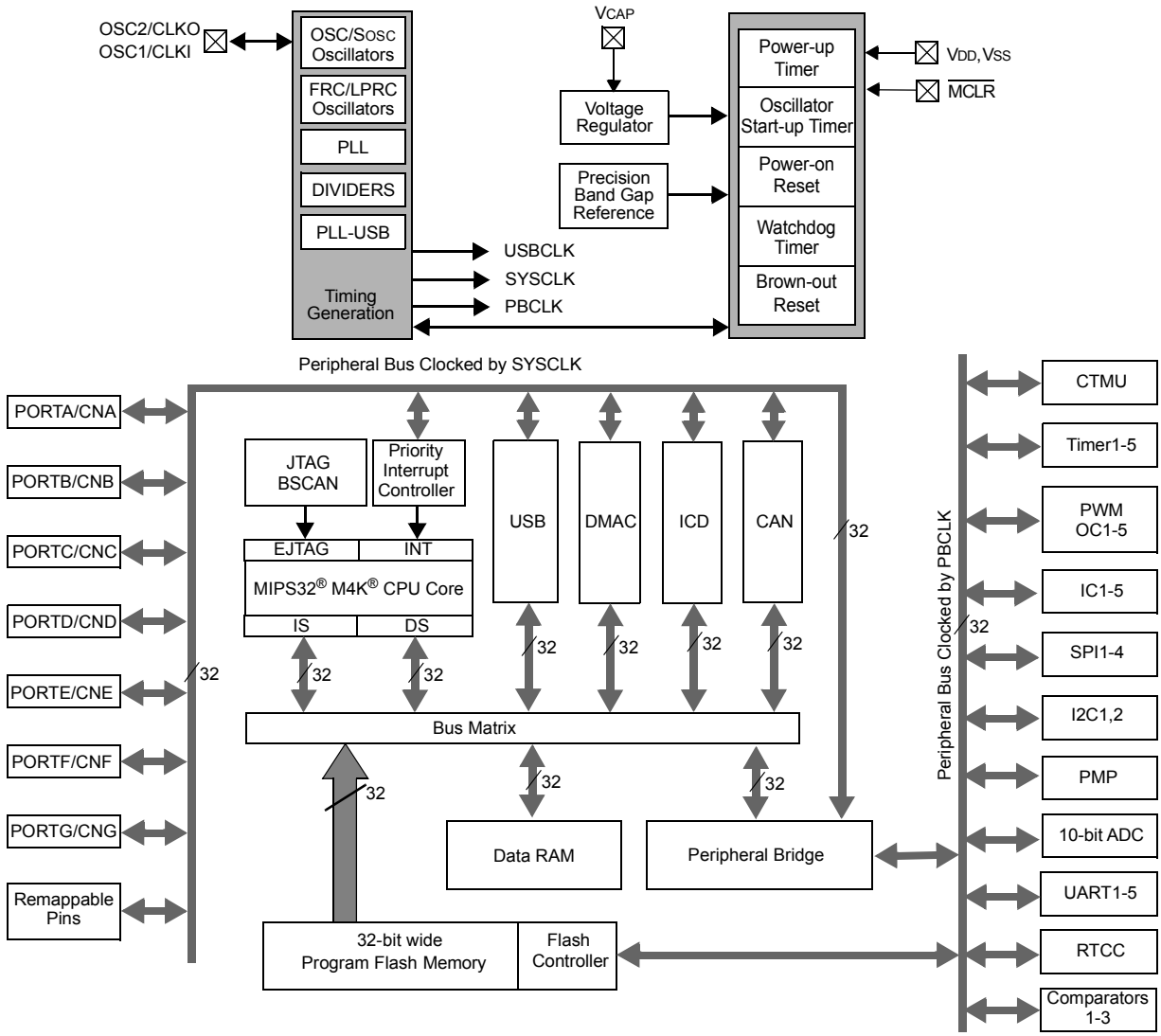
**Note 1:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

This document contains device-specific information for PIC32MX1XX/2XX/5XX 64/100-pin devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX1XX/2XX/5XX 64/100-pin family of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

**FIGURE 1-1: PIC32MX1XX/2XX/5XX 64/100-PIN BLOCK DIAGRAM**




**Note:** Not all features are available on all devices. Refer to **TABLE 1: "PIC32MX1XX/2XX/5XX 64/100-pin Controller Family Features"** for the list of features by device.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | 64-pin QFN/ TQFP | 100-pin TQFP | | | |
| AN0 | 16 | 25 | I | Analog | Analog input channels. |
| AN1 | 15 | 24 | I | Analog | |
| AN2 | 14 | 23 | I | Analog | |
| AN3 | 13 | 22 | I | Analog | |
| AN4 | 12 | 21 | I | Analog | |
| AN5 | 11 | 20 | I | Analog | |
| AN6 | 17 | 26 | I | Analog | |
| AN7 | 18 | 27 | I | Analog | |
| AN8 | 21 | 32 | I | Analog | |
| AN9 | 22 | 33 | I | Analog | |
| AN10 | 23 | 34 | I | Analog | |
| AN11 | 24 | 35 | I | Analog | |
| AN12 | 27 | 41 | I | Analog | |
| AN13 | 28 | 42 | I | Analog | |
| AN14 | 29 | 43 | I | Analog | |
| AN15 | 30 | 44 | I | Analog | |
| AN16 | 4 | 10 | I | Analog | |
| AN17 | 5 | 11 | I | Analog | |
| AN18 | 6 | 12 | I | Analog | |
| AN19 | 8 | 14 | I | Analog | |
| AN20 | 62 | 98 | I | Analog | |
| AN21 | 64 | 100 | I | Analog | |
| AN22 | 1 | 3 | I | Analog | |
| AN23 | 2 | 4 | I | Analog | |
| AN24 | 49 | 76 | I | Analog | |
| AN25 | 50 | 77 | I | Analog | |
| AN26 | 51 | 78 | I | Analog | |
| AN27 | 3 | 5 | I | Analog | |
| AN28 | — | 1 | I | Analog | |
| AN29 | — | 6 | I | Analog | |
| AN30 | — | 7 | I | Analog | |
| AN31 | — | 8 | I | Analog | |
| AN32 | — | 18 | I | Analog | |
| AN33 | — | 19 | I | Analog | |
| AN34 | — | 39 | I | Analog | |
| AN35 | — | 40 | I | Analog | |

**Legend:** CMOS = CMOS compatible input or output Analog = Analog input I = Input O = Output
ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer P = Power

**Note 1:** This pin is only available on devices without a USB module.

**2:** This pin is only available on devices with a USB module.

**3:** This pin is not available on 64-pin devices with a USB module.

**4:** This pin is only available on 100-pin devices without a USB module.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | 64-pin QFN/ TQFP | 100-pin TQFP | | | |
| AN36 | — | 47 | I | Analog | Analog input channels. |
| AN37 | — | 48 | I | Analog | |
| AN38 | — | 52 | I | Analog | |
| AN39 | — | 53 | I | Analog | |
| AN40 | — | 79 | I | Analog | |
| AN41 | — | 80 | I | Analog | |
| AN42 | — | 83 | I | Analog | |
| AN43 | — | 84 | I | Analog | |
| AN44 | — | 87 | I | Analog | |
| AN45 | — | 88 | I | Analog | |
| AN46 | — | 93 | I | Analog | |
| AN47 | — | 94 | I | Analog | |
| CLKI | 39 | 63 | I | ST/CMOS | External clock source input. Always associated with OSC1 pin function. |
| CLKO | 40 | 64 | O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with the OSC2 pin function. |
| OSC1 | 39 | 63 | I | ST/CMOS | Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise. |
| OSC2 | 40 | 64 | O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. |
| SOSCI | 47 | 73 | I | ST/CMOS | 32.768 kHz low-power oscillator crystal input; CMOS otherwise. |
| SOSCO | 48 | 74 | O | — | 32.768 kHz low-power oscillator crystal output. |
| IC1 | PPS | PPS | I | ST | Capture Input 1-5 |
| IC2 | PPS | PPS | I | ST | |
| IC3 | PPS | PPS | I | ST | |
| IC4 | PPS | PPS | I | ST | |
| IC5 | PPS | PPS | I | ST | |
| OC1 | PPS | PPS | O | ST | Output Compare Output 1 |
| OC2 | PPS | PPS | O | ST | Output Compare Output 2 |
| OC3 | PPS | PPS | O | ST | Output Compare Output 3 |
| OC4 | PPS | PPS | O | ST | Output Compare Output 4 |
| OC5 | PPS | PPS | O | ST | Output Compare Output 5 |
| OCFA | PPS | PPS | I | ST | Output Compare Fault A Input |
| OCFB | 30 | 44 | I | ST | Output Compare Fault B Input |

**Legend:** CMOS = CMOS compatible input or output Analog = Analog input I = Input O = Output
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**4:** This pin is only available on 100-pin devices without a USB module.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | 64-pin QFN/ TQFP | 100-pin TQFP | | | |
| INT0 | 35(1), 46(2) | 55(1), 72(2) | I | ST | External Interrupt 0 |
| INT1 | PPS | PPS | I | ST | External Interrupt 1 |
| INT2 | PPS | PPS | I | ST | External Interrupt 2 |
| INT3 | PPS | PPS | I | ST | External Interrupt 3 |
| INT4 | PPS | PPS | I | ST | External Interrupt 4 |
| RA0 | — | 17 | I/O | ST | PORTA is a bidirectional I/O port |
| RA1 | — | 38 | I/O | ST | |
| RA2 | — | 58 | I/O | ST | |
| RA3 | — | 59 | I/O | ST | |
| RA4 | — | 60 | I/O | ST | |
| RA5 | — | 61 | I/O | ST | |
| RA6 | — | 91 | I/O | ST | |
| RA7 | — | 92 | I/O | ST | |
| RA9 | — | 28 | I/O | ST | |
| RA10 | — | 29 | I/O | ST | |
| RA14 | — | 66 | I/O | ST | |
| RA15 | — | 67 | I/O | ST | |
| RB0 | 16 | 25 | I/O | ST | PORTB is a bidirectional I/O port |
| RB1 | 15 | 24 | I/O | ST | |
| RB2 | 14 | 23 | I/O | ST | |
| RB3 | 13 | 22 | I/O | ST | |
| RB4 | 12 | 21 | I/O | ST | |
| RB5 | 11 | 20 | I/O | ST | |
| RB6 | 17 | 26 | I/O | ST | |
| RB7 | 18 | 27 | I/O | ST | |
| RB8 | 21 | 32 | I/O | ST | |
| RB9 | 22 | 33 | I/O | ST | |
| RB10 | 23 | 34 | I/O | ST | |
| RB11 | 24 | 35 | I/O | ST | |
| RB12 | 27 | 41 | I/O | ST | |
| RB13 | 28 | 42 | I/O | ST | |
| RB14 | 29 | 43 | I/O | ST | |
| RB15 | 30 | 44 | I/O | ST | |

**Legend:** CMOS = CMOS compatible input or output Analog = Analog input I = Input O = Output
ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer P = Power

**Note 1:** This pin is only available on devices without a USB module.

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**4:** This pin is only available on 100-pin devices without a USB module.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | 64-pin QFN/ TQFP | 100-pin TQFP | | | |
| RC1 | — | 6 | I/O | ST | PORTC is a bidirectional I/O port |
| RC2 | — | 7 | I/O | ST | |
| RC3 | — | 8 | I/O | ST | |
| RC4 | — | 9 | I/O | ST | |
| RC12 | 39 | 63 | I/O | ST | |
| RC13 | 47 | 73 | I/O | ST | |
| RC14 | 48 | 74 | I/O | ST | |
| RC15 | 40 | 64 | I/O | ST | |
| RD0 | 46 | 72 | I/O | ST | PORTD is a bidirectional I/O port |
| RD1 | 49 | 76 | I/O | ST | |
| RD2 | 50 | 77 | I/O | ST | |
| RD3 | 51 | 78 | I/O | ST | |
| RD4 | 52 | 81 | I/O | ST | |
| RD5 | 53 | 82 | I/O | ST | |
| RD6 | 54 | 83 | I/O | ST | |
| RD7 | 55 | 84 | I/O | ST | |
| RD8 | 42 | 68 | I/O | ST | |
| RD9 | 43 | 69 | I/O | ST | |
| RD10 | 44 | 70 | I/O | ST | |
| RD11 | 45 | 71 | I/O | ST | |
| RD12 | — | 79 | I/O | ST | |
| RD13 | — | 80 | I/O | ST | |
| RD14 | — | 47 | I/O | ST | |
| RD15 | — | 48 | I/O | ST | |
| RE0 | 60 | 93 | I/O | ST | PORTE is a bidirectional I/O port |
| RE1 | 61 | 94 | I/O | ST | |
| RE2 | 62 | 98 | I/O | ST | |
| RE3 | 63 | 99 | I/O | ST | |
| RE4 | 64 | 100 | I/O | ST | |
| RE5 | 1 | 3 | I/O | ST | |
| RE6 | 2 | 4 | I/O | ST | |
| RE7 | 3 | 5 | I/O | ST | |
| RE8 | — | 18 | I/O | ST | |
| RE9 | — | 19 | I/O | ST | |

**Legend:** CMOS = CMOS compatible input or output Analog = Analog input I = Input O = Output
ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer P = Power

**Note 1:** This pin is only available on devices without a USB module.

**2:** This pin is only available on devices with a USB module.

**3:** This pin is not available on 64-pin devices with a USB module.

**4:** This pin is only available on 100-pin devices without a USB module.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | 64-pin QFN/ TQFP | 100-pin TQFP | | | |
| RF0 | 58 | 87 | I/O | ST | PORTF is a bidirectional I/O port |
| RF1 | 59 | 88 | I/O | ST | |
| RF2 | 34(3) | 52 | I/O | ST | |
| RF3 | 33 | 51 | I/O | ST | |
| RF4 | 31 | 49 | I/O | ST | |
| RF5 | 32 | 50 | I/O | ST | |
| RF6 | 35(1) | 55(1) | I/O | ST | |
| RF7 | — | 54(4) | I/O | ST | |
| RF8 | — | 53 | I/O | ST | |
| RF12 | — | 40 | I/O | ST | |
| RF13 | — | 39 | I/O | ST | |
| RG0 | — | 90 | I/O | ST | PORTG is a bidirectional I/O port |
| RG1 | — | 89 | I/O | ST | |
| RG2 | 37(1) | 57(1) | I/O | ST | |
| RG3 | 36(1) | 56(1) | I/O | ST | |
| RG6 | 4 | 10 | I/O | ST | |
| RG7 | 5 | 11 | I/O | ST | |
| RG8 | 6 | 12 | I/O | ST | |
| RG9 | 8 | 14 | I/O | ST | |
| RG12 | — | 96 | I/O | ST | |
| RG13 | — | 97 | I/O | ST | |
| RG14 | — | 95 | I/O | ST | |
| RG15 | — | 1 | I/O | ST | |
| T1CK | 48 | 74 | I | ST | Timer1 External Clock Input |
| T2CK | PPS | PPS | I | ST | Timer2 External Clock Input |
| T3CK | PPS | PPS | I | ST | Timer3 External Clock Input |
| T4CK | PPS | PPS | I | ST | Timer4 External Clock Input |
| T5CK | PPS | PPS | I | ST | Timer5 External Clock Input |
| $\overline{U1CTS}$ | PPS | PPS | I | ST | UART1 Clear to Send |
| $\overline{U1RTS}$ | PPS | PPS | O | — | UART1 Ready to Send |
| U1RX | PPS | PPS | I | ST | UART1 Receive |
| U1TX | PPS | PPS | O | — | UART1 Transmit |
| $\overline{U2CTS}$ | PPS | PPS | I | ST | UART2 Clear to Send |
| $\overline{U2RTS}$ | PPS | PPS | O | — | UART2 Ready to Send |
| U2RX | PPS | PPS | I | ST | UART2 Receive |
| U2TX | PPS | PPS | O | — | UART2 Transmit |

**Legend:** CMOS = CMOS compatible input or output Analog = Analog input I = Input O = Output
ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer P = Power

**Note 1:** This pin is only available on devices without a USB module.

**2:** This pin is only available on devices with a USB module.

**3:** This pin is not available on 64-pin devices with a USB module.

**4:** This pin is only available on 100-pin devices without a USB module.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | 64-pin QFN/ TQFP | 100-pin TQFP | | | |
| U3CTS | PPS | PPS | I | ST | UART3 Clear to Send |
| U3RTS | PPS | PPS | O | — | UART3 Ready to Send |
| U3RX | PPS | PPS | I | ST | UART3 Receive |
| U3TX | PPS | PPS | O | — | UART3 Transmit |
| U4CTS | PPS | PPS | I | ST | UART4 Clear to Send |
| U4RTS | PPS | PPS | O | — | UART4 Ready to Send |
| U4RX | PPS | PPS | I | ST | UART4 Receive |
| U4TX | PPS | PPS | O | — | UART4 Transmit |
| U5CTS | — | PPS | I | ST | UART5 Clear to Send |
| U5RTS | — | PPS | O | — | UART5 Ready to Send |
| U5RX | — | PPS | I | ST | UART5 Receive |
| U5TX | — | PPS | O | — | UART5 Transmit |
| SCK1 | 35(1), 50(2) | 55(1), 70(2) | I/O | ST | Synchronous Serial Clock Input/Output for SPI1 |
| SDI1 | PPS | PPS | I | — | SPI1 Data In |
| SDO1 | PPS | PPS | O | ST | SPI1 Data Out |
| SS1 | PPS | PPS | I/O | — | SPI1 Slave Synchronization for Frame Pulse I/O |
| SCK2 | 4 | 10 | I/O | ST | Synchronous Serial Clock Input/Output for SPI2 |
| SDI2 | PPS | PPS | I | — | SPI2 Data In |
| SDO2 | PPS | PPS | O | ST | SPI2 Data Out |
| SS2 | PPS | PPS | I/O | — | SPI2 Slave Synchronization for Frame Pulse I/O |
| SCK3 | 29 | 39 | I/O | ST | Synchronous Serial Clock Input/Output for SPI3 |
| SDI3 | PPS | PPS | I | — | SPI3 Data In |
| SDO3 | PPS | PPS | O | ST | SPI3 Data Out |
| SS3 | PPS | PPS | I/O | — | SPI3 Slave Synchronization for Frame Pulse I/O |
| SCK4 | — | 48 | I/O | ST | Synchronous Serial Clock Input/Output for SPI4 |
| SDI4 | — | PPS | I | — | SPI4 Data In |
| SDO4 | — | PPS | O | ST | SPI4 Data Out |
| SS4 | — | PPS | I/O | — | SPI4 Slave Synchronization for Frame Pulse I/O |
| SCL1 | 37(1), 44(2) | 57(1), 66(2) | I/O | ST | Synchronous Serial Clock Input/Output for I2C1 |
| SDA1 | 36(1), 43(2) | 56(1), 67(2) | I/O | ST | Synchronous Serial Data Input/Output for I2C1 |
| SCL2 | 32 | 58 | I/O | ST | Synchronous Serial Clock Input/Output for I2C2 |
| SDA2 | 31 | 59 | I/O | ST | Synchronous Serial Data Input/Output for I2C2 |
| TMS | 23 | 17 | I | ST | JTAG Test Mode Select Pin |
| TCK | 27 | 38 | I | ST | JTAG Test Clock Input Pin |
| TDI | 28 | 60 | I | — | JTAG Test Clock Input Pin |
| TDO | 24 | 61 | O | — | JTAG Test Clock Output Pin |

**Legend:** CMOS = CMOS compatible input or output Analog = Analog input I = Input O = Output
ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer P = Power

**Note 1:** This pin is only available on devices without a USB module.

**2:** This pin is only available on devices with a USB module.

**3:** This pin is not available on 64-pin devices with a USB module.

**4:** This pin is only available on 100-pin devices without a USB module.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | 64-pin QFN/ TQFP | 100-pin TQFP | | | |
| RTCC | 42 | 68 | O | — | Real-Time Clock Alarm Output |
| CVREFOUT | 23 | 34 | O | Analog | Comparator Voltage Reference (Output) |
| C1INA | 11 | 20 | I | Analog | Comparator 1 Inputs |
| C1INB | 12 | 21 | I | Analog | |
| C1INC | 5 | 11 | I | Analog | |
| C1IND | 4 | 10 | I | Analog | |
| C2INA | 13 | 22 | I | Analog | Comparator 2 Inputs |
| C2INB | 14 | 23 | I | Analog | |
| C2INC | 8 | 14 | I | Analog | |
| C2IND | 6 | 12 | I | Analog | |
| C3INA | 58 | 87 | I | Analog | Comparator 3 Inputs |
| C3INB | 55 | 84 | I | Analog | |
| C3INC | 54 | 83 | I | Analog | |
| C3IND | 51 | 78 | I | Analog | |
| C1OUT | PPS | PPS | O | — | Comparator 1 Output |
| C2OUT | PPS | PPS | O | — | Comparator 2 Output |
| C3OUT | PPS | PPS | O | — | Comparator 3 Output |
| PMALL | 30 | 44 | O | TTL/ST | Parallel Master Port Address Latch Enable Low Byte |
| PMALH | 29 | 43 | O | TTL/ST | Parallel Master Port Address Latch Enable High Byte |
| PMA0 | 30 | 44 | O | TTL/ST | Parallel Master Port Address bit 0 Input (Buffered Slave modes) and Output (Master modes) |
| PMA1 | 29 | 43 | O | TTL/ST | Parallel Master Port Address bit 0 Input (Buffered Slave modes) and Output (Master modes) |

**Legend:** CMOS = CMOS compatible input or output Analog = Analog input I = Input O = Output
ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer P = Power

**Note 1:** This pin is only available on devices without a USB module.

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**4:** This pin is only available on 100-pin devices without a USB module.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | 64-pin QFN/ TQFP | 100-pin TQFP | | | |
| PMA2 | 8 | 14 | O | TTL/ST | Parallel Master Port data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes) |
| PMA3 | 6 | 12 | O | TTL/ST | |
| PMA4 | 5 | 11 | O | TTL/ST | |
| PMA5 | 4 | 10 | O | TTL/ST | |
| PMA6 | 16 | 29 | O | TTL/ST | |
| PMA7 | 22 | 28 | O | TTL/ST | |
| PMA8 | 32 | 50 | O | TTL/ST | |
| PMA9 | 31 | 49 | O | TTL/ST | |
| PMA10 | 28 | 42 | O | TTL/ST | |
| PMA11 | 27 | 41 | O | TTL/ST | |
| PMA12 | 24 | 35 | O | TTL/ST | |
| PMA13 | 23 | 34 | O | TTL/ST | |
| PMA14 | 45 | 71 | O | TTL/ST | |
| PMA15 | 44 | 70 | O | TTL/ST | |
| PMCS1 | 45 | 71 | O | TTL/ST | Parallel Master Port data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes) |
| PMCS2 | 44 | 70 | O | TTL/ST | |
| PMD0 | 60 | 93 | I/O | TTL/ST | |
| PMD1 | 61 | 94 | I/O | TTL/ST | |
| PMD2 | 62 | 98 | I/O | TTL/ST | |
| PMD3 | 63 | 99 | I/O | TTL/ST | |
| PMD4 | 64 | 100 | I/O | TTL/ST | |
| PMD5 | 1 | 3 | I/O | TTL/ST | |
| PMD6 | 2 | 4 | I/O | TTL/ST | |
| PMD7 | 3 | 5 | I/O | TTL/ST | |
| PMD8 | — | 90 | I/O | TTL/ST | |
| PMD9 | — | 89 | I/O | TTL/ST | |
| PMD10 | — | 88 | I/O | TTL/ST | |
| PMD11 | — | 87 | I/O | TTL/ST | |
| PMD12 | — | 79 | I/O | TTL/ST | |
| PMD13 | — | 80 | I/O | TTL/ST | |
| PMD14 | — | 83 | I/O | TTL/ST | |
| PMD15 | — | 84 | I/O | TTL/ST | |
| PMRD | 53 | 82 | O | — | Parallel Master Port Read Strobe |
| PMWR | 52 | 81 | O | — | Parallel Master Port Write Strobe |
| $V_{BUS}$ **(2)** | 34 | 54 | I | Analog | USB Bus Power Monitor |

**Legend:** CMOS = CMOS compatible input or output Analog = Analog input I = Input O = Output
ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer P = Power

**Note 1:** This pin is only available on devices without a USB module.

**2:** This pin is only available on devices with a USB module.

**3:** This pin is not available on 64-pin devices with a USB module.

**4:** This pin is only available on 100-pin devices without a USB module.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | 64-pin QFN/ TQFP | 100-pin TQFP | | | |
| $V_{USB3V3}$(2) | 35 | 55 | P | — | USB internal transceiver supply. If the USB module is not used, this pin must be connected to $V_{DD}$. |
| $V_{BUSON}$(2) | 11 | 20 | O | — | USB Host and OTG bus power control Output |
| D+(2) | 37 | 57 | I/O | Analog | USB D+ |
| D-(2) | 36 | 56 | I/O | Analog | USB D- |
| USBID(2) | 33 | 51 | I | ST | USB OTG ID Detect |
| PGED1 | 16 | 25 | I/O | ST | Data I/O pin for Programming/Debugging Communication Channel 1 |
| PGEC1 | 15 | 24 | I | ST | Clock Input pin for Programming/Debugging Communication Channel 1 |
| PGED2 | 18 | 27 | I/O | ST | Data I/O Pin for Programming/Debugging Communication Channel 2 |
| PGEC2 | 17 | 26 | I | ST | Clock Input Pin for Programming/Debugging Communication Channel 2 |
| PGED3 | 13 | 22 | I/O | ST | Data I/O Pin for Programming/Debugging Communication Channel 3 |
| PGEC3 | 14 | 23 | I | ST | Clock Input Pin for Programming/Debugging Communication Channel 3 |
| CTED1 | — | 17 | I | ST | CTMU External Edge Input 1 |
| CTED2 | — | 38 | I | ST | CTMU External Edge Input 2 |
| CTED3 | 18 | 27 | I | ST | CTMU External Edge Input 3 |
| CTED4 | 22 | 33 | I | ST | CTMU External Edge Input 4 |
| CTED5 | 29 | 43 | I | ST | CTMU External Edge Input 5 |
| CTED6 | 30 | 44 | I | ST | CTMU External Edge Input 6 |
| CTED7 | — | 9 | I | ST | CTMU External Edge Input 7 |
| CTED8 | — | 92 | I | ST | CTMU External Edge Input 8 |
| CTED9 | — | 60 | I | ST | CTMU External Edge Input 9 |
| CTED10 | 21 | 32 | I | ST | CTMU External Edge Input 10 |
| CTED11 | 23 | 34 | I | ST | CTMU External Edge Input 11 |
| CTED12 | 15 | 24 | I | ST | CTMU External Edge Input 12 |
| CTED13 | 14 | 23 | I | ST | CTMU External Edge Input 13 |
| C1RX | PPS | PPS | I | ST | Enhanced CAN Receive |
| C1TX | PPS | PPS | O | ST | Enhanced CAN Transmit |

**Legend:** CMOS = CMOS compatible input or output Analog = Analog input I = Input O = Output
ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer P = Power

**Note 1:** This pin is only available on devices without a USB module.

**2:** This pin is only available on devices with a USB module.

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**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | 64-pin QFN/ TQFP | 100-pin TQFP | | | |
| $\overline{MCLR}$ | 7 | 13 | I | ST | Master Clear (Reset) input. This pin is an active-low Reset to the device. |
| AVDD | 19 | 30 | P | P | Positive supply for analog modules. This pin must be connected at all times. |
| AVSS | 20 | 31 | P | P | Ground reference for analog modules |
| VDD | 10, 26, 38, 57 | 2, 16, 37, 46, 62, 86 | P | — | Positive supply for peripheral logic and I/O pins |
| VCAP | 56 | 85 | P | — | Capacitor for Internal Voltage Regulator |
| VSS | 9, 25, 41 | 15, 36, 45, 65, 75 | P | — | Ground reference for logic and I/O pins |
| VREF+ | 16 | 29 | P | Analog | Analog Voltage Reference (High) Input |
| VREF- | 15 | 28 | P | Analog | Analog Voltage Reference (Low) Input |

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**Note 1:** This pin is only available on devices without a USB module.

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**NOTES:**

## 2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MCUS

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

### 2.1 Basic Connection Requirements

Getting started with the PIC32MX1XX/2XX/5XX 64/100-pin family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins, even if the ADC module is not used (see **2.2 "Decoupling Capacitors"**)
- VCAP pin (see **2.3 "Capacitor on Internal Voltage Regulator (VCAP)"**)
- $\overline{\text{MCLR}}$ pin (see **2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins, used for In-Circuit Serial Programming (ICSP™) and debugging purposes (see **2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins, when external oscillator source is used (see **2.7 "External Oscillator Pins"**)

The following pins may be required:

VREF+/VREF- pins, used when external voltage reference for the ADC module is implemented.

**Note:** The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

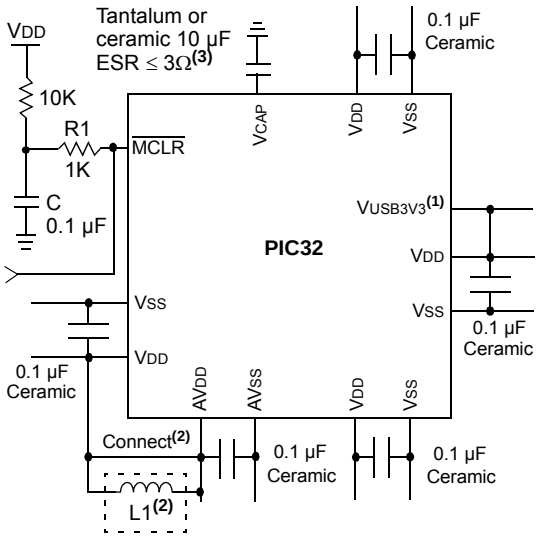
### 2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 µF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

**FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION**




**Note 1:** If the USB module is not used, this pin must be connected to VDD.

**2:** As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 3Ω and the inductor capacity greater than 10 mA.

Where:

$$f \quad \frac{FCNV}{2} \quad \text{(i.e., ADC conversion rate/2)}$$

$$f \quad \frac{1}{(2\pi\sqrt{LC})}$$

$$L \quad \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

**2:** Aluminum or electrolytic capacitors should not be used. ESR ≤ 3Ω from -40°C to 125°C @ SYSCLK frequency (i.e., MIPS).

### 2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 µF to 47 µF. This capacitor should be located as close to the device as possible.

## 2.3 Capacitor on Internal Voltage Regulator (VCAP)

### 2.3.1 INTERNAL REGULATOR MODE

A low-ESR (3 ohm) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output. The VCAP pin must not be connected to VDD, and must have a CEFC capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. Refer to **Section 31.0 "40 MHz Electrical Characteristics"** for additional information on CEFC specifications.

## 2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

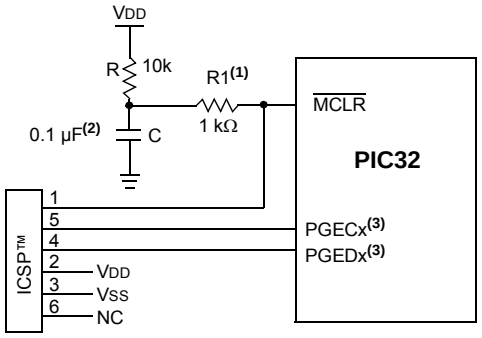
- Device Reset
- Device programming and debugging

Pulling The MCLR pin low generates a device Reset. Figure 2-2 illustrates a typical MCLR circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

**FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS**




**Note 1:** 470Ω ≤ R1 ≤ 1Ω will limit any current flowing into MCLR from the external capacitor C, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met without interfering with the Debug/Programmer tools.

**2:** The capacitor can be sized to prevent unintentional Resets from brief glitches or to extend the device Reset period during POR.

**3:** No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.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## 2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input voltage low (VIL) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE™.

For more information on MPLAB ICD 3 and MPLAB REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- *"Using MPLAB® ICD 3"* (poster) DS50001765
- *"MPLAB® ICD 3 Design Advisory"* DS50001764
- *"MPLAB® REAL ICE™ In-Circuit Debugger User's Guide"* DS50001616
- *"Using MPLAB® REAL ICE™ Emulator"* (poster) DS50001749

## 2.6 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

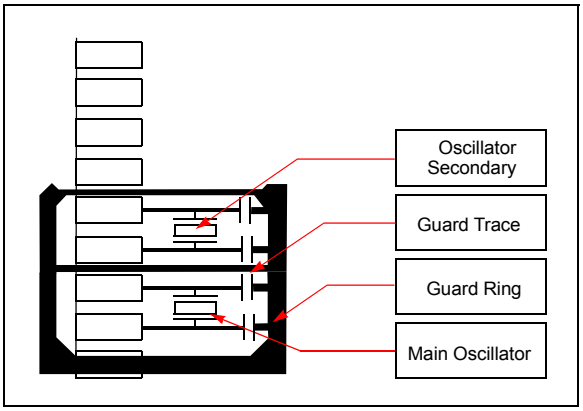
Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer or debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input voltage low (VIL) requirements

## 2.7 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 8.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

**FIGURE 2-3: SUGGESTED OSCILLATOR CIRCUIT PLACEMENT**



### 2.7.1 CRYSTAL OSCILLATOR DESIGN CONSIDERATION

The following examples are used to calculate the Primary Oscillator loading capacitor values:

- CIN = PIC32_OSC2_Pin Capacitance = ~4-5 pF
- COUT = PIC32_OSC1_Pin Capacitance = ~4-5 pF
- C1 and C2 = XTAL manufacturing recommended loading capacitance
- Estimated PCB stray capacitance, (i.e.,12 mm length) = 2.5 pF

**EXAMPLE 2-1: CRYSTAL LOAD CAPACITOR CALCULATION**

Crystal manufacturer recommended: $C1 = C2 = 15\ pF$

Therefore:

$$C_{LOAD} = \{([C_{IN} + C1] * [C_{OUT} + C2]) / [C_{IN} + C1 + C2 + C_{OUT}]\} + \text{estimated oscillator PCB stray capacitance}$$
$$= \{([5 + 15][5 + 15]) / [5 + 15 + 15 + 5]\} + 2.5\ pF$$
$$= \{([20][20]) / [40]\} + 2.5$$
$$= 10 + 2.5 = 12.5\ pF$$

Rounded to the nearest standard value or 13 pF in this example for Primary Oscillator crystals “C1” and “C2”.

The following tips are used to increase oscillator gain, (i.e., to increase peak-to-peak oscillator signal):

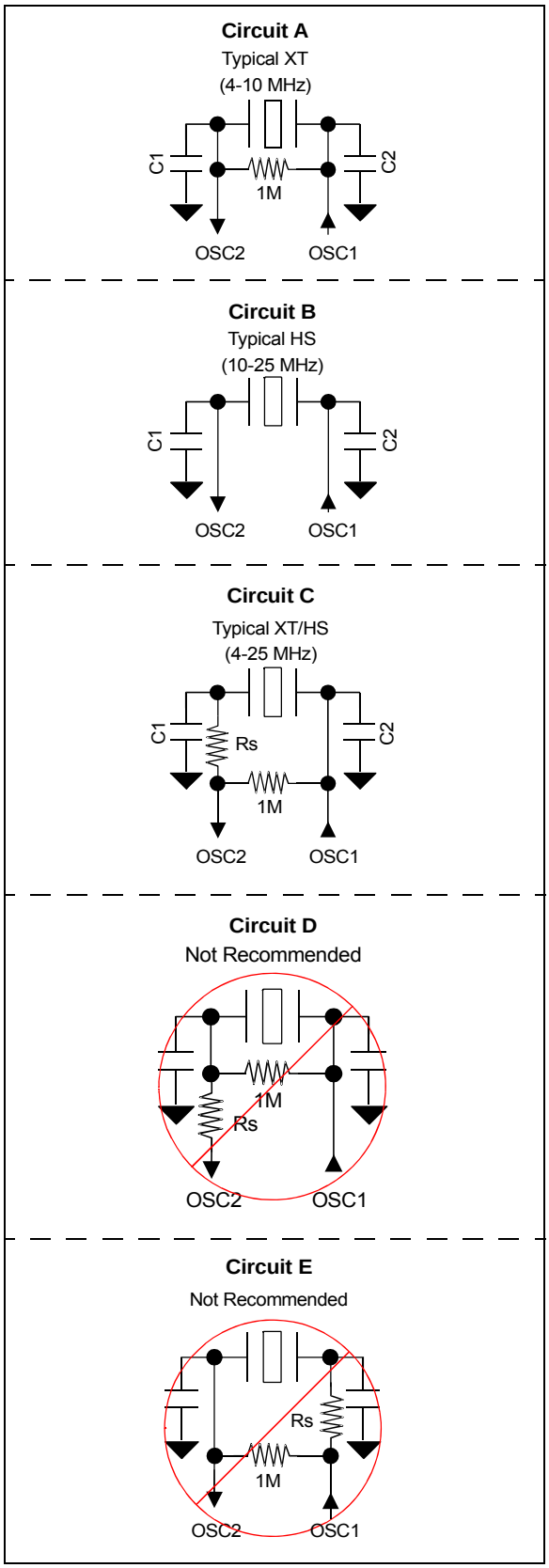
- Select a crystal with a lower “minimum” power drive rating
- Select an crystal oscillator with a lower XTAL manufacturing “ESR” rating.
- Add a parallel resistor across the crystal. The smaller the resistor value the greater the gain. It is recommended to stay in the range of 600k to 1M
- C1 and C2 values also affect the gain of the oscillator. The lower the values, the higher the gain.
- C2/C1 ratio also affects gain. To increase the gain, make C1 slightly smaller than C2, which will also help start-up performance.

**Note:** Do not add excessive gain such that the oscillator signal is clipped, flat on top of the sine wave. If so, you need to reduce the gain or add a series resistor, RS, as shown in circuit “C” in Figure 2-4. Failure to do so will stress and age the crystal, which can result in an early failure. Adjust the gain to trim the max peak-to-peak to ~VDD-0.6V. When measuring the oscillator signal you must use a FET scope probe or a probe with ≤ 1.5 pF or the scope probe itself will unduly change the gain and peak-to-peak levels.

#### 2.7.1.1 Additional Microchip References

- AN588 *“PICmicro® Microcontroller Oscillator Design Guide”*
- AN826 *“Crystal Oscillator Basics and Crystal Selection for rfPIC™ and PICmicro® Devices”*
- AN849 *“Basic PICmicro® Oscillator Design”*

**FIGURE 2-4: PRIMARY CRYSTAL OSCILLATOR CIRCUIT RECOMMENDATIONS**





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## 2.8 Unused I/Os

Unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic-low state.

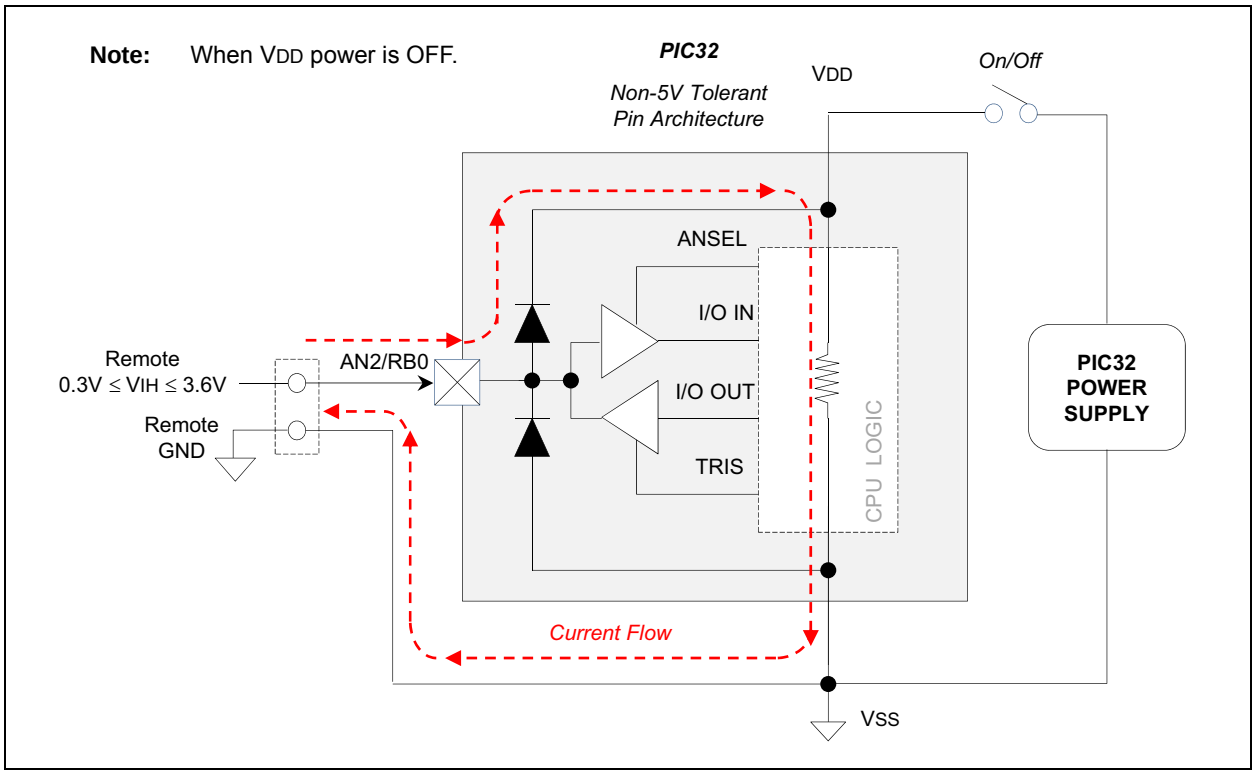
Alternatively, inputs can be reserved by connecting the pin to VSS through a 1k to 10k resistor and configuring the pin as an input.

## 2.9 Considerations When Interfacing to Remotely Powered Circuits

### 2.9.1 NON-5V TOLERANT INPUT PINS

A quick review of the absolute maximum rating section in **31.0 "40 MHz Electrical Characteristics"** will indicate that the voltage on any non-5v tolerant pin may not exceed AVDD/VDD + 0.3V. Figure 2-5 shows an example of a remote circuit using an independent power source, which is powered while connected to a PIC32 non-5V tolerant circuit that is not powered.

**FIGURE 2-5: PIC32 NON-5V TOLERANT CIRCUIT EXAMPLE**





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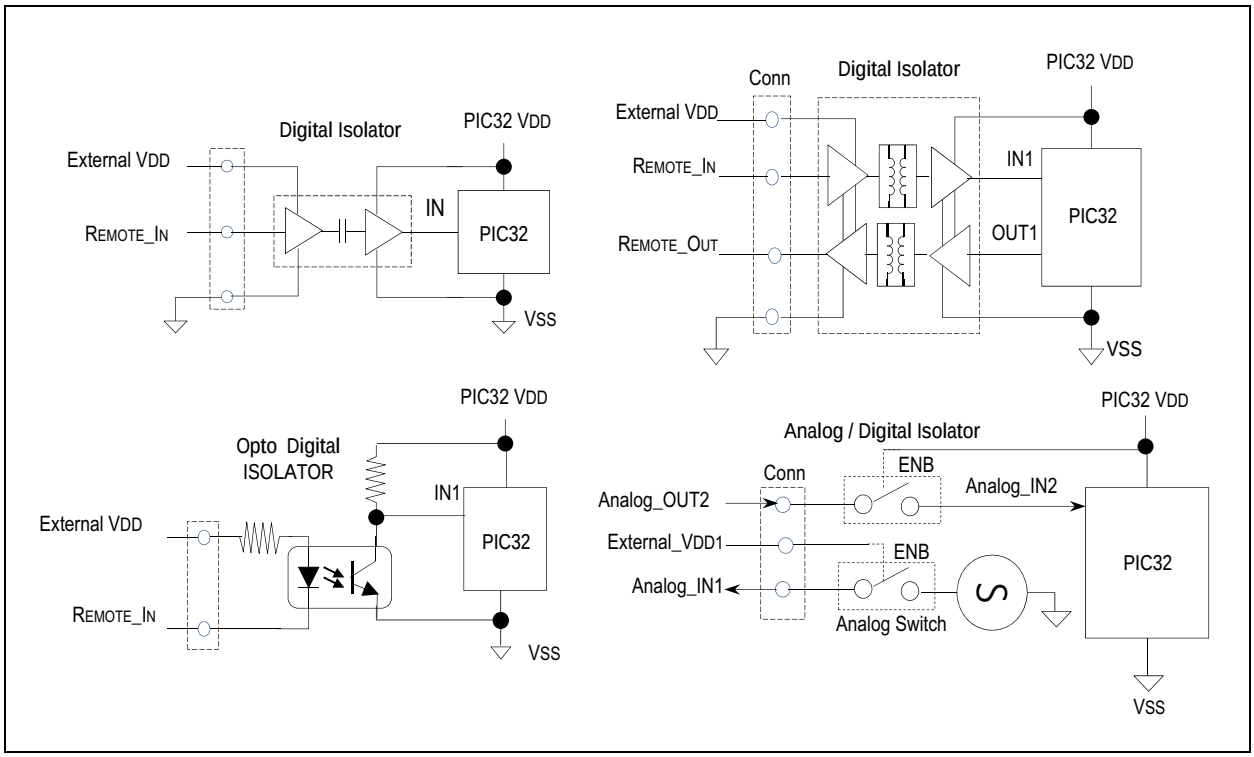
Without proper signal isolation, on non-5V tolerant pins, the remote signal can power the PIC32 device through the high side ESD protection diodes. Besides violating the absolute maximum rating specification when VDD of the PIC32 device is restored and ramping up or ramping down, it can also negatively affect the internal Power-on Reset (POR) and Brown-out Reset (BOR) circuits, which can lead to improper initialization of internal PIC32 logic circuits. In these cases, it is recommended to implement digital or analog signal isolation as depicted in Figure 2-6, as appropriate. This is indicative of all industry microcontrollers and not just Microchip products.

**TABLE 2-1: EXAMPLES OF DIGITAL/ ANALOG ISOLATORS WITH OPTIONAL LEVEL TRANSLATION**

| Example Digital/Analog Signal Isolation Circuits | Inductive Coupling | Capacitive Coupling | Opto Coupling | Analog/Digital Switch |
|---|---|---|---|---|
| ADuM7241 / 40 ARZ (1 Mbps) | X | — | — | — |
| ADuM7241 / 40 CRZ (25 Mbps) | X | — | — | — |
| ISO721 | — | X | — | — |
| LTV-829S (2 Channel) | — | — | X | — |
| LTV-849S (4 Channel) | — | — | X | — |
| FSA266 / NC7WB66 | — | — | — | X |

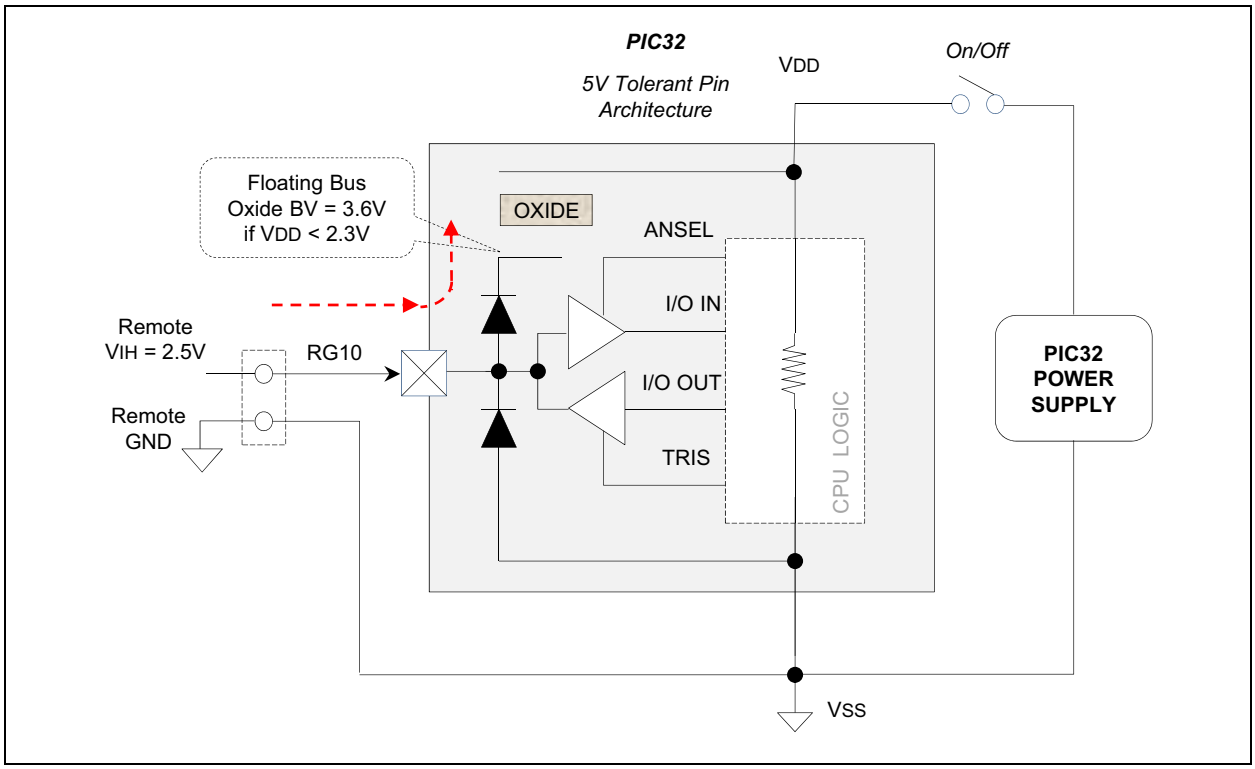
**FIGURE 2-6: DIGITAL/ANALOG SIGNAL ISOLATION CIRCUITS**



### 2.9.2 5V TOLERANT INPUT PINS

The internal high side diode on 5V tolerant pins are bussed to an internal floating node, rather than being connected to VDD, as shown in Figure 2-7. Voltages on these pins, if VDD < 2.3V, should not exceed roughly 3.2V relative to VSS of the PIC32 device. Voltage of 3.6V or higher will violate the absolute maximum specification, and will stress the oxide layer separating the high side floating node, which impacts device reliability. If a remotely powered "digital-only" signal can be guaranteed to always be ≤ 3.2V relative to Vss on the PIC32 device side, a 5V tolerant pin could be used without the need for a digital isolator. This is assuming there is not a ground loop issue, logic ground of the two circuits not at the same absolute level, and a remote logic low input is not less than VSS - 0.3V.

**FIGURE 2-7: PIC32 5V TOLERANT PIN ARCHITECTURE EXAMPLE**





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## 2.10 Typical Application Connection Examples

Examples of typical application connections are shown in Figure 2-8, Figure 2-9, and Figure 2-10.

**FIGURE 2-8: CAPACITIVE TOUCH SENSING WITH GRAPHICS APPLICATION**

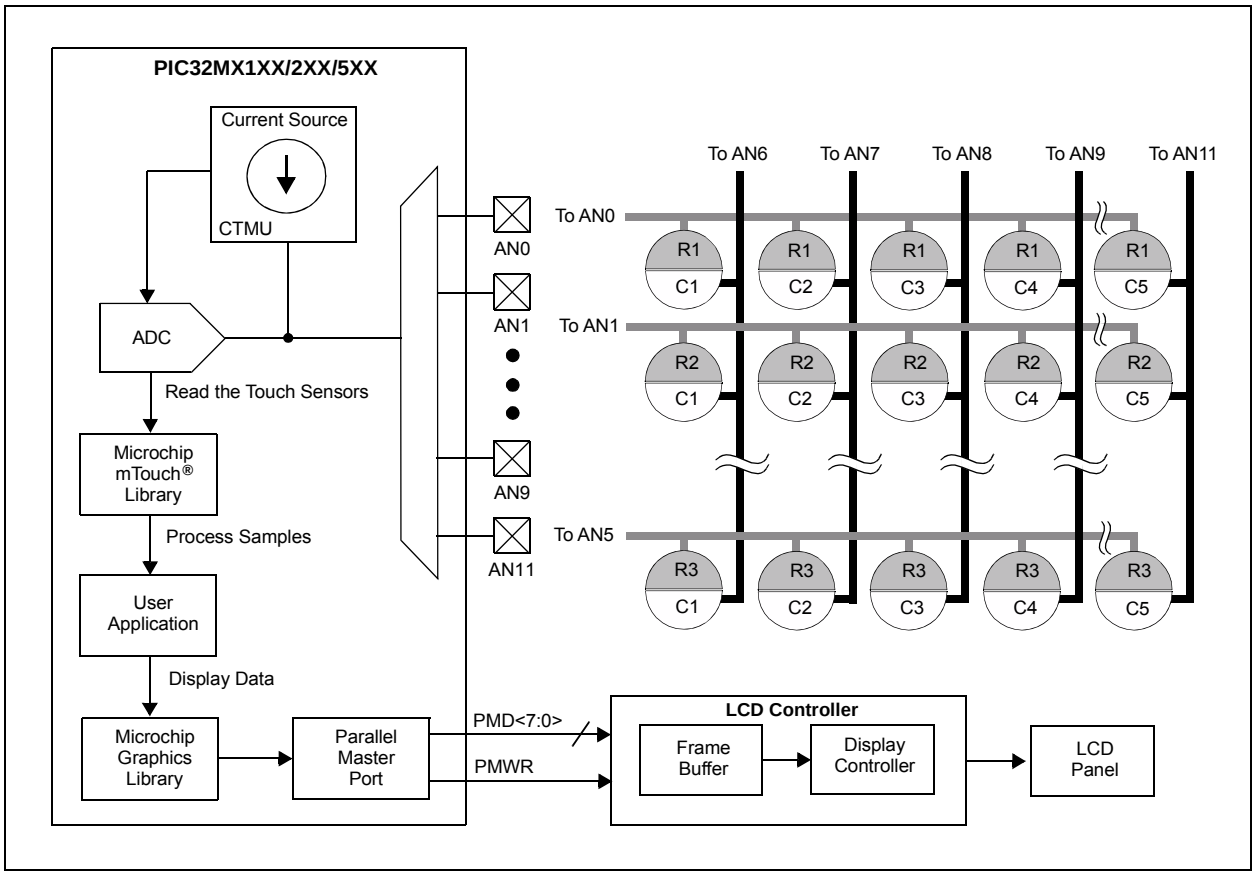



**FIGURE 2-9: AUDIO PLAYBACK APPLICATION**

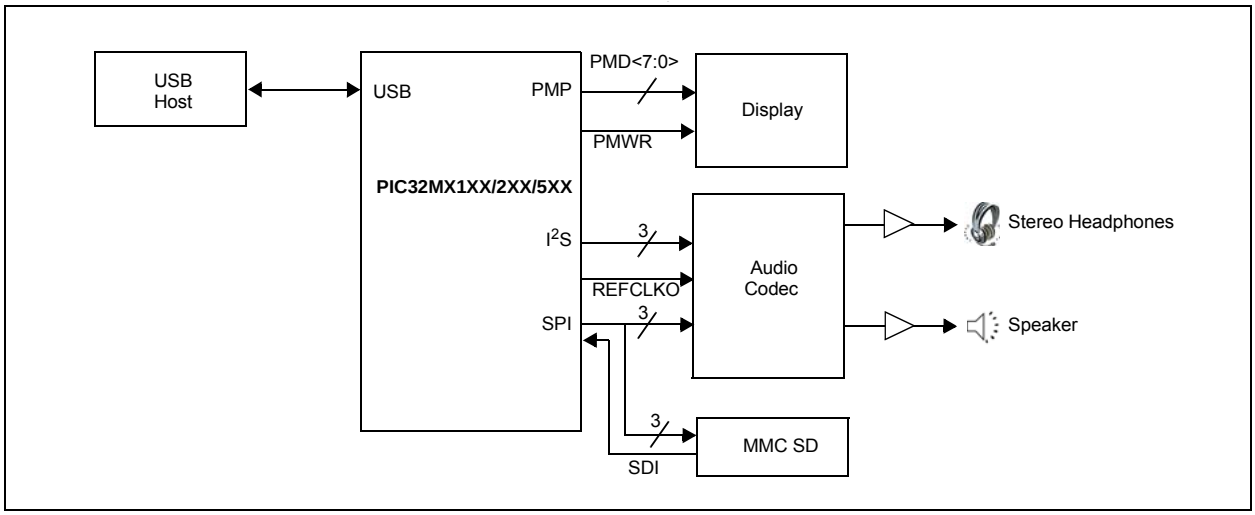
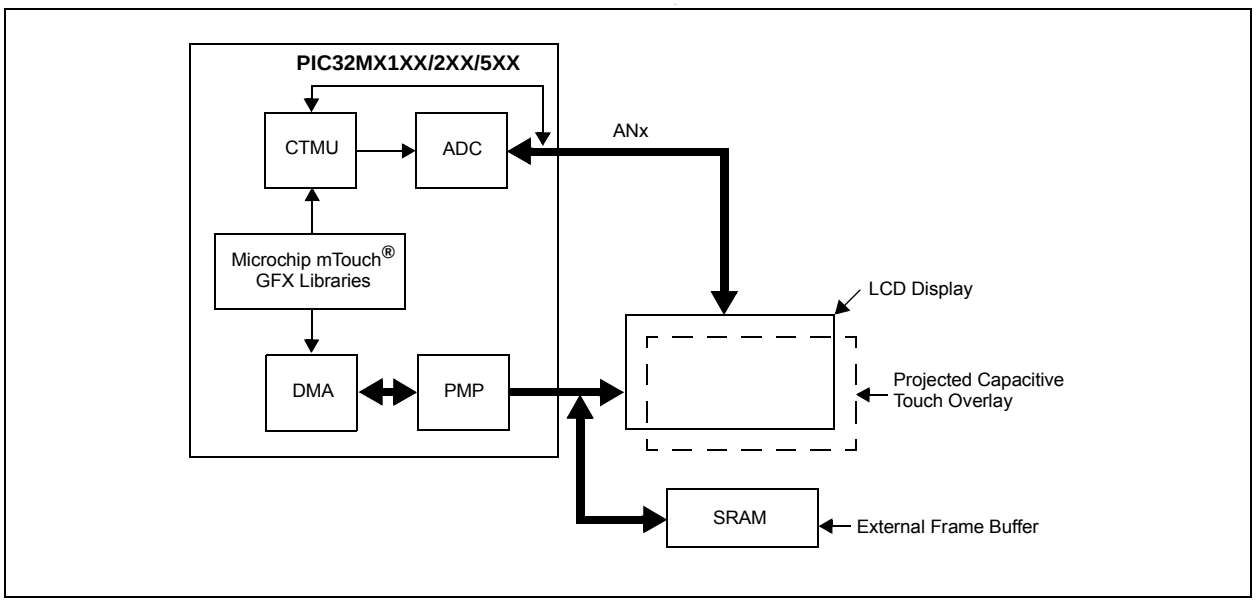


**FIGURE 2-10: LOW-COST CONTROLLERLESS (LCC) GRAPHICS APPLICATION WITH PROJECTED CAPACITIVE TOUCH**





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## 3.0 CPU

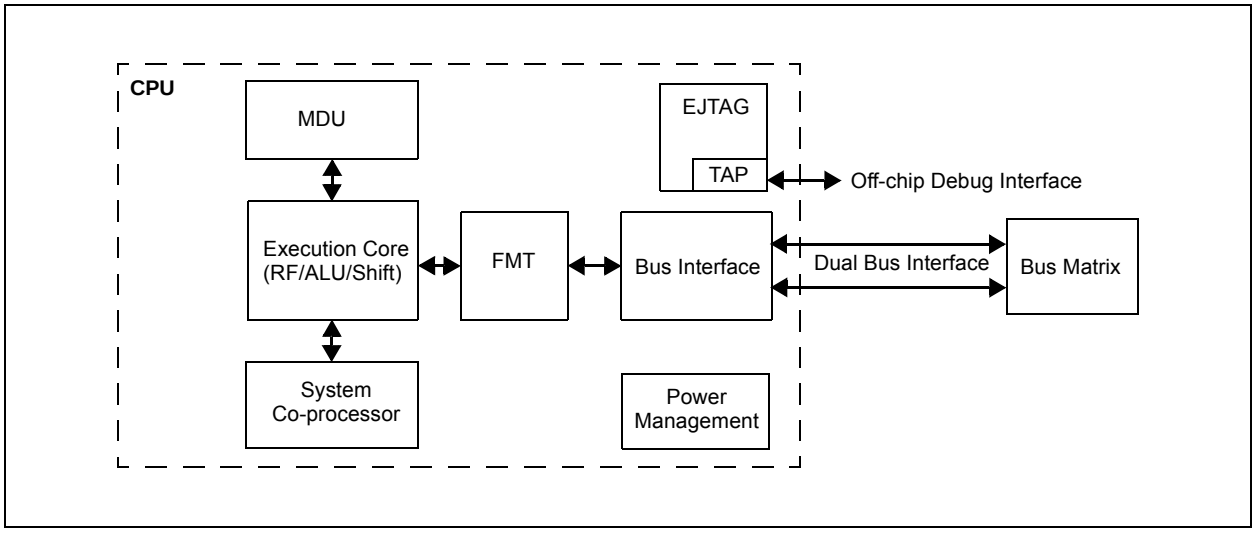
**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2. "CPU"** (DS60001113) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). Resources for the MIPS32® M4K® Processor Core are available at http://www.imgtec.com.

The the MIPS32® M4K® Processor Core is the heart of the PIC32MX1XX/2XX/5XX 64/100-pin device processor. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of instruction execution to the proper destinations.

### 3.1 Features

- 5-stage pipeline
- 32-bit address and data paths
- MIPS32® Enhanced Architecture (Release 2):
  - Multiply-accumulate and multiply-subtract instructions
  - Targeted multiply instruction
  - Zero/One detect instructions
  - `WAIT` instruction
  - Conditional move instructions (`MOVN`, `MOVZ`)
  - Vectored interrupts
  - Programmable exception vector base
  - Atomic interrupt enable/disable
  - Bit field manipulation instructions
- MIPS16e® Code Compression:
  - 16-bit encoding of 32-bit instructions to improve code density
  - Special PC-relative instructions for efficient loading of addresses and constants
  - `SAVE` and `RESTORE` macro instructions for setting up and tearing down stack frames within subroutines
  - Improved support for handling 8 and 16-bit data types
- Simple Fixed Mapping Translation (FMT) Mechanism:
- Simple Dual Bus Interface:
  - Independent 32-bit address and data buses
  - Transactions can be aborted to improve interrupt latency
- Autonomous Multiply/Divide Unit (MDU):
  - Maximum issue rate of one 32x16 multiply per clock
  - Maximum issue rate of one 32x32 multiply every other clock
  - Early-in iterative divide. Minimum 11 and maximum 33 clock latency (dividend (*rs*) sign extension-dependent)
- Power Control:
  - Minimum frequency: 0 MHz
  - Low-Power mode (triggered by `WAIT` instruction)
  - Extensive use of local gated clocks
- EJTAG Debug:
  - Support for single stepping
  - Virtual instruction and data address/value
  - Breakpoints

**FIGURE 3-1: MIPS32® M4K® PROCESSOR CORE BLOCK DIAGRAM**



## 3.2 Architecture Overview

The MIPS32® M4K® processor core contains several logic blocks working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution Unit
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Fixed Mapping Translation (FMT)
- Dual Internal Bus interfaces
- Power Management
- MIPS16e® Support
- Enhanced JTAG (EJTAG) Controller

### 3.2.1 EXECUTION UNIT

The MIPS32® M4K® processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Bypass multiplexers used to avoid stalls when executing instruction streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the `CLZ` and `CLO` instructions
- Arithmetic Logic Unit (ALU) for performing bitwise logical operations
- Shifter and store aligner

### 3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The MIPS32® M4K® processor core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the *rs* operand. The second number ('16' of 32x16) represents the *rt* operand. The PIC32 core only checks the value of the latter (*rt)* operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU.

Divide operations are implemented with a simple 1 bit per clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16-bit wide *rs*, 15 iterations are skipped and for a 24-bit wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent `MDU` instruction while a divide is still active causes an IU pipeline stall until the divide operation is completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the PIC32 core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

**TABLE 3-1: MIPS32® M4K® PROCESSOR CORE HIGH-PERFORMANCE INTEGER MULTIPLY/ DIVIDE UNIT LATENCIES AND REPEAT RATES**

| Op code | Operand Size (mul *rt*) (div *rs*) | Latency | Repeat Rate |
|---|---|---|---|
| `MULT/MULTU, MADD/MADDU, MSUB/MSUBU` | 16 bits | 1 | 1 |
| | 32 bits | 2 | 2 |
| `MUL` | 16 bits | 2 | 1 |
| | 32 bits | 3 | 2 |
| `DIV/DIVU` | 8 bits | 12 | 11 |
| | 16 bits | 19 | 18 |
| | 24 bits | 26 | 25 |
| | 32 bits | 33 | 32 |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The MIPS architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the General Purpose Register file.

In addition to the HI/LO targeted operations, the MIPS32® architecture also defines a multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

### 3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. Configuration information, such as presence of options like MIPS16e®, is also available by accessing the CP0 registers, listed in Table 3-2.

**TABLE 3-2: COPROCESSOR 0 REGISTERS**

| Register Number | Register Name | Function |
|---|---|---|
| 0-6 | Reserved | Reserved in the PIC32MX1XX/2XX/5XX 64/100-pin family core. |
| 7 | HWREna | Enables access via the RDHWR instruction to selected hardware registers. |
| 8 | BadVAddr(1) | Reports the address for the most recent address-related exception. |
| 9 | Count(1) | Processor cycle count. |
| 10 | Reserved | Reserved in the PIC32MX1XX/2XX/5XX 64/100-pin family core. |
| 11 | Compare(1) | Timer interrupt control. |
| 12 | Status(1) | Processor status and control. |
| 12 | IntCtl(1) | Interrupt system status and control. |
| 13 | Cause(1) | Cause of last general exception. |
| 14 | EPC(1) | Program counter at last exception. |
| 15 | PRId | Processor identification and revision. |
| 15 | EBASE | Exception vector base register. |
| 16 | Config | Configuration register. |
| 16 | Config1 | Configuration register 1. |
| 16 | Config2 | Configuration register 2. |
| 16 | Config3 | Configuration register 3. |
| 17-22 | Reserved | Reserved in the PIC32MX1XX/2XX/5XX 64/100-pin family core. |
| 23 | Debug(2) | Debug control and exception status. |
| 24 | DEPC(2) | Program counter at last debug exception. |
| 25-29 | Reserved | Reserved in the PIC32MX1XX/2XX/5XX 64/100-pin family core. |
| 30 | ErrorEPC(1) | Program counter at last error. |
| 31 | DESAVE(2) | Debug handler scratchpad register. |

**Note 1:** Registers used in exception processing.
**2:** Registers used during debug.

Coprocessor 0 also contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including alignment errors in data, external events or program errors. Table 3-3 lists the exception types in order of priority.

**TABLE 3-3: MIPS32® M4K® PROCESSOR CORE EXCEPTION TYPES**

| Exception | Description |
|---|---|
| Reset | Assertion $\overline{\text{MCLR}}$ or a Power-on Reset (POR). |
| DSS | EJTAG debug single step. |
| DINT | EJTAG debug interrupt. Caused by the assertion of the external *EJ_DINT* input or by setting the EjtagBrk bit in the ECR register. |
| NMI | Assertion of NMI signal. |
| Interrupt | Assertion of unmasked hardware or software interrupt signal. |
| DIB | EJTAG debug hardware instruction break matched. |
| AdEL | Fetch address alignment error. Fetch reference to protected address. |
| IBE | Instruction fetch bus error. |
| DBp | EJTAG breakpoint (execution of SDBBP instruction). |
| Sys | Execution of SYSCALL instruction. |
| Bp | Execution of BREAK instruction. |
| RI | Execution of a reserved instruction. |
| CpU | Execution of a coprocessor instruction for a coprocessor that is not enabled. |
| CEU | Execution of a CorExtend instruction when CorExtend is not enabled. |
| Ov | Execution of an arithmetic instruction that overflowed. |
| Tr | Execution of a trap (when trap condition is true). |
| DDBL/DDBS | EJTAG Data Address Break (address only) or EJTAG data value break on store (address + value). |
| AdEL | Load address alignment error. Load reference to protected address. |
| AdES | Store address alignment error. Store to protected address. |
| DBE | Load or store bus error. |
| DDBL | EJTAG data hardware breakpoint matched in load data compare. |

## 3.3 Power Management

The MIPS® M4K® processor core offers a number of power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or Halting the clocks, which reduces system power consumption during Idle periods.

### 3.3.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking Power-Down mode is through execution of the WAIT instruction. For more information on power management, see **Section 27.0 "Power-Saving Features"**.

### 3.3.2 LOCAL CLOCK GATING

The majority of the power consumed by the PIC32MX-1XX/2XX/5XX 64/100-pin family core is in the clock tree and clocking registers. The PIC32MX family uses extensive use of local gated-clocks to reduce this dynamic power consumption.

## 3.4 EJTAG Debug Support

The MIPS® M4K® processor core provides for an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard User mode and Kernel modes of operation, the M4K® core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (DERET) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification define which registers are selected and how they are used.


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## 4.0 MEMORY ORGANIZATION

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source.For detailed information, refer to **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX1XX/2XX/5XX 64/100-pin microcontrollers provide 4 GB of unified virtual memory address space. All memory regions, including program, data memory, SFRs and Configuration registers, reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, the data memory can be made executable, allowing PIC32MX1XX/2XX/5XX 64/100-pin devices to execute from data memory.

The key features include:

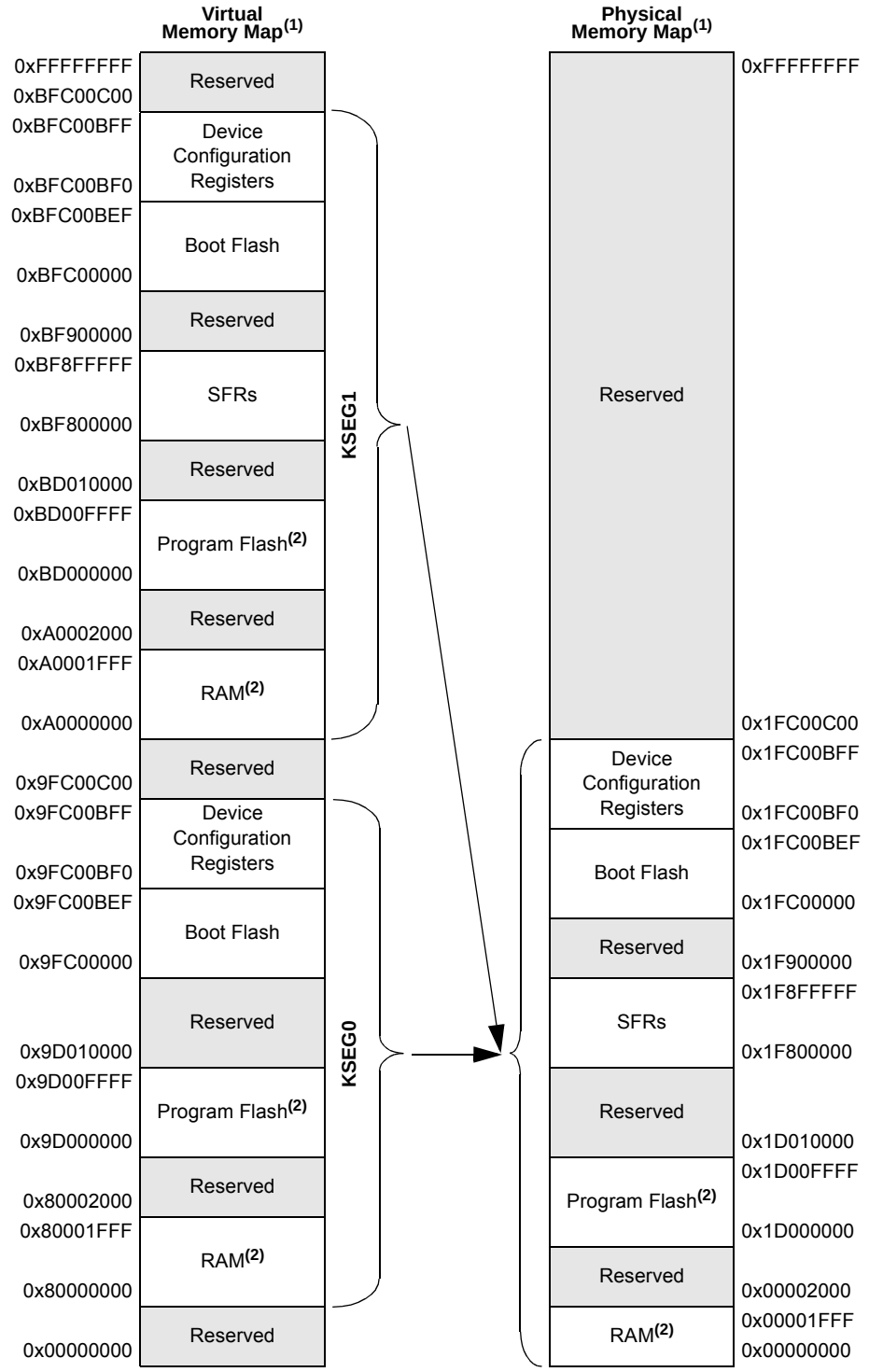
- 32-bit native data width
- Separate User (KUSEG) and Kernel (KSEG0/KSEG1) mode address space
- Flexible program Flash memory partitioning
- Flexible data RAM partitioning for data and program space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Simple memory mapping with Fixed Mapping Translation (FMT) unit

### 4.1 Memory Layout

PIC32MX1XX/2XX/5XX 64/100-pin microcontrollers implement two address schemes: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by bus master peripherals, such as DMA and the Flash controller, that access memory independently of the CPU.

The memory maps for the PIC32MX1XX/2XX/5XX 64/100-pin devices are illustrated in Figure 4-1 through Figure 4-4.

**FIGURE 4-1: MEMORY MAP FOR DEVICES WITH 64 KB OF PROGRAM MEMORY + 8 KB RAM**




**Note 1:** Memory areas are not shown to scale.

**2:** The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).


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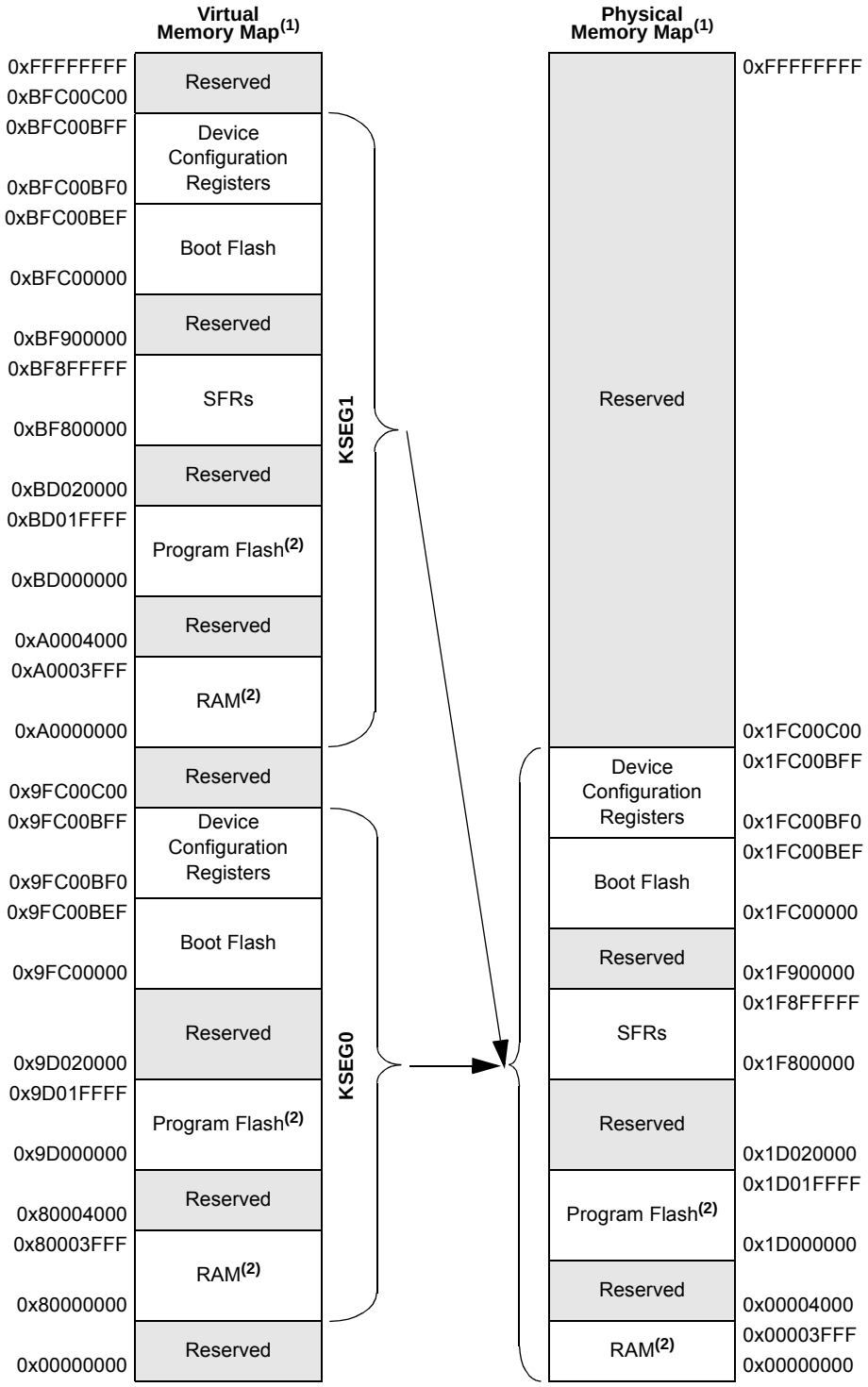
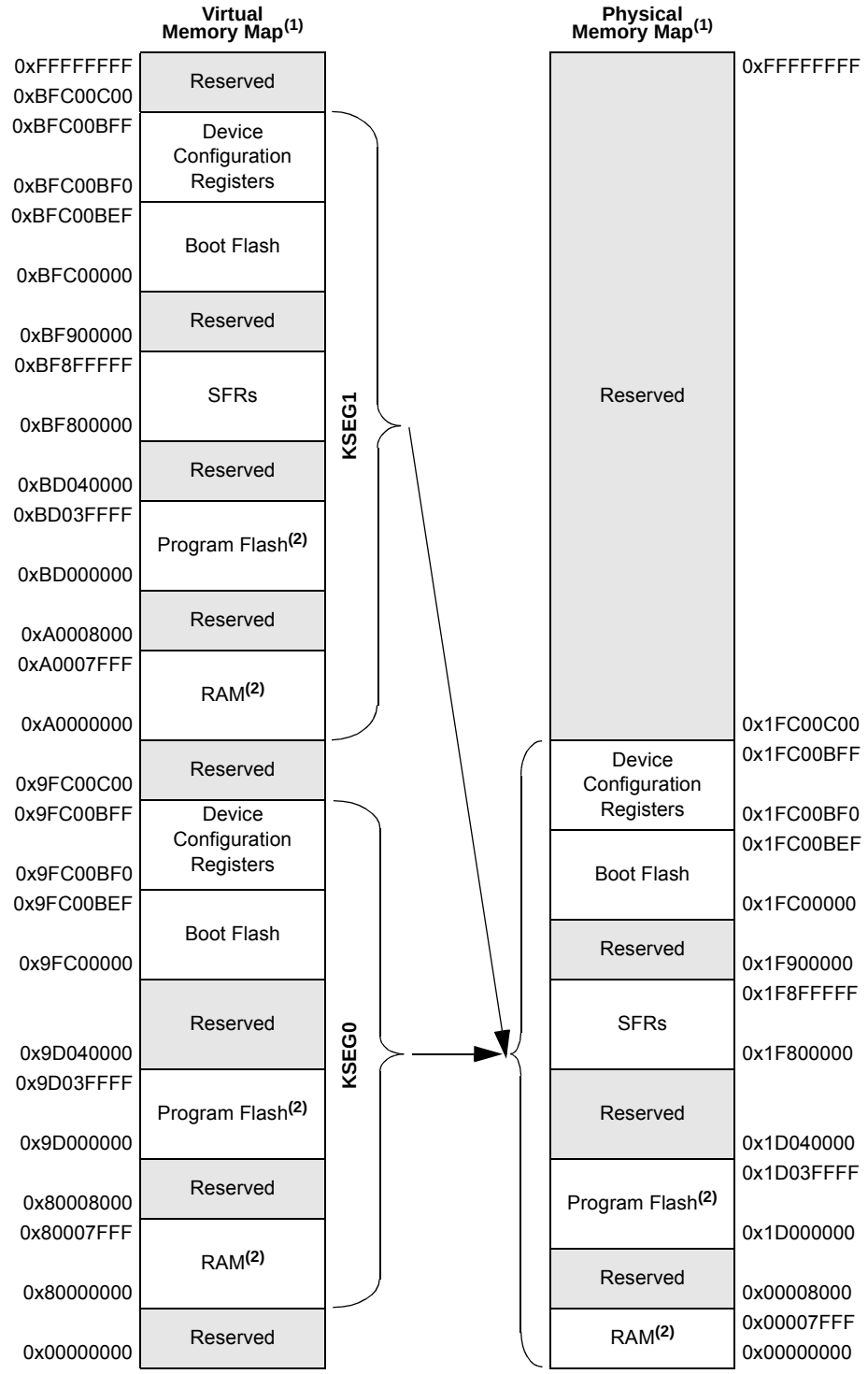
**FIGURE 4-2: MEMORY MAP FOR DEVICES WITH 128 KB OF PROGRAM MEMORY + 16 KB RAM**




**Note 1:** Memory areas are not shown to scale.

**2:** The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

**FIGURE 4-3: MEMORY MAP FOR DEVICES WITH 256 KB OF PROGRAM MEMORY + 32 KB RAM**




**Note 1:** Memory areas are not shown to scale.

**2:** The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).


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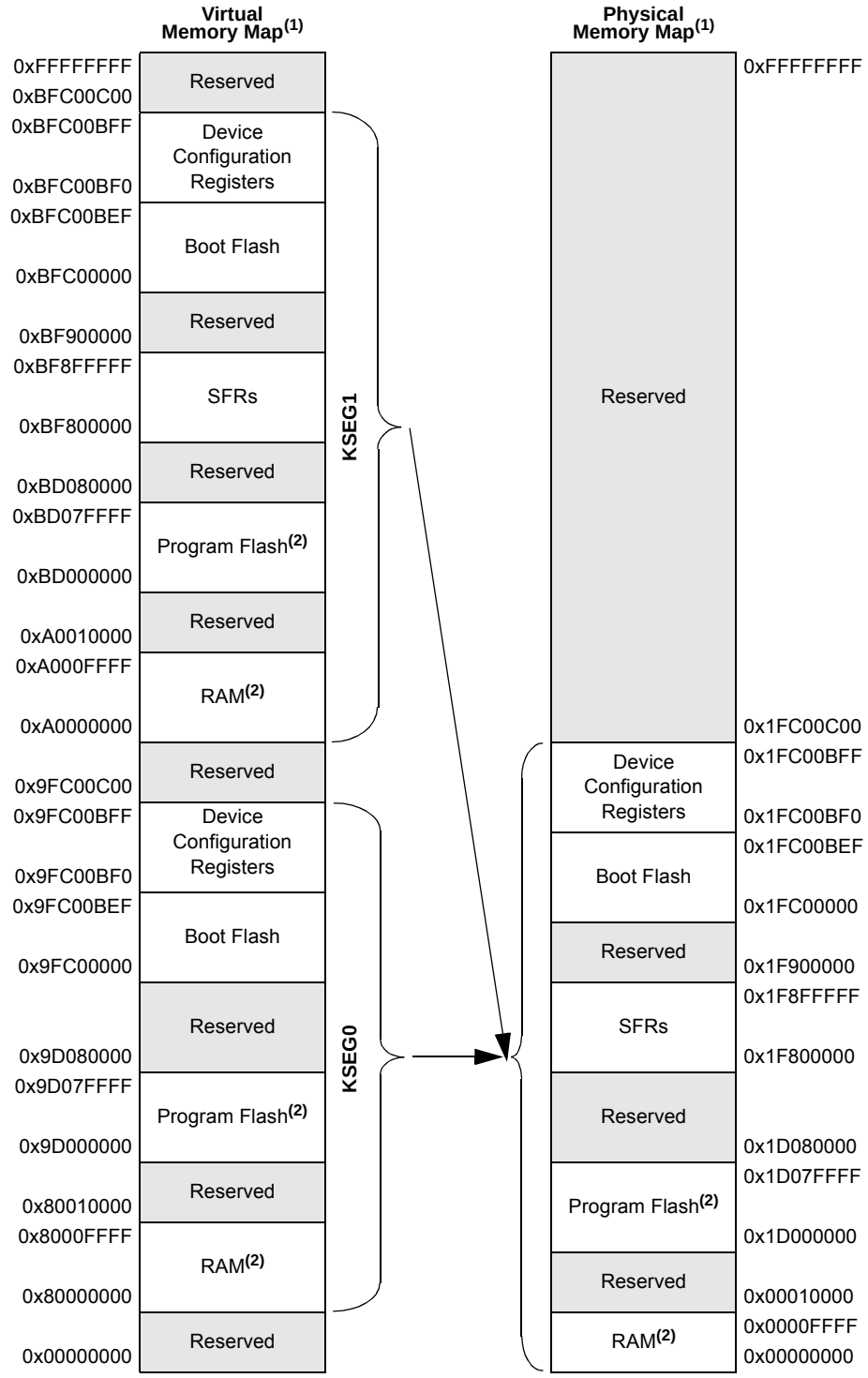
**FIGURE 4-4: MEMORY MAP FOR DEVICES WITH 512 KB OF PROGRAM MEMORY + 64 KB RAM**




**Note 1:** Memory areas are not shown to scale.

**2:** The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

**TABLE 4-1: SFR MEMORY MAP**

| Peripheral | Virtual Address | |
|---|---|---|
| | Base | Offset Start |
| Interrupt Controller | 0xBF88 | 0x1000 |
| Bus Matrix | | 0x2000 |
| DMA | | 0x3000 |
| USB | | 0x5000 |
| PORTA-PORTG | | 0x6000 |
| CAN1 | | 0xB000 |
| Watchdog Timer | 0xBF80 | 0x0000 |
| RTCC | | 0x0200 |
| Timer1-Timer5 | | 0x0600 |
| IC1-IC5 | | 0x2000 |
| OC1-OC5 | | 0x3000 |
| I2C1-I2C2 | | 0x5000 |
| SPI1-SPI4 | | 0x5800 |
| UART1-UART5 | | 0x6000 |
| PMP | | 0x7000 |
| ADC1 | | 0x9000 |
| DAC | | 0x9800 |
| Comparator 1, 2, 3 | | 0xA000 |
| Oscillator | | 0xF000 |
| Device and Revision ID | | 0xF200 |
| Flash Controller | | 0xF400 |
| PPS | | 0xFA00 |
| Configuration | 0xBFC0 | 0x0BF0 |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## 4.2 Special Function Register Maps

**TABLE 4-2: BUS MATRIX REGISTER MAP**

| Virtual Address (BF88_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 2000 | BMXCON(1) | 31:16 | — | — | — | — | — | BMXCHEDMA | — | — | — | — | — | BMXERRIXI | BMXERRICD | BMXERRDMA | BMXERRDS | BMXERRIS | 041F |
| | | 15:0 | — | — | — | — | — | — | — | — | — | BMXWSDRM | — | — | — | BMXARB<2:0> | | | 0047 |
| 2010 | BMXDKPBA(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BMXDKPBA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 2020 | BMXDUDBA(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BMXDUDBA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 2030 | BMXDUPBA(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BMXDUPBA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 2040 | BMXDRMSZ | 31:16 | BMXDRMSZ<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 2050 | BMXPUPBA(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | BMXPUPBA<19:16> | | | | 0000 |
| | | 15:0 | BMXPUPBA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 2060 | BMXPFMSZ | 31:16 | BMXPFMSZ<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 2070 | BMXBOOTSZ | 31:16 | BMXBOOTSZ<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

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## 4.3 Control Registers

Register 4-1 through Register 4-8 are used for setting the RAM and Flash memory partitions for data and code.

**REGISTER 4-1: BMXCON: BUS MATRIX CONFIGURATION REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| | — | — | — | BMX ERRIXI | BMX ERRICD | BMX ERRDMA | BMX ERRDS | BMX ERRIS |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | R/W-1 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-1 |
| | — | BMX WSDRM | — | — | — | BMXARB<2:0> | | |

| Legend: | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **BMXERRIXI:** Enable Bus Error from IXI bit
1 = Enable bus error exceptions for unmapped address accesses initiated from IXI shared bus
0 = Disable bus error exceptions for unmapped address accesses initiated from IXI shared bus

bit 19 **BMXERRICD:** Enable Bus Error from ICD Debug Unit bit
1 = Enable bus error exceptions for unmapped address accesses initiated from ICD
0 = Disable bus error exceptions for unmapped address accesses initiated from ICD

bit 18 **BMXERRDMA:** Bus Error from DMA bit
1 = Enable bus error exceptions for unmapped address accesses initiated from DMA
0 = Disable bus error exceptions for unmapped address accesses initiated from DMA

bit 17 **BMXERRDS:** Bus Error from CPU Data Access bit (disabled in Debug mode)
1 = Enable bus error exceptions for unmapped address accesses initiated from CPU data access
0 = Disable bus error exceptions for unmapped address accesses initiated from CPU data access

bit 16 **BMXERRIS:** Bus Error from CPU Instruction Access bit (disabled in Debug mode)
1 = Enable bus error exceptions for unmapped address accesses initiated from CPU instruction access
0 = Disable bus error exceptions for unmapped address accesses initiated from CPU instruction access

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **BMXWSDRM:** CPU Instruction or Data Access from Data RAM Wait State bit
1 = Data RAM accesses from CPU have one wait state for address setup
0 = Data RAM accesses from CPU have zero wait states for address setup

bit 5-3 **Unimplemented:** Read as '0'

bit 2-0 **BMXARB<2:0>:** Bus Matrix Arbitration Mode bits
111 = Reserved (using these configuration modes will produce undefined behavior)
•
•
•
011 = Reserved (using these configuration modes will produce undefined behavior)
010 = Arbitration Mode 2
001 = Arbitration Mode 1 (default)
000 = Arbitration Mode 0


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**REGISTER 4-2: BMXDKPBA: DATA RAM KERNEL PROGRAM BASE ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 |
| | BMXDKPBA<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | BMXDKPBA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDKPBA<15:10>:** DRM Kernel Program Base Address bits
When non-zero, this value selects the relative base address for kernel program space in RAM

bit 9-0 **BMXDKPBA<9:0>:** Read-Only bits
Value is always '0', which forces 1 KB increments

**Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernel mode data usage.

**2:** The value in this register must be less than or equal to BMXDRMSZ.

**REGISTER 4-3: BMXDUDBA: DATA RAM USER DATA BASE ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 |
| | BMXDUDBA<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | BMXDUDBA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDUDBA<15:10>:** DRM User Data Base Address bits

When non-zero, the value selects the relative base address for User mode data space in RAM, the value must be greater than BMXDKPBA.

bit 9-0 **BMXDUDBA<9:0>:** Read-Only bits

Value is always '0', which forces 1 KB increments

**Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernel mode data usage.

**2:** The value in this register must be less than or equal to BMXDRMSZ.


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**REGISTER 4-4: BMXDUPBA: DATA RAM USER PROGRAM BASE ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 |
| | BMXDUPBA<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | BMXDUPBA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDUPBA<15:10>:** DRM User Program Base Address bits

When non-zero, the value selects the relative base address for User mode program space in RAM, BMXDUPBA must be greater than BMXDUDBA.

bit 9-0 **BMXDUPBA<9:0>:** Read-Only bits

Value is always '0', which forces 1 KB increments

**Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernel mode data usage.

**2:** The value in this register must be less than or equal to BMXDRMSZ.

**REGISTER 4-5: BMXDRMSZ: DATA RAM SIZE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R | R | R | R | R | R | R | R |
| | BMXDRMSZ<31:24> | | | | | | | |
| 23:16 | R | R | R | R | R | R | R | R |
| | BMXDRMSZ<23:16> | | | | | | | |
| 15:8 | R | R | R | R | R | R | R | R |
| | BMXDRMSZ<15:8> | | | | | | | |
| 7:0 | R | R | R | R | R | R | R | R |
| | BMXDRMSZ<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **BMXDRMSZ<31:0>:** Data RAM Memory (DRM) Size bits
Static value that indicates the size of the Data RAM in bytes:
0x00002000 = Device has 8 KB RAM
0x00004000 = Device has 16 KB RAM
0x00008000 = Device has 32 KB RAM
0x00010000 = Device has 64 KB RAM

**REGISTER 4-6: BMXPUPBA: PROGRAM FLASH (PFM) USER PROGRAM BASE ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | BMXPUPBA<19:16> | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 | R-0 |
| | BMXPUPBA<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | BMXPUPBA<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-20 **Unimplemented:** Read as '0'

bit 19-11 **BMXPUPBA<19:11>:** Program Flash (PFM) User Program Base Address bits

bit 10-0 **BMXPUPBA<10:0>:** Read-Only bits
Value is always '0', which forces 2 KB increments

**Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernel mode data usage.
**2:** The value in this register must be less than or equal to BMXPFMSZ.


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**REGISTER 4-7: BMXPFMSZ: PROGRAM FLASH (PFM) SIZE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R | R | R | R | R | R | R | R |
| | BMXPFMSZ<31:24> | | | | | | | |
| 23:16 | R | R | R | R | R | R | R | R |
| | BMXPFMSZ<23:16> | | | | | | | |
| 15:8 | R | R | R | R | R | R | R | R |
| | BMXPFMSZ<15:8> | | | | | | | |
| 7:0 | R | R | R | R | R | R | R | R |
| | BMXPFMSZ<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **BMXPFMSZ<31:0>:** Program Flash Memory (PFM) Size bits
Static value that indicates the size of the PFM in bytes:
0x00010000 = Device has 64 KB Flash
0x00020000 = Device has 128 KB Flash
0x00040000 = Device has 256 KB Flash
0x00080000 = Device has 512 KB Flash

**REGISTER 4-8: BMXBOOTSZ: BOOT FLASH (IFM) SIZE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R | R | R | R | R | R | R | R |
| | BMXBOOTSZ<31:24> | | | | | | | |
| 23:16 | R | R | R | R | R | R | R | R |
| | BMXBOOTSZ<23:16> | | | | | | | |
| 15:8 | R | R | R | R | R | R | R | R |
| | BMXBOOTSZ<15:8> | | | | | | | |
| 7:0 | R | R | R | R | R | R | R | R |
| | BMXBOOTSZ<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **BMXBOOTSZ<31:0>:** Boot Flash Memory (BFM) Size bits
Static value that indicates the size of the Boot PFM in bytes:
0x00000C00 = Device has 3 KB Boot Flash

**NOTES:**


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## 5.0 INTERRUPT CONTROLLER

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Interrupt Controller"** (DS60001108) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX1XX/2XX/5XX 64/100-pin devices generate interrupt requests in response to interrupt events from peripheral modules. The interrupt control module exists externally to the CPU logic and prioritizes the interrupt events before presenting them to the CPU.

The PIC32MX1XX/2XX/5XX 64/100-pin interrupt module includes the following features:

- Up to 76 interrupt sources
- Up to 46 interrupt vectors
- Single and multi-vector mode operations
- Five external interrupts with edge polarity control
- Interrupt proximity timer
- Seven user-selectable priority levels for each vector
- Four user-selectable subpriority levels within each priority
- Software can generate any interrupt
- User-configurable interrupt vector table location
- User-configurable interrupt vector spacing

**Note:** The dedicated shadow register set is not available on these devices.

**FIGURE 5-1: INTERRUPT CONTROLLER MODULE BLOCK DIAGRAM**

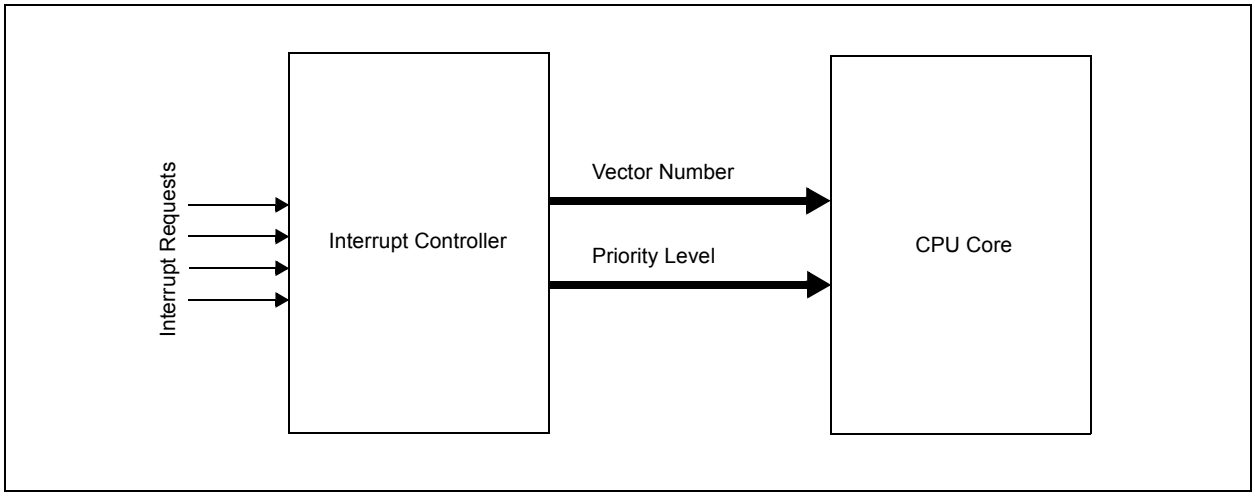

**TABLE 5-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION**

| Interrupt Source(1) | IRQ # | Vector # | Interrupt Bit Location | | | | Persistent Interrupt |
|---|---|---|---|---|---|---|---|
| | | | Flag | Enable | Priority | Sub-priority | |
| Highest Natural Order Priority | | | | | | | |
| CT – Core Timer Interrupt | 0 | 0 | IFS0<0> | IEC0<0> | IPC0<4:2> | IPC0<1:0> | No |
| CS0 – Core Software Interrupt 0 | 1 | 1 | IFS0<1> | IEC0<1> | IPC0<12:10> | IPC0<9:8> | No |
| CS1 – Core Software Interrupt 1 | 2 | 2 | IFS0<2> | IEC0<2> | IPC0<20:18> | IPC0<17:16> | No |
| INT0 – External Interrupt | 3 | 3 | IFS0<3> | IEC0<3> | IPC0<28:26> | IPC0<25:24> | No |
| T1 – Timer1 | 4 | 4 | IFS0<4> | IEC0<4> | IPC1<4:2> | IPC1<1:0> | No |
| IC1E – Input Capture 1 Error | 5 | 5 | IFS0<5> | IEC0<5> | IPC1<12:10> | IPC1<9:8> | Yes |
| IC1 – Input Capture 1 | 6 | 5 | IFS0<6> | IEC0<6> | IPC1<12:10> | IPC1<9:8> | Yes |
| OC1 – Output Compare 1 | 7 | 6 | IFS0<7> | IEC0<7> | IPC1<20:18> | IPC1<17:16> | No |
| INT1 – External Interrupt 1 | 8 | 7 | IFS0<8> | IEC0<8> | IPC1<28:26> | IPC1<25:24> | No |
| T2 – Timer2 | 9 | 8 | IFS0<9> | IEC0<9> | IPC2<4:2> | IPC2<1:0> | No |
| IC2E – Input Capture 2 | 10 | 9 | IFS0<10> | IEC0<10> | IPC2<12:10> | IPC2<9:8> | Yes |
| IC2 – Input Capture 2 | 11 | 9 | IFS0<11> | IEC0<11> | IPC2<12:10> | IPC2<9:8> | Yes |
| OC2 – Output Compare 2 | 12 | 10 | IFS0<12> | IEC0<12> | IPC2<20:18> | IPC2<17:16> | No |
| INT2 – External Interrupt 2 | 13 | 11 | IFS0<13> | IEC0<13> | IPC2<28:26> | IPC2<25:24> | No |
| T3 – Timer3 | 14 | 12 | IFS0<14> | IEC0<14> | IPC3<4:2> | IPC3<1:0> | No |
| IC3E – Input Capture 3 | 15 | 13 | IFS0<15> | IEC0<15> | IPC3<12:10> | IPC3<9:8> | Yes |
| IC3 – Input Capture 3 | 16 | 13 | IFS0<16> | IEC0<16> | IPC3<12:10> | IPC3<9:8> | Yes |
| OC3 – Output Compare 3 | 17 | 14 | IFS0<17> | IEC0<17> | IPC3<20:18> | IPC3<17:16> | No |
| INT3 – External Interrupt 3 | 18 | 15 | IFS0<18> | IEC0<18> | IPC3<28:26> | IPC3<25:24> | No |
| T4 – Timer4 | 19 | 16 | IFS0<19> | IEC0<19> | IPC4<4:2> | IPC4<1:0> | No |
| IC4E – Input Capture 4 Error | 20 | 17 | IFS0<20> | IEC0<20> | IPC4<12:10> | IPC4<9:8> | Yes |
| IC4 – Input Capture 4 | 21 | 17 | IFS0<21> | IEC0<21> | IPC4<12:10> | IPC4<9:8> | Yes |
| OC4 – Output Compare 4 | 22 | 18 | IFS0<22> | IEC0<22> | IPC4<20:18> | IPC4<17:16> | No |
| INT4 – External Interrupt 4 | 23 | 19 | IFS0<23> | IEC0<23> | IPC4<28:26> | IPC4<25:24> | No |
| T5 – Timer5 | 24 | 20 | IFS0<24> | IEC0<24> | IPC5<4:2> | IPC5<1:0> | No |
| IC5E – Input Capture 5 Error | 25 | 21 | IFS0<25> | IEC0<25> | IPC5<12:10> | IPC5<9:8> | Yes |
| IC5 – Input Capture 5 | 26 | 21 | IFS0<26> | IEC0<26> | IPC5<12:10> | IPC5<9:8> | Yes |
| OC5 – Output Compare 5 | 27 | 22 | IFS0<27> | IEC0<27> | IPC5<20:18> | IPC5<17:16> | No |
| AD1 – ADC1 Convert done | 28 | 23 | IFS0<28> | IEC0<28> | IPC5<28:26> | IPC5<25:24> | Yes |
| FSCM – Fail-Safe Clock Monitor | 29 | 24 | IFS0<29> | IEC0<29> | IPC6<4:2> | IPC6<1:0> | No |
| RTCC – Real-Time Clock and Calendar | 30 | 25 | IFS0<30> | IEC0<30> | IPC6<12:10> | IPC6<9:8> | No |
| FCE – Flash Control Event | 31 | 26 | IFS0<31> | IEC0<31> | IPC6<20:18> | IPC6<17:16> | No |
| CMP1 – Comparator Interrupt | 32 | 27 | IFS1<0> | IEC1<0> | IPC6<28:26> | IPC6<25:24> | No |
| CMP2 – Comparator Interrupt | 33 | 28 | IFS1<1> | IEC1<1> | IPC7<4:2> | IPC7<1:0> | No |
| USB – USB Interrupts | 34 | 29 | IFS1<2> | IEC1<2> | IPC7<12:10> | IPC7<9:8> | Yes |
| SPI1E – SPI1 Fault | 35 | 30 | IFS1<3> | IEC1<3> | IPC7<20:18> | IPC7<17:16> | Yes |
| SPI1RX – SPI1 Receive Done | 36 | 30 | IFS1<4> | IEC1<4> | IPC7<20:18> | IPC7<17:16> | Yes |
| SPI1TX – SPI1 Transfer Done | 37 | 30 | IFS1<5> | IEC1<5> | IPC7<20:18> | IPC7<17:16> | Yes |
| U1E – UART1 Fault | 38 | 31 | IFS1<6> | IEC1<6> | IPC7<28:26> | IPC7<25:24> | Yes |
| U1RX – UART1 Receive Done | 39 | 31 | IFS1<7> | IEC1<7> | IPC7<28:26> | IPC7<25:24> | Yes |
| U1TX – UART1 Transfer Done | 40 | 31 | IFS1<8> | IEC1<8> | IPC7<28:26> | IPC7<25:24> | Yes |
| I2C1B – I2C1 Bus Collision Event | 41 | 32 | IFS1<9> | IEC1<9> | IPC8<4:2> | IPC8<1:0> | Yes |
| I2C1S – I2C1 Slave Event | 42 | 32 | IFS1<10> | IEC1<10> | IPC8<4:2> | IPC8<1:0> | Yes |
| I2C1M – I2C1 Master Event | 43 | 32 | IFS1<11> | IEC1<11> | IPC8<4:2> | IPC8<1:0> | Yes |

**Note 1:** Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MX1XX/2XX/5XX 64/100-pin Controller Family Features"** for the list of available peripherals.

**2:** This interrupt source is not available on 64-pin devices.


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**TABLE 5-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)**

| Interrupt Source[1] | IRQ # | Vector # | Interrupt Bit Location | | | | Persistent Interrupt |
|---|---|---|---|---|---|---|---|
| | | | Flag | Enable | Priority | Sub-priority | |
| CNA – PORTA Input Change Interrupt | 44 | 33 | IFS1<12> | IEC1<12> | IPC8<12:10> | IPC8<9:8> | Yes |
| CNB – PORTB Input Change Interrupt | 45 | 33 | IFS1<13> | IEC1<13> | IPC8<12:10> | IPC8<9:8> | Yes |
| CNC – PORTC Input Change Interrupt | 46 | 33 | IFS1<14> | IEC1<14> | IPC8<12:10> | IPC8<9:8> | Yes |
| CND – PORTD Input Change Interrupt | 47 | 33 | IFS1<15> | IEC1<15> | IPC8<12:10> | IPC8<9:8> | Yes |
| CNE – PORTE Input Change Interrupt | 48 | 33 | IFS1<16> | IEC1<16> | IPC8<12:10> | IPC8<9:8> | Yes |
| CNF – PORTF Input Change Interrupt | 49 | 33 | IFS1<17> | IEC1<17> | IPC8<12:10> | IPC8<9:8> | Yes |
| CNG – PORTG Input Change Interrupt | 50 | 33 | IFS1<18> | IEC1<18> | IPC8<12:10> | IPC8<9:8> | Yes |
| PMP – Parallel Master Port | 51 | 34 | IFS1<19> | IEC1<19> | IPC8<20:18> | IPC8<17:16> | Yes |
| PMPE – Parallel Master Port Error | 52 | 34 | IFS1<20> | IEC1<20> | IPC8<20:18> | IPC8<17:16> | Yes |
| SPI2E – SPI2 Fault | 53 | 35 | IFS1<21> | IEC1<21> | IPC8<28:26> | IPC8<25:24> | Yes |
| SPI2RX – SPI2 Receive Done | 54 | 35 | IFS1<22> | IEC1<22> | IPC8<28:26> | IPC8<25:24> | Yes |
| SPI2TX – SPI2 Transfer Done | 55 | 35 | IFS1<23> | IEC1<23> | IPC8<28:26> | IPC8<25:24> | Yes |
| U2E – UART2 Error | 56 | 36 | IFS1<24> | IEC1<24> | IPC9<4:2> | IPC9<1:0> | Yes |
| U2RX – UART2 Receiver | 57 | 36 | IFS1<25> | IEC1<25> | IPC9<4:2> | IPC9<1:0> | Yes |
| U2TX – UART2 Transmitter | 58 | 36 | IFS1<26> | IEC1<26> | IPC9<4:2> | IPC9<1:0> | Yes |
| I2C2B – I2C2 Bus Collision Event | 59 | 37 | IFS1<27> | IEC1<27> | IPC9<12:10> | IPC9<9:8> | Yes |
| I2C2S – I2C2 Slave Event | 60 | 37 | IFS1<28> | IEC1<28> | IPC9<12:10> | IPC9<9:8> | Yes |
| I2C2M – I2C2 Master Event | 61 | 37 | IFS1<29> | IEC1<29> | IPC9<12:10> | IPC9<9:8> | Yes |
| U3E – UART3 Error | 62 | 38 | IFS1<30> | IEC1<30> | IPC9<20:18> | IPC9<17:16> | Yes |
| U3RX – UART3 Receiver | 63 | 38 | IFS1<31> | IEC1<31> | IPC9<20:18> | IPC9<17:16> | Yes |
| U3TX – UART3 Transmitter | 64 | 38 | IFS2<0> | IEC2<0> | IPC9<20:18> | IPC9<17:16> | Yes |
| U4E – UART4 Error | 65 | 39 | IFS2<1> | IEC2<1> | IPC9<28:26> | IPC9<25:24> | Yes |
| U4RX – UART4 Receiver | 66 | 39 | IFS2<2> | IEC2<2> | IPC9<28:26> | IPC9<25:24> | Yes |
| U4TX – UART4 Transmitter | 67 | 39 | IFS2<3> | IEC2<3> | IPC9<28:26> | IPC9<25:24> | Yes |
| U5E – UART5 Error[2] | 68 | 40 | IFS2<4> | IEC2<4> | IPC10<4:2> | IPC10<1:0> | Yes |
| U5RX – UART5 Receiver[2] | 69 | 40 | IFS2<5> | IEC2<5> | IPC10<4:2> | IPC10<1:0> | Yes |
| U5TX – UART5 Transmitter[2] | 70 | 40 | IFS2<6> | IEC2<6> | IPC10<4:2> | IPC10<1:0> | Yes |
| CTMU – CTMU Event[2] | 71 | 41 | IFS2<7> | IEC2<7> | IPC10<12:10> | IPC10<9:8> | Yes |
| DMA0 – DMA Channel 0 | 72 | 42 | IFS2<8> | IEC2<8> | IPC10<20:18> | IPC10<17:16> | No |
| DMA1 – DMA Channel 1 | 73 | 43 | IFS2<9> | IEC2<9> | IPC10<28:26> | IPC10<25:24> | No |
| DMA2 – DMA Channel 2 | 74 | 44 | IFS2<10> | IEC2<10> | IPC11<4:2> | IPC11<1:0> | No |
| DMA3 – DMA Channel 3 | 75 | 45 | IFS2<11> | IEC2<11> | IPC11<12:10> | IPC11<9:8> | No |
| CMP3 – Comparator 3 Interrupt | 76 | 46 | IFS2<12> | IEC2<12> | IPC11<20:18> | IPC11<17:16> | No |
| CAN1 – CAN1 Event | 77 | 47 | IFS2<13> | IEC2<13> | IPC11<28:26> | IPC11<25:24> | Yes |
| SPI3E – SPI3 Fault | 78 | 48 | IFS2<14> | IEC2<14> | IPC12<4:2> | IPC12<1:0> | Yes |
| SPI3RX – SPI3 Receive Done | 79 | 48 | IFS2<15> | IEC2<15> | IPC12<4:2> | IPC12<1:0> | Yes |
| SPI3TX – SPI3 Transfer Done | 80 | 48 | IFS2<16> | IEC2<16> | IPC12<4:2> | IPC12<1:0> | Yes |
| SPI4E – SPI4 Fault[2] | 81 | 49 | IFS2<17> | IEC2<17> | IPC12<12:10> | IPC12<9:8> | Yes |
| SPI4RX – SPI4 Receive Done[2] | 82 | 49 | IFS2<18> | IEC2<18> | IPC12<12:10> | IPC12<9:8> | Yes |
| SPI4TX – SPI4 Transfer Done[2] | 83 | 49 | IFS2<19> | IEC2<19> | IPC12<12:10> | IPC12<9:8> | Yes |
| Lowest Natural Order Priority | | | | | | | |

**Note 1:** Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MX1XX/2XX/5XX 64/100-pin Controller Family Features"** for the list of available peripherals.

**2:** This interrupt source is not available on 64-pin devices.

## 5.1 Interrupts Control Registers

### TABLE 5-2: INTERRUPT REGISTER MAP

| Virtual Address (BF88_#) | Register Name(3) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 1000 | INTCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | MVEC | — | TPC<2:0> | | | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 0000 |
| 1010 | INTSTAT(4) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | SRIPL<2:0> | | | — | — | VEC<5:0> | | | | | | 0000 |
| 1020 | IPTMR | 31:16 | IPTMR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 1030 | IFS0 | 31:16 | FCEIF | RTCCIF | FSCMIF | AD1IF | OC5IF | IC5IF | IC5EIF | T5IF | INT4IF | OC4IF | IC4IF | IC4EIF | T4IF | INT3IF | OC3IF | IC3IF | 0000 |
| | | 15:0 | IC3EIF | T3IF | INT2IF | OC2IF | IC2IF | IC2EIF | T2IF | INT1IF | OC1IF | IC1IF | IC1EIF | T1IF | INT0IF | CS1IF | CS0IF | CTIF | 0000 |
| 1040 | IFS1 | 31:16 | U3RXIF | U3EIF | I2C2MIF | I2C2SIF | I2C2BIF | U2TXIF | U2RXIF | U2EIF | SPI2TXIF | SPI2RXIF | SPI2EIF | PMPEIF | PMPIF | CNGIF | CNFIF | CNEIF | 0000 |
| | | 15:0 | CNDIF | CNCIF | CNBIF | CNAIF | I2C1MIF | I2C1SIF | I2C1BIF | U1TXIF | U1RXIF | U1EIF | SPI1TXIF | SPI1RXIF | SPI1EIF | USBIF(2) | CMP2IF | CMP1IF | 0000 |
| 1050 | IFS2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | SPI4TXIF(1) | SPI4RXIF(1) | SPI4EIF(1) | SPI3TXIF | 0000 |
| | | 15:0 | SPI3RXIF | SPI3EIF | CANIF | CMP3IF | DMA3IF | DMA2IF | DMA1IF | DMA0IF | CTMUIF | U5TXIF(1) | U5RXIF(1) | U5EIF(1) | U4TXIF | U4RXIF | U4EIF | U3TXIF | 0000 |
| 1060 | IEC0 | 31:16 | FCEIE | RTCCIE | FSCMIE | AD1IE | OC5IE | IC5IE | IC5EIE | T5IE | INT4IE | OC4IE | IC4IE | IC4EIE | T4IE | INT3IE | OC3IE | IC3IE | 0000 |
| | | 15:0 | IC3EIE | T3IE | INT2IE | OC2IE | IC2IE | IC2EIE | T2IE | INT1IE | OC1IE | IC1IE | IC1EIE | T1IE | INT0IE | CS1IE | CS0IE | CTIE | 0000 |
| 1070 | IEC1 | 31:16 | U3RXIE | U3EIE | I2C2MIE | I2C2SIE | I2C2BIE | U2TXIE | U2RXIE | U2EIE | SPI2TXIE | SPI2RXIE | SPI2EIE | PMPEIE | PMPIE | CNGIE | CNFIE | CNEIE | 0000 |
| | | 15:0 | CNDIE | CNCIE | CNBIE | CNAIE | I2C1MIE | I2C1SIE | I2C1BIE | U1TXIE | U1RXIE | U1EIE | SPI1TXIE | SPI1RXIE | SPI1EIE | USBIE(2) | CMP2IE | CMP1IE | 0000 |
| 1080 | IEC2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | DMA3IE | DMA2IE | DMA1IE | DMA0IE | CTMUIE | U5TXIE(1) | U5RXIE(1) | U5EIE(1) | U4TXIE | U4RXIE | U4EIE | U3TXIE | 0000 |
| 1090 | IPC0 | 31:16 | — | — | — | INT0IP<2:0> | | | INT0IS<1:0> | | — | — | — | CS1IP<2:0> | | | CS1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CS0IP<2:0> | | | CS0IS<1:0> | | — | — | — | CTIP<2:0> | | | CTIS<1:0> | | 0000 |
| 10A0 | IPC1 | 31:16 | — | — | — | INT1IP<2:0> | | | INT1IS<1:0> | | — | — | — | OC1IP<2:0> | | | OC1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC1IP<2:0> | | | IC1IS<1:0> | | — | — | — | T1IP<2:0> | | | T1IS<1:0> | | 0000 |
| 10B0 | IPC2 | 31:16 | — | — | — | INT2IP<2:0> | | | INT2IS<1:0> | | — | — | — | OC2IP<2:0> | | | OC2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC2IP<2:0> | | | IC2IS<1:0> | | — | — | — | T2IP<2:0> | | | T2IS<1:0> | | 0000 |
| 10C0 | IPC3 | 31:16 | — | — | — | INT3IP<2:0> | | | INT3IS<1:0> | | — | — | — | OC3IP<2:0> | | | OC3IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC3IP<2:0> | | | IC3IS<1:0> | | — | — | — | T3IP<2:0> | | | T3IS<1:0> | | 0000 |
| 10D0 | IPC4 | 31:16 | — | — | — | INT4IP<2:0> | | | INT4IS<1:0> | | — | — | — | OC4IP<2:0> | | | OC4IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC4IP<2:0> | | | IC4IS<1:0> | | — | — | — | T4IP<2:0> | | | T4IS<1:0> | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This bit is only available on 100-pin devices.

**2:** This bit is only implemented on devices with a USB module.

**3:** With the exception of those noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

**4:** This register does not have associated CLR, SET, and INV registers.

**5:** This bit is only implemented on devices with a CAN module.



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**TABLE 5-2: INTERRUPT REGISTER MAP (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(3) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 10E0 | IPC5 | 31:16 | — | — | — | AD1IP<2:0> | | | AD1IS<1:0> | | — | — | — | OC5IP<2:0> | | | OC5IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC5IP<2:0> | | | IC5IS<1:0> | | — | — | — | T5IP<2:0> | | | T5IS<1:0> | | 0000 |
| 10F0 | IPC6 | 31:16 | — | — | — | CMP1IP<2:0> | | | CMP1IS<1:0> | | — | — | — | FCEIP<2:0> | | | FCEIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | RTCCIP<2:0> | | | RTCCIS<1:0> | | — | — | — | FSCMIP<2:0> | | | FSCMIS<1:0> | | 0000 |
| 1100 | IPC7 | 31:16 | — | — | — | U1IP<2:0> | | | U1IS<1:0> | | — | — | — | SPI1IP<2:0> | | | SPI1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | USBIP<2:0>(2) | | | USBIS<1:0>(2) | | — | — | — | CMP2IP<2:0> | | | CMP2IS<1:0> | | 0000 |
| 1110 | IPC8 | 31:16 | — | — | — | SPI2IP<2:0> | | | SPI2IS<1:0> | | — | — | — | PMPIP<2:0> | | | PMPIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CNIP<2:0> | | | CNIS<1:0> | | — | — | — | I2C1IP<2:0> | | | I2C1IS<1:0> | | 0000 |
| 1120 | IPC9 | 31:16 | — | — | — | U4IP<2:0> | | | U4IS<1:0> | | — | — | — | U3IP<2:0> | | | U3IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | I2C2IP<2:0> | | | I2C2IS<1:0> | | — | — | — | U2IP<2:0> | | | U2IS<1:0> | | 0000 |
| 1130 | IPC10 | 31:16 | — | — | — | DMA1IP<2:0> | | | DMA1IS<1:0> | | — | — | — | DMA0IP<2:0> | | | DMA0IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CTMUIP<2:0> | | | CTMUIS<1:0> | | — | — | — | U5IP<2:0> | | | U5IS<1:0> | | 0000 |
| 1140 | IPC11 | 31:16 | — | — | — | CANIP<2:0>(5) | | | CANIS<1:0>(5) | | — | — | — | CMP3IP<2:0> | | | CMP3IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | DMA3IP<2:0> | | | DMA3IS<1:0> | | — | — | — | DMA2IP<2:0> | | | DMA2IS<1:0> | | 0000 |
| 1150 | IPC12 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | SPI4P<2:0>(1) | | | SPI4S<1:0>(1) | | — | — | — | SPI3P<2:0> | | | SPI3S<1:0> | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This bit is only available on 100-pin devices.

**2:** This bit is only implemented on devices with a USB module.

**3:** With the exception of those noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

**4:** This register does not have associated CLR, SET, and INV registers.

**5:** This bit is only implemented on devices with a CAN module.

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**REGISTER 5-1: INTCON: INTERRUPT CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | MVEC | — | TPC<2:0> | | |
| 7:0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-13 **Unimplemented:** Read as '0'

bit 12 **MVEC:** Multi Vector Configuration bit
- 1 = Interrupt controller configured for multi vectored mode
- 0 = Interrupt controller configured for single vectored mode

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **TPC<2:0>:** Interrupt Proximity Timer Control bits
- 111 = Interrupts of group priority 7 or lower start the Interrupt Proximity timer
- 110 = Interrupts of group priority 6 or lower start the Interrupt Proximity timer
- 101 = Interrupts of group priority 5 or lower start the Interrupt Proximity timer
- 100 = Interrupts of group priority 4 or lower start the Interrupt Proximity timer
- 011 = Interrupts of group priority 3 or lower start the Interrupt Proximity timer
- 010 = Interrupts of group priority 2 or lower start the Interrupt Proximity timer
- 001 = Interrupts of group priority 1 start the Interrupt Proximity timer
- 000 = Disables Interrupt Proximity timer

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **INT4EP:** External Interrupt 4 Edge Polarity Control bit
- 1 = Rising edge
- 0 = Falling edge

bit 3 **INT3EP:** External Interrupt 3 Edge Polarity Control bit
- 1 = Rising edge
- 0 = Falling edge

bit 2 **INT2EP:** External Interrupt 2 Edge Polarity Control bit
- 1 = Rising edge
- 0 = Falling edge

bit 1 **INT1EP:** External Interrupt 1 Edge Polarity Control bit
- 1 = Rising edge
- 0 = Falling edge

bit 0 **INT0EP:** External Interrupt 0 Edge Polarity Control bit
- 1 = Rising edge
- 0 = Falling edge


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**REGISTER 5-2: INTSTAT: INTERRUPT STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | SRIPL<2:0>(1) | | |
| 7:0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | VEC<5:0>(1) | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-11 **Unimplemented:** Read as '0'

bit 10-8 **SRIPL<2:0>:** Requested Priority Level bits(1)

111-000 = The priority level of the latest interrupt presented to the CPU

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **VEC<5:0>:** Interrupt Vector bits(1)

11111-00000 = The interrupt vector that is presented to the CPU

**Note 1:** This value should only be used when the interrupt controller is configured for Single Vector mode.

**REGISTER 5-3: IPTMR: INTERRUPT PROXIMITY TIMER REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IPTMR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IPTMR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IPTMR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IPTMR<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **IPTMR<31:0>:** Interrupt Proximity Timer Reload bits
Used by the Interrupt Proximity Timer as a reload value when the Interrupt Proximity timer is triggered by an interrupt event.

**REGISTER 5-4: IFSx: INTERRUPT FLAG STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IFS31 | IFS30 | IFS29 | IFS28 | IFS27 | IFS26 | IFS25 | IFS24 |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IFS23 | IFS22 | IFS21 | IFS20 | IFS19 | IFS18 | IFS17 | IFS16 |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IFS15 | IFS14 | IFS13 | IFS12 | IFS11 | IFS10 | IFS9 | IFS8 |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IFS7 | IFS6 | IFS5 | IFS4 | IFS3 | IFS2 | IFS1 | IFS0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **IFS31-IFS0:** Interrupt Flag Status bits
1 = Interrupt request has occurred
0 = No interrupt request has occurred

**Note:** This register represents a generic definition of the IFSx register. Refer to Table 5-1 for the exact bit definitions.

**REGISTER 5-5: IECx: INTERRUPT ENABLE CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IEC31 | IEC30 | IEC29 | IEC28 | IEC27 | IEC26 | IEC25 | IEC24 |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IEC23 | IEC22 | IEC21 | IEC20 | IEC19 | IEC18 | IEC17 | IEC16 |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IEC15 | IEC14 | IEC13 | IEC12 | IEC11 | IEC10 | IEC9 | IEC8 |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IEC7 | IEC6 | IEC5 | IEC4 | IEC3 | IEC2 | IEC1 | IEC0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **IEC31-IEC0:** Interrupt Enable bits
1 = Interrupt is enabled
0 = Interrupt is disabled

**Note:** This register represents a generic definition of the IECx register. Refer to Table 5-1 for the exact bit definitions.


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**REGISTER 5-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP3<2:0> | | | IS3<1:0> | |
| 23:16 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP2<2:0> | | | IS2<1:0> | |
| 15:8 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP1<2:0> | | | IS1<1:0> | |
| 7:0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP0<2:0> | | | IS0<1:0> | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP3<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP2<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 17-16 **IS2<1:0>:** Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

bit 12-10 **IP1<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

**Note:** This register represents a generic definition of the IPCx register. Refer to Table 5-1 for the exact bit definitions.

**REGISTER 5-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER (CONTINUED)**

bit 9-8 **IS1<1:0>:** Interrupt Subpriority bits
11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-2 **IP0<2:0>:** Interrupt Priority bits
111 = Interrupt priority is 7
•
•
•
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 1-0 **IS0<1:0>:** Interrupt Subpriority bits
11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0

| **Note:** | This register represents a generic definition of the IPCx register. Refer to Table 5-1 for the exact bit definitions. |
|---|---|


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## 6.0 FLASH PROGRAM MEMORY

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. "Flash Program Memory"** (DS60001121) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX1XX/2XX/5XX 64/100-pin devices contain an internal Flash program memory for executing user code. There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming™ (ICSP™)

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is available in **Section 5. "Flash Program Memory"** (DS60001121) in the *"PIC32 Family Reference Manual".*

EJTAG is performed using the EJTAG port of the device and an EJTAG capable programmer.

ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP.

The EJTAG and ICSP methods are described in the "*PIC32 Flash Programming Specification*" (DS60001145), which can be downloaded from the Microchip web site.

**Note:** On PIC32MX1XX/2XX/5XX 64/100-pin devices, the Flash page size is 1 KB and the row size is 128 bytes (256 IW and 32 IW, respectively).

## 6.1 Control Registers

**TABLE 6-1: FLASH CONTROLLER REGISTER MAP**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| F400 | NVMCON(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | WR | WREN | WRERR | LVDERR | LVDSTAT | — | — | — | — | — | — | — | NVMOP<3:0> | | | | 0000 |
| F410 | NVMKEY | 31:16 | NVMKEY<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| F420 | NVMADDR(1) | 31:16 | NVMADDR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| F430 | NVMDATA | 31:16 | NVMDATA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| F440 | NVMSRC ADDR | 31:16 | NVMSRCADDR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.



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**REGISTER 6-1: NVMCON: PROGRAMMING CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R-0 | R-0 | R-0 | U-0 | U-0 | U-0 |
| | WR | WREN(1) | WRERR(2) | LVDERR(2) | LVDSTAT(2) | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | NVMOP<3:0> | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **WR:** Write Control bit
This bit is writable when WREN = 1 and the unlock sequence is followed.
1 = Initiate a Flash operation. Hardware clears this bit when the operation completes
0 = Flash operation complete or inactive

bit 14 **WREN:** Write Enable bit(1)
1 = Enable writes to WR bit and enables LVD circuit
0 = Disable writes to WR bit and disables LVD circuit
This is the only bit in this register reset by a device Reset.

bit 13 **WRERR:** Write Error bit(2)
This bit is read-only and is automatically set by hardware.
1 = Program or erase sequence did not complete successfully
0 = Program or erase sequence completed normally

bit 12 **LVDERR:** Low-Voltage Detect Error bit (LVD circuit must be enabled)(2)
This bit is read-only and is automatically set by hardware.
1 = Low-voltage detected (possible data corruption, if WRERR is set)
0 = Voltage level is acceptable for programming

bit 11 **LVDSTAT:** Low-Voltage Detect Status bit (LVD circuit must be enabled)(2)
This bit is read-only and is automatically set, and cleared, by hardware.
1 = Low-voltage event active
0 = Low-voltage event NOT active

bit 10-4 **Unimplemented:** Read as '0'

bit 3-0 **NVMOP<3:0>:** NVM Operation bits
These bits are writable when WREN = 0.
1111 =Reserved
•
•
•
0111 = Reserved
0110 =No operation
0101 =Program Flash (PFM) erase operation: erases PFM, if all pages are not write-protected
0100 =Page erase operation: erases page selected by NVMADDR, if it is not write-protected
0011 =Row program operation: programs row selected by NVMADDR, if it is not write-protected
0010 =No operation
0001 =Word program operation: programs word selected by NVMADDR, if it is not write-protected
0000 = No operation

**Note 1:** This bit is cleared by any reset (i.e., POR, BOR, WDT, $\overline{\text{MCLR}}$, SWR).

**2:** This bit is only cleared by setting NVMOP = 0000, and initiating a Flash WR operation or a POR. Any other kind of reset (i.e., BOR, WDT, $\overline{\text{MCLR}}$) does not clear this bit.

**REGISTER 6-2: NVMKEY: PROGRAMMING UNLOCK REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| | NVMKEY<31:24> | | | | | | | |
| 23:16 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| | NVMKEY<23:16> | | | | | | | |
| 15:8 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| | NVMKEY<15:8> | | | | | | | |
| 7:0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| | NVMKEY<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **NVMKEY<31:0>:** Unlock Register bits
These bits are write-only, and read as '0' on any read.

**Note:** This register is used as part of the unlock sequence to prevent inadvertent writes to the PFM.

**REGISTER 6-3: NVMADDR: FLASH ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMADDR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMADDR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMADDR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMADDR<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **NVMADDR<31:0>:** Flash Address bits
Bulk/Chip/PFM Erase: Address is ignored
Page Erase: Address identifies the page to erase
Row Program: Address identifies the row to program
Word Program: Address identifies the word to program


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**REGISTER 6-4: NVMDATA: FLASH PROGRAM DATA REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMDATA<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMDATA<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMDATA<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMDATA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **NVMDATA<31:0>:** Flash Programming Data bits

**Note:** The bits in this register are only reset by a Power-on Reset (POR).

**REGISTER 6-5: NVMSRCADDR: SOURCE DATA ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMSRCADDR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMSRCADDR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMSRCADDR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMSRCADDR<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **NVMSRCADDR<31:0>:** Source Data Address bits

The system physical address of the data to be programmed into the Flash when the NVMOP<3:0> bits (NVMCON<3:0>) are set to perform row programming.

**NOTES:**


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## 7.0 RESETS

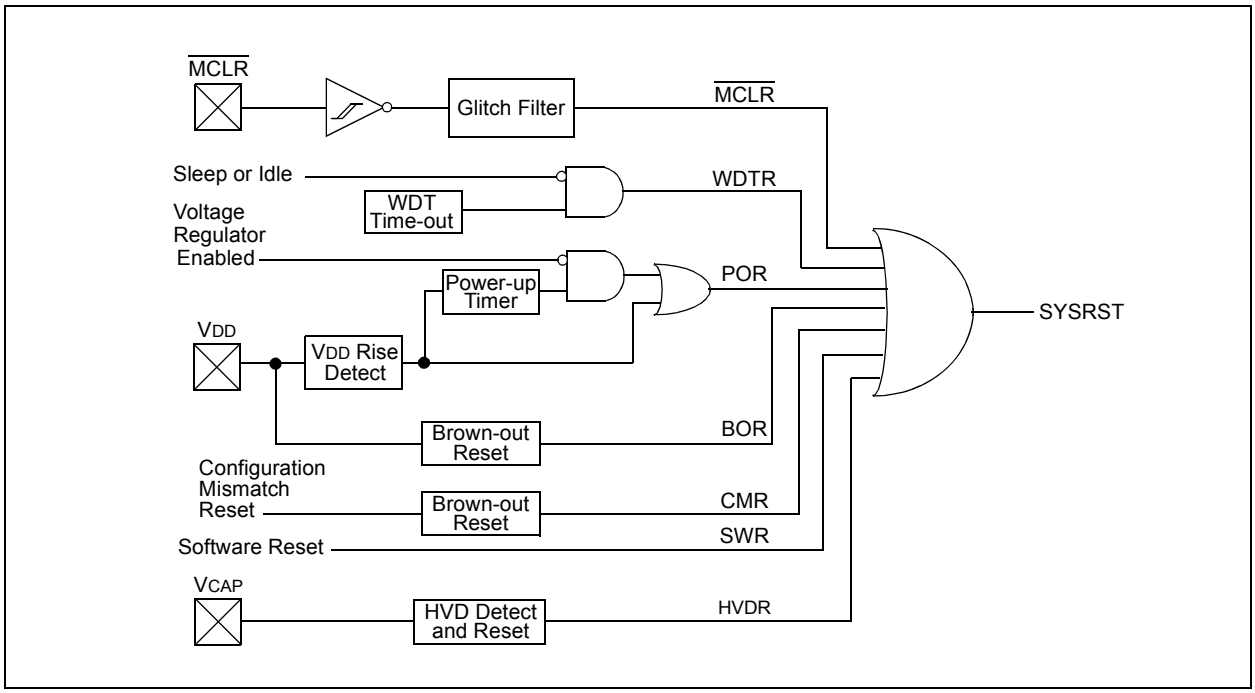
**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. "Resets"** (DS60001118) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The following is a list of device Reset sources:

- POR: Power-on Reset
- $\overline{\text{MCLR}}$: Master Clear Reset pin
- SWR: Software Reset
- WDTR: Watchdog Timer Reset
- BOR: Brown-out Reset
- CMR: Configuration Mismatch Reset
- HVDR: High Voltage Detect Reset

A simplified block diagram of the Reset module is illustrated in Figure 7-1.

**FIGURE 7-1: SYSTEM RESET BLOCK DIAGRAM**



## 7.1 Control Registers

**TABLE 7-1: RESET SFR SUMMARY**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| F600 | RCON | 31:16 | — | — | HVDR | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CMR | VREGS | EXTR | SWR | — | WDTO | SLEEP | IDLE | BOR | POR | xxxx(1) |
| F610 | RSWRST | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SWRST | 0000 |

**Legend:** — = unimplemented, read as '0'. Address offset values are shown in hexadecimal.

**Note 1:** The Reset value is dependent on the DEVCFGx Configuration bits and the type of reset.



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**REGISTER 7-1: RCON: RESET CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | R/W-0, HS | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | HVDR | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0, HS | R/W-0 |
| | — | — | — | — | — | — | CMR | VREGS |
| 7:0 | R/W-0, HS | R/W-0, HS | U-0 | R/W-0, HS | R/W-0, HS | R/W-0, HS | R/W-1, HS | R/W-1, HS |
| | EXTR | SWR | — | WDTO | SLEEP | IDLE | BOR(1) | POR(1) |

| Legend: | HS = Set by hardware | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-30 **Unimplemented:** Read as '0'

bit 29 **HVDR:** High Voltage Detect Reset Flag bit
- 1 = High Voltage Detect (HVD) Reset has occurred, voltage on VCAP > 2.5V
- 0 = HVD Reset has not occurred

bit 28-10 **Unimplemented:** Read as '0'

bit 9 **CMR:** Configuration Mismatch Reset Flag bit
- 1 = Configuration mismatch Reset has occurred
- 0 = Configuration mismatch Reset has not occurred

bit 8 **VREGS:** Voltage Regulator Standby Enable bit
- 1 = Regulator is enabled and is on during Sleep mode
- 0 = Regulator is disabled and is off during Sleep mode

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin Flag bit
- 1 = Master Clear (pin) Reset has occurred
- 0 = Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset Flag bit
- 1 = Software Reset was executed
- 0 = Software Reset as not executed

bit 5 **Unimplemented:** Read as '0'

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
- 1 = WDT Time-out has occurred
- 0 = WDT Time-out has not occurred

bit 3 **SLEEP:** Wake From Sleep Flag bit
- 1 = Device was in Sleep mode
- 0 = Device was not in Sleep mode

bit 2 **IDLE:** Wake From Idle Flag bit
- 1 = Device was in Idle mode
- 0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit(1)
- 1 = Brown-out Reset has occurred
- 0 = Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit(1)
- 1 = Power-on Reset has occurred
- 0 = Power-on Reset has not occurred

**Note 1:** User software must clear this bit to view next detection.

**REGISTER 7-2: RSWRST: SOFTWARE RESET REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | W-0, HC |
| | — | — | — | — | — | — | — | SWRST(1) |

| Legend: | HC = Cleared by hardware | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **SWRST:** Software Reset Trigger bit(1)
- 1 = Enable software Reset event
- 0 = No effect

**Note 1:** The system unlock sequence must be performed before the SWRST bit can be written. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.


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## 8.0 OSCILLATOR CONFIGURATION

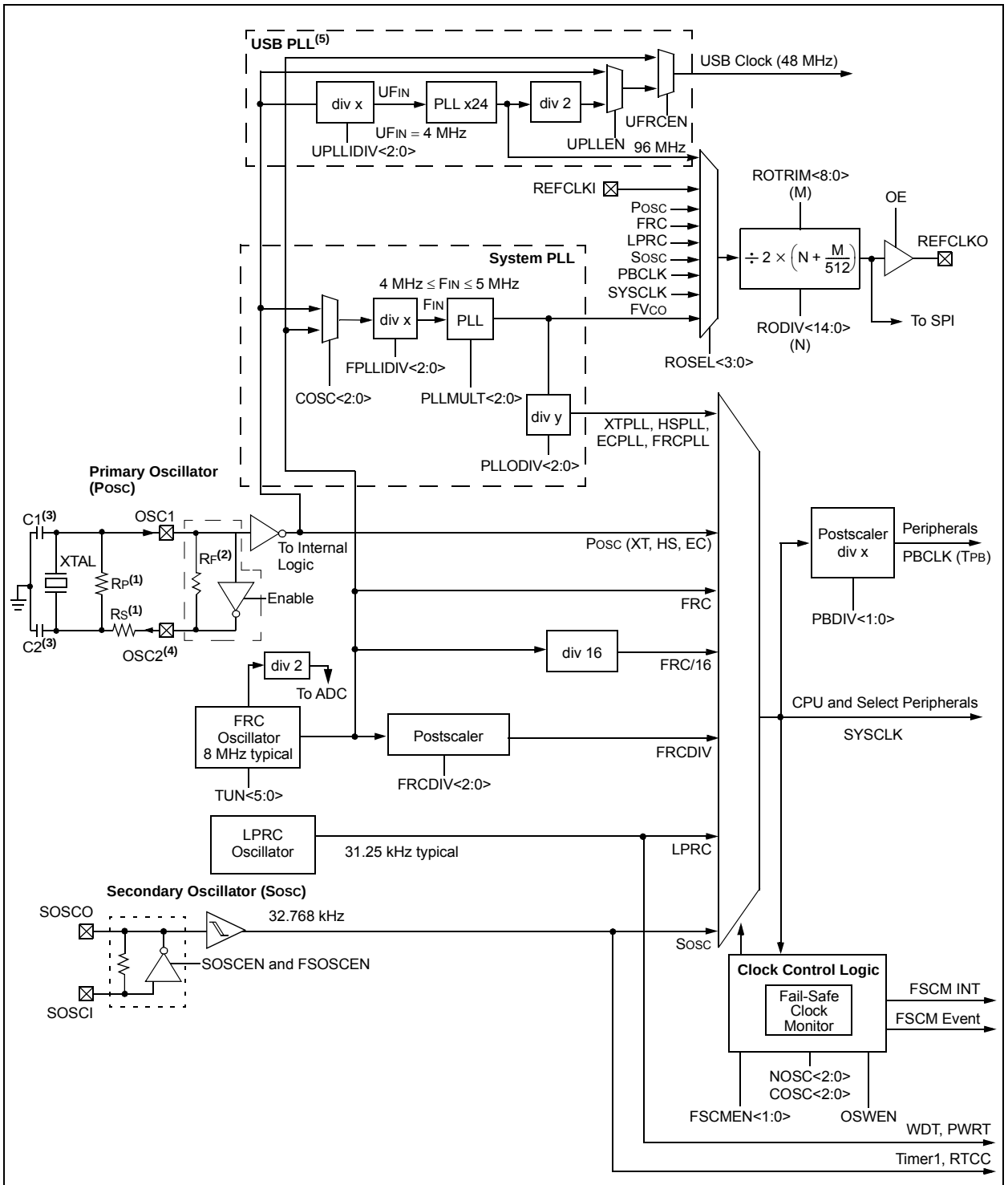
**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 6. "Oscillator Configuration"** (DS60001112) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The PIC32MX1XX/2XX/5XX 64/100-pin oscillator system has the following modules and features:

- A Total of four external and internal oscillator options as clock sources
- On-Chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-Chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Dedicated On-Chip PLL for USB peripheral

A block diagram of the oscillator system is provided in Figure 8-1.

**FIGURE 8-1: PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY CLOCK DIAGRAM**




**Notes: 1.** A series resistor, RS, may be required for AT strip cut crystals or eliminate clipping. Alternately, to increase oscillator circuit gain, add a parallel resistor, RP, with a value of 1 MΩ.

**2.** The internal feedback resistor, RF, is typically in the range of 2 MΩ to 10 MΩ.

**3.** Refer to **Section 6. "Oscillator Configuration"** (DS60001112) in the "*PIC32 Family Reference Manual*" for determining the best oscillator components.

**4.** PBCLK out is available on the OSC2 pin in certain clock modes.

**5.** USB PLL is available on PIC32MX2XX/5XX devices only.


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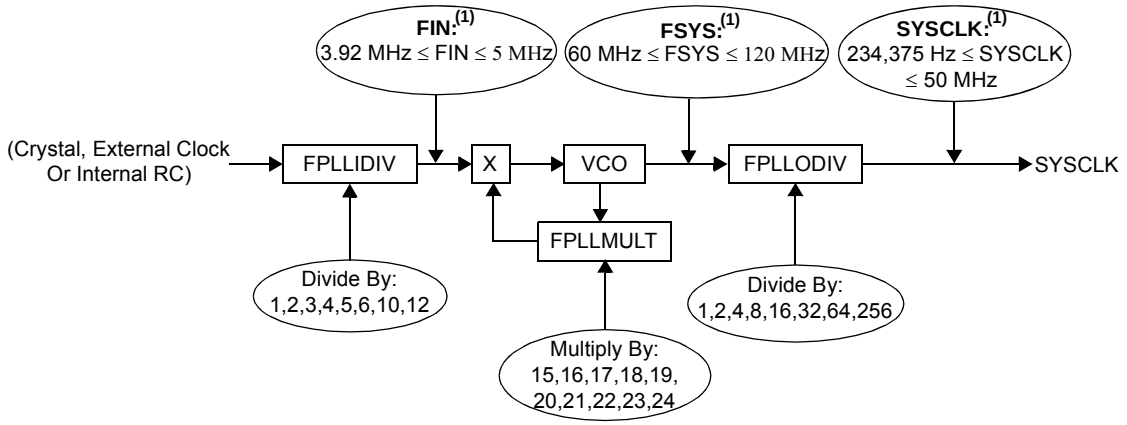
**FIGURE 8-2: PIC32MX1XX/2XX/5XX PLL BLOCK DIAGRAM**




**Note 1:** This frequency range must be satisfied at all times if the PLL is enabled and software is updating the corresponding bits in the OSCON register.

## 8.1 Control Registers

**TABLE 8-1: OSCILLATOR CONFIGURATION REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| F000 | OSCCON | 31:16 | — | — | PLLODIV<2:0> | | | FRCDIV<2:0> | | | — | SOSCRDY | PBDIVRDY | PBDIV<1:0> | | PLLMULT<2:0> | | | x1xx(2) |
| | | 15:0 | — | COSC<2:0> | | | — | NOSC<2:0> | | | CLKLOCK | ULOCK | SLOCK | SLPEN | CF | UFRCEN(3) | SOSCEN | OSWEN | xxxx(2) |
| F010 | OSCTUN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | TUN<5:0> | | | | | | 0000 |
| F020 | REFOCON | 31:16 | — | RODIV<14:0> | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | ON | — | SIDL | OE | RSLP | — | DIVSWEN | ACTIVE | — | — | — | — | ROSEL<3:0> | | | | 0000 |
| F030 | REFOTRIM | 31:16 | ROTRIM<8:0> | | | | | | | | | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** With the exception of those noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

**2:** Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

**3:** This bit is only available on devices with a USB module.

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**REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | R/W-y | R/W-y | R/W-y | R/W-0 | R/W-0 | R/W-1 |
| | — | — | PLLODIV<2:0> | | | FRCDIV<2:0> | | |
| 23:16 | U-0 | R-0 | R-1 | R/W-y | R/W-y | R/W-y | R/W-y | R/W-y |
| | — | SOSCRDY | PBDIVRDY | PBDIV<1:0> | | PLLMULT<2:0> | | |
| 15:8 | U-0 | R-0 | R-0 | R-0 | U-0 | R/W-y | R/W-y | R/W-y |
| | — | COSC<2:0> | | | — | NOSC<2:0> | | |
| 7:0 | R/W-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-y | R/W-0 |
| | CLKLOCK | ULOCK(1) | SLOCK | SLPEN | CF | UFRCEN(1) | SOSCEN | OSWEN |

| Legend: | y = Value set from Configuration bits on POR | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-30 **Unimplemented:** Read as '0'

bit 29-27 **PLLODIV<2:0>:** Output Divider for PLL
- 111 = PLL output divided by 256
- 110 = PLL output divided by 64
- 101 = PLL output divided by 32
- 100 = PLL output divided by 16
- 011 = PLL output divided by 8
- 010 = PLL output divided by 4
- 001 = PLL output divided by 2
- 000 = PLL output divided by 1

bit 26-24 **FRCDIV<2:0>:** Internal Fast RC (FRC) Oscillator Clock Divider bits
- 111 = FRC divided by 256
- 110 = FRC divided by 64
- 101 = FRC divided by 32
- 100 = FRC divided by 16
- 011 = FRC divided by 8
- 010 = FRC divided by 4
- 001 = FRC divided by 2 (default setting)
- 000 = FRC divided by 1

bit 23 **Unimplemented:** Read as '0'

bit 22 **SOSCRDY:** Secondary Oscillator (SOSC) Ready Indicator bit
- 1 = Indicates that the Secondary Oscillator is running and is stable
- 0 = Secondary Oscillator is still warming up or is turned off

bit 21 **PBDIVRDY:** Peripheral Bus Clock (PBCLK) Divisor Ready bit
- 1 = PBDIV<1:0> bits can be written
- 0 = PBDIV<1:0> bits cannot be written

bit 20-19 **PBDIV<1:0>:** Peripheral Bus Clock (PBCLK) Divisor bits
- 11 = PBCLK is SYSCLK divided by 8 (default)
- 10 = PBCLK is SYSCLK divided by 4
- 01 = PBCLK is SYSCLK divided by 2
- 00 = PBCLK is SYSCLK divided by 1

**Note 1:** This bit is available on PIC32MX2XX/5XX devices only.

**Note:** Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

**REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)**

bit 18-16 **PLLMULT<2:0>:** Phase-Locked Loop (PLL) Multiplier bits
- 111 = Clock is multiplied by 24
- 110 = Clock is multiplied by 21
- 101 = Clock is multiplied by 20
- 100 = Clock is multiplied by 19
- 011 = Clock is multiplied by 18
- 010 = Clock is multiplied by 17
- 001 = Clock is multiplied by 16
- 000 = Clock is multiplied by 15

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits
- 111 = Internal Fast RC (FRC) Oscillator divided by OSCCON<FRCDIV> bits
- 110 = Internal Fast RC (FRC) Oscillator divided by 16
- 101 = Internal Low-Power RC (LPRC) Oscillator
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator (POSC) with PLL module (XTPLL, HSPLL or ECPLL)
- 010 = Primary Oscillator (POSC) (XT, HS or EC)
- 001 = Internal Fast RC Oscillator with PLL module via Postscaler (FRCPLL)
- 000 = Internal Fast RC (FRC) Oscillator

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits
- 111 = Internal Fast RC Oscillator (FRC) divided by OSCCON<FRCDIV> bits
- 110 = Internal Fast RC Oscillator (FRC) divided by 16
- 101 = Internal Low-Power RC (LPRC) Oscillator
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator with PLL module (XTPLL, HSPLL or ECPLL)
- 010 = Primary Oscillator (XT, HS or EC)
- 001 = Internal Fast Internal RC Oscillator with PLL module via Postscaler (FRCPLL)
- 000 = Internal Fast Internal RC Oscillator (FRC)

On Reset, these bits are set to the value of the FNOSC Configuration bits (DEVCFG1<2:0>).

bit 7 **CLKLOCK:** Clock Selection Lock Enable bit

If clock switching and monitoring is disabled (FCKSM<1:0> = 1x):
- 1 = Clock and PLL selections are locked
- 0 = Clock and PLL selections are not locked and may be modified

If clock switching and monitoring is enabled (FCKSM<1:0> = 0x):
Clock and PLL selections are never locked and may be modified.

bit 6 **ULOCK:** USB PLL Lock Status bit(1)
- 1 = Indicates that the USB PLL module is in lock or USB PLL module start-up timer is satisfied
- 0 = Indicates that the USB PLL module is out of lock or USB PLL module start-up timer is in progress or USB PLL is disabled

bit 5 **SLOCK:** PLL Lock Status bit
- 1 = PLL module is in lock or PLL module start-up timer is satisfied
- 0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled

bit 4 **SLPEN:** Sleep Mode Enable bit
- 1 = Device will enter Sleep mode when a WAIT instruction is executed
- 0 = Device will enter Idle mode when a WAIT instruction is executed

bit 3 **CF:** Clock Fail Detect bit
- 1 = FSCM has detected a clock failure
- 0 = No clock failure has been detected

**Note 1:** This bit is available on PIC32MX2XX/5XX devices only.

| **Note:** | Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details. |
|---|---|


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**REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)**

bit 2 **UFRCEN:** USB FRC Clock Enable bit(1)
- 1 = Enable FRC as the clock source for the USB clock source
- 0 = Use the Primary Oscillator or USB PLL as the USB clock source

bit 1 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit
- 1 = Enable Secondary Oscillator
- 0 = Disable Secondary Oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit
- 1 = Initiate an oscillator switch to selection specified by NOSC<2:0> bits
- 0 = Oscillator switch is complete

**Note 1:** This bit is available on PIC32MX2XX/5XX devices only.

**Note:** Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

**REGISTER 8-2: OSCTUN: FRC TUNING REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | R-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | R-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | TUN<5:0>(1) | | | | | |

| Legend: | y = Value set from Configuration bits on POR | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits(1)

100000 = Center frequency -12.5%
100001 =
•
•
•
111111 =
000000 = Center frequency. Oscillator runs at minimal frequency (8 MHz)
000001 =
•
•
•
011110 =
011111 = Center frequency +12.5%

**Note 1:** OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step size is an approximation, and is neither characterized, nor tested.

**Note:** Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.


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**REGISTER 8-3: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | RODIV<14:8>(1) | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RODIV<7:0>(3) | | | | | | | |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0, HC | R-0, HS, HC |
| | ON | — | SIDL | OE | RSLP(2) | — | DIVSWEN | ACTIVE |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | ROSEL<3:0>(1) | | | |

| Legend: | HC = Hardware Clearable | HS = Hardware Settable | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **Unimplemented:** Read as '0'

bit 30-16 **RODIV<14:0>:** Reference Clock Divider bits(1)

This value selects the Reference Clock Divider bits. See Figure 8-1 for more information.

bit 15 **ON:** Output Enable bit

1 = Reference Oscillator Module enabled
0 = Reference Oscillator Module disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Peripheral Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12 **OE:** Reference Clock Output Enable bit

1 = Reference clock is driven out on REFCLKO pin
0 = Reference clock is not driven out on REFCLKO pin

bit 11 **RSLP:** Reference Oscillator Module Run in Sleep bit(2)

1 = Reference Oscillator Module output continues to run in Sleep
0 = Reference Oscillator Module output is disabled in Sleep

bit 10 **Unimplemented:** Read as '0'

bit 9 **DIVSWEN:** Divider Switch Enable bit

1 = Divider switch is in progress
0 = Divider switch is complete

bit 8 **ACTIVE:** Reference Clock Request Status bit

1 = Reference clock request is active
0 = Reference clock request is not active

bit 7-4 **Unimplemented:** Read as '0'

**Note 1:** The ROSEL and RODIV bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.

**2:** This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.

**3:** While the ON bit is set to '1', writes to these bits do not take effect until the DIVSWEN bit is also set to '1'.

**REGISTER 8-3: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER (CONTINUED)**

bit 3-0 **ROSEL<3:0>:** Reference Clock Source Select bits(1)

1111 = Reserved; do not use
•
•
•
1001 = Reserved; do not use
1000 = REFCLKI
0111 = System PLL output
0110 = USB PLL output
0101 = SOSC
0100 = LPRC
0011 = FRC
0010 = POSC
0001 = PBCLK
0000 = SYSCLK

**Note 1:** The ROSEL and RODIV bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.

**2:** This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.

**3:** While the ON bit is set to '1', writes to these bits do not take effect until the DIVSWEN bit is also set to '1'.


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**REGISTER 8-4: REFOTRIM: REFERENCE OSCILLATOR TRIM REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ROTRIM<8:1> | | | | | | | |
| 23:16 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ROTRIM<0> | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| **Legend:** | y = Value set from Configuration bits on POR | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-23 **ROTRIM<8:0>:** Reference Oscillator Trim bits

111111111 = 511/512 divisor added to RODIV value
111111110 = 510/512 divisor added to RODIV value
•
•
•
100000000 = 256/512 divisor added to RODIV value
•
•
•
000000010 = 2/512 divisor added to RODIV value
000000001 = 1/512 divisor added to RODIV value
000000000 = 0/512 divisor added to RODIV value

bit 22-0 **Unimplemented:** Read as '0'

**Note:** While the ON bit (REFOCON<15>) is '1', writes to this register do not take effect until the DIVSWEN bit is also set to '1'.

**NOTES:**


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## 9.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

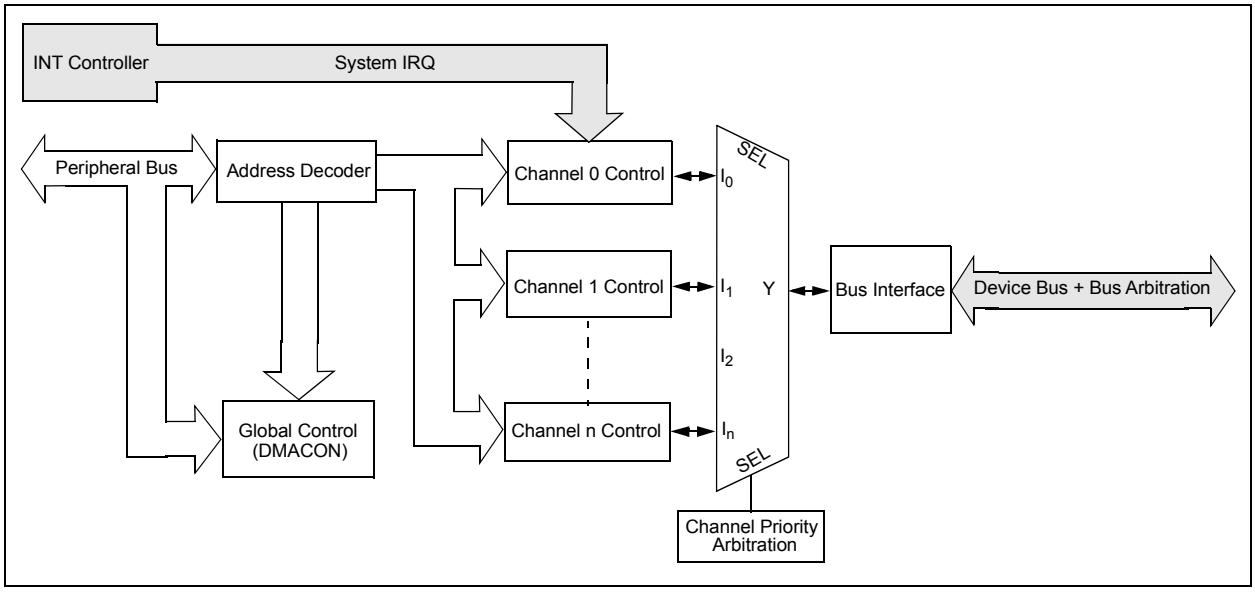
**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The PIC32 Direct Memory Access (DMA) controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the PIC32 (such as Peripheral Bus (PBUS) devices: SPI, UART, PMP, etc.) or memory itself.

The following are some of the key features of the DMA controller module:

- Four identical channels, each featuring:
  - Auto-increment source and destination address registers
  - Source and destination pointers
  - Memory to memory and memory to peripheral transfers
- Automatic word-size detection:
  - Transfer granularity, down to byte level
  - Bytes need not be word-aligned at source and destination
- Fixed priority channel arbitration
- Flexible DMA channel operating modes:
  - Manual (software) or automatic (interrupt) DMA requests
  - One-Shot or Auto-Repeat Block Transfer modes
  - Channel-to-channel chaining
- Flexible DMA requests:
  - A DMA request can be selected from any of the peripheral interrupt sources
  - Each channel can select any (appropriate) observable interrupt as its DMA request source
  - A DMA transfer abort can be selected from any of the peripheral interrupt sources
  - Pattern (data) match transfer termination
- Multiple DMA channel status interrupts:
  - DMA channel block transfer complete
  - Source empty or half empty
  - Destination full or half full
  - DMA transfer aborted due to an external event
  - Invalid DMA address generated
- DMA debug support features:
  - Most recent address accessed by a DMA channel
  - Most recent DMA channel to transfer data
- CRC Generation module:
  - CRC module can be assigned to any of the available channels
  - CRC module is highly configurable

**FIGURE 9-1: DMA BLOCK DIAGRAM**



## 9.1 Control Registers

### TABLE 9-1: DMA GLOBAL REGISTER MAP

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 3000 | DMACON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | — | SUSPEND | DMABUSY | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 3010 | DMASTAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RDWR | DMACH<2:0> | | | 0000 |
| 3020 | DMAADDR | 31:16 | DMAADDR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

### TABLE 9-2: DMA CRC REGISTER MAP

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 3030 | DCRCCON | 31:16 | — | — | BYTO<1:0> | | WBO | — | — | BITO | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | PLEN<4:0> | | | | | CRCEN | CRCAPP | CRCTYP | — | — | CRCCH<2:0> | | | 0000 |
| 3040 | DCRCDATA | 31:16 | DCRCDATA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 3050 | DCRCXOR | 31:16 | DCRCXOR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.



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**TABLE 9-3: DMA CHANNEL 0 THROUGH CHANNEL 3 REGISTER MAP**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 3060 | DCH0CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHBUSY | — | — | — | — | — | — | CHCHNS | CHEN | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | | 0000 |
| 3070 | DCH0ECON | 31:16 | — | — | — | — | — | — | — | — | CHAIRQ<7:0> | | | | | | | | 00FF |
| | | 15:0 | CHSIRQ<7:0> | | | | | | | | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — | FFF8 |
| 3080 | DCH0INT | 31:16 | — | — | — | — | — | — | — | — | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF | 0000 |
| 3090 | DCH0SSA | 31:16 | CHSSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 30A0 | DCH0DSA | 31:16 | CHDSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 30B0 | DCH0SSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 30C0 | DCH0DSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 30D0 | DCH0SPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 30E0 | DCH0DPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 30F0 | DCH0CSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3100 | DCH0CPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3110 | DCH0DAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHPDAT<7:0> | | | | | | | | 0000 |
| 3120 | DCH1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHBUSY | — | — | — | — | — | — | CHCHNS | CHEN | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | | 0000 |
| 3130 | DCH1ECON | 31:16 | — | — | — | — | — | — | — | — | CHAIRQ<7:0> | | | | | | | | 00FF |
| | | 15:0 | CHSIRQ<7:0> | | | | | | | | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — | FFF8 |
| 3140 | DCH1INT | 31:16 | — | — | — | — | — | — | — | — | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF | 0000 |
| 3150 | DCH1SSA | 31:16 | CHSSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 3160 | DCH1DSA | 31:16 | CHDSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

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**TABLE 9-3: DMA CHANNEL 0 THROUGH CHANNEL 3 REGISTER MAP (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 3170 | DCH1SSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3180 | DCH1DSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3190 | DCH1SPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 31A0 | DCH1DPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 31B0 | DCH1CSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 31C0 | DCH1CPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 31D0 | DCH1DAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHPDAT<7:0> | | | | | | | | 0000 |
| 31E0 | DCH2CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHBUSY | — | — | — | — | — | — | CHCHNS | CHEN | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | | 0000 |
| 31F0 | DCH2ECON | 31:16 | — | — | — | — | — | — | — | — | CHAIRQ<7:0> | | | | | | | | 00FF |
| | | 15:0 | CHSIRQ<7:0> | | | | | | | | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — | FFF8 |
| 3200 | DCH2INT | 31:16 | — | — | — | — | — | — | — | — | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF | 0000 |
| 3210 | DCH2SSA | 31:16 | CHSSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 3220 | DCH2DSA | 31:16 | CHDSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 3230 | DCH2SSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3240 | DCH2DSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3250 | DCH2SPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3260 | DCH2DPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3270 | DCH2CSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.



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**TABLE 9-3: DMA CHANNEL 0 THROUGH CHANNEL 3 REGISTER MAP (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 3280 | DCH2CPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3290 | DCH2DAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHPDAT<7:0> | | | | | | | | 0000 |
| 32A0 | DCH3CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHBUSY | — | — | — | — | — | — | CHCHNS | CHEN | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | | 0000 |
| 32B0 | DCH3ECON | 31:16 | — | — | — | — | — | — | — | — | CHAIRQ<7:0> | | | | | | | | 00FF |
| | | 15:0 | CHSIRQ<7:0> | | | | | | | | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — | FFF8 |
| 32C0 | DCH3INT | 31:16 | — | — | — | — | — | — | — | — | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF | 0000 |
| 32D0 | DCH3SSA | 31:16 | CHSSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 32E0 | DCH3DSA | 31:16 | CHDSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 32F0 | DCH3SSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3300 | DCH3DSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3310 | DCH3SPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3320 | DCH3DPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3330 | DCH3CSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3340 | DCH3CPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3350 | DCH3DAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHPDAT<7:0> | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

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**REGISTER 9-1: DMACON: DMA CONTROLLER CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
| | ON(1) | — | — | SUSPEND | DMABUSY(1) | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** DMA On bit(1)
- 1 = DMA module is enabled
- 0 = DMA module is disabled

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **SUSPEND:** DMA Suspend bit
- 1 = DMA transfers are suspended to allow CPU uninterrupted access to data bus
- 0 = DMA operates normally

bit 11 **DMABUSY:** DMA Module Busy bit(1)
- 1 = DMA module is active
- 0 = DMA module is disabled and not actively transferring data

bit 10-0 **Unimplemented:** Read as '0'

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.


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**REGISTER 9-2: DMASTAT: DMA STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
| | — | — | — | — | RDWR | DMACH<2:0> | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **RDWR:** Read/Write Status bit
1 = Last DMA bus access was a read
0 = Last DMA bus access was a write

bit 2-0 **DMACH<2:0>:** DMA Channel bits
These bits contain the value of the most recent active DMA channel.

**REGISTER 9-3: DMAADDR: DMA ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | DMAADDR<31:24> | | | | | | | |
| 23:16 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | DMAADDR<23:16> | | | | | | | |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | DMAADDR<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | DMAADDR<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **DMAADDR<31:0>:** DMA Module Address bits
These bits contain the address of the most recent DMA access.

**REGISTER 9-4: DCRCCON: DMA CRC CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 |
| | — | — | BYTO<1:0> | | WBO(1) | — | — | BITO |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | PLEN<4:0> | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | CRCEN | CRCAPP(1) | CRCTYP | — | — | CRCCH<2:0> | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **BYTO<1:0>:** CRC Byte Order Selection bits
- 11 = Endian byte swap on half-word boundaries (i.e., source half-word order with reverse source byte order per half-word)
- 10 = Swap half-words on word boundaries (i.e., reverse source half-word order with source byte order per half-word)
- 01 = Endian byte swap on word boundaries (i.e., reverse source byte order)
- 00 = No swapping (i.e., source byte order)

bit 27 **WBO:** CRC Write Byte Order Selection bit(1)
- 1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>
- 0 = Source data is written to the destination unaltered

bit 26-25 **Unimplemented:** Read as '0'

bit 24 **BITO:** CRC Bit Order Selection bit(1

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
- 1 = The IP header checksum is calculated Least Significant bit (LSb) first (i.e., reflected)
- 0 = The IP header checksum is calculated Most Significant bit (MSb) first (i.e., not reflected)

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
- 1 = The LFSR CRC is calculated Least Significant bit first (i.e., reflected)
- 0 = The LFSR CRC is calculated Most Significant bit first (i.e., not reflected)

bit 23-13 **Unimplemented:** Read as '0'

bit 12-8 **PLEN<4:0>:** Polynomial Length bits(1)

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
These bits are unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
Denotes the length of the polynomial – 1.

bit 7 **CRCEN:** CRC Enable bit
- 1 = CRC module is enabled and channel transfers are routed through the CRC module
- 0 = CRC module is disabled and channel transfers proceed normally

**Note 1:** When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.


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**REGISTER 9-4: DCRCCON: DMA CRC CONTROL REGISTER (CONTINUED)**

bit 6 **CRCAPP:** CRC Append Mode bit(1)
- 1 = The DMA transfers data from the source into the CRC but NOT to the destination. When a block transfer completes the DMA writes the calculated CRC value to the location given by CHxDSA
- 0 = The DMA transfers data from the source through the CRC obeying WBO as it writes the data to the destination

bit 5 **CRCTYP:** CRC Type Selection bit
- 1 = The CRC module will calculate an IP header checksum
- 0 = The CRC module will calculate a LFSR CRC

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **CRCCH<2:0>:** CRC Channel Select bits
- 111 = CRC is assigned to Channel 7
- 110 = CRC is assigned to Channel 6
- 101 = CRC is assigned to Channel 5
- 100 = CRC is assigned to Channel 4
- 011 = CRC is assigned to Channel 3
- 010 = CRC is assigned to Channel 2
- 001 = CRC is assigned to Channel 1
- 000 = CRC is assigned to Channel 0

**Note 1:** When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

**REGISTER 9-5: DCRCDATA: DMA CRC DATA REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCDATA<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCDATA<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCDATA<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCDATA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **DCRCDATA<31:0>:** CRC Data Register bits

Writing to this register will seed the CRC generator. Reading from this register will return the current value of the CRC. Bits greater than PLEN will return '0' on any read.

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
Only the lower 16 bits contain IP header checksum information. The upper 16 bits are always '0'. Data written to this register is converted and read back in 1's complement form (i.e., current IP header checksum value).

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
Bits greater than PLEN will return '0' on any read.

**REGISTER 9-6: DCRCXOR: DMA CRCXOR ENABLE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCXOR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCXOR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCXOR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCXOR<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **DCRCXOR<31:0>:** CRC XOR Register bits

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
This register is unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
1 = Enable the XOR input to the Shift register
0 = Disable the XOR input to the Shift register; data is shifted in directly from the previous stage in the register


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**REGISTER 9-7: DCHxCON: DMA CHANNEL 'x' CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
| | CHBUSY | — | — | — | — | — | — | CHCHNS(1) |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R-0 | R/W-0 | R/W-0 |
| | CHEN(2) | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **CHBUSY:** Channel Busy bit
- 1 = Channel is active or has been enabled
- 0 = Channel is inactive or has been disabled

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **CHCHNS:** Chain Channel Selection bit(1)
- 1 = Chain to channel lower in natural priority (CH1 will be enabled by CH2 transfer complete)
- 0 = Chain to channel higher in natural priority (CH1 will be enabled by CH0 transfer complete)

bit 7 **CHEN:** Channel Enable bit(2)
- 1 = Channel is enabled
- 0 = Channel is disabled

bit 6 **CHAED:** Channel Allow Events If Disabled bit
- 1 = Channel start/abort events will be registered, even if the channel is disabled
- 0 = Channel start/abort events will be ignored if the channel is disabled

bit **CHCHN:** Channel Chain Enable bit
- 1 = Allow channel to be chained
- 0 = Do not allow channel to be chained

bit 4 **CHAEN:** Channel Automatic Enable bit
- 1 = Channel is continuously enabled, and not automatically disabled after a block transfer is complete
- 0 = Channel is disabled on block transfer complete

bit 3 **Unimplemented:** Read as '0'

bit 2 **CHEDET:** Channel Event Detected bit
- 1 = An event has been detected
- 0 = No events have been detected

bit 1-0 **CHPRI<1:0>:** Channel Priority bits
- 11 = Channel has priority 3 (highest)
- 10 = Channel has priority 2
- 01 = Channel has priority 1
- 00 = Channel has priority 0

**Note 1:** The chain selection bit takes effect when chaining is enabled (i.e., CHCHN = 1).

**2:** When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

**REGISTER 9-8: DCHxECON: DMA CHANNEL 'x' EVENT CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| | CHAIRQ<7:0>(1) | | | | | | | |
| 15:8 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| | CHSIRQ<7:0>(1) | | | | | | | |
| 7:0 | S-0 | S-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
| | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — |

| Legend: | S = Settable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **CHAIRQ<7:0>:** Channel Transfer Abort IRQ bits(1)
- 11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag
- •
- •
- •
- 00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag
- 00000000 = Interrupt 0 will abort any transfers in progress and set CHAIF flag

bit 15-8 **CHSIRQ<7:0>:** Channel Transfer Start IRQ bits(1)
- 11111111 = Interrupt 255 will initiate a DMA transfer
- •
- •
- •
- 00000001 = Interrupt 1 will initiate a DMA transfer
- 00000000 = Interrupt 0 will initiate a DMA transfer

bit 7 **CFORCE:** DMA Forced Transfer bit
- 1 = A DMA transfer is forced to begin when this bit is written to a '1'
- 0 = This bit always reads '0'

bit 6 **CABORT:** DMA Abort Transfer bit
- 1 = A DMA transfer is aborted when this bit is written to a '1'
- 0 = This bit always reads '0'

bit 5 **PATEN:** Channel Pattern Match Abort Enable bit
- 1 = Abort transfer and clear CHEN on pattern match
- 0 = Pattern match is disabled

bit 4 **SIRQEN:** Channel Start IRQ Enable bit
- 1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs
- 0 = Interrupt number CHSIRQ is ignored and does not start a transfer

bit 3 **AIRQEN:** Channel Abort IRQ Enable bit
- 1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs
- 0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer

bit 2-0 **Unimplemented:** Read as '0'

**Note 1:** See **Table 5-1: "Interrupt IRQ, Vector and Bit Location"** for the list of available interrupt IRQ sources.


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**REGISTER 9-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **CHSDIE:** Channel Source Done Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 22 **CHSHIE:** Channel Source Half Empty Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 21 **CHDDIE:** Channel Destination Done Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 20 **CHDHIE:** Channel Destination Half Full Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 19 **CHBCIE:** Channel Block Transfer Complete Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 18 **CHCCIE:** Channel Cell Transfer Complete Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 17 **CHTAIE:** Channel Transfer Abort Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 16 **CHERIE:** Channel Address Error Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **CHSDIF:** Channel Source Done Interrupt Flag bit
- 1 = Channel Source Pointer has reached end of source (CHSPTR = CHSSIZ)
- 0 = No interrupt is pending

bit 6 **CHSHIF:** Channel Source Half Empty Interrupt Flag bit
- 1 = Channel Source Pointer has reached midpoint of source (CHSPTR = CHSSIZ/2)
- 0 = No interrupt is pending

bit 5 **CHDDIF:** Channel Destination Done Interrupt Flag bit
- 1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ)
- 0 = No interrupt is pending

**REGISTER 9-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER (CONTINUED)**

bit 4 **CHDHIF:** Channel Destination Half Full Interrupt Flag bit
- 1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
- 0 = No interrupt is pending

bit 3 **CHBCIF:** Channel Block Transfer Complete Interrupt Flag bit
- 1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs
- 0 = No interrupt is pending

bit 2 **CHCCIF:** Channel Cell Transfer Complete Interrupt Flag bit
- 1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
- 0 = No interrupt is pending

bit 1 **CHTAIF:** Channel Transfer Abort Interrupt Flag bit
- 1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
- 0 = No interrupt is pending

bit 0 **CHERIF:** Channel Address Error Interrupt Flag bit
- 1 = A channel address error has been detected
  Either the source or the destination address is invalid.
- 0 = No interrupt is pending


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**REGISTER 9-10: DCHxSSA: DMA CHANNEL 'x' SOURCE START ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSSA<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSSA<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSSA<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSSA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **CHSSA<31:0>** Channel Source Start Address bits
Channel source start address.

**Note:** This must be the physical address of the source.

**REGISTER 9-11: DCHxDSA: DMA CHANNEL 'x' DESTINATION START ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHDSA<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHDSA<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHDSA<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHDSA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **CHDSA<31:0>:** Channel Destination Start Address bits
Channel destination start address.

**Note:** This must be the physical address of the destination.

**REGISTER 9-12: DCHxSSIZ: DMA CHANNEL 'x' SOURCE SIZE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSSIZ<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSSIZ<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHSSIZ<15:0>:** Channel Source Size bits

1111111111111111 = 65,535 byte source size
.
.
.
0000000000000010 = 2 byte source size
0000000000000001 = 1 byte source size
0000000000000000 = 65,536 byte source size

**REGISTER 9-13: DCHxDSIZ: DMA CHANNEL 'x' DESTINATION SIZE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHDSIZ<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHDSIZ<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHDSIZ<15:0>:** Channel Destination Size bits

1111111111111111 = 65,535 byte destination size
.
.
.
0000000000000010 = 2 byte destination size
0000000000000001 = 1 byte destination size
0000000000000000 = 65,536 byte destination size


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**REGISTER 9-14: DCHxSPTR: DMA CHANNEL 'x' SOURCE POINTER REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | CHSPTR<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | CHSPTR<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHSPTR<15:0>:** Channel Source Pointer bits

1111111111111111 = Points to byte 65,535 of the source
•
•
•
0000000000000001 = Points to byte 1 of the source
0000000000000000 = Points to byte 0 of the source

**Note:** When in Pattern Detect mode, this register is reset on a pattern detect.

**REGISTER 9-15: DCHxDPTR: DMA CHANNEL 'x' DESTINATION POINTER REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | CHDPTR<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | CHDPTR<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHDPTR<15:0>:** Channel Destination Pointer bits

1111111111111111 = Points to byte 65,535 of the destination
•
•
•
0000000000000001 = Points to byte 1 of the destination
0000000000000000 = Points to byte 0 of the destination

**REGISTER 9-16: DCHxCSIZ: DMA CHANNEL 'x' CELL-SIZE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHCSIZ<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHCSIZ<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCSIZ<15:0>:** Channel Cell-Size bits

1111111111111111 = 65,535 bytes transferred on an event
.
.
.
0000000000000010 = 2 bytes transferred on an event
0000000000000001= 1 byte transferred on an event
0000000000000000 = 65,536 bytes transferred on an event

**REGISTER 9-17: DCHxCPTR: DMA CHANNEL 'x' CELL POINTER REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | CHCPTR<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | CHCPTR<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCPTR<7:0>:** Channel Cell Progress Pointer bits

1111111111111111 = 65,535 bytes have been transferred since the last event
.
.
.
0000000000000001 = 1 byte has been transferred since the last event
0000000000000000 = 0 bytes have been transferred since the last event

**Note:** When in Pattern Detect mode, this register is reset on a pattern detect.


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**REGISTER 9-18: DCHxDAT: DMA CHANNEL 'x' PATTERN DATA REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHPDAT<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CHPDAT<7:0>:** Channel Data Register bits

Pattern Terminate mode:
Data to be matched must be stored in this register to allow terminate on match.

All other modes:
Unused.

**NOTES:**


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## 10.0 USB ON-THE-GO (OTG)

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 27. "USB On-The-Go (OTG)"** (DS60001126) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 full-speed and low-speed embedded host, full-speed device or OTG implementation with a minimum of external components. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32 USB OTG module is presented in Figure 10-1.

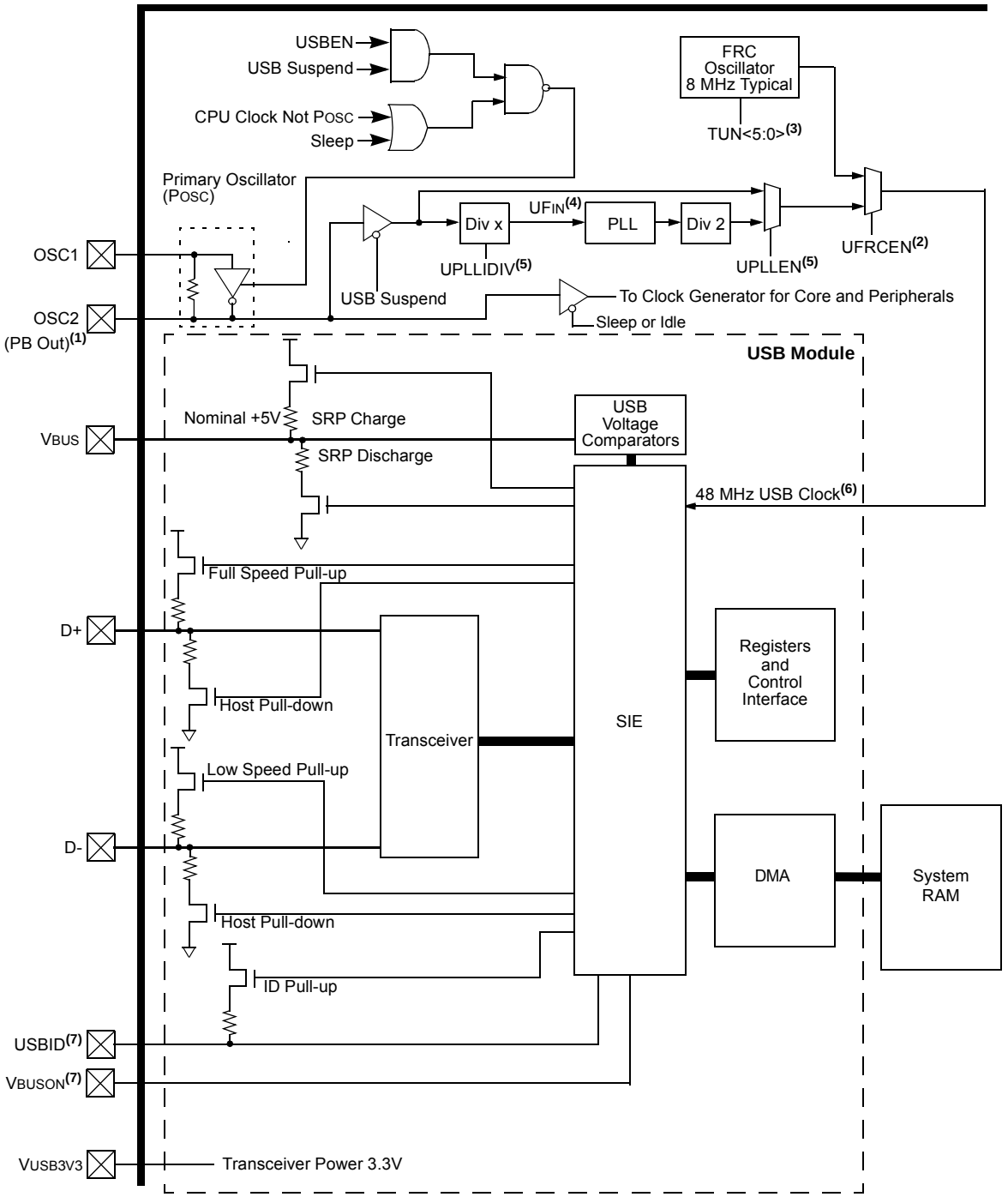
The clock generator provides the 48 MHz clock required for USB full-speed and low-speed communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers and generates the hardware protocol for data transfers. The USB DMA controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module.

The PIC32 USB module includes the following features:

- USB Full-speed support for host and device
- Low-speed host support
- USB OTG support
- Integrated signaling resistors
- Integrated analog comparators for VBUS monitoring
- Integrated USB transceiver
- Transaction handshaking performed by hardware
- Endpoint buffering anywhere in system RAM
- Integrated DMA to access system RAM and Flash

**Note:** The implementation and use of the USB specifications, and other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (also referred to as USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

**FIGURE 10-1: PIC32MX1XX/2XX/5XX USB INTERFACE DIAGRAM**




**Note 1:** PB clock is only available on this pin for select EC modes.
**2:** This bit field is contained in the OSCCON register.
**3:** This bit field is contained in the OSCTRM register.
**4:** USB PLL UFIN requirements: 4 MHz.
**5:** This bit field is contained in the DEVCFG2 register.
**6:** A 48 MHz clock is required for proper USB operation.
**7:** Pins can be used as GPIO when the USB module is disabled or if the USB is enabled but DEVCFG3<31:30> = '0b00.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## 10.1 Control Registers

**TABLE 10-1: USB REGISTER MAP**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 5040 | U1OTGIR(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | IDIF | T1MSECIF | LSTATEIF | ACTVIF | SESVDIF | SESENDIF | — | VBUSVDIF | 0000 |
| 5050 | U1OTGIE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | IDIE | T1MSECIE | LSTATEIE | ACTVIE | SESVDIE | SESENDIE | — | VBUSVDIE | 0000 |
| 5060 | U1OTGSTAT(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | ID | — | LSTATE | — | SESVD | SESEND | — | VBUSVD | 0000 |
| 5070 | U1OTGCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | DPPULUP | DMPULUP | DPPULDWN | DMPULDWN | VBUSON | OTGEN | VBUSCHG | VBUSDIS | 0000 |
| 5080 | U1PWRC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | UACTPND(4) | — | — | USLPGRD | USBBUSY | — | USUSPEND | USBPWR | 0000 |
| 5200 | U1IR(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | STALLIF | ATTACHIF | RESUMEIF | IDLEIF | TRNIF | SOFIF | UERRIF | URSTIF | 0000 |
| | | | | | | | | | | | | | | | | | | DETACHIF | 0000 |
| 5210 | U1IE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | STALLIE | ATTACHIE | RESUMEIE | IDLEIE | TRNIE | SOFIE | UERRIE | URSTIE | 0000 |
| | | | | | | | | | | | | | | | | | | DETACHIE | 0000 |
| 5220 | U1EIR(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | BTSEF | BMXEF | DMAEF | BTOEF | DFN8EF | CRC16EF | CRC5EF | PIDEF | 0000 |
| | | | | | | | | | | | | | | | | | EOFEF | | 0000 |
| 5230 | U1EIE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | BTSEE | BMXEE | DMAEE | BTOEE | DFN8EE | CRC16EE | CRC5EE | PIDEE | 0000 |
| | | | | | | | | | | | | | | | | | EOFEE | | 0000 |
| 5240 | U1STAT(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | ENDPT<3:0> | | | | DIR | PPBI | — | — | 0000 |
| 5250 | U1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | JSTATE | SE0 | PKTDIS | USBRST | HOSTEN | RESUME | PPBRST | USBEN | 0000 |
| | | | | | | | | | | | | | TOKBUSY | | | | | SOFEN | 0000 |
| 5260 | U1ADDR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | LSPDEN | DEVADDR<6:0> | | | | | | | 0000 |
| 5270 | U1BDTP1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | BDTPTRL<15:9> | | | | | | | — | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

**2:** This register does not have associated SET and INV registers.

**3:** This register does not have associated CLR, SET and INV registers.

**4:** Reset value for this bit is undefined.

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**TABLE 10-1: USB REGISTER MAP (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 5280 | U1FRML(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | FRML<7:0> | | | | | | | | 0000 |
| 5290 | U1FRMH(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | FRMH<2:0> | | | 0000 |
| 52A0 | U1TOK | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | PID<3:0> | | | | EP<3:0> | | | | 0000 |
| 52B0 | U1SOF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CNT<7:0> | | | | | | | | 0000 |
| 52C0 | U1BDTP2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | BDTPTRH<23:16> | | | | | | | | 0000 |
| 52D0 | U1BDTP3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | BDTPTRU<31:24> | | | | | | | | 0000 |
| 52E0 | U1CNFG1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | UTEYE | — | — | USBSIDL | LSDEV | — | — | UASUSPND | 0000 |
| 5300 | U1EP0 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | LSPD | RETRYDIS | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5310 | U1EP1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5320 | U1EP2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5330 | U1EP3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5340 | U1EP4 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5350 | U1EP5 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5360 | U1EP6 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5370 | U1EP7 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5380 | U1EP8 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

**2:** This register does not have associated SET and INV registers.

**3:** This register does not have associated CLR, SET and INV registers.

**4:** Reset value for this bit is undefined.



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**TABLE 10-1: USB REGISTER MAP (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 5390 | U1EP9 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 53A0 | U1EP10 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 53B0 | U1EP11 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 53C0 | U1EP12 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 53D0 | U1EP13 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 53E0 | U1EP14 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 53F0 | U1EP15 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

**2:** This register does not have associated SET and INV registers.

**3:** This register does not have associated CLR, SET and INV registers.

**4:** Reset value for this bit is undefined.

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**REGISTER 10-1: U1OTGIR: USB OTG INTERRUPT STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | U-0 | R/WC-0, HS |
| | IDIF | T1MSECIF | LSTATEIF | ACTVIF | SESVDIF | SESENDIF | — | VBUSVDIF |

| **Legend:** | WC = Write '1' to clear | HS = Hardware Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIF:** ID State Change Indicator bit
- 1 = Change in ID state detected
- 0 = No change in ID state detected

bit 6 **T1MSECIF:** 1 Millisecond Timer bit
- 1 = 1 millisecond timer has expired
- 0 = 1 millisecond timer has not expired

bit 5 **LSTATEIF:** Line State Stable Indicator bit
- 1 = USB line state has been stable for 1millisecond, but different from last time
- 0 = USB line state has not been stable for 1 millisecond

bit 4 **ACTVIF:** Bus Activity Indicator bit
- 1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
- 0 = Activity has not been detected

bit 3 **SESVDIF:** Session Valid Change Indicator bit
- 1 = VBUS voltage has dropped below the session end level
- 0 = VBUS voltage has not dropped below the session end level

bit 2 **SESENDIF:** B-Device VBUS Change Indicator bit
- 1 = A change on the session end input was detected
- 0 = No change on the session end input was detected

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIF:** A-Device VBUS Change Indicator bit
- 1 = Change on the session valid input detected
- 0 = No change on the session valid input detected


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**REGISTER 10-2: U1OTGIE: USB OTG INTERRUPT ENABLE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 |
| | IDIE | T1MSECIE | LSTATEIE | ACTVIE | SESVDIE | SESENDIE | — | VBUSVDIE |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIE:** ID Interrupt Enable bit
1 = ID interrupt enabled
0 = ID interrupt disabled

bit 6 **T1MSECIE:** 1 Millisecond Timer Interrupt Enable bit
1 = 1 millisecond timer interrupt enabled
0 = 1 millisecond timer interrupt disabled

bit 5 **LSTATEIE:** Line State Interrupt Enable bit
1 = Line state interrupt enabled
0 = Line state interrupt disabled

bit 4 **ACTVIE:** Bus Activity Interrupt Enable bit
1 = ACTIVITY interrupt enabled
0 = ACTIVITY interrupt disabled

bit 3 **SESVDIE:** Session Valid Interrupt Enable bit
1 = Session valid interrupt enabled
0 = Session valid interrupt disabled

bit 2 **SESENDIE:** B-Session End Interrupt Enable bit
1 = B-session end interrupt enabled
0 = B-session end interrupt disabled

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIE:** A-VBUS Valid Interrupt Enable bit
1 = A-VBUS valid interrupt enabled
0 = A-VBUS valid interrupt disabled

**REGISTER 10-3: U1OTGSTAT: USB OTG STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R-0 | U-0 | R-0 | U-0 | R-0 | R-0 | U-0 | R-0 |
| | ID | — | LSTATE | — | SESVD | SESEND | — | VBUSVD |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **ID:** ID Pin State Indicator bit
- 1 = No cable is attached or a Type-B cable has been plugged into the USB receptacle
- 0 = A Type-A cable has been plugged into the USB receptacle

bit 6 **Unimplemented:** Read as '0'

bit 5 **LSTATE:** Line State Stable Indicator bit
- 1 = USB line state (U1CON<SE0> and U1CON<JSTATE>) has been stable for the previous 1 ms
- 0 = USB line state (U1CON<SE0> and U1CON<JSTATE>) has not been stable for the previous 1 ms

bit 4 **Unimplemented:** Read as '0'

bit 3 **SESVD:** Session Valid Indicator bit
- 1 = VBUS voltage is above Session Valid on the A or B device
- 0 = VBUS voltage is below Session Valid on the A or B device

bit 2 **SESEND:** B-Device Session End Indicator bit
- 1 = VBUS voltage is below Session Valid on the B device
- 0 = VBUS voltage is above Session Valid on the B device

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVD:** A-Device VBUS Valid Indicator bit
- 1 = VBUS voltage is above Session Valid on the A device
- 0 = VBUS voltage is below Session Valid on the A device


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**REGISTER 10-4: U1OTGCON: USB OTG CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DPPULUP | DMPULUP | DPPULDWN | DMPULDWN | VBUSON | OTGEN | VBUSCHG | VBUSDIS |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **DPPULUP:** D+ Pull-Up Enable bit
- 1 = D+ data line pull-up resistor is enabled
- 0 = D+ data line pull-up resistor is disabled

bit 6 **DMPULUP:** D- Pull-Up Enable bit
- 1 = D- data line pull-up resistor is enabled
- 0 = D- data line pull-up resistor is disabled

bit 5 **DPPULDWN:** D+ Pull-Down Enable bit
- 1 = D+ data line pull-down resistor is enabled
- 0 = D+ data line pull-down resistor is disabled

bit 4 **DMPULDWN:** D- Pull-Down Enable bit
- 1 = D- data line pull-down resistor is enabled
- 0 = D- data line pull-down resistor is disabled

bit 3 **VBUSON:** VBUS Power-on bit
- 1 = VBUS line is powered
- 0 = VBUS line is not powered

bit 2 **OTGEN:** OTG Functionality Enable bit
- 1 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under software control
- 0 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under USB hardware control

bit 1 **VBUSCHG:** VBUS Charge Enable bit
- 1 = VBUS line is charged through a pull-up resistor
- 0 = VBUS line is not charged through a resistor

bit 0 **VBUSDIS:** VBUS Discharge Enable bit
- 1 = VBUS line is discharged through a pull-down resistor
- 0 = VBUS line is not discharged through a resistor

**REGISTER 10-5: U1PWRC: USB POWER CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| | UACTPND | — | — | USLPGRD | USBBUSY | — | USUSPEND | USBPWR |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UACTPND:** USB Activity Pending bit
- 1 = USB bus activity has been detected; but an interrupt is pending, it has not been generated yet
- 0 = An interrupt is not pending

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USLPGRD:** USB Sleep Entry Guard bit
- 1 = Sleep entry is blocked if USB bus activity is detected or if a notification is pending
- 0 = USB module does not block Sleep entry

bit 3 **USBBUSY:** USB Module Busy bit(1)
- 1 = USB module is active or disabled, but not ready to be enabled
- 0 = USB module is not active and is ready to be enabled

**Note:** When USBPWR = 0 and USBBUSY = 1, status from all other registers is invalid and writes to all USB module registers produce undefined results.

bit 2 **Unimplemented:** Read as '0'

bit 1 **USUSPEND:** USB Suspend Mode bit
- 1 = USB module is placed in Suspend mode
  (The 48 MHz USB clock will be gated off. The transceiver is placed in a low-power state.)
- 0 = USB module operates normally

bit 0 **USBPWR:** USB Operation Enable bit
- 1 = USB module is turned on
- 0 = USB module is disabled
  (Outputs held inactive, device pins not used by USB, analog features are shut down to reduce power consumption.)


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**REGISTER 10-6: U1IR: USB INTERRUPT REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R-0 | R/WC-0, HS |
| | STALLIF | ATTACHIF(1) | RESUMEIF(2) | IDLEIF | TRNIF(3) | SOFIF | UERRIF(4) | URSTIF(5) / DETACHIF(6) |

| Legend: | WC = Write '1' to clear | HS = Hardware Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **STALLIF:** STALL Handshake Interrupt bit
1 = In Host mode, a STALL handshake was received during the handshake phase of the transaction
In Device mode, a STALL handshake was transmitted during the handshake phase of the transaction
0 = STALL handshake has not been sent

bit 6 **ATTACHIF:** Peripheral Attach Interrupt bit(1)
1 = Peripheral attachment was detected by the USB module
0 = Peripheral attachment was not detected

bit 5 **RESUMEIF:** Resume Interrupt bit(2)
1 = K-State is observed on the D+ or D- pin for 2.5 µs
0 = K-State is not observed

bit 4 **IDLEIF:** Idle Detect Interrupt bit
1 = Idle condition detected (constant Idle state of 3 ms or more)
0 = No Idle condition detected

bit 3 **TRNIF:** Token Processing Complete Interrupt bit(3)
1 = Processing of current token is complete; a read of the U1STAT register will provide endpoint information
0 = Processing of current token not complete

bit 2 **SOFIF:** SOF Token Interrupt bit
1 = SOF token received by the peripheral or the SOF threshold reached by the host
0 = SOF token was not received nor threshold reached

bit 1 **UERRIF:** USB Error Condition Interrupt bit(4)
1 = Unmasked error condition has occurred
0 = Unmasked error condition has not occurred

bit 0 **URSTIF:** USB Reset Interrupt bit (Device mode)(5)
1 = Valid USB Reset has occurred
0 = No USB Reset has occurred

bit 0 **DETACHIF:** USB Detach Interrupt bit (Host mode)(6)
1 = Peripheral detachment was detected by the USB module
0 = Peripheral detachment was not detected

**Note 1:** This bit is valid only if the HOSTEN bit is set (see Register 10-11), there is no activity on the USB for 2.5 µs, and the current bus state is not SE0.
**2:** When not in Suspend mode, this interrupt should be disabled.
**3:** Clearing this bit will cause the STAT FIFO to advance.
**4:** Only error conditions enabled through the U1EIE register will set this bit.
**5:** Device mode.
**6:** Host mode.

**REGISTER 10-7: U1IE: USB INTERRUPT ENABLE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | STALLIE | ATTACHIE | RESUMEIE | IDLEIE | TRNIE | SOFIE | UERRIE(1) | URSTIE(2) / DETACHIE(3) |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **STALLIE:** STALL Handshake Interrupt Enable bit
- 1 = STALL interrupt enabled
- 0 = STALL interrupt disabled

bit 6 **ATTACHIE:** ATTACH Interrupt Enable bit
- 1 = ATTACH interrupt enabled
- 0 = ATTACH interrupt disabled

bit 5 **RESUMEIE:** RESUME Interrupt Enable bit
- 1 = RESUME interrupt enabled
- 0 = RESUME interrupt disabled

bit 4 **IDLEIE:** Idle Detect Interrupt Enable bit
- 1 = Idle interrupt enabled
- 0 = Idle interrupt disabled

bit 3 **TRNIE:** Token Processing Complete Interrupt Enable bit
- 1 = TRNIF interrupt enabled
- 0 = TRNIF interrupt disabled

bit 2 **SOFIE:** SOF Token Interrupt Enable bit
- 1 = SOFIF interrupt enabled
- 0 = SOFIF interrupt disabled

bit 1 **UERRIE:** USB Error Interrupt Enable bit(1)
- 1 = USB Error interrupt enabled
- 0 = USB Error interrupt disabled

bit 0 **URSTIE:** USB Reset Interrupt Enable bit(2)
- 1 = URSTIF interrupt enabled
- 0 = URSTIF interrupt disabled

**DETACHIE:** USB Detach Interrupt Enable bit(3)
- 1 = DATTCHIF interrupt enabled
- 0 = DATTCHIF interrupt disabled

**Note 1:** For an interrupt to propagate USBIF, the UERRIE bit (U1IE<1>) must be set.
**2:** Device mode.
**3:** Host mode.


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**REGISTER 10-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS |
| | BTSEF | BMXEF | DMAEF(1) | BTOEF(2) | DFN8EF | CRC16EF | CRC5EF(4) / EOFEF(3,5) | PIDEF |

| Legend: | WC = Write '1' to clear | HS = Hardware Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEF:** Bit Stuff Error Flag bit
- 1 = Packet rejected due to bit stuff error
- 0 = Packet accepted

bit 6 **BMXEF:** Bus Matrix Error Flag bit
- 1 = The base address, of the BDT, or the address of an individual buffer pointed to by a BDT entry, is invalid.
- 0 = No address error

bit 5 **DMAEF:** DMA Error Flag bit(1)
- 1 = USB DMA error condition detected
- 0 = No DMA error

bit 4 **BTOEF:** Bus Turnaround Time-Out Error Flag bit(2)
- 1 = Bus turnaround time-out has occurred
- 0 = No bus turnaround time-out

bit 3 **DFN8EF:** Data Field Size Error Flag bit
- 1 = Data field received is not an integral number of bytes
- 0 = Data field received is an integral number of bytes

bit 2 **CRC16EF:** CRC16 Failure Flag bit
- 1 = Data packet rejected due to CRC16 error
- 0 = Data packet accepted

**Note 1:** This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.

**2:** This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.

**3:** This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.

**4:** Device mode.

**5:** Host mode.

**REGISTER 10-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER (CONTINUED)**

bit 1 **CRC5EF:** CRC5 Host Error Flag bit(4)
1 = Token packet rejected due to CRC5 error
0 = Token packet accepted
**EOFEF:** EOF Error Flag bit(3,5)
1 = EOF error condition detected
0 = No EOF error condition

bit 0 **PIDEF:** PID Check Failure Flag bit
1 = PID check failed
0 = PID check passed

**Note 1:** This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.

**2:** This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.

**3:** This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.

**4:** Device mode.

**5:** Host mode.


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**REGISTER 10-9: U1EIE: USB ERROR INTERRUPT ENABLE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BTSEE | BMXEE | DMAEE | BTOEE | DFN8EE | CRC16EE | CRC5EE(1) / EOFEE(2) | PIDEE |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEE:** Bit Stuff Error Interrupt Enable bit
- 1 = BTSEF interrupt enabled
- 0 = BTSEF interrupt disabled

bit 6 **BMXEE:** Bus Matrix Error Interrupt Enable bit
- 1 = BMXEF interrupt enabled
- 0 = BMXEF interrupt disabled

bit 5 **DMAEE:** DMA Error Interrupt Enable bit
- 1 = DMAEF interrupt enabled
- 0 = DMAEF interrupt disabled

bit 4 **BTOEE:** Bus Turnaround Time-out Error Interrupt Enable bit
- 1 = BTOEF interrupt enabled
- 0 = BTOEF interrupt disabled

bit 3 **DFN8EE:** Data Field Size Error Interrupt Enable bit
- 1 = DFN8EF interrupt enabled
- 0 = DFN8EF interrupt disabled

bit 2 **CRC16EE:** CRC16 Failure Interrupt Enable bit
- 1 = CRC16EF interrupt enabled
- 0 = CRC16EF interrupt disabled

bit 1 **CRC5EE:** CRC5 Host Error Interrupt Enable bit(1)
- 1 = CRC5EF interrupt enabled
- 0 = CRC5EF interrupt disabled

**EOFEE:** EOF Error Interrupt Enable bit(2)
- 1 = EOF interrupt enabled
- 0 = EOF interrupt disabled

bit 0 **PIDEE:** PID Check Failure Interrupt Enable bit
- 1 = PIDEF interrupt enabled
- 0 = PIDEF interrupt disabled

**Note 1:** Device mode.
**2:** Host mode.

**Note:** For an interrupt to propagate USBIF, the UERRIE bit (U1IE<1>) must be set.

**REGISTER 10-10: U1STAT: USB STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R-x | R-x | R-x | R-x | R-x | R-x | U-0 | U-0 |
| | ENDPT<3:0> | | | | DIR | PPBI | — | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-4 **ENDPT<3:0>:** Encoded Number of Last Endpoint Activity bits
(Represents the number of the BDT, updated by the last USB transfer.)

1111 = Endpoint 15
1110 = Endpoint 14
•
•
•
0001 = Endpoint 1
0000 = Endpoint 0

bit 3 **DIR:** Last BD Direction Indicator bit

1 = Last transaction was a transmit transfer (TX)
0 = Last transaction was a receive transfer (RX)

bit 2 **PPBI:** Ping-Pong BD Pointer Indicator bit

1 = The last transaction was to the ODD BD bank
0 = The last transaction was to the EVEN BD bank

bit 1-0 **Unimplemented:** Read as '0'

**Note:** The U1STAT register is a window into a 4-byte FIFO maintained by the USB module. U1STAT value is only valid when the TRNIF bit (U1IR<3>) is active. Clearing the TRNIF bit advances the FIFO. Data in register is invalid when the TRNIF bit = 0.


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**REGISTER 10-11: U1CON: USB CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R-x | R-x | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | JSTATE | SE0 | PKTDIS(4) / TOKBUSY(1,5) | USBRST | HOSTEN(2) | RESUME(3) | PPBRST | USBEN(4) / SOFEN(5) |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **JSTATE:** Live Differential Receiver JSTATE flag bit
1 = JSTATE detected on the USB
0 = No JSTATE detected

bit 6 **SE0:** Live Single-Ended Zero flag bit
1 = Single Ended Zero detected on the USB
0 = No Single Ended Zero detected

bit 5 **PKTDIS:** Packet Transfer Disable bit(4)
1 = Token and packet processing disabled (set upon SETUP token received)
0 = Token and packet processing enabled
**TOKBUSY:** Token Busy Indicator bit(1,5)
1 = Token being executed by the USB module
0 = No token being executed

bit 4 **USBRST:** Module Reset bit(5)
1 = USB reset generated
0 = USB reset terminated

bit 3 **HOSTEN:** Host Mode Enable bit(2)
1 = USB host capability enabled
0 = USB host capability disabled

bit 2 **RESUME:** RESUME Signaling Enable bit(3)
1 = RESUME signaling activated
0 = RESUME signaling disabled

**Note 1:** Software is required to check this bit before issuing another token command to the U1TOK register (see Register 10-15).
**2:** All host control logic is reset any time that the value of this bit is toggled.
**3:** Software must set the RESUME bit for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a low-speed EOP to the RESUME signaling when this bit is cleared.
**4:** Device mode.
**5:** Host mode.

**REGISTER 10-11: U1CON: USB CONTROL REGISTER (CONTINUED)**

bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
1 = Reset all Even/Odd buffer pointers to the EVEN BD banks
0 = Even/Odd buffer pointers not being Reset

bit 0 **USBEN:** USB Module Enable bit(4)
1 = USB module and supporting circuitry enabled
0 = USB module and supporting circuitry disabled

**SOFEN:** SOF Enable bit(5)
1 = SOF token sent every 1 ms
0 = SOF token disabled

**Note 1:** Software is required to check this bit before issuing another token command to the U1TOK register (see Register 10-15).
**2:** All host control logic is reset any time that the value of this bit is toggled.
**3:** Software must set the RESUME bit for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a low-speed EOP to the RESUME signaling when this bit is cleared.
**4:** Device mode.
**5:** Host mode.


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**REGISTER 10-12: U1ADDR: USB ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | LSPDEN | DEVADDR<6:0> | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPDEN:** Low Speed Enable Indicator bit
1 = Next token command to be executed at Low Speed
0 = Next token command to be executed at Full Speed

bit 6-0 **DEVADDR<6:0>:** 7-bit USB Device Address bits

**REGISTER 10-13: U1FRML: USB FRAME NUMBER LOW REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | FRML<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **FRML<7:0>:** The 11-bit Frame Number Lower bits
The register bits are updated with the current frame number whenever a SOF TOKEN is received.

**REGISTER 10-14: U1FRMH: USB FRAME NUMBER HIGH REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 |
| | — | — | — | — | — | FRMH<2:0> | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-3 **Unimplemented:** Read as '0'

bit 2-0 **FRMH<2:0>:** The Upper 3 bits of the Frame Numbers bits
The register bits are updated with the current frame number whenever a SOF TOKEN is received.

**REGISTER 10-15: U1TOK: USB TOKEN REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PID<3:0>(1) | | | | EP<3:0> | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-4 **PID<3:0>:** Token Type Indicator bits(1)
0001 = OUT (TX) token type transaction
1001 = IN (RX) token type transaction
1101 = SETUP (TX) token type transaction
**Note:** All other values are reserved and must not be used.

bit 3-0 **EP<3:0>:** Token Command Endpoint Address bits
The four bit value must specify a valid endpoint.

**Note 1:** All other values are reserved and must not be used.


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**REGISTER 10-16: U1SOF: USB SOF THRESHOLD REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CNT<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CNT<7:0>:** SOF Threshold Value bits

Typical values of the threshold are:
01001010 = 64-byte packet
00101010 = 32-byte packet
00011010 =16-byte packet
00010010 =8-byte packet

**REGISTER 10-17: U1BDTP1: USB BDT PAGE 1 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
| | BDTPTRL<15:9> | | | | | | | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-1 **BDTPTRL<15:9>:** BDT Base Address bits

This 7-bit value provides address bits 15 through 9 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

bit 0 **Unimplemented:** Read as '0'

**REGISTER 10-18: U1BDTP2: USB BDT PAGE 2 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BDTPTRH<23:16> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRH<23:16>:** BDT Base Address bits

This 8-bit value provides address bits 23 through 16 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

**REGISTER 10-19: U1BDTP3: USB BDT PAGE 3 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BDTPTRU<31:24> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRU<31:24>:** BDT Base Address bits

This 8-bit value provides address bits 31 through 24 of the BDT base address, defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.


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**REGISTER 10-20: U1CNFG1: USB CONFIGURATION 1 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 |
| | UTEYE | — | — | USBSIDL | USBSIDL | — | — | UASUSPND |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UTEYE:** USB Eye-Pattern Test Enable bit
- 1 = Eye-Pattern Test enabled
- 0 = Eye-Pattern Test disabled

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USBSIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when device enters Idle mode
- 0 = Continue module operation in Idle mode

bit 3 **LSDEV:** Low-Speed Device Enable bit
- 1 = USB module operates in Low-Speed Device mode only
- 0 = USB module operates in OTG, Host, or Full-Speed Device mode

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **UASUSPND:** Automatic Suspend Enable bit
- 1 = USB module automatically suspends upon entry to Sleep mode. See the USUSPEND bit (U1PWRC<1>) in Register 10-5.
- 0 = USB module does not automatically suspend upon entry to Sleep mode. Software must use the USUSPEND bit (U1PWRC<1>) to suspend the module, including the USB 48 MHz clock

**REGISTER 10-21: U1EP0-U1EP15: USB ENDPOINT CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | LSPD | RETRYDIS | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPD:** Low-Speed Direct Connection Enable bit (Host mode and U1EP0 only)
1 = Direct connection to a low-speed device enabled
0 = Direct connection to a low-speed device disabled; hub required with PRE_PID

bit 6 **RETRYDIS:** Retry Disable bit (Host mode and U1EP0 only)
1 = Retry NAKed transactions disabled
0 = Retry NAKed transactions enabled; retry done in hardware

bit 5 **Unimplemented:** Read as '0'

bit 4 **EPCONDIS:** Bidirectional Endpoint Control bit
If EPTXEN = 1 and EPRXEN = 1:
1 = Disable Endpoint n from Control transfers; only TX and RX transfers allowed
0 = Enable Endpoint n for Control (SETUP) transfers; TX and RX transfers also allowed
Otherwise, this bit is ignored.

bit 3 **EPRXEN:** Endpoint Receive Enable bit
1 = Endpoint n receive enabled
0 = Endpoint n receive disabled

bit 2 **EPTXEN:** Endpoint Transmit Enable bit
1 = Endpoint n transmit enabled
0 = Endpoint n transmit disabled

bit 1 **EPSTALL:** Endpoint Stall Status bit
1 = Endpoint n was stalled
0 = Endpoint n was not stalled

bit 0 **EPHSHK:** Endpoint Handshake Enable bit
1 = Endpoint Handshake enabled
0 = Endpoint Handshake disabled (typically used for isochronous endpoints)


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## 11.0 I/O PORTS

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. "I/O Ports"** (DS60001120) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

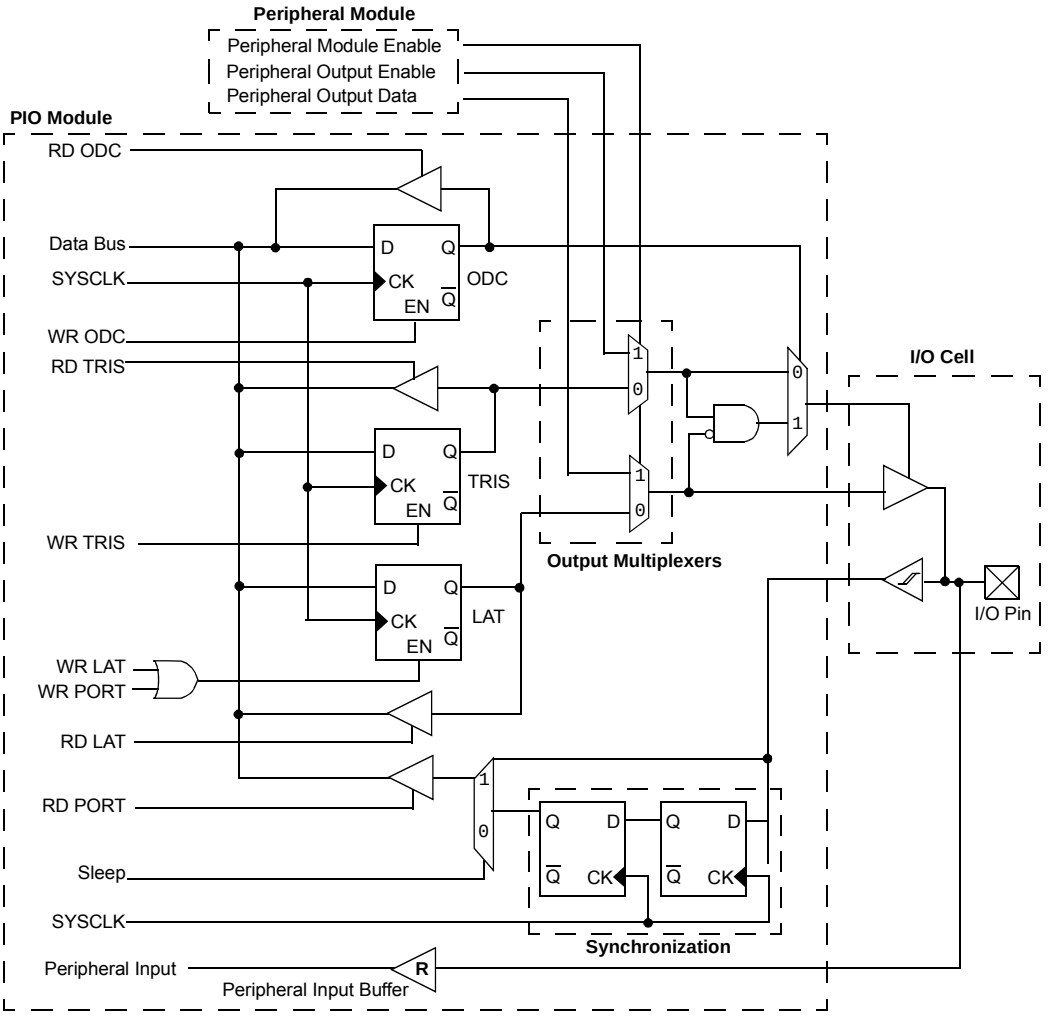
General purpose I/O pins are the simplest of peripherals. They allow the PIC® MCU to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate functions. These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

The following are the key features of this module:

- Individual output pin open-drain enable or disable
- Individual input pin weak pull-up and pull-down
- Monitor selective inputs and generate interrupt when change in pin state is detected
- Operation during CPU Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers

Figure 11-1 illustrates a block diagram of a typical multiplexed I/O port.

**FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL MULTIPLEXED PORT STRUCTURE**




**Legend:** R = Peripheral input buffer types may vary. Refer to Table 1-1 for peripheral details.

**Note:** This block diagram is a general representation of a shared port/peripheral structure for illustration purposes only. The actual structure for any specific port/peripheral combination may be different than shown here.

## 11.1 Parallel I/O (PIO) Ports

All port pins have ten registers directly associated with their operation as digital I/O. The data direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

### 11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx, and TRISx registers for data control, some port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin, regardless of the output function including PPS remapped output functions to act as an open-drain output. The only exception is the $I^2C$ pins that are open drain by default.

The open-drain feature allows the presence of outputs higher than VDD (e.g., 5V) on any desired 5V-tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

See the **"Device Pin Tables"** section for the available pins and their functionality.

### 11.1.2 CONFIGURING ANALOG AND DIGITAL PORT PINS

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs must have their corresponding ANSEL and TRIS bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default. The ANSELx register bit, when cleared, disables the corresponding digital input buffer pin(s).

If the TRIS bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or Comparator module. The TRISx bits only control the corresponding digital output buffer pin(s).

When the PORT register is read, all pins configured as analog input channels are read as cleared (a low level; i.e., when ANSELx = 1; TRISx = x).

Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

### 11.1.3 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically, this instruction would be an NOP.

### 11.1.4 INPUT CHANGE NOTIFICATION

The input Change Notification (CN) function of the I/O ports allows the PIC32MX1XX/2XX/5XX 64/100-pin devices to generate interrupt requests to the processor in response to a change-of-state on selected input pins. This feature can detect input change-of-states even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a change-of-state.

Five control registers are associated with the CN functionality of each I/O port. The CNENx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

The CNSTATx register indicates whether a change occurred on the corresponding pin since the last read of the PORTx bit.

### 11.1.5 INTERNALLY SELECTABLE PULL-UPS AND PULL-DOWNS

Each I/O pin also has a weak pull-up and every I/O pin has a weak pull-down connected to it, which are independent of any other I/O pin functionality (i.e., PPS, Open Drain, or CN). The pull-ups act as a current source or sink source connected to the pin, and eliminate the need for external resistors when push-button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

| | |
|---|---|
| **Note:** | Pull-ups and pull-downs on change notification pins should always be disabled when the port pin is configured as a digital output. They should also be disabled on 5V tolerant pins when the pin voltage can exceed VDD. |

An additional control register (CNCONx) is shown in Register 11-3.

## 11.2 CLR, SET, and INV Registers

Every I/O module register has a corresponding CLR (clear), SET (set) and INV (invert) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the affects of a write operation to a SET, CLR or INV register, the base register must be read.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## 11.3 Peripheral Pin Select

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only options.

Peripheral pin select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The peripheral pin select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. Peripheral pin select is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

### 11.3.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the peripheral pin select feature include the designation “RPn” in their full pin designation, where “RP” designates a remappable peripheral and “n” is the remappable port number.

### 11.3.2 AVAILABLE PERIPHERALS

The peripherals managed by the peripheral pin select are all digital-only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the peripheral pin select feature. This is because the peripheral’s function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include $I^2C$ among others. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

### 11.3.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral pin select features are controlled through two sets of SFRs: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral’s input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

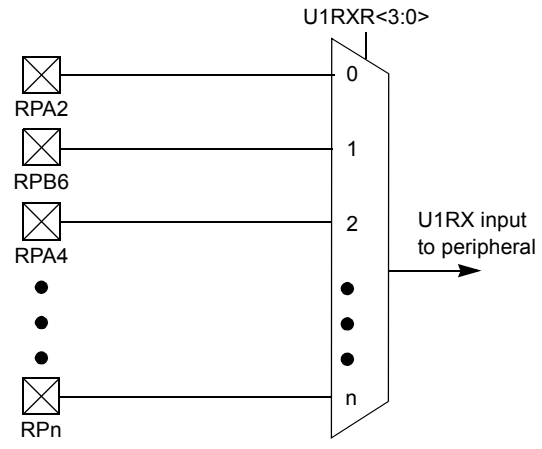
The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

### 11.3.4 INPUT MAPPING

The inputs of the peripheral pin select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The [*pin name*]R registers, where [*pin name*] refers to the peripheral pins listed in Table 11-1, are used to configure peripheral input mapping (see Register 11-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table 11-1.

For example, Figure 11-2 illustrates the remappable pin selection for the U1RX input.

**FIGURE 11-2: REMAPPABLE INPUT EXAMPLE FOR U1RX**




**Note:** For input only, peripheral pin select functionality does not have priority over TRISx settings. Therefore, when configuring RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to ‘1’).

**TABLE 11-1: INPUT PIN SELECTION**

| Peripheral Pin | [*pin name*]R SFR | [*pin name*]R bits | [*pin name*]R Value to RPn Pin Selection |
|---|---|---|---|
| INT3 | INT3R | INT3R<3:0> | 0000 = RPD2<br>0001 = RPG8<br>0010 = RPF4<br>0011 = RPD10<br>0100 = RPF1<br>0101 = RPB9<br>0110 = RPB10<br>0111 = RPC14<br>1000 = RPB5(7)<br>1001 = Reserved<br>1010 = RPC1(3)<br>1011 = RPD14(3)<br>1100 = RPG1(3)<br>1101 = RPA14(3)<br>1110 = Reserved<br>1111 = RPF2(1) |
| T2CK | T2CKR | T2CKR<3:0> | |
| IC3 | IC3R | IC3R<3:0> | |
| U1RX | U1RXR | U1RXR<3:0> | |
| U2RX | U2RXR | U2RXR<3:0> | |
| $\overline{\text{U5CTS}}$(3) | U5CTSR | U5CTSR<3:0> | |
| SDI3 | SDI3R | SDI3R<3:0> | |
| SDI4(3) | SDI4R | SDI4R<3:0> | |
| REFCLKI | REFCLKIR | REFCLKIR<3:0> | |
| INT4 | INT4R | INT4R<3:0> | 0000 = RPD3<br>0001 = RPG7<br>0010 = RPF5<br>0011 = RPD11<br>0100 = RPF0<br>0101 = RPB1<br>0110 = RPE5<br>0111 = RPC13<br>1000 = RPB3<br>1001 = RPF12(3)<br>1010 = RPC4(3)<br>1011 = RPD15(3)<br>1100 = RPG0(3)<br>1101 = RPA15(3)<br>1110 = RPF2(1)<br>1111 = RPF7(2) |
| T5CK | T5CKR | T5CKR<3:0> | |
| IC4 | IC4R | IC4R<3:0> | |
| U3RX | U3RXR | U3RXR<3:0> | |
| $\overline{\text{U4CTS}}$ | U4CTSR | U4CTSR<3:0> | |
| SDI1 | SDI1R | SDI1R<3:0> | |
| SDI2 | SDI2R | SDI2R<3:0> | |
| C1RX(5) | C1RXR(5) | C1RXR<3:0>(5) | |
| INT2 | INT2R | INT2R<3:0> | 0000 = RPD9<br>0001 = RPG6<br>0010 = RPB8<br>0011 = RPB15<br>0100 = RPD4<br>0101 = RPB0<br>0110 = RPE3<br>0111 = RPB7<br>1000 = Reserved<br>1001 = RPF12(3)<br>1010 = RPD12(3)<br>1011 = RPF8(3)<br>1100 = RPC3(3)<br>1101 = RPE9(3)<br>1110 = RPD14(3)<br>1111 = RPB2 |
| T4CK | T4CKR | T4CKR<3:0> | |
| IC2 | IC2R | IC2R<3:0> | |
| IC5 | IC5R | IC5R<3:0> | |
| $\overline{\text{U1CTS}}$ | U1CTSR | U1CTSR<3:0> | |
| $\overline{\text{U2CTS}}$ | U2CTSR | U2CTSR<3:0> | |
| $\overline{\text{SS1}}$ | SS1R | SS1R<3:0> | |
| $\overline{\text{SS3}}$ | SS3R | SS1R<3:0> | |
| $\overline{\text{SS4}}$(3) | SS3R | SS3R<3:0> | |

**Note 1:** This selection is not available on 64-pin USB devices.

**2:** This selection is only available on 100-pin General Purpose devices.

**3:** This selection is not available on 64-pin devices.

**4:** This selection is not available when USBID functionality is used on USB devices.

**5:** This selection is not available on devices without a CAN module.

**6:** This selection is not available on USB devices.

**7:** This selection is not available when VBUSON functionality is used on USB devices.


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**TABLE 11-1: INPUT PIN SELECTION (CONTINUED)**

| Peripheral Pin | [*pin name*]R SFR | [*pin name*]R bits | [*pin name*]R Value to RPn Pin Selection |
|---|---|---|---|
| INT1 | INT1R | INT1R<3:0> | 0000 = RPD1<br>0001 = RPG9<br>0010 = RPB14<br>0011 = RPD0<br>0100 = RPD8<br>0101 = RPB6<br>0110 = RPD5<br>0111 = RPB2<br>1000 = RPF3(4)<br>1001 = RPF13(3)<br>1010 = Reserved<br>1011 = RPF2(1)<br>1100 = RPC2(3)<br>1101 = RPE8(3)<br>1110 = Reserved<br>1111 = Reserved |
| T3CK | T3CKR | T3CKR<3:0> | |
| IC1 | IC1R | IC1R<3:0> | |
| $\overline{\text{U3CTS}}$ | U3CTSR | U3CTSR<3:0> | |
| U4RX | U4RXR | U4RXR<3:0> | |
| U5RX | U5RXR | U5RXR<3:0> | |
| $\overline{\text{SS2}}$ | SS2R | SS2R<3:0> | |
| OCFA | OCFAR | OCFAR<3:0> | |

**Note 1:** This selection is not available on 64-pin USB devices.

**2:** This selection is only available on 100-pin General Purpose devices.

**3:** This selection is not available on 64-pin devices.

**4:** This selection is not available when USBID functionality is used on USB devices.

**5:** This selection is not available on devices without a CAN module.

**6:** This selection is not available on USB devices.

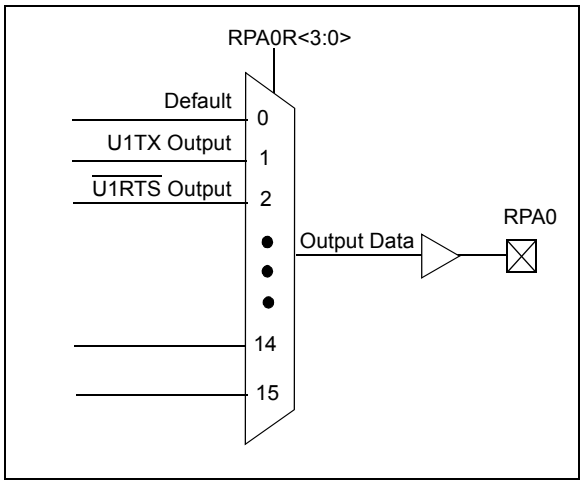
**7:** This selection is not available when VBUSON functionality is used on USB devices.

### 11.3.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the peripheral pin select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPnR registers (Register 11-2) are used to control output mapping. Like the [*pin name*]R registers, each register contains sets of 4 bit fields. The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table 11-2 and Figure 11-3).

A null output is associated with the output register reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

**FIGURE 11-3: EXAMPLE OF MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPA0**




### 11.3.6 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC32 devices include two features to prevent alterations to the peripheral map:

- Control register lock sequence
- Configuration bit select lock

#### 11.3.6.1 Control Register Lock

Under normal operation, writes to the RPnR and [*pin name*]R registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK Configuration bit (CFGCON<13>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear the IOLOCK bit, an unlock sequence must be executed. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

#### 11.3.6.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPnR and [*pin name*]R registers. The IOL1WAY Configuration bit (DEVCFG3<29>) blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure does not execute, and the peripheral pin select control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session.


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**TABLE 11-2: OUTPUT PIN SELECTION**

| RPn Port Pin | RPnR SFR | RPnR bits | RPnR Value to Peripheral Selection |
|---|---|---|---|
| RPD2 | RPD2R | RPD2R<3:0> | 0000 = No Connect<br>0001 = U3TX<br>0010 = U4RTS<br>0011 = Reserved<br>0100 = Reserved<br>0101 = Reserved<br>0110 = SDO2<br>0111 = Reserved<br>1000 = Reserved<br>1001 = Reserved<br>1010 = Reserved<br>1011 = OC3<br>1100 = C1TX(5)<br>1101 = C2OUT<br>1110 = SDO3<br>1111 = SDO4(3) |
| RPG8 | RPG8R | RPG8R<3:0> | |
| RPF4 | RPF4R | RPF4R<3:0> | |
| RPD10 | RPD10R | RPD10R<3:0> | |
| RPF1 | RPF1R | RPF1R<3:0> | |
| RPB9 | RPB9R | RPB9R<3:0> | |
| RPB10 | RPB10R | RPB10R<3:0> | |
| RPC14 | RPC14R | RPC14R<3:0> | |
| RPB5(7) | RPB5R | RPB5R<3:0> | |
| RPC1(3) | RPC1R | RPC1R<3:0> | |
| RPD14(3) | RPD14R | RPD14R<3:0> | |
| RPG1(3) | RPG1R | RPG1R<3:0> | |
| RPA14(3) | RPA14R | RPA14R<3:0> | |
| RPD3 | RPD3R | RPD3R<3:0> | 0000 = No Connect<br>0001 = U2TX<br>0010 = Reserved<br>0011 = U1TX<br>0100 = U5RTS(3)<br>0101 = Reserved<br>0110 = SDO2<br>0111 = Reserved<br>1000 = SDO1<br>1001 = Reserved<br>1010 = Reserved<br>1011 = OC4<br>1100 = Reserved<br>1101 = C3OUT<br>1110 = SDO3<br>1111 = SDO4(3) |
| RPG7 | RPG7R | RPG7R<3:0> | |
| RPF5 | RPF5R | RPF5R<3:0> | |
| RPD11 | RPD11R | RPD11R<3:0> | |
| RPF0 | RPF0R | RPF0R<3:0> | |
| RPB1 | RPB1R | RPB1R<3:0> | |
| RPE5 | RPE5R | RPE5R<3:0> | |
| RPC13 | RPC13R | RPC13R<3:0> | |
| RPB3 | RPB3R | RPB3R<3:0> | |
| RPF3(4) | RPF3R | RPF3R<3:0> | |
| RPC4(3) | RPC4R | RPC4R<3:0> | |
| RPD15(3) | RPD15R | RPD15R<3:0> | |
| RPG0(3) | RPG0R | RPG0R<3:0> | |
| RPA15(3) | RPA15R | RPA15R<3:0> | |

**Note 1:** This selection is not available on 64-pin USB devices.

**2:** This selection is only available on 100-pin General Purpose devices.

**3:** This selection is not available on 64-pin devices.

**4:** This selection is not available when USBID functionality is used on USB devices.

**5:** This selection is not available on devices without a CAN module.

**6:** This selection is not available on USB devices.

**7:** This selection is not available when VBUSON functionality is used on USB devices.

**TABLE 11-2: OUTPUT PIN SELECTION (CONTINUED)**

| RPn Port Pin | RPnR SFR | RPnR bits | RPnR Value to Peripheral Selection |
|---|---|---|---|
| RPD9 | RPD9R | RPD9R<3:0> | 0000 = No Connect<br>0001 = U3RTS<br>0010 = U4TX<br>0011 = REFCLKO<br>0100 = U5TX(3)<br>0101 = Reserved<br>0110 = Reserved<br>0111 = SS1<br>1000 = SDO1<br>1001 = Reserved<br>1010 = Reserved<br>1011 = OC5<br>1100 = Reserved<br>1101 = C1OUT<br>1110 = SS3<br>1111 = SS4(3) |
| RPG6 | RPG6R | RPG6R<3:0> | |
| RPB8 | RPB8R | RPB8R<3:0> | |
| RPB15 | RPB15R | RPB15R<3:0> | |
| RPD4 | RPD4R | RPD4R<3:0> | |
| RPB0 | RPB0R | RPB0R<3:0> | |
| RPE3 | RPE3R | RPE3R<3:0> | |
| RPB7 | RPB7R | RPB7R<3:0> | |
| RPB2 | RPB2R | RPB2R<3:0> | |
| RPF12(3) | RPF12R | RPF12R<3:0> | |
| RPD12(3) | RPD12R | RPD12R<3:0> | |
| RPF8(3) | RPF8R | RPF8R<3:0> | |
| RPC3(3) | RPC3R | RPC3R<3:0> | |
| RPE9(3) | RPE9R | RPE9R<3:0> | |
| RPD1 | RPD1R | RPD1R<3:0> | 0000 = No Connect<br>0001 = U2RTS<br>0010 = Reserved<br>0011 = U1RTS<br>0100 = U5TX(3)<br>0101 = Reserved<br>0110 = SS2<br>0111 = Reserved<br>1000 = SDO1<br>1001 = Reserved<br>1010 = Reserved<br>1011 = OC2<br>1100 = OC1<br>1101 = Reserved<br>1110 = Reserved<br>1111 = Reserved |
| RPG9 | RPG9R | RPG9R<3:0> | |
| RPB14 | RPB14R | RPB14R<3:0> | |
| RPD0 | RPD0R | RPD0R<3:0> | |
| RPD8 | RPD8R | RPD8R<3:0> | |
| RPB6 | RPB6R | RPB6R<3:0> | |
| RPD5 | RPD5R | RPD5R<3:0> | |
| RPF3(1) | RPF3R | RPF3R<3:0> | |
| RPF6(2) | RPF6R | RPF6R<3:0> | |
| RPF13(3) | RPF13R | RPF13R<3:0> | |
| RPC2(3) | RPC2R | RPC2R<3:0> | |
| RPE8(3) | RPE8R | RPE8R<3:0> | |
| RPF2(1) | RPF2R | RPF2R<3:0> | |

**Note 1:** This selection is not available on 64-pin USB devices.

**2:** This selection is only available on 100-pin General Purpose devices.

**3:** This selection is not available on 64-pin devices.

**4:** This selection is not available when USBID functionality is used on USB devices.

**5:** This selection is not available on devices without a CAN module.

**6:** This selection is not available on USB devices.

**7:** This selection is not available when VBUSON functionality is used on USB devices.


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## 11.4 Control Registers

**TABLE 11-3: PORTA REGISTER MAP 100-PIN DEVICES ONLY**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6000 | ANSELA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | ANSELA10 | ANSELA9 | — | — | — | — | — | — | — | — | — | 0060 |
| 6010 | TRISA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRISA15 | TRISA14 | — | — | — | TRISA10 | TRISA9 | — | TRISA7 | TRISA6 | TRISA5 | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | C6FF |
| 6020 | PORTA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RA15 | RA14 | — | — | — | RA10 | RA9 | — | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | xxxx |
| 6030 | LATA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LATA15 | LATA14 | — | — | — | LATA10 | LATA9 | — | LATA7 | LATA6 | LATA5 | LATA4 | LATA3 | LATA2 | LATA1 | LATA0 | xxxx |
| 6040 | ODCA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ODCA15 | ODCA14 | — | — | — | ODCA10 | ODCA9 | — | ODCA7 | ODCA6 | ODCA5 | ODCA4 | ODCA3 | ODCA2 | ODCA1 | ODCA0 | 0000 |
| 6050 | CNPUA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPUA15 | CNPUA14 | — | — | — | CNPUA10 | CNPUA9 | — | CNPUA7 | CNPUA6 | CNPUA5 | CNPUA4 | CNPUA3 | CNPUA2 | CNPUA1 | CNPUA0 | 0000 |
| 6060 | CNPDA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPDA15 | CNPDA14 | — | — | — | CNPDA10 | CNPDA9 | — | CNPDA7 | CNPDA6 | CNPDA5 | CNPDA4 | CNPDA3 | CNPDA2 | CNPDA1 | CNPDA0 | 0000 |
| 6070 | CNCONA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6080 | CNENA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNIEA15 | CNIEA14 | — | — | — | CNIEA10 | CNIEA9 | — | CNIEA7 | CNIEA6 | CNIEA5 | CNIEA4 | CNIEA3 | CNIEA2 | CNIEA1 | CNIEA0 | 0000 |
| 6090 | CNSTATA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CN STATA15 | CN STATA14 | — | — | — | CN STATA10 | CN STATA9 | — | CN STATA7 | CN STATA6 | CN STATA5 | CN STATA4 | CN STATA3 | CN STATA2 | CN STATA1 | CN STATA0 | 0000 |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

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**TABLE 11-4: PORTB REGISTER MAP**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6100 | ANSELB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ANSELB15 | ANSELB14 | ANSELB13 | ANSELB12 | ANSELB11 | ANSELB10 | ANSELB9 | ANSELB8 | ANSELB7 | ANSELB6 | ANSELB5 | ANSELB4 | ANSELB3 | ANSELB2 | ANSELB1 | ANSELB0 | FFFF |
| 6110 | TRISB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRISB15 | TRISB14 | TRISB13 | TRISB12 | TRISB11 | TRISB10 | TRISB9 | TRISB8 | TRISB7 | TRISB6 | TRISB5 | TRISB4 | TRISB3 | TRISB2 | TRISB1 | TRISB0 | FFFF |
| 6120 | PORTB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 | xxxx |
| 6130 | LATB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LATB15 | LATB14 | LATB13 | LATB12 | LATB11 | LATB10 | LATB9 | LATB8 | LATB7 | LATB6 | LATB5 | LATB4 | LATB3 | LATB2 | LATB1 | LATB0 | xxxx |
| 6140 | ODCB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ODCB15 | ODCB14 | ODCB13 | ODCB12 | ODCB11 | ODCB10 | ODCB9 | ODCB8 | ODCB7 | ODCB6 | ODCB5 | ODCB4 | ODCB3 | ODCB2 | ODCB1 | ODCB0 | 0000 |
| 6150 | CNPUB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPUB15 | CNPUB14 | CNPUB13 | CNPUB12 | CNPUB11 | CNPUB10 | CNPUB9 | CNPUB8 | CNPUB7 | CNPUB6 | CNPUB5 | CNPUB4 | CNPUB3 | CNPUB2 | CNPUB1 | CNPUB0 | 0000 |
| 6160 | CNPDB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPDB15 | CNPDB14 | CNPDB13 | CNPDB12 | CNPDB11 | CNPDB10 | CNPDB9 | CNPDB8 | CNPDB7 | CNPDB6 | CNPDB5 | CNPDB4 | CNPDB3 | CNPDB2 | CNPDB1 | CNPDB0 | 0000 |
| 6170 | CNCONB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6180 | CNENB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNIEB15 | CNIEB14 | CNIEB13 | CNIEB12 | CNIEB11 | CNIEB10 | CNIEB9 | CNIEB8 | CNIEB7 | CNIEB6 | CNIEB5 | CNIEB4 | CNIEB3 | CNIEB2 | CNIEB1 | CNIEB0 | 0000 |
| 6190 | CNSTATB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CN STATB15 | CN STATB14 | CN STATB13 | CN STATB12 | CN STATB11 | CN STATB10 | CN STATB9 | CN STATB8 | CN STATB7 | CN STATB6 | CN STATB5 | CN STATB4 | CN STATB3 | CN STATB2 | CN STATB1 | CN STATB0 | 0000 |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.



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**TABLE 11-5: PORTC REGISTER MAP FOR 100-PIN DEVICES ONLY**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6200 | ANSELC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | ANSELC3 | ANSELC2 | ANSELC1 | — | 000E |
| 6210 | TRISC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRISC15 | TRISC14 | TRISC13 | TRISC12 | — | — | — | — | — | — | — | TRISC4 | TRISC3 | TRISC2 | TRISC1 | — | FFFF |
| 6220 | PORTC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RC15 | RC14 | RC13 | RC12 | — | — | — | — | — | — | — | RC4 | RC3 | RC2 | RC1 | — | xxxx |
| 6230 | LATC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LATC15 | LATC14 | LATC13 | LATC12 | — | — | — | — | — | — | — | LATC4 | LATC3 | LATC2 | LATC1 | — | xxxx |
| 6240 | ODCC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ODCC15 | ODCC14 | ODCC13 | ODCC12 | — | — | — | — | — | — | — | ODCC4 | ODCC3 | ODCC2 | ODCC1 | — | 0000 |
| 6250 | CNPUC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPUC15 | CNPUC14 | CNPUC13 | CNPUC12 | — | — | — | — | — | — | — | CNPUC4 | CNPUC3 | CNPUC2 | CNPUC1 | — | 0000 |
| 6260 | CNPDC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPDC15 | CNPDC14 | CNPDC13 | CNPDC12 | — | — | — | — | — | — | — | CNPDC4 | CNPDC3 | CNPDC2 | CNPDC1 | — | 0000 |
| 6270 | CNCONC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6280 | CNENC | 31:16 | — | — | | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNIEC15 | CNIEC14 | CNIEC13 | CNIEC12 | — | — | — | — | — | — | — | CNIEC4 | CNIEC3 | CNIEC2 | CNIEC1 | — | 0000 |
| 6290 | CNSTATC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNSTATC15 | CNSTATC14 | CNSTATC13 | CNSTATC12 | — | — | — | — | — | — | — | CNSTATC4 | CNSTATC3 | CNSTATC2 | CNSTATC1 | — | 0000 |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

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**TABLE 11-6: PORTC REGISTER MAP FOR 64-PIN DEVICES ONLY**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6200 | ANSELC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | ANSELC3 | ANSELC2 | ANSELC1 | — | 000E |
| 6210 | TRISC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRISC15 | TRISC14 | TRISC13 | TRISC12 | — | — | — | — | — | — | — | — | — | — | — | — | F000 |
| 6220 | PORTC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RC15 | RC14 | RC13 | RC12 | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| 6230 | LATC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LATC15 | LATC14 | LATC13 | LATC12 | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| 6240 | ODCC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ODCC15 | ODCC14 | ODCC13 | ODCC12 | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6250 | CNPUC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPUC15 | CNPUC14 | CNPUC13 | CNPUC12 | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6260 | CNPDC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPDC15 | CNPDC14 | CNPDC13 | CNPDC12 | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6270 | CNCONC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6280 | CNENC | 31:16 | — | — | | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNIEC15 | CNIEC14 | CNIEC13 | CNIEC12 | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6290 | CNSTATC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNSTATC15 | CNSTATC14 | CNSTATC13 | CNSTATC12 | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.



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**TABLE 11-7: PORTD REGISTER MAP FOR 100-PIN DEVICES ONLY**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6300 | ANSELD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ANSELD15 | ANSELD14 | ANSELD13 | ANSELD12 | — | — | — | — | ANSELD7 | ANSELD6 | — | — | ANSELD3 | ANSELD2 | ANSELD1 | — | F0CE |
| 6310 | TRISD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRISD15 | TRISD14 | TRISD13 | TRISD12 | TRISD11 | TRISD10 | TRISD9 | TRISD8 | TRISD7 | TRISD6 | TRISD5 | TRISD4 | TRISD3 | TRISD2 | TRISD1 | TRISD0 | FFFF |
| 5320 | PORTD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RD15 | RD14 | RD13 | RD12 | RD11 | RD10 | RD9 | RD8 | RD7 | RD6 | RD5 | RD4 | RD3 | RD2 | RD1 | RD0 | xxxx |
| 6330 | LATD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LATD15 | LATD14 | LATD13 | LATD12 | LATD11 | LATD10 | LATD9 | LATD8 | LATD7 | LATD6 | LATD5 | LATD4 | LATD3 | LATD2 | LATD1 | LATD0 | xxxx |
| 6340 | ODCD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ODCD15 | ODCD14 | ODCD13 | ODCD12 | ODCD11 | ODCD10 | ODCD9 | ODCD8 | ODCD7 | ODCD6 | ODCD5 | ODCD4 | ODCD3 | ODCD2 | ODCD1 | ODCD0 | 0000 |
| 6350 | CNPUD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPUD15 | CNPUD14 | CNPUD13 | CNPUD12 | CNPUD11 | CNPUD10 | CNPUD9 | CNPUD8 | CNPUD7 | CNPUD6 | CNPUD5 | CNPUD4 | CNPUD3 | CNPUD2 | CNPUD1 | CNPUD0 | 0000 |
| 6360 | CNPDD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPDD15 | CNPDD14 | CNPDD13 | CNPDD12 | CNPDD11 | CNPDD10 | CNPDD9 | CNPDD8 | CNPDD7 | CNPDD6 | CNPDD5 | CNPDD4 | CNPDD3 | CNPDD2 | CNPDD1 | CNPDD0 | 0000 |
| 6370 | CNCOND | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6380 | CNEND | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNIED15 | CNIED14 | CNIED13 | CNIED12 | CNIED11 | CNIED10 | CNIED9 | CNIED8 | CNIED7 | CNIED6 | CNIED5 | CNIED4 | CNIED3 | CNIED2 | CNIED1 | CNIED0 | 0000 |
| 6390 | CNSTATD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNS TATD15 | CN STATD14 | CN STATD13 | CN STATD12 | CN STATD11 | CN STATD10 | CN STATD9 | CN STATD8 | CN STATD7 | CN STATD6 | CN STATD5 | CN STATD4 | CN STATD3 | CN STATD2 | CN STATD1 | CN STATD0 | 0000 |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

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**TABLE 11-8: PORTD REGISTER MAP FOR 64-PIN DEVICES ONLY**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6300 | ANSELD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | ANSELD3 | ANSELD2 | ANSELD1 | — | 000E |
| 6310 | TRISD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | TRISD11 | TRISD10 | TRISD9 | TRISD8 | TRISD7 | TRISD6 | TRISD5 | TRISD4 | TRISD3 | TRISD2 | TRISD1 | TRISD0 | 0FFF |
| 5320 | PORTD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | RD11 | RD10 | RD9 | RD8 | RD7 | RD6 | RD5 | RD4 | RD3 | RD2 | RD1 | RD0 | xxxx |
| 6330 | LATD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | LATD11 | LATD10 | LATD9 | LATD8 | LATD7 | LATD6 | LATD5 | LATD4 | LATD3 | LATD2 | LATD1 | LATD0 | xxxx |
| 6340 | ODCD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | ODCD11 | ODCD10 | ODCD9 | ODCD8 | ODCD7 | ODCD6 | ODCD5 | ODCD4 | ODCD3 | ODCD2 | ODCD1 | ODCD0 | 0000 |
| 6350 | CNPUD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | CNPUD11 | CNPUD10 | CNPUD9 | CNPUD8 | CNPUD7 | CNPUD6 | CNPUD5 | CNPUD4 | CNPUD3 | CNPUD2 | CNPUD1 | CNPUD0 | 0000 |
| 6360 | CNPDD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | CNPDD11 | CNPDD10 | CNPDD9 | CNPDD8 | CNPDD7 | CNPDD6 | CNPDD5 | CNPDD4 | CNPDD3 | CNPDD2 | CNPDD1 | CNPDD0 | 0000 |
| 6370 | CNCOND | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6380 | CNEND | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | CNIED11 | CNIED10 | CNIED9 | CNIED8 | CNIED7 | CNIED6 | CNIED5 | CNIED4 | CNIED3 | CNIED2 | CNIED1 | CNIED0 | 0000 |
| 6390 | CNSTATD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | CN STATD11 | CN STATD10 | CN STATD9 | CN STATD8 | CN STATD7 | CN STATD6 | CN STATD5 | CN STATD4 | CN STATD3 | CN STATD2 | CN STATD1 | CN STATD0 | 0000 |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.



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**TABLE 11-9: PORTE REGISTER MAP FOR 100-PIN DEVICES ONLY**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6400 | ANSELE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | ANSELE9 | ANSELE8 | ANSELE7 | ANSELE6 | ANSELE5 | ANSELE4 | — | ANSELE2 | ANSELE1 | ANSELE0 | 03F7 |
| 6410 | TRISE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | TRISE9 | TRISE8 | TRISE7 | TRISE6 | TRISE5 | TRISE4 | TRISE3 | TRISE2 | TRISE1 | TRISE0 | 03FF |
| 6420 | PORTE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | RE9 | RE8 | RE7 | RE6 | RE5 | RE4 | RE3 | RE2 | RE1 | RE0 | xxxx |
| 6440 | LATE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | LATE9 | LATE8 | LATE7 | LATE6 | LATE5 | LATE4 | LATE3 | LATE2 | LATE1 | LATE0 | xxxx |
| 6440 | ODCE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | ODCE9 | ODCE8 | ODCE7 | ODCE6 | ODCE5 | ODCE4 | ODCE3 | ODCE2 | ODCE1 | ODCE0 | 0000 |
| 6450 | CNPUE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CNPUE9 | CNPUE8 | CNPUE7 | CNPUE6 | CNPUE5 | CNPUE4 | CNPDE3 | CNPUE2 | CNPUE1 | CNPUE0 | 0000 |
| 6460 | CNPDE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CNPDE9 | CNPDE8 | CNPDE7 | CNPDE6 | CNPDE5 | CNPDE4 | CNPDE3 | CNPDE2 | CNPDE1 | CNPDE0 | 0000 |
| 6470 | CNCONE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6480 | CNENE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CNIEE9 | CNIEE8 | CNIEE7 | CNIEE6 | CNIEE5 | CNIEE4 | CNIEE3 | CNIEE2 | CNIEE1 | CNIEE0 | 0000 |
| 6490 | CNSTATE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CN STATE9 | CN STATE8 | CN STATE7 | CN STATE6 | CN STATE5 | CN STATE4 | CN STATE3 | CN STATE2 | CN STATE1 | CN STATE0 | 0000 |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

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**TABLE 11-10: PORTE REGISTER MAP FOR 64-PIN DEVICES ONLY**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6400 | ANSELE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | ANSELE7 | ANSELE6 | ANSELE5 | ANSELE4 | — | ANSELE2 | — | — | 03F4 |
| 6410 | TRISE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | TRISE7 | TRISE6 | TRISE5 | TRISE4 | TRISE3 | TRISE2 | TRISE1 | TRISE0 | 00FF |
| 6420 | PORTE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | RE7 | RE6 | RE5 | RE4 | RE3 | RE2 | RE1 | RE0 | xxxx |
| 6440 | LATE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | LATE7 | LATE6 | LATE5 | LATE4 | LATE3 | LATE2 | LATE1 | LATE0 | xxxx |
| 6440 | ODCE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | ODCE7 | ODCE6 | ODCE5 | ODCE4 | ODCE3 | ODCE2 | ODCE1 | ODCE0 | 0000 |
| 6450 | CNPUE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CNPUE7 | CNPUE6 | CNPUE5 | CNPUE4 | CNPDE3 | CNPUE2 | CNPUE1 | CNPUE0 | 0000 |
| 6460 | CNPDE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CNPDE7 | CNPDE6 | CNPDE5 | CNPDE4 | CNPDE3 | CNPDE2 | CNPDE1 | CNPDE0 | 0000 |
| 6470 | CNCONE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6480 | CNENE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CNIEE7 | CNIEE6 | CNIEE5 | CNIEE4 | CNIEE3 | CNIEE2 | CNIEE1 | CNIEE0 | 0000 |
| 6490 | CNSTATE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CN STATE7 | CN STATE6 | CN STATE5 | CN STATE4 | CN STATE3 | CN STATE2 | CN STATE1 | CN STATE0 | 0000 |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.



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**TABLE 11-11: PORTF REGISTER MAP FOR PIC32MX130F128L, PIC32MX150F256L, AND PIC32MX170F512L DEVICES ONLY**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6500 | ANSELF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | ANSELE13 | ANSELE12 | — | — | — | ANSELE8 | — | — | — | — | — | ANSELE2 | ANSELE1 | ANSELE0 | 3107 |
| 6510 | TRISF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | TRISF13 | TRISF12 | — | — | — | TRISF8 | TRISF7 | TRISF6 | TRISF5 | TRISF4 | TRISF3 | TRISF2 | TRISF1 | TRISF0 | 31FF |
| 6520 | PORTF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | RF13 | RF12 | — | — | — | RF8 | RF7 | RF6 | RF5 | RF4 | RF3 | RF2 | RF1 | RF0 | xxxx |
| 6530 | LATF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | LATF13 | LATF12 | — | — | — | LATF8 | LATF7 | LATF6 | LATF5 | LATF4 | LATF3 | LATF2 | LATF1 | LATF0 | xxxx |
| 6540 | ODCF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | ODCF13 | ODCF12 | — | — | — | ODCF8 | ODCF7 | ODCF6 | ODCF5 | ODCF4 | ODCF3 | ODCF2 | ODCF1 | ODCF0 | 0000 |
| 6550 | CNPUF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | CNPUF13 | CNPUF12 | — | — | — | CNPUF8 | CNPUF7 | CNPUF6 | CNPUF5 | CNPUF4 | CNPDF3 | CNPUF2 | CNPUF1 | CNPUF0 | 0000 |
| 6560 | CNPDF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | CNPDF13 | CNPDF12 | — | — | — | CNPDF8 | CNPDF7 | CNPDF6 | CNPDF5 | CNPDF4 | CNPDF3 | CNPDF2 | CNPDF1 | CNPDF0 | 0000 |
| 6570 | CNCONF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6580 | CNENF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | CNIEF13 | CNIEF12 | — | — | — | CNIEF8 | CNIEF7 | CNIEF6 | CNIEF5 | CNIEF4 | CNIEF3 | CNIEF2 | CNIEF1 | CNIEF0 | 0000 |
| 6590 | CNSTATF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | CN STATF13 | CN STATF12 | — | — | — | CN STATF8 | CN STATF7 | CN STATF6 | CN STATF5 | CN STATF4 | CN STATF3 | CN STATF2 | CN STATF1 | CN STATF0 | 0000 |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

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**TABLE 11-12: PORTF REGISTER MAP FOR PIC32MX230F128L, PIC32MX530F128L, PIC32MX250F256L, PIC32MX550F256L, PIC32MX270F512L, AND PIC32MX570F512L DEVICES ONLY**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6500 | ANSELF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | ANSELE13 | ANSELE12 | — | — | — | ANSELE8 | — | — | — | — | — | ANSELE2 | ANSELE1 | ANSELE0 | 3107 |
| 6510 | TRISF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | TRISF13 | TRISF12 | — | — | — | TRISF8 | — | — | TRISF5 | TRISF4 | TRISF3 | TRISF2 | TRISF1 | TRISF0 | 313F |
| 6520 | PORTF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | RF13 | RF12 | — | — | — | RF8 | — | — | RF5 | RF4 | RF3 | RF2 | RF1 | RF0 | xxxx |
| 6530 | LATF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | LATF13 | LATF12 | — | — | — | LATF8 | — | — | LATF5 | LATF4 | LATF3 | LATF2 | LATF1 | LATF0 | xxxx |
| 6540 | ODCF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | ODCF13 | ODCF12 | — | — | — | ODCF8 | — | — | ODCF5 | ODCF4 | ODCF3 | ODCF2 | ODCF1 | ODCF0 | 0000 |
| 6550 | CNPUF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | CNPUF13 | CNPUF12 | — | — | — | CNPUF8 | — | — | CNPUF5 | CNPUF4 | CNPDF3 | CNPUF2 | CNPUF1 | CNPUF0 | 0000 |
| 6560 | CNPDF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | CNPDF13 | CNPDF12 | — | — | — | CNPDF8 | — | — | CNPDF5 | CNPFF4 | CNPDF3 | CNPDF2 | CNPDF1 | CNPDF0 | 0000 |
| 6570 | CNCONF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6580 | CNENF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | CNIEF13 | CNIEF12 | — | — | — | CNIEF8 | — | — | CNIEF5 | CNIEF4 | CNIEF3 | CNIEF2 | CNIEF1 | CNIEF0 | 0000 |
| 6590 | CNSTATF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | CN STATF13 | CN STATF12 | — | — | — | CN STATF8 | — | — | CN STATF5 | CN STATF4 | CN STATF3 | CN STATF2 | CN STATF1 | CN STATF0 | 0000 |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.



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**TABLE 11-13: PORTF REGISTER MAP FOR PIC32MX120F064H, PIC32MX130F128H, PIC32MX150F256H, AND PIC32MX170F512H DEVICES ONLY**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6510 | TRISF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | TRISF6 | TRISF5 | TRISF4 | TRISF3 | TRISF2 | TRISF1 | TRISF0 | 007F |
| 6520 | PORTF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | RF6 | RF5 | RF4 | RF3 | RF2 | RF1 | RF0 | xxxx |
| 6530 | LATF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | LATF6 | LATF5 | LATF4 | LATF3 | LATF2 | LATF1 | LATF0 | xxxx |
| 6540 | ODCF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | ODCF6 | ODCF5 | ODCF4 | ODCF3 | ODCF2 | ODCF1 | ODCF0 | 0000 |
| 6550 | CNPUF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | CNPUF6 | CNPUF5 | CNPUF4 | CNPUF3 | CNPUF2 | CNPUF1 | CNPUF0 | 0000 |
| 6560 | CNPDF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | CNPDF6 | CNPDF5 | CNPDF4 | CNPDF3 | CNPDF2 | CNPDF1 | CNPDF0 | 0000 |
| 6570 | CNCONF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6580 | CNENF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | CNIEF6 | CNIEF5 | CNIEF4 | CNIEF3 | CNIEF2 | CNIEF1 | CNIEF0 | 0000 |
| 6590 | CNSTATF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | CN STATF6 | CN STATF5 | CN STATF4 | CN STATF3 | CN STATF2 | CN STATF1 | CN STATF0 | 0000 |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

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**TABLE 11-14: PORTF REGISTER MAP FOR PIC32MX230F128H, PIC32MX530F128H, PIC32MX250F256H, PIC32MX550F256H, PIC32MX270F512H, AND PIC32MX570F512H DEVICES ONLY**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6510 | TRISF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | TRISF5 | TRISF4 | TRISF3 | — | TRISF1 | TRISF0 | 003B |
| 6520 | PORTF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | RF5 | RF4 | RF3 | — | RF1 | RF0 | xxxx |
| 6530 | LATF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | LATF5 | LATF4 | LATF3 | — | LATF1 | LATF0 | xxxx |
| 6540 | ODCF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | ODCF5 | ODCF4 | ODCF3 | — | ODCF1 | ODCF0 | 0000 |
| 6550 | CNPUF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | CNPUF5 | CNPUF4 | CNPUF3 | — | CNPUF1 | CNPUF0 | 0000 |
| 6560 | CNPDF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | CNPDF5 | CNPDF4 | CNPDF3 | — | CNPDF1 | CNPDF0 | 0000 |
| 6570 | CNCONF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6580 | CNENF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | CNIEF5 | CNIEF4 | CNIEF3 | — | CNIEF1 | CNIEF0 | 0000 |
| 6590 | CNSTATF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | CN STATF5 | CN STATF4 | CN STATF3 | — | CN STATF1 | CN STATF0 | 0000 |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.



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**TABLE 11-15: PORTG REGISTER MAP FOR 100-PIN DEVICES ONLY**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6600 | ANSELG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ANSELG15 | — | — | — | — | — | ANSELG9 | ANSELG8 | ANSELG7 | ANSELG6 | — | — | — | — | — | — | 83C0 |
| 6610 | TRISG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRISG15 | TRISG14 | TRISG13 | TRISG12 | — | — | TRISG9 | TRISG8 | TRISG7 | TRISG6 | — | — | TRISG3 | TRISG2 | TRISG1 | TRISG0 | F3CF |
| 6620 | PORTG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RG15 | RG14 | RG13 | RG12 | — | — | RG9 | RG8 | RG7 | RG6 | — | — | RG3(2) | RG2(2) | RG1 | RG0 | xxxx |
| 6630 | LATG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LATG15 | LATG14 | LATG13 | LATG12 | — | — | LATG9 | LATG8 | LATG7 | LATG6 | — | — | LATG3 | LATG2 | LATG1 | LATG0 | xxxx |
| 6640 | ODCG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ODCG15 | ODCG14 | ODCG13 | ODCG12 | — | — | ODCG9 | ODCG8 | ODCG7 | ODCG6 | — | — | ODCG3 | ODCG2 | ODCG1 | ODCG0 | 0000 |
| 6650 | CNPUG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPUG15 | CNPUG14 | CNPUG13 | CNPUG12 | — | — | CNPUG9 | CNPUG8 | CNPUG7 | CNPUG6 | — | — | CNPUG3 | CNPUG2 | CNPUG1 | CNPUG0 | 0000 |
| 6660 | CNPDG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPDG15 | CNPDG14 | CNPDG13 | CNPDG12 | — | — | CNPDG9 | CNPDG8 | CNPDG7 | CNPDG6 | — | — | CNPDG3 | CNPDG2 | CNPDG1 | CNPDG0 | 0000 |
| 6670 | CNCONG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6680 | CNENG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNIEG15 | CNIEG14 | CNIEG13 | CNIEG12 | — | — | CNIEG9 | CNIEG8 | CNIEG7 | CNIEG6 | — | — | CNIEG3 | CNIEG2 | CNIEG1 | CNIEG0 | 0000 |
| 6690 | CNSTATG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CN STATG15 | CN STATG14 | CN STATG13 | CN STATG12 | — | — | CN STATG9 | CN STATG8 | CN STATG7 | CN STATG6 | — | — | CN STATG3 | CN STATG2 | CN STATG1 | CN STATG0 | 0000 |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

**2:** This bit is only available on devices without a USB module.

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**TABLE 11-16: PORTG REGISTER MAP FOR 64-PIN DEVICES ONLY**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6600 | ANSELG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | ANSELG9 | ANSELG8 | ANSELG7 | ANSELG6 | — | — | — | — | — | — | 03C0 |
| 6610 | TRISG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | TRISG9 | TRISG8 | TRISG7 | TRISG6 | — | — | TRISG3 | TRISG2 | — | — | 03CC |
| 6620 | PORTG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | RG9 | RG8 | RG7 | RG6 | — | — | RG3(2) | RG2(2) | — | — | xxxx |
| 6630 | LATG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | LATG9 | LATG8 | LATG7 | LATG6 | — | — | LATG3 | LATG2 | — | — | xxxx |
| 6640 | ODCG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | ODCG9 | ODCG8 | ODCG7 | ODCG6 | — | — | ODCG3 | ODCG2 | — | — | 0000 |
| 6650 | CNPUG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CNPUG9 | CNPUG8 | CNPUG7 | CNPUG6 | — | — | CNPUG3 | CNPUG2 | — | — | 0000 |
| 6660 | CNPDG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CNPDG9 | CNPDG8 | CNPDG7 | CNPDG6 | — | — | CNPDG3 | CNPDG2 | — | — | 0000 |
| 6670 | CNCONG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6680 | CNENG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CNIEG9 | CNIEG8 | CNIEG7 | CNIEG6 | — | — | CNIEG3 | CNIEG2 | — | — | 0000 |
| 6690 | CNSTATG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CN STATG9 | CN STATG8 | CN STATG7 | CN STATG6 | — | — | CN STATG3 | CN STATG2 | — | — | 0000 |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

**2:** This bit is only available on devices without a USB module.



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**TABLE 11-17: PERIPHERAL PIN SELECT INPUT REGISTER MAP**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| FA04 | INT1R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | INT1R<3:0> | | | | 0000 |
| FA08 | INT2R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | INT2R<3:0> | | | | 0000 |
| FA0C | INT3R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | INT3R<3:0> | | | | 0000 |
| FA10 | INT4R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | INT4R<3:0> | | | | 0000 |
| FA18 | T2CKR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | T2CKR<3:0> | | | | 0000 |
| FA1C | T3CKR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | T3CKR<3:0> | | | | 0000 |
| FA20 | T4CKR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | T4CKR<3:0> | | | | 0000 |
| FA24 | T5CKR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | T5CKR<3:0> | | | | 0000 |
| FA28 | IC1R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | IC1R<3:0> | | | | 0000 |
| FA2C | IC2R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | IC2R<3:0> | | | | 0000 |
| FA30 | IC3R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | IC3R<3:0> | | | | 0000 |
| FA34 | IC4R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | IC4R<3:0> | | | | 0000 |
| FA38 | IC5R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | IC5R<3:0> | | | | 0000 |
| FA48 | OCFAR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | OCFAR<3:0> | | | | 0000 |
| FA50 | U1RXR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | U1RXR<3:0> | | | | 0000 |
| FA54 | U1CTSR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | U1CTSR<3:0> | | | | 0000 |
| FA58 | U2RXR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | U2RXR<3:0> | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 11-17: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| FA5C | U2CTSR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | U2CTSR<3:0> | | | | 0000 |
| FA60 | U3RXR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | U3RXR<3:0> | | | | 0000 |
| FA64 | U3CTSR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | U3CTSR<3:0> | | | | 0000 |
| FA68 | U4RXR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | U4RXR<3:0> | | | | 0000 |
| FA6C | U4CTSR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | U4CTSR<3:0> | | | | 0000 |
| FA70 | U5RXR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | U5RXR<3:0> | | | | 0000 |
| FA74 | U5CTSR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | U5CTSR<3:0> | | | | 0000 |
| FA84 | SDI1R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | SDI1R<3:0> | | | | 0000 |
| FA88 | SS1R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | SS1R<3:0> | | | | 0000 |
| FA90 | SDI2R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | SDI2R<3:0> | | | | 0000 |
| FA94 | SS2R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | SS2R<3:0> | | | | 0000 |
| FA9C | SDI3R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | SDI3R<3:0> | | | | 0000 |
| FAA0 | SS3R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | SS3R<3:0> | | | | 0000 |
| FAA8 | SDI4R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | SDI4R<3:0> | | | | 0000 |
| FAAC | SS4R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | SS4R<3:0> | | | | 0000 |
| FAC8 | C1RXR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | C1RXR<3:0> | | | | 0000 |
| FAD0 | REFCLKIR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | REFCLKIR<3:0> | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 11-18: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| FB38 | RPA14R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPA14<3:0> | | | | 0000 |
| FB3C | RPA15R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPA15<3:0> | | | | 0000 |
| FB40 | RPB0R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB0<3:0> | | | | 0000 |
| FB44 | RPB1R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB1<3:0> | | | | 0000 |
| FB48 | RPB2R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB2<3:0> | | | | 0000 |
| FB4C | RPB3R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB3<3:0> | | | | 0000 |
| FB54 | RPB5R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB5<3:0> | | | | 0000 |
| FB58 | RPB6R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB6<3:0> | | | | 0000 |
| FB5C | RPB7R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB7<3:0> | | | | 0000 |
| FB60 | RPB8R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB8<3:0> | | | | 0000 |
| FB64 | RPB9R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB9<3:0> | | | | 0000 |
| FB68 | RPB10R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB10<3:0> | | | | 0000 |
| FB78 | RPB14R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB14<3:0> | | | | 0000 |
| FB7C | RPB15R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB15<3:0> | | | | 0000 |
| FB84 | RPC1R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPC1<3:0> | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register is not available if the associated RPx function is not present on the device. Refer to the pin table for the specific device to determine availability.

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**TABLE 11-18: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| FB88 | RPC2R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPC2<3:0> | | | | 0000 |
| FB8C | RPC3R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPC3<3:0> | | | | 0000 |
| FB90 | RPC4R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPC4<3:0> | | | | 0000 |
| FBB4 | RPC13R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPC13<3:0> | | | | 0000 |
| FBB8 | RPC14R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPC14<3:0> | | | | 0000 |
| FBC0 | RPD0R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPD0<3:0> | | | | 0000 |
| FBC4 | RPD1R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPD1<3:0> | | | | 0000 |
| FBC8 | RPD2R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPD2<3:0> | | | | 0000 |
| FBCC | RPD3R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPD3<3:0> | | | | 0000 |
| FBD0 | RPD4R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPD4<3:0> | | | | 0000 |
| FBD4 | RPD5R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPD5<3:0> | | | | 0000 |
| FBE0 | RPD8R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPD8<3:0> | | | | 0000 |
| FBE4 | RPD9R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPD9<3:0> | | | | 0000 |
| FBE8 | RPD10R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPD10<3:0> | | | | 0000 |
| FBEC | RPD11R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPD11<3:0> | | | | 0000 |
| FBF0 | RPD12R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPD12<3:0> | | | | 0000 |
| FBF8 | RPD14R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPD14<3:0> | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register is not available if the associated RPx function is not present on the device. Refer to the pin table for the specific device to determine availability.



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**TABLE 11-18: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| FBFC | RPD15R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPD15<3:0> | | | | 0000 |
| FC0C | RPE3R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPE3<3:0> | | | | 0000 |
| FC14 | RPE5R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPE5<3:0> | | | | 0000 |
| FC20 | RPE8R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPE8<3:0> | | | | 0000 |
| FC24 | RPE9R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPE9<3:0> | | | | 0000 |
| FC40 | RPF0R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPF0<3:0> | | | | 0000 |
| FC44 | RPF1R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPF1<3:0> | | | | 0000 |
| FC48 | RPF2R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPF2<3:0> | | | | 0000 |
| FC4C | RPF3R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPF3<3:0> | | | | 0000 |
| FC50 | RPF4R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPF4<3:0> | | | | 0000 |
| FC54 | RPF5R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPF5<3:0> | | | | 0000 |
| FC58 | RPF6R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPF6<3:0> | | | | 0000 |
| FC5C | RPF7R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPF6<3:0> | | | | 0000 |
| FC60 | RPF8R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPF7<3:0> | | | | 0000 |
| FC70 | RPF12R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPF12<3:0> | | | | 0000 |
| FC74 | RPF13R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPF13<3:0> | | | | 0000 |
| FC80 | RPG0R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPG0<3:0> | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register is not available if the associated RPx function is not present on the device. Refer to the pin table for the specific device to determine availability.

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**TABLE 11-18: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| FC84 | RPG1R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPG1<3:0> | | | | 0000 |
| FC98 | RPG6R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPG6<3:0> | | | | 0000 |
| FC9C | RPG7R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPG7<3:0> | | | | 0000 |
| FCA0 | RPG8R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPG8<3:0> | | | | 0000 |
| FCA4 | RPG9R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPG9<3:0> | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register is not available if the associated RPx function is not present on the device. Refer to the pin table for the specific device to determine availability.



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**REGISTER 11-1: [*pin name*]R: PERIPHERAL PIN SELECT INPUT REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | [*pin name*]R<3:0> | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-4 **Unimplemented:** Read as '0'

bit 3-0 **[*pin name*]R<3:0>:** Peripheral Pin Select Input bits
Where [*pin name*] refers to the pins that are used to configure peripheral input mapping. See Table 11-1 for input pin selection values.

**Note:** Register values can only be changed if the IOLOCK Configuration bit (CFGCON<13>) = 0.

**REGISTER 11-2: RPnR: PERIPHERAL PIN SELECT OUTPUT REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | RPnR<3:0> | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-4 **Unimplemented:** Read as '0'

bit 3-0 **RPnR<3:0>:** Peripheral Pin Select Output bits
See Table 11-2 for output pin selection values.

**Note:** Register values can only be changed if the IOLOCK Configuration bit (CFGCON<13>) = 0.

**REGISTER 11-3: CNCONx: CHANGE NOTICE CONTROL FOR PORTx REGISTER (x = A – G)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ON | — | SIDL | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Change Notice (CN) Control ON bit
- 1 = CN is enabled
- 0 = CN is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit
- 1 = CPU Idle Mode halts CN operation
- 0 = CPU Idle does not affect CN operation

bit 12-0 **Unimplemented:** Read as '0'


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## 12.0 TIMER1

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

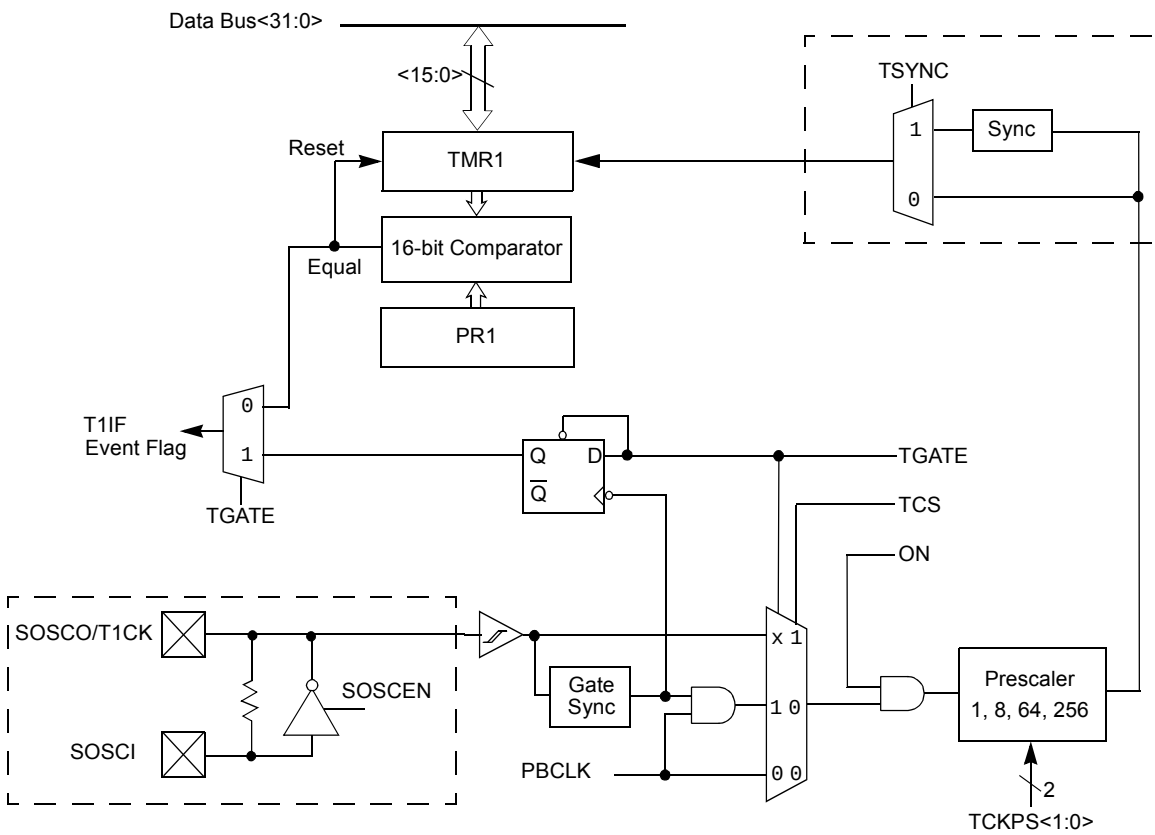
This family of PIC32 devices features one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can also be used with the Low-Power Secondary Oscillator (SOSC) for Real-Time Clock (RTC) applications. The following modes are supported:

- Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

### 12.1 Additional Supported Features

- Selectable clock prescaler
- Timer operation during CPU Idle and Sleep mode
- Fast bit manipulation using CLR, SET and INV registers
- Asynchronous mode can be used with the SOSC to function as a Real-Time Clock (RTC)

**FIGURE 12-1: TIMER1 BLOCK DIAGRAM**




**Note:** The default state of the SOSCEN (OSCCON<1>) bit during a device Reset is controlled by the FSOSCEN bit in Configuration Word, DEVCFG1.

## 12.2 Control Registers

**TABLE 12-1: TIMER1 REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0600 | T1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | TWDIS | TWIP | — | — | — | TGATE | — | TCKPS<1:0> | | — | TSYNC | TCS | — | 0000 |
| 0610 | TMR1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR1<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0620 | PR1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR1<15:0> | | | | | | | | | | | | | | | | FFFF |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.



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**REGISTER 12-1: T1CON: TYPE A TIMER CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R-0 | U-0 | U-0 | U-0 |
| | ON(1) | — | SIDL | TWDIS | TWIP | — | — | — |
| 7:0 | R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 |
| | TGATE | — | TCKPS<1:0> | | — | TSYNC | TCS | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit(1)
- 1 = Timer is enabled
- 0 = Timer is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue operation when device enters Idle mode
- 0 = Continue operation even in Idle mode

bit 12 **TWDIS:** Asynchronous Timer Write Disable bit
- 1 = Writes to TMR1 are ignored until pending write operation completes
- 0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)

bit 11 **TWIP:** Asynchronous Timer Write in Progress bit

In Asynchronous Timer mode:
- 1 = Asynchronous write to TMR1 register in progress
- 0 = Asynchronous write to TMR1 register complete

In Synchronous Timer mode:
This bit is read as '0'.

bit 10-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit

When TCS = 1:
This bit is ignored.

When TCS = 0:
- 1 = Gated time accumulation is enabled
- 0 = Gated time accumulation is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5-4 **TCKPS<1:0>:** Timer Input Clock Prescale Select bits
- 11 = 1:256 prescale value
- 10 = 1:64 prescale value
- 01 = 1:8 prescale value
- 00 = 1:1 prescale value

bit 3 **Unimplemented:** Read as '0'

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**REGISTER 12-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)**

bit 2 **TSYNC:** Timer External Clock Input Synchronization Selection bit

When TCS = 1:

1 = External clock input is synchronized

0 = External clock input is not synchronized

When TCS = 0:

This bit is ignored.

bit 1 **TCS:** Timer Clock Source Select bit

1 = External clock from TxCKI pin

0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.


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## 13.0 TIMER2/3, TIMER4/5

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

This family of PIC32 devices features four synchronous 16-bit timers (default) that can operate as a free-running interval timer for various timing applications and counting external events. The following modes are supported:

- Synchronous internal 16-bit timer
- Synchronous internal 16-bit gated timer
- Synchronous external 16-bit timer

Two 32-bit synchronous timers are available by combining Timer2 with Timer3 and Timer4 with Timer5. The 32-bit timers can operate in three modes:

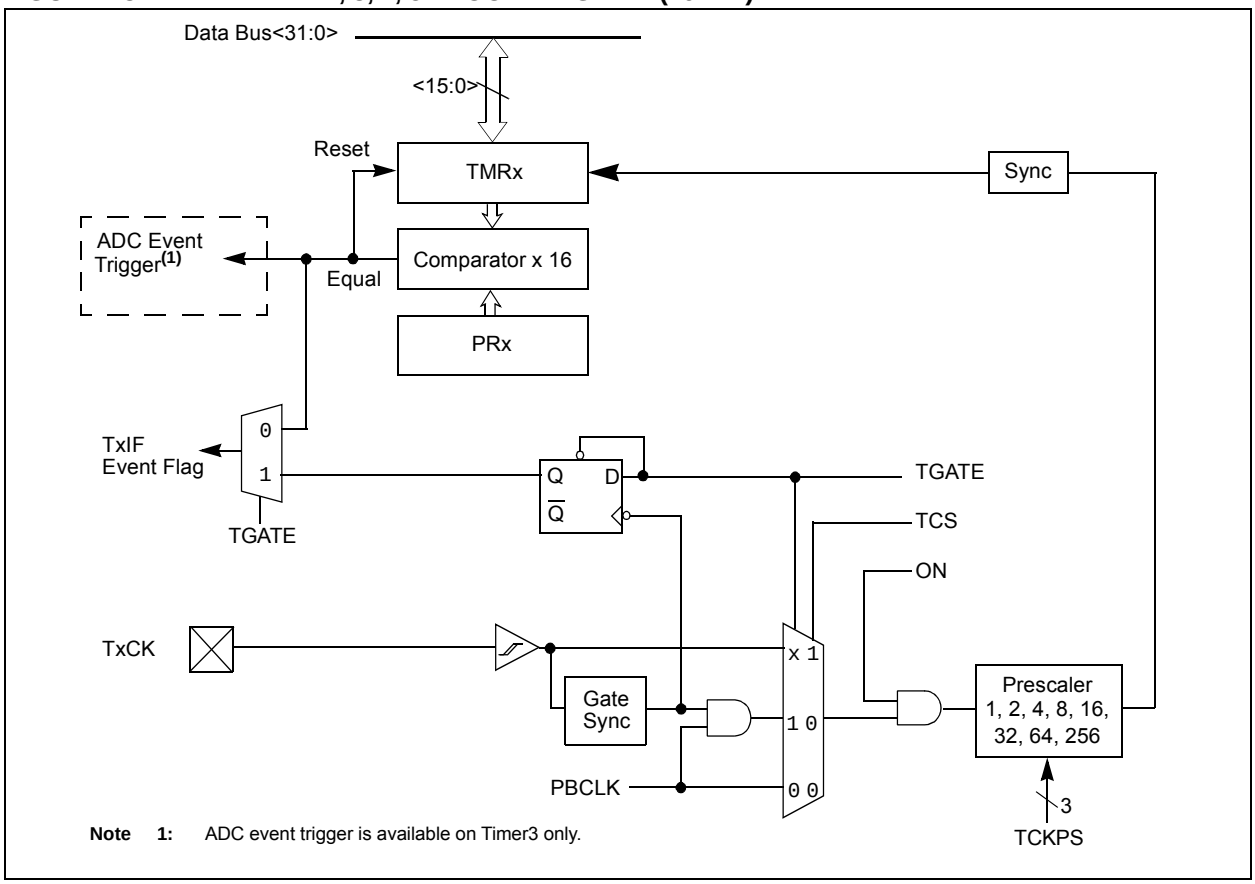
- Synchronous internal 32-bit timer
- Synchronous internal 32-bit gated timer
- Synchronous external 32-bit timer

**Note:** In this chapter, references to registers, TxCON, TMRx and PRx, use 'x' to represent Timer2 through 5 in 16-bit modes. In 32-bit modes, 'x' represents Timer2 or 4; 'y' represents Timer3 or 5.

### 13.1 Additional Supported Features

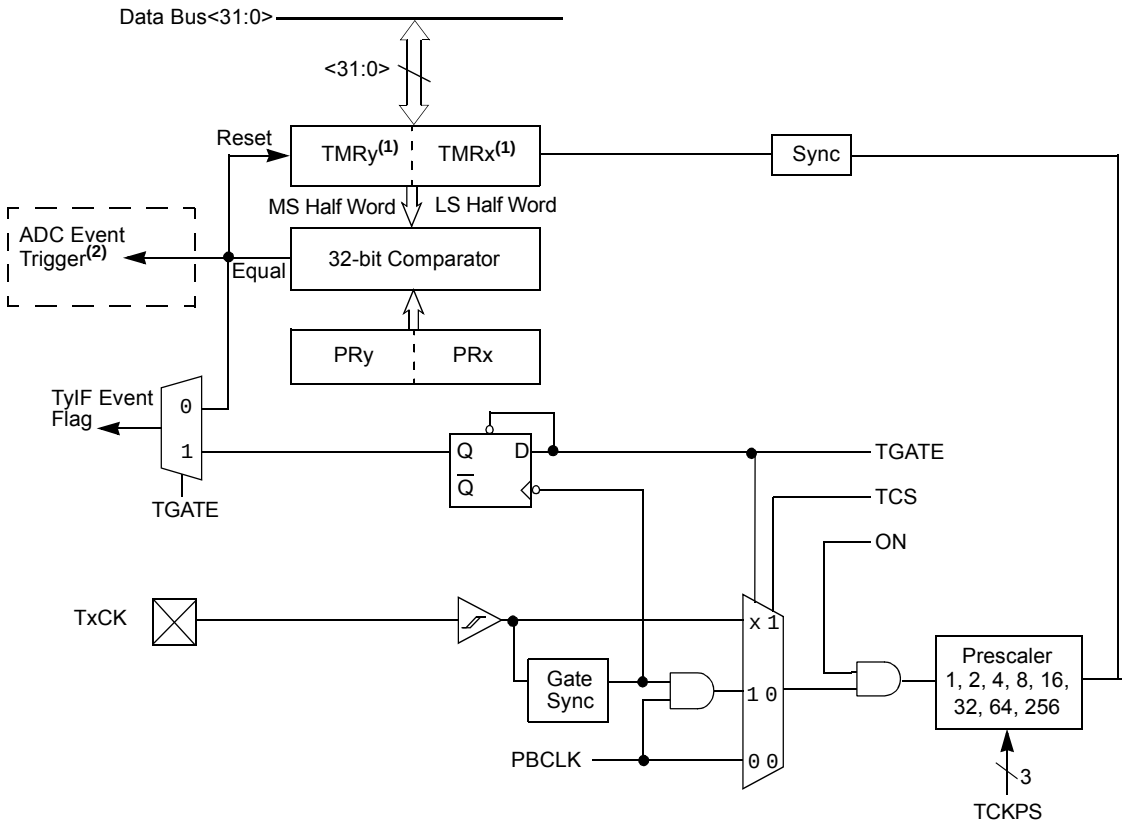
- Selectable clock prescaler
- Timers operational during CPU idle
- Time base for Input Capture and Output Compare modules (Timer2 and Timer3 only)
- ADC event trigger (Timer3 in 16-bit mode, Timer2/3 in 32-bit mode)
- Fast bit manipulation using CLR, SET and INV registers

**FIGURE 13-1: TIMER2, 3, 4, 5 BLOCK DIAGRAM (16-BIT)**




**Note 1:** ADC event trigger is available on Timer3 only.

**FIGURE 13-2: TIMER2/3, 4/5 BLOCK DIAGRAM (32-BIT)(1)**




**Note 1:** In this diagram, the use of 'x' in registers, TxCON, TMRx, PRx and TxCK, refers to either Timer2 or Timer4; the use of 'y' in registers, TyCON, TMRy, PRy, TyIF, refers to either Timer3 or Timer5.

**2:** ADC event trigger is available only on the Timer2/3 pair.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## 13.2 Control Registers

**TABLE 13-1: TIMER2 THROUGH TIMER5 REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0800 | T2CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | TGATE | TCKPS<2:0> | | | T32 | — | TCS | — | 0000 |
| 0810 | TMR2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR2<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0820 | PR2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR2<15:0> | | | | | | | | | | | | | | | | FFFF |
| 0A00 | T3CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | TGATE | TCKPS<2:0> | | | — | — | TCS | — | 0000 |
| 0A10 | TMR3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR3<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0A20 | PR3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR3<15:0> | | | | | | | | | | | | | | | | FFFF |
| 0C00 | T4CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | TGATE | TCKPS<2:0> | | | T32 | — | TCS | — | 0000 |
| 0C10 | TMR4 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR4<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0C20 | PR4 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR4<15:0> | | | | | | | | | | | | | | | | FFFF |
| 0E00 | T5CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | TGATE | TCKPS<2:0> | | | — | — | TCS | — | 0000 |
| 0E10 | TMR5 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR5<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0E20 | PR5 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR5<15:0> | | | | | | | | | | | | | | | | FFFF |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

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**REGISTER 13-1: TxCON: TYPE B TIMER 'x' CONTROL REGISTER ('x' = 2 THROUGH 5)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ON(1,3) | — | SIDL(4) | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 |
| | TGATE(3) | TCKPS<2:0>(3) | | | T32(2) | — | TCS(3) | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit(1,3)
- 1 = Module is enabled
- 0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit(4)
- 1 = Discontinue operation when device enters Idle mode
- 0 = Continue operation even in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit(3)

When TCS = 1:
This bit is ignored and is read as '0'.

When TCS = 0:
- 1 = Gated time accumulation is enabled
- 0 = Gated time accumulation is disabled

bit 6-4 **TCKPS<2:0>:** Timer Input Clock Prescale Select bits(3)
- 111 = 1:256 prescale value
- 110 = 1:64 prescale value
- 101 = 1:32 prescale value
- 100 = 1:16 prescale value
- 011 = 1:8 prescale value
- 010 = 1:4 prescale value
- 001 = 1:2 prescale value
- 000 = 1:1 prescale value

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** This bit is available only on even numbered timers (Timer2 and Timer4).

**3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3 and Timer5). All timer functions are set through the even numbered timers.

**4:** While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.


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**REGISTER 13-1: TxCON: TYPE B TIMER 'x' CONTROL REGISTER (CONTINUED)('x' = 2**

bit 3 **T32:** 32-Bit Timer Mode Select bit(2)
1 = Odd numbered and even numbered timers form a 32-bit timer
0 = Odd numbered and even numbered timers form a separate 16-bit timer

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer Clock Source Select bit(3)
1 = External clock from TxCK pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** This bit is available only on even numbered timers (Timer2 and Timer4).

**3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3 and Timer5). All timer functions are set through the even numbered timers.

**4:** While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

**NOTES:**


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## 14.0 WATCHDOG TIMER (WDT)

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin Family family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. "Watchdog, Deadman, and Power-up Timers"** (DS60001114) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Watchdog Timer (WDT), when enabled, operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are some of the key features of the WDT module:

- Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle

**FIGURE 14-1: WATCHDOG AND POWER-UP TIMER BLOCK DIAGRAM**

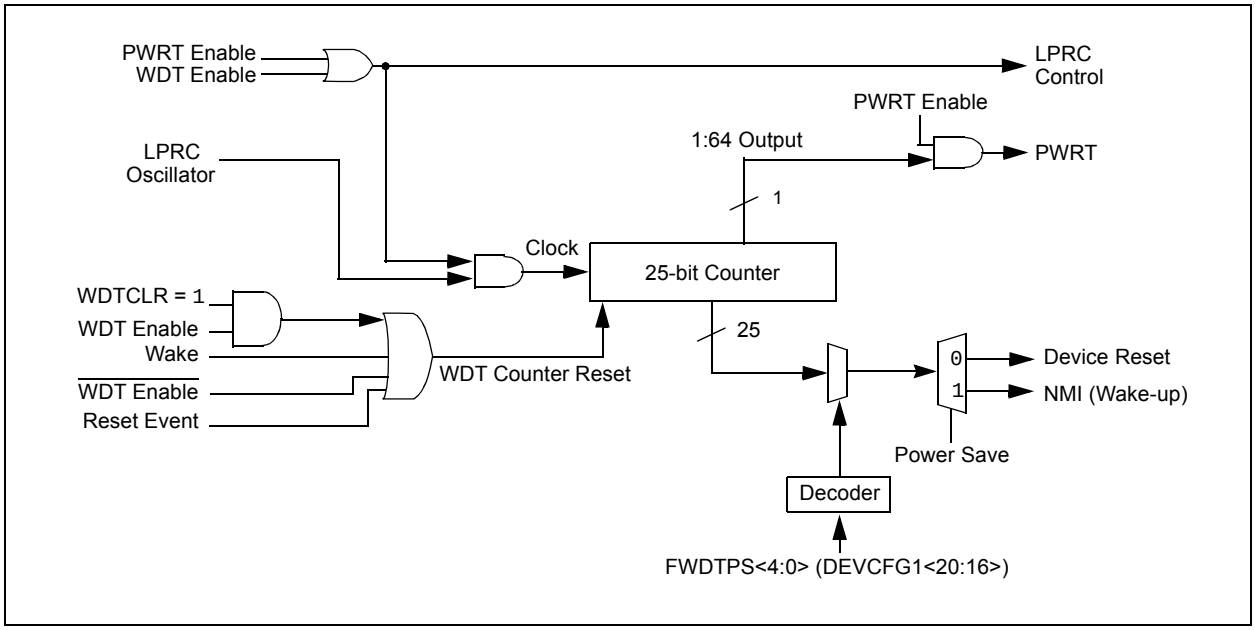

**TABLE 14-1: WATCHDOG TIMER REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0000 | WDTCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | — | — | — | — | — | — | — | SWDTPS<4:0> | | | | | WDTWINEN | WDTCLR | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**REGISTER 14-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ON(1,2) | — | — | — | — | — | — | — |
| 7:0 | U-0 | R-y | R-y | R-y | R-y | R-y | R/W-0 | R/W-0 |
| | — | SWDTPS<4:0> | | | | | WDTWINEN | WDTCLR |

| Legend: | y = Values set from Configuration bits on POR | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Watchdog Timer Enable bit(1,2)
- 1 = Enables the WDT if it is not enabled by the device configuration
- 0 = Disable the WDT if it was enabled in software

bit 14-7 **Unimplemented:** Read as '0'

bit 6-2 **SWDTPS<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value from Device Configuration bits
On reset, these bits are set to the values of the WDTPS <4:0> of Configuration bits.

bit 1 **WDTWINEN:** Watchdog Timer Window Enable bit
- 1 = Enable windowed Watchdog Timer
- 0 = Disable windowed Watchdog Timer

bit 0 **WDTCLR:** Watchdog Timer Reset bit
- 1 = Writing a '1' will clear the WDT
- 0 = Software cannot force this bit to a '0'

**Note 1:** A read of this bit results in a '1' if the Watchdog Timer is enabled by the device configuration or software.

**2:** When using the 1:1 PBCLK divisor, the user software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**NOTES:**


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## 15.0 INPUT CAPTURE

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Input Capture"** (DS60001122) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The following events cause capture events:

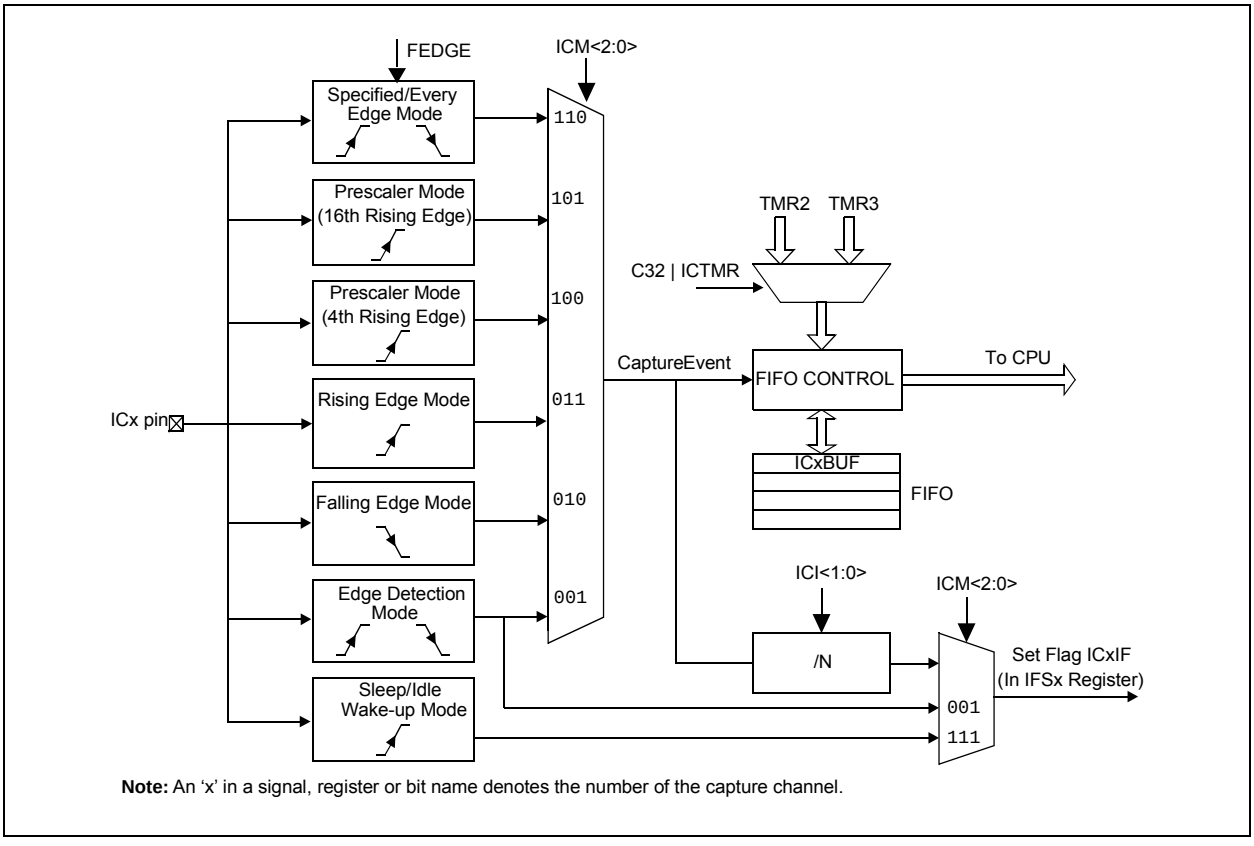
- Simple capture event modes:
  - Capture timer value on every falling edge of input at ICx pin
  - Capture timer value on every rising edge of input at ICx pin
  - Capture timer value on every edge (rising and falling)
  - Capture timer value on every edge (rising and falling), specified edge first.
- Prescaler capture event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

The other operational features include:

- Device wake-up from capture pin during CPU Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values
  Interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts

**FIGURE 15-1: INPUT CAPTURE BLOCK DIAGRAM**




**Note:** An 'x' in a signal, register or bit name denotes the number of the capture channel.

## 15.1 Control Registers

**TABLE 15-1: INPUT CAPTURE 1 THROUGH INPUT CAPTURE 5 REGISTER MAP**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 2000 | IC1CON(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | FEDGE | C32 | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| 2010 | IC1BUF | 31:16 | IC1BUF<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 2200 | IC2CON(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | FEDGE | C32 | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| 2210 | IC2BUF | 31:16 | IC2BUF<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 2400 | IC3CON(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | FEDGE | C32 | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| 2410 | IC3BUF | 31:16 | IC3BUF<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 2600 | IC4CON(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | FEDGE | C32 | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| 2610 | IC4BUF | 31:16 | IC4BUF<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 2800 | IC5CON(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | FEDGE | C32 | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| 2810 | IC5BUF | 31:16 | IC5BUF<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.



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**REGISTER 15-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER ('x' = 1 THROUGH 5)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | ON(1) | — | SIDL | — | — | — | FEDGE | C32 |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 |
| | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit | |
| -n = Bit Value at POR: ('0', '1', x = unknown) | | P = Programmable bit | r = Reserved bit |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Input Capture Module Enable bit(1)
- 1 = Module enabled
- 0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit
- 1 = Halt in CPU Idle mode
- 0 = Continue to operate in CPU Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **FEDGE:** First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)
- 1 = Capture rising edge first
- 0 = Capture falling edge first

bit 8 **C32:** 32-bit Capture Select bit
- 1 = 32-bit timer resource capture
- 0 = 16-bit timer resource capture

bit 7 **ICTMR:** Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is '1')
- 0 = Timer3 is the counter source for capture
- 1 = Timer2 is the counter source for capture

bit 6-5 **ICI<1:0>:** Interrupt Control bits
- 11 = Interrupt on every fourth capture event
- 10 = Interrupt on every third capture event
- 01 = Interrupt on every second capture event
- 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
- 1 = Input capture overflow occurred
- 0 = No input capture overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
- 1 = Input capture buffer is not empty; at least one more capture value can be read
- 0 = Input capture buffer is empty

**Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**REGISTER 15-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER (CONTINUED)('x' = 1**

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits

111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
110 = Simple Capture Event mode – every edge, specified edge first and every edge thereafter
101 = Prescaled Capture Event mode – every sixteenth rising edge
100 = Prescaled Capture Event mode – every fourth rising edge
011 = Simple Capture Event mode – every rising edge
010 = Simple Capture Event mode – every falling edge
001 = Edge Detect mode – every edge (rising and falling)
000 = Input Capture module is disabled

**Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.


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## 16.0 OUTPUT COMPARE

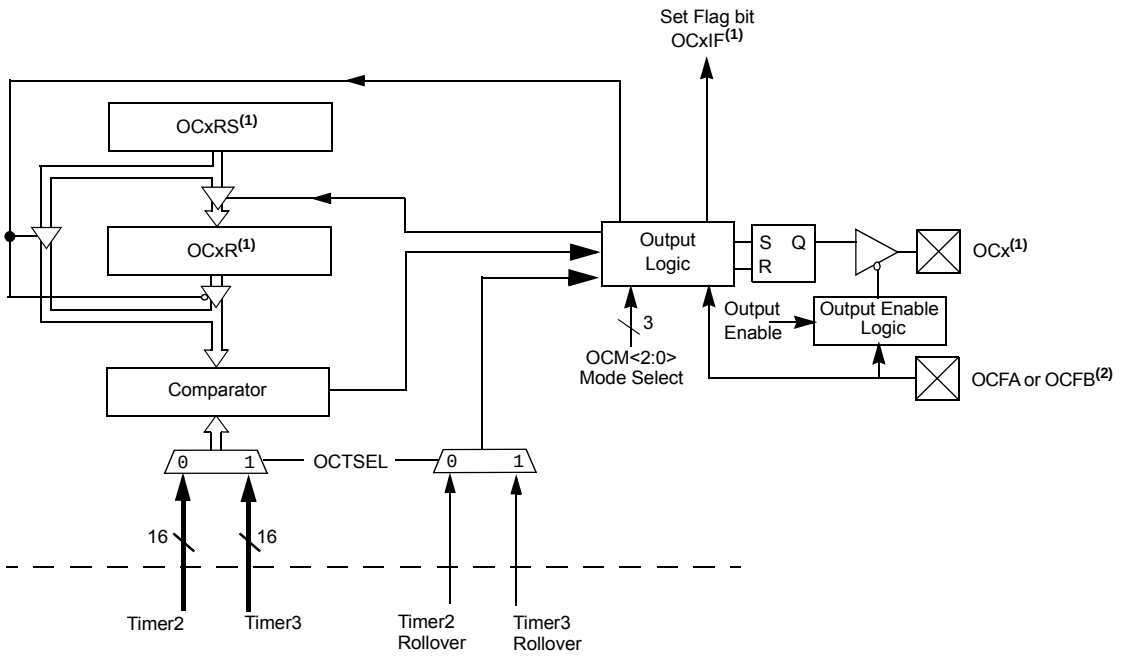
**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 16. "Output Compare"** (DS60001111) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Output Compare module is used to generate a single pulse or a train of pulses in response to selected time base events. For all modes of operation, the Output Compare module compares the values stored in the OCxR and/or the OCxRS registers to the value in the selected timer. When a match occurs, the Output Compare module generates an event based on the selected mode of operation.

The following are the key features of this module:

- Multiple Output Compare modules in a device
- Programmable interrupt generation on compare event
- Single and Dual Compare modes
- Single and continuous output pulse generation
- Pulse-Width Modulation (PWM) mode
- Hardware-based PWM Fault detection and automatic output disable
- Can operate from either of two available 16-bit time bases or a single 32-bit time base

**FIGURE 16-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM**




**Note 1:** Where 'x' is shown, reference is made to the registers associated with the respective output compare channels, 1 through 5.

**2:** The OCFA pin controls the OC1-OC4 channels. The OCFB pin controls the OC5 channel.

## 16.1 Control Registers

**TABLE 16-1: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 5 REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 3000 | OC1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | OC32 | OCFLT | OCTSEL | OCM<2:0> | | | 0000 |
| 3010 | OC1R | 31:16 | OC1R<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 3020 | OC1RS | 31:16 | OC1RS<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 3200 | OC2CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | OC32 | OCFLT | OCTSEL | OCM<2:0> | | | 0000 |
| 3210 | OC2R | 31:16 | OC2R<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 3220 | OC2RS | 31:16 | OC2RS<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 3400 | OC3CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | OC32 | OCFLT | OCTSEL | OCM<2:0> | | | 0000 |
| 3410 | OC3R | 31:16 | OC3R<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 3420 | OC3RS | 31:16 | OC3RS<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 3600 | OC4CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | OC32 | OCFLT | OCTSEL | OCM<2:0> | | | 0000 |
| 3610 | OC4R | 31:16 | OC4R<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 3620 | OC4RS | 31:16 | OC4RS<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 3800 | OC5CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | OC32 | OCFLT | OCTSEL | OCM<2:0> | | | 0000 |
| 3810 | OC5R | 31:16 | OC5R<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 3820 | OC5RS | 31:16 | OC5RS<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.



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**REGISTER 16-1: OCxCON: OUTPUT COMPARE 'x' CONTROL REGISTER ('x' = 1 THROUGH 5)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ON(1) | — | SIDL | — | — | — | — | — |
| 7:0 | U-0 | U-0 | R/W-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | OC32 | OCFLT(2) | OCTSEL | OCM<2:0> | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Output Compare Peripheral On bit(1)
- 1 = Output Compare peripheral is enabled
- 0 = Output Compare peripheral is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue operation when CPU enters Idle mode
- 0 = Continue operation in Idle mode

bit 12-6 **Unimplemented:** Read as '0'

bit 5 **OC32:** 32-bit Compare Mode bit
- 1 = OCxR<31:0> and/or OCxRS<31:0> are used for comparisons to the 32-bit timer source
- 0 = OCxR<15:0> and OCxRS<15:0> are used for comparisons to the 16-bit timer source

bit 4 **OCFLT:** PWM Fault Condition Status bit(2)
- 1 = PWM Fault condition has occurred (cleared in HW only)
- 0 = No PWM Fault condition has occurred

bit 3 **OCTSEL:** Output Compare Timer Select bit
- 1 = Timer3 is the clock source for this Output Compare module
- 0 = Timer2 is the clock source for this Output Compare module

bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits
- 111 = PWM mode on OCx; Fault pin enabled
- 110 = PWM mode on OCx; Fault pin disabled
- 101 = Initialize OCx pin low; generate continuous output pulses on OCx pin
- 100 = Initialize OCx pin low; generate single output pulse on OCx pin
- 011 = Compare event toggles OCx pin
- 010 = Initialize OCx pin high; compare event forces OCx pin low
- 001 = Initialize OCx pin low; compare event forces OCx pin high
- 000 = Output compare peripheral is disabled but continues to draw current

**Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** This bit is only used when OCM<2:0> = '111'. It is read as '0' in all other modes.

**NOTES:**


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## 17.0 SERIAL PERIPHERAL INTERFACE (SPI)

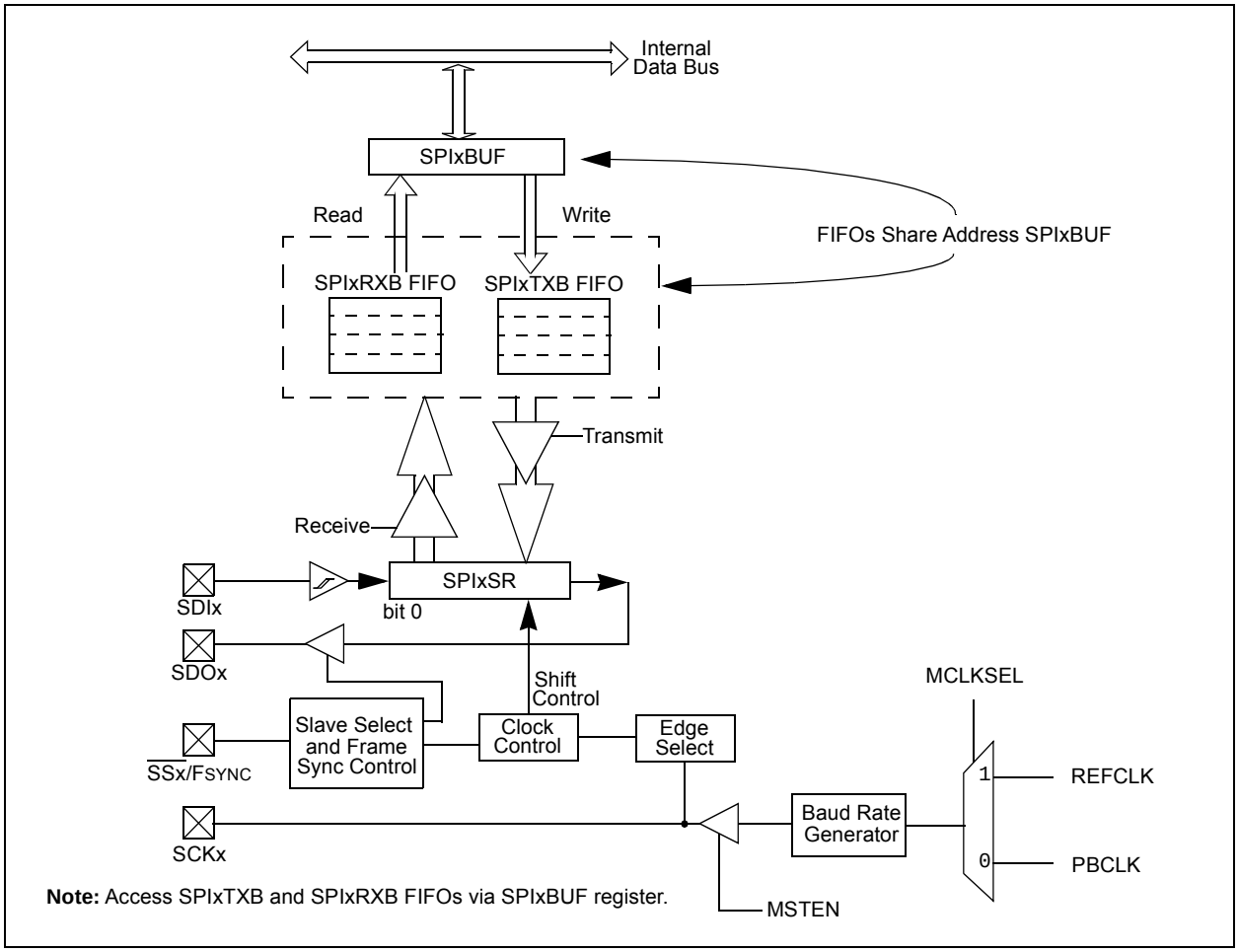
**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The SPI module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontroller devices. These peripheral devices may be Serial EEPROMs, Shift registers, display drivers, Analog-to-Digital Converters (ADC), etc. The PIC32 SPI module is compatible with Motorola® SPI and SIOP interfaces.

Some of the key features of the SPI module are:

- Master and Slave modes support
- Four different clock formats
- Enhanced Framed SPI protocol support
- User-configurable 8-bit, 16-bit and 32-bit data width
- Separate SPI FIFO buffers for receive and transmit
  - FIFO buffers act as 4/8/16-level deep FIFOs based on 32/16/8-bit data width
- Programmable interrupt event on every 8-bit, 16-bit and 32-bit data transfer
- Operation during CPU Sleep and Idle mode
- Audio Codec Support:
  - $I^2S$ protocol
  - Left-justified
  - Right-justified
  - PCM

**FIGURE 17-1: SPI MODULE BLOCK DIAGRAM**




**Note:** Access SPIxTXB and SPIxRXB FIFOs via SPIxBUF register.

## 17.1 Control Registers

**TABLE 17-1: SPI1 THROUGH SPI4 REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 5800 | SPI1CON | 31:16 | FRMEN | FRMSYNC | FRMPOL | MSSEN | FRMSYPW | FRMCNT<2:0> | | | MCLKSEL | — | — | — | — | — | SPIFE | ENHBUF | 0000 |
| | | 15:0 | ON | — | SIDL | DISSDO | MODE32 | MODE16 | SMP | CKE | SSEN | CKP | MSTEN | DISSDI | STXISEL<1:0> | | SRXISEL<1:0> | | 0000 |
| 5810 | SPI1STAT | 31:16 | — | — | — | RXBUFELM<4:0> | | | | | — | — | — | TXBUFELM<4:0> | | | | | 0000 |
| | | 15:0 | — | — | — | FRMERR | SPIBUSY | — | — | SPITUR | SRMT | SPIROV | SPIRBE | — | SPITBE | — | SPITBF | SPIRBF | 19EB |
| 5820 | SPI1BUF | 31:16 | DATA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 5830 | SPI1BRG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | BRG<8:0> | | | | | | | | | 0000 |
| 5840 | SPI1CON2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | SPI SGNEXT | — | — | FRM ERREN | SPI ROVEN | SPI TUREN | IGNROV | IGNTUR | AUDEN | — | — | — | AUD MONO | — | AUDMOD<1:0> | | 0000 |
| 5A00 | SPI2CON | 31:16 | FRMEN | FRMSYNC | FRMPOL | MSSEN | FRMSYPW | FRMCNT<2:0> | | | MCLKSEL | — | — | — | — | — | SPIFE | ENHBUF | 0000 |
| | | 15:0 | ON | — | SIDL | DISSDO | MODE32 | MODE16 | SMP | CKE | SSEN | CKP | MSTEN | DISSDI | STXISEL<1:0> | | SRXISEL<1:0> | | 0000 |
| 5A10 | SPI2STAT | 31:16 | — | — | — | RXBUFELM<4:0> | | | | | — | — | — | TXBUFELM<4:0> | | | | | 0000 |
| | | 15:0 | — | — | — | FRMERR | SPIBUSY | — | — | SPITUR | SRMT | SPIROV | SPIRBE | — | SPITBE | — | SPITBF | SPIRBF | 19EB |
| 5A20 | SPI2BUF | 31:16 | DATA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 5A30 | SPI2BRG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | BRG<8:0> | | | | | | | | | 0000 |
| 5A40 | SPI2CON2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | SPI SGNEXT | — | — | FRM ERREN | SPI ROVEN | SPI TUREN | IGNROV | IGNTUR | AUDEN | — | — | — | AUD MONO | — | AUDMOD<1:0> | | 0000 |
| 5C00 | SPI3CON | 31:16 | FRMEN | FRMSYNC | FRMPOL | MSSEN | FRMSYPW | FRMCNT<2:0> | | | MCLKSEL | — | — | — | — | — | SPIFE | ENHBUF | 0000 |
| | | 15:0 | ON | — | SIDL | DISSDO | MODE32 | MODE16 | SMP | CKE | SSEN | CKP | MSTEN | DISSDI | STXISEL<1:0> | | SRXISEL<1:0> | | 0000 |
| 5C10 | SPI3STAT | 31:16 | — | — | — | RXBUFELM<4:0> | | | | | — | — | — | TXBUFELM<4:0> | | | | | 0000 |
| | | 15:0 | — | — | — | FRMERR | SPIBUSY | — | — | SPITUR | SRMT | SPIROV | SPIRBE | — | SPITBE | — | SPITBF | SPIRBF | 19EB |
| 5C20 | SPI3BUF | 31:16 | DATA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 5C30 | SPI3BRG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | BRG<8:0> | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table except SPIxBUF have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

**2:** This register is only available on 100-pin devices.



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**TABLE 17-1: SPI1 THROUGH SPI4 REGISTER MAP (CONTINUED)**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 5C40 | SPI3CON2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | SPI SGNEXT | — | — | FRM ERREN | SPI ROVEN | SPI TUREN | IGNROV | IGNTUR | AUDEN | — | — | — | AUD MONO | — | AUDMOD<1:0> | | 0000 |
| 5E00 | SPI4CON(2) | 31:16 | FRMEN | FRMSYNC | FRMPOL | MSSEN | FRMSYPW | FRMCNT<2:0> | | | MCLKSEL | — | — | — | — | — | SPIFE | ENHBUF | 0000 |
| | | 15:0 | ON | — | SIDL | DISSDO | MODE32 | MODE16 | SMP | CKE | SSEN | CKP | MSTEN | DISSDI | STXISEL<1:0> | | SRXISEL<1:0> | | 0000 |
| 5E10 | SPI4STAT(2) | 31:16 | — | — | — | RXBUFELM<4:0> | | | | | — | — | — | TXBUFELM<4:0> | | | | | 0000 |
| | | 15:0 | — | — | — | FRMERR | SPIBUSY | — | — | SPITUR | SRMT | SPIROV | SPIRBE | — | SPITBE | — | SPITBF | SPIRBF | 19EB |
| 5E20 | SPI4BUF(2) | 31:16 | DATA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 5E30 | SPI4BRG(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | BRG<8:0> | | | | | | | | | 0000 |
| 5E40 | SPI4CON2(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | SPI SGNEXT | — | — | FRM ERREN | SPI ROVEN | SPI TUREN | IGNROV | IGNTUR | AUDEN | — | — | — | AUD MONO | — | AUDMOD<1:0> | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table except SPIxBUF have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

**2:** This register is only available on 100-pin devices.

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**REGISTER 17-1: SPIxCON: SPI CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FRMEN | FRMSYNC | FRMPOL | MSSEN | FRMSYPW | FRMCNT<2:0> | | |
| 23:16 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | MCLKSEL(2) | — | — | — | — | — | SPIFE | ENHBUF(2) |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ON(1) | — | SIDL | DISSDO | MODE32 | MODE16 | SMP | CKE(3) |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SSEN | CKP(4) | MSTEN | DISSDI | STXISEL<1:0> | | SRXISEL<1:0> | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **FRMEN:** Framed SPI Support bit
1 = Framed SPI support is enabled ($\overline{SSx}$ pin used as FSYNC input/output)
0 = Framed SPI support is disabled

bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on $\overline{SSx}$ pin bit (Framed SPI mode only)
1 = Frame sync pulse input (Slave mode)
0 = Frame sync pulse output (Master mode)

bit 29 **FRMPOL:** Frame Sync Polarity bit (Framed SPI mode only)
1 = Frame pulse is active-high
0 = Frame pulse is active-low

bit 28 **MSSEN:** Master Mode Slave Select Enable bit
1 = Slave select SPI support enabled. The $\overline{SS}$ pin is automatically driven during transmission in Master mode. Polarity is determined by the FRMPOL bit.
0 = Slave select SPI support is disabled.

bit 27 **FRMSYPW:** Frame Sync Pulse Width bit
1 = Frame sync pulse is one character wide
0 = Frame sync pulse is one clock wide

bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits. Controls the number of data characters transmitted per pulse. This bit is only valid in FRAMED_SYNC mode.
111 = Reserved; do not use
110 = Reserved; do not use
101 = Generate a frame sync pulse on every 32 data characters
100 = Generate a frame sync pulse on every 16 data characters
011 = Generate a frame sync pulse on every 8 data characters
010 = Generate a frame sync pulse on every 4 data characters
001 = Generate a frame sync pulse on every 2 data characters
000 = Generate a frame sync pulse on every data character

bit 23 **MCLKSEL:** Master Clock Enable bit(2)
1 = REFCLK is used by the Baud Rate Generator
0 = PBCLK is used by the Baud Rate Generator

bit 22-18 **Unimplemented:** Read as '0'

**Note 1:** When using the 1:1 PBCLK divisor, the user software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** This bit can only be written when the ON bit = 0.

**3:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

**4:** When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.


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**REGISTER 17-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)**

bit 17 **SPIFE:** Frame Sync Pulse Edge Select bit (Framed SPI mode only)
1 = Frame synchronization pulse coincides with the first bit clock
0 = Frame synchronization pulse precedes the first bit clock

bit 16 **ENHBUF:** Enhanced Buffer Enable bit(2)
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled

bit 15 **ON:** SPI Peripheral On bit(1)
1 = SPI Peripheral is enabled
0 = SPI Peripheral is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue operation when CPU enters in Idle mode
0 = Continue operation in Idle mode

bit 12 **DISSDO:** Disable SDOx pin bit
1 = SDOx pin is not used by the module. Pin is controlled by associated PORT register
0 = SDOx pin is controlled by the module

bit 11-10 **MODE<32,16>:** 32/16-Bit Communication Select bits
When AUDEN = 1:
MODE32 MODE16 Communication
11 24-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame
10 32-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame
01 16-bit Data, 16-bit FIFO, 32-bit Channel/64-bit Frame
00 16-bit Data, 16-bit FIFO, 16-bit Channel/32-bit Frame

When AUDEN = 0:
MODE32 MODE16 Communication
1x 32-bit
01 16-bit
00 8-bit

bit 9 **SMP:** SPI Data Input Sample Phase bit
Master mode (MSTEN = 1):
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time
Slave mode (MSTEN = 0):
SMP value is ignored when SPI is used in Slave mode. The module always uses SMP = 0.

bit 8 **CKE:** SPI Clock Edge Select bit(3)
1 = Serial output data changes on transition from active clock state to Idle clock state (see CKP bit)
0 = Serial output data changes on transition from Idle clock state to active clock state (see CKP bit)

bit 7 **SSEN:** Slave Select Enable (Slave mode) bit
1 = $\overline{SSx}$ pin used for Slave mode
0 = SSx pin not used for Slave mode, pin controlled by port function.

bit 6 **CKP:** Clock Polarity Select bit(4)
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode

**Note 1:** When using the 1:1 PBCLK divisor, the user software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** This bit can only be written when the ON bit = 0.

**3:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

**4:** When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.

**REGISTER 17-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)**

bit 4 **DISSDI:** Disable SDI bit
1 = SDI pin is not used by the SPI module (pin is controlled by PORT function)
0 = SDI pin is controlled by the SPI module

bit 3-2 **STXISEL<1:0>:** SPI Transmit Buffer Empty Interrupt Mode bits
11 = Interrupt is generated when the buffer is not full (has one or more empty elements)
10 = Interrupt is generated when the buffer is empty by one-half or more
01 = Interrupt is generated when the buffer is completely empty
00 = Interrupt is generated when the last transfer is shifted out of SPISR and transmit operations are complete

bit 1-0 **SRXISEL<1:0>:** SPI Receive Buffer Full Interrupt Mode bits
11 = Interrupt is generated when the buffer is full
10 = Interrupt is generated when the buffer is full by one-half or more
01 = Interrupt is generated when the buffer is not empty
00 = Interrupt is generated when the last word in the receive buffer is read (i.e., buffer is empty)

**Note 1:** When using the 1:1 PBCLK divisor, the user software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** This bit can only be written when the ON bit = 0.

**3:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

**4:** When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.


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**REGISTER 17-2: SPIxCON2: SPI CONTROL REGISTER 2**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SPISGNEXT | — | — | FRMERREN | SPIROVEN | SPITUREN | IGNROV | IGNTUR |
| 7:0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| | AUDEN(1) | — | — | — | AUDMONO(1,2) | — | AUDMOD<1:0>(1,2) | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **SPISGNEXT:** Sign Extend Read Data from the RX FIFO bit
- 1 = Data from RX FIFO is sign extended
- 0 = Data from RX FIFO is not sign extened

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit
- 1 = Frame Error overflow generates error events
- 0 = Frame Error does not generate error events

bit 11 **SPIROVEN:** Enable Interrupt Events via SPIROV bit
- 1 = Receive overflow generates error events
- 0 = Receive overflow does not generate error events

bit 10 **SPITUREN:** Enable Interrupt Events via SPITUR bit
- 1 = Transmit Underrun Generates Error Events
- 0 = Transmit Underrun Does Not Generates Error Events

bit 9 **IGNROV:** Ignore Receive Overflow bit (for Audio Data Transmissions)
- 1 = A ROV is not a critical error; during ROV data in the fifo is not overwritten by receive data
- 0 = A ROV is a critical error which stop SPI operation

bit 8 **IGNTUR:** Ignore Transmit Underrun bit (for Audio Data Transmissions)
- 1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty
- 0 = A TUR is a critical error which stop SPI operation

bit 7 **AUDEN:** Enable Audio CODEC Support bit(1)
- 1 = Audio protocol enabled
- 0 = Audio protocol disabled

bit 6-5 **Unimplemented:** Read as '0'

bit 3 **AUDMONO:** Transmit Audio Data Format bit(1,2)
- 1 = Audio data is mono (Each data word is transmitted on both left and right channels)
- 0 = Audio data is stereo

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **AUDMOD<1:0>:** Audio Protocol Mode bit(1,2)
- 11 = PCM/DSP mode
- 10 = Right Justified mode
- 01 = Left Justified mode
- 00 = $I^2S$ mode

**Note 1:** This bit can only be written when the ON bit = 0.

**2:** This bit is only valid for AUDEN = 1.

**REGISTER 17-3: SPIxSTAT: SPI STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | — | — | — | RXBUFELM<4:0> | | | | |
| 23:16 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | — | — | — | TXBUFELM<4:0> | | | | |
| 15:8 | U-0 | U-0 | U-0 | R/C-0, HS | R-0 | U-0 | U-0 | R-0 |
| | — | — | — | FRMERR | SPIBUSY | — | — | SPITUR |
| 7:0 | R-0 | R/W-0 | R-0 | U-0 | R-1 | U-0 | R-0 | R-0 |
| | SRMT | SPIROV | SPIRBE | — | SPITBE | — | SPITBF | SPIRBF |

| **Legend:** | C = Clearable bit | HS = Set in hardware | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (valid only when ENHBUF = 1)

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (valid only when ENHBUF = 1)

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **FRMERR:** SPI Frame Error status bit
1 = Frame error detected
0 = No Frame error detected
This bit is only valid when FRMEN = 1.

bit 11 **SPIBUSY:** SPI Activity Status bit
1 = SPI peripheral is currently busy with some transactions
0 = SPI peripheral is currently idle

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **SPITUR:** Transmit Under Run bit
1 = Transmit buffer has encountered an underrun condition
0 = Transmit buffer has no underrun condition
This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module, or writing a '0' to SPITUR.

bit 7 **SRMT:** Shift Register Empty bit (valid only when ENHBUF = 1)
1 = When SPI module shift register is empty
0 = When SPI module shift register is not empty

bit 6 **SPIROV:** Receive Overflow Flag bit
1 = A new data is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.
0 = No overflow has occurred
This bit is set in hardware; can bit only be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module, or by writing a '0' to SPIROV.

bit 5 **SPIRBE:** RX FIFO Empty bit (valid only when ENHBUF = 1)
1 = RX FIFO is empty (CRPTR = SWPTR)
0 = RX FIFO is not empty (CRPTR ≠ SWPTR)

bit 4 **Unimplemented:** Read as '0'


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**REGISTER 17-3: SPIxSTAT: SPI STATUS REGISTER (CONTINUED)**

bit 3 **SPITBE:** SPI Transmit Buffer Empty Status bit
1 = Transmit buffer, SPIxTXB is empty
0 = Transmit buffer, SPIxTXB is not empty
Automatically set in hardware when SPI transfers data from SPIxTXB to SPIxSR.
Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB.

bit 2 **Unimplemented:** Read as '0'

bit 1 **SPITBF:** SPI Transmit Buffer Full Status bit
1 = Transmit not yet started, SPITXB is full
0 = Transmit buffer is not full
Standard Buffer Mode:
Automatically set in hardware when the core writes to the SPIBUF location, loading SPITXB.
Automatically cleared in hardware when the SPI module transfers data from SPITXB to SPISR.
Enhanced Buffer Mode:
Set when CWPTR + 1 = SRPTR; cleared otherwise

bit 0 **SPIRBF:** SPI Receive Buffer Full Status bit
1 = Receive buffer, SPIxRXB is full
0 = Receive buffer, SPIxRXB is not full
Standard Buffer Mode:
Automatically set in hardware when the SPI module transfers data from SPIxSR to SPIxRXB.
Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.
Enhanced Buffer Mode:
Set when SWPTR + 1 = CRPTR; cleared otherwise

**NOTES:**


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## 18.0 INTER-INTEGRATED CIRCUIT ($I^2C$)

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. "Inter-Integrated Circuit ($I^2C$)"** (DS60001116) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

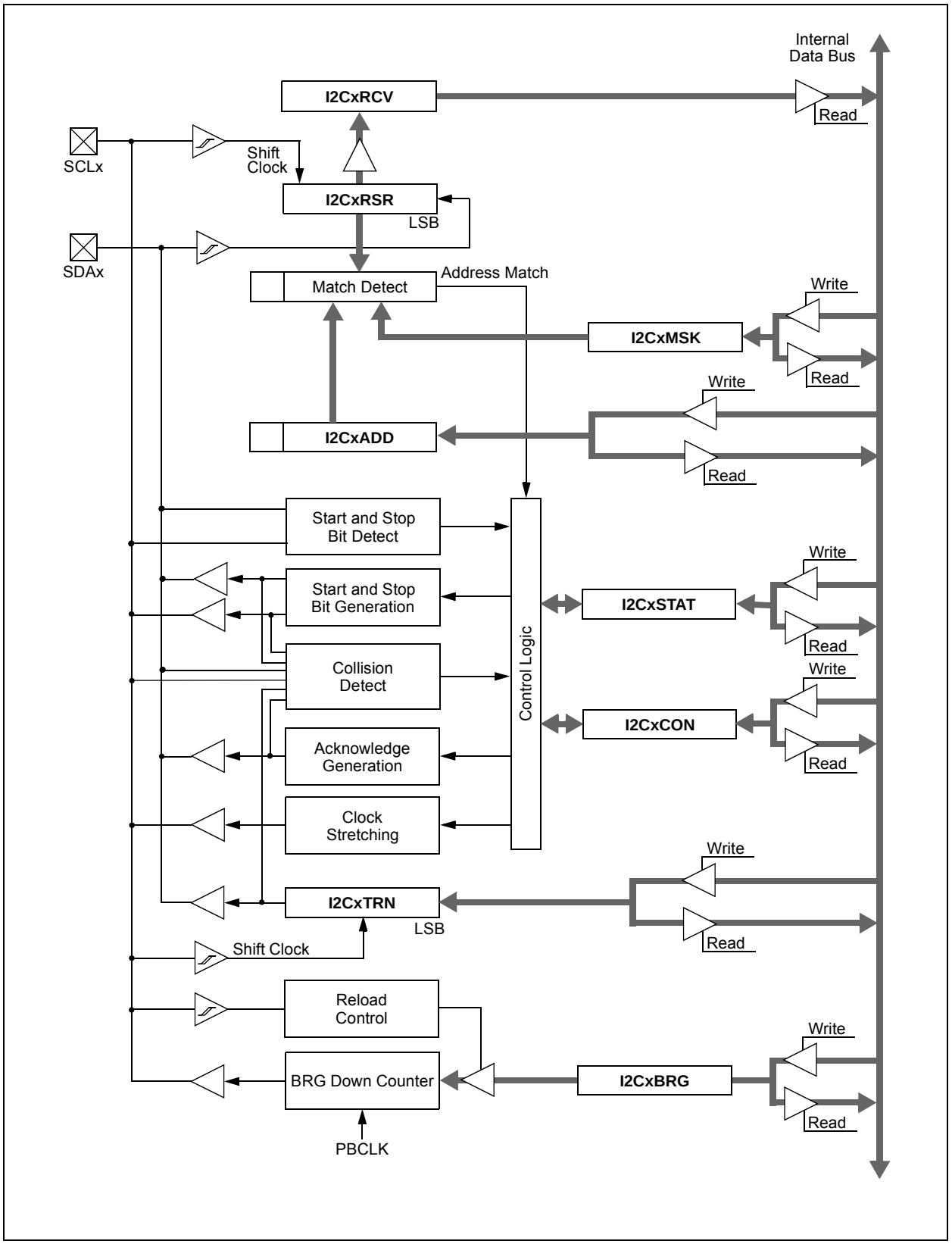
The $I^2C$ module provides complete hardware support for both Slave and Multi-Master modes of the $I^2C$ serial communication standard. Figure 18-1 illustrates the $I^2C$ module block diagram.

Each $I^2C$ module has a 2-pin interface: the SCLx pin is clock and the SDAx pin is data.

Each $I^2C$ module offers the following key features:

- $I^2C$ interface supporting both master and slave operation
- $I^2C$ Slave mode supports 7-bit and 10-bit addressing
- $I^2C$ Master mode supports 7-bit and 10-bit addressing
- $I^2C$ port allows bidirectional transfers between master and slaves
- Serial clock synchronization for the $I^2C$ port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- $I^2C$ supports multi-master operation; detects bus collision and arbitrates accordingly
- Provides support for address bit masking

**FIGURE 18-1: I²C BLOCK DIAGRAM**





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## 18.1 Control Registers

**TABLE 18-1: I2C1 AND I2C2 REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 5000 | I2C1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | SCLREL | STRICT | A10M | DISSLW | SMEN | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | BFFF |
| 5010 | I2C1STAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 | IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF | 0000 |
| 5020 | I2C1ADD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | Address Register | | | | | | | | | | 0000 |
| 5030 | I2C1MSK | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | Address Mask Register | | | | | | | | | | 0000 |
| 5040 | I2C1BRG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | Baud Rate Generator Register | | | | | | | | | | | | 0000 |
| 5050 | I2C1TRN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Transmit Register | | | | | | | | 0000 |
| 5060 | I2C1RCV | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Receive Register | | | | | | | | 0000 |
| 5100 | I2C2CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | SCLREL | STRICT | A10M | DISSLW | SMEN | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | BFFF |
| 5110 | I2C2STAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 | IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF | 0000 |
| 5120 | I2C2ADD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | Address Register | | | | | | | | | | 0000 |
| 5130 | I2C2MSK | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | Address Mask Register | | | | | | | | | | 0000 |
| 5140 | I2C2BRG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | Baud Rate Generator Register | | | | | | | | | | | | 0000 |
| 5150 | I2C2TRN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Transmit Register | | | | | | | | 0000 |
| 5160 | I2C2RCV | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Receive Register | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table except I2CxRCV have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

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**REGISTER 18-1: I2CxCON: I²C 'x' CONTROL REGISTER ('x' = 1 AND 2)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-1, HC | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ON(1) | — | SIDL | SCLREL | STRICT | A10M | DISSLW | SMEN |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0, HC | R/W-0, HC | R/W-0, HC | R/W-0, HC | R/W-0, HC |
| | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN |

| Legend: | HC = Cleared in Hardware | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** I²C Enable bit(1)
- 1 = Enables the I²C module and configures the SDA and SCL pins as serial port pins
- 0 = Disables the I²C module; all I²C pins are controlled by PORT functions

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when device enters Idle mode
- 0 = Continue module operation in Idle mode

bit 12 **SCLREL:** SCLx Release Control bit (when operating as I²C slave)
- 1 = Release SCLx clock
- 0 = Hold SCLx clock low (clock stretch)

If STREN = 1:
Bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.

If STREN = 0:
Bit is R/S (i.e., software can only write '1' to release clock). Hardware clear at beginning of slave transmission.

bit 11 **STRICT:** Strict I²C Reserved Address Rule Enable bit
- 1 = Strict reserved addressing is enforced. Device does not respond to reserved address space or generate addresses in reserved address space.
- 0 = Strict I²C Reserved Address Rule not enabled

bit 10 **A10M:** 10-bit Slave Address bit
- 1 = I2CxADD is a 10-bit slave address
- 0 = I2CxADD is a 7-bit slave address

bit 9 **DISSLW:** Disable Slew Rate Control bit
- 1 = Slew rate control disabled
- 0 = Slew rate control enabled

bit 8 **SMEN:** SMBus Input Levels bit
- 1 = Enable I/O pin thresholds compliant with SMBus specification
- 0 = Disable SMBus input thresholds

**Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.


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**REGISTER 18-1: I2CxCON: I$^2$C 'x' CONTROL REGISTER (CONTINUED)('x' = 1 AND 2)**

bit 7 **GCEN:** General Call Enable bit (when operating as I$^2$C slave)
1 = Enable interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)
0 = General call address disabled

bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I$^2$C slave)
Used in conjunction with SCLREL bit.
1 = Enable software or receive clock stretching
0 = Disable software or receive clock stretching

bit 5 **ACKDT:** Acknowledge Data bit (when operating as I$^2$C master, applicable during master receive)
Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Send NACK during Acknowledge
0 = Send ACK during Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit
(when operating as I$^2$C master, applicable during master receive)
1 = Initiate Acknowledge sequence on SDAx and SCLx pins and transmit ACKDT data bit. Hardware clear at end of master Acknowledge sequence.
0 = Acknowledge sequence not in progress

bit 3 **RCEN:** Receive Enable bit (when operating as I$^2$C master)
1 = Enables Receive mode for I$^2$C. Hardware clear at end of eighth bit of master receive data byte.
0 = Receive sequence not in progress

bit 2 **PEN:** Stop Condition Enable bit (when operating as I$^2$C master)
1 = Initiate Stop condition on SDAx and SCLx pins. Hardware clear at end of master Stop sequence.
0 = Stop condition not in progress

bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I$^2$C master)
1 = Initiate Repeated Start condition on SDAx and SCLx pins. Hardware clear at end of master Repeated Start sequence.
0 = Repeated Start condition not in progress

bit 0 **SEN:** Start Condition Enable bit (when operating as I$^2$C master)
1 = Initiate Start condition on SDAx and SCLx pins. Hardware clear at end of master Start sequence.
0 = Start condition not in progress

**Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**REGISTER 18-2: I2CxSTAT: I$^2$C STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R-0, HSC | R-0, HSC | U-0 | U-0 | U-0 | R/C-0, HS | R-0, HSC | R-0, HSC |
| | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 |
| 7:0 | R/C-0, HS | R/C-0, HS | R-0, HSC | R/C-0, HSC | R/C-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC |
| | IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF |

| Legend: | HS = Set in hardware | HSC = Hardware set/cleared | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | C = Clearable bit |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ACKSTAT:** Acknowledge Status bit
(when operating as I$^2$C master, applicable to master transmit operation)
1 = Acknowledge was not received from slave
0 = Acknowledge was received from slave
Hardware set or clear at end of slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as I$^2$C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge.

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware set at detection of bus collision. This condition can only be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware set when address matches general call address. Hardware clear at Stop detection.

bit 8 **ADD10:** 10-bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.

bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write the I2CxTRN register failed because the I$^2$C module is busy
0 = No collision
Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

bit 5 **D_A:** Data/Address bit (when operating as I$^2$C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was device address
Hardware clear at device address match. Hardware set by reception of slave byte.


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**REGISTER 18-2: I2CxSTAT: I$^2$C STATUS REGISTER (CONTINUED)**

bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware set or clear when Start, Repeated Start or Stop detected.

bit 3 **S:** Start bit
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware set or clear when Start, Repeated Start or Stop detected.

bit 2 **R_W:** Read/Write Information bit (when operating as I$^2$C slave)
1 = Read – indicates data transfer is output from slave
0 = Write – indicates data transfer is input to slave
Hardware set or clear after reception of I$^2$C device address byte.

bit 1 **RBF:** Receive Buffer Full Status bit
1 = Receive complete, I2CxRCV is full
0 = Receive not complete, I2CxRCV is empty
Hardware set when I2CxRCV is written with received byte. Hardware clear when software reads I2CxRCV.

bit 0 **TBF:** Transmit Buffer Full Status bit
1 = Transmit in progress, I2CxTRN is full
0 = Transmit complete, I2CxTRN is empty
Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.

**NOTES:**


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## 19.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS60001107) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

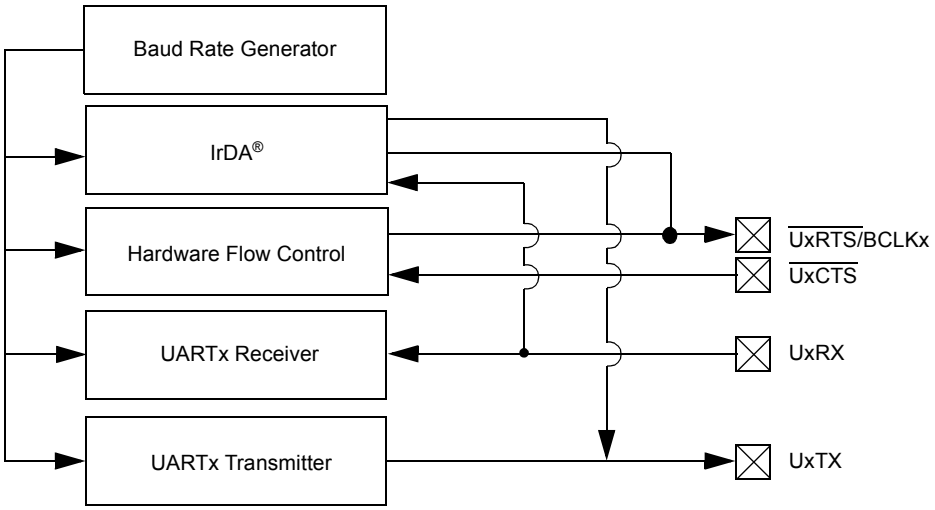
The UART module is one of the serial I/O modules available in PIC32MX1XX/2XX/5XX 64/100-pin family devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols, such as RS-232, RS-485, LIN and IrDA®. The module also supports the hardware flow control option, with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA encoder and decoder.

The primary features of the UART module are:

- Full-duplex, 8-bit or 9-bit data transmission
- Even, odd or no parity options (for 8-bit data)
- One or two Stop bits
- Hardware auto-baud feature
- Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 38 bps to 12.5 Mbps at 50 MHz
- 8-level deep First-In-First-Out (FIFO) transmit data buffer
- 8-level deep FIFO receive data buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt-only on address detect ($9^{th}$ bit = 1)
- Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- LIN Protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support

Figure 19-1 illustrates a simplified block diagram of the UART.

**FIGURE 19-1: UART SIMPLIFIED BLOCK DIAGRAM**




**Note:** Not all pins are available for all UART modules. Refer to the device-specific pin diagram for more information.

## 19.1 Control Registers

**TABLE 19-1: UART1 THROUGH UART5 REGISTER MAP**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6000 | U1MODE(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 6010 | U1STA(1) | 31:16 | — | — | — | — | — | — | — | ADM_EN | ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | FFFF |
| 6020 | U1TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 6030 | U1RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |
| 6040 | U1BRG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |
| 6200 | U2MODE(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 6210 | U2STA(1) | 31:16 | — | — | — | — | — | — | — | ADM_EN | ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | FFFF |
| 6220 | U2TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 6230 | U2RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |
| 6240 | U2BRG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |
| 6400 | U3MODE(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 6410 | U3STA(1) | 31:16 | — | — | — | — | — | — | — | ADM_EN | ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | FFFF |
| 6420 | U3TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 6430 | U3RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

**2:** This register is only available on 100-pin devices.



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**TABLE 19-1: UART1 THROUGH UART5 REGISTER MAP (CONTINUED)**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6440 | U3BRG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |
| 6600 | U4MODE(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 6610 | U4STA(1) | 31:16 | — | — | — | — | — | — | — | ADM_EN | ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | FFFF |
| 6620 | U4TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 6630 | U4RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |
| 6640 | U4BRG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |
| 6800 | U5MODE(1,2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 6810 | U5STA(1,2) | 31:16 | — | — | — | — | — | — | — | ADM_EN | ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | FFFF |
| 6820 | U5TXREG(1,2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 6830 | U5RXREG(1,2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |
| 6840 | U5BRG(1,2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

**2:** This register is only available on 100-pin devices.

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**REGISTER 19-1: UxMODE: UARTx MODE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| | ON(1) | — | SIDL | IREN | RTSMD | — | UEN<1:0> | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** UARTx Enable bit(1)
- 1 = UARTx is enabled. UARTx pins are controlled by UARTx as defined by UEN<1:0> and UTXEN control bits
- 0 = UARTx is disabled. All UARTx pins are controlled by corresponding bits in the PORTx, TRISx and LATx registers; UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue operation when device enters Idle mode
- 0 = Continue operation in Idle mode

bit 12 **IREN:** IrDA Encoder and Decoder Enable bit
- 1 = IrDA is enabled
- 0 = IrDA is disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
- 1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
- 0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Enable bits
- 11 = UxTX, UxRX and UxBCLK pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
- 10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
- 01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
- 00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/UxBCLK pins are controlled by corresponding bits in the PORTx register

bit 7 **WAKE:** Enable Wake-up on Start bit Detect During Sleep Mode bit
- 1 = Wake-up enabled
- 0 = Wake-up disabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
- 1 = Loopback mode is enabled
- 0 = Loopback mode is disabled

**Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.


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**REGISTER 19-1: UxMODE: UARTx MODE REGISTER (CONTINUED)**

bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Enable baud rate measurement on the next character – requires reception of Sync character (0x55); cleared by hardware upon completion
0 = Baud rate measurement disabled or completed

bit 4 **RXINV:** Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'

bit 3 **BRGH:** High Baud Rate Enable bit
1 = High-Speed mode – 4x baud clock enabled
0 = Standard Speed mode – 16x baud clock enabled

bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Selection bit
1 = 2 Stop bits
0 = 1 Stop bit

**Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**REGISTER 19-2: UxSTA: UARTx STATUS AND CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
| | — | — | — | — | — | — | — | ADM_EN |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ADDR<7:0> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-1 |
| | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R-1 | R-0 | R-0 | R/W-0 | R-0 |
| | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-25 **Unimplemented:** Read as '0'

bit 24 **ADM_EN:** Automatic Address Detect Mode Enable bit
- 1 = Automatic Address Detect mode is enabled
- 0 = Automatic Address Detect mode is disabled

bit 23-16 **ADDR<7:0>:** Automatic Address Mask bits

When the ADM_EN bit is '1', this value defines the address character to use for automatic address detection.

bit 15-14 **UTXISEL<1:0>:** TX Interrupt Mode Selection bits
- 11 = Reserved, do not use
- 10 = Interrupt is generated and asserted while the transmit buffer is empty
- 01 = Interrupt is generated and asserted when all characters have been transmitted
- 00 =Interrupt is generated and asserted while the transmit buffer contains at least one empty space

bit 13 **UTXINV:** Transmit Polarity Inversion bit

If IrDA mode is disabled (i.e., IREN (UxMODE<12>) is '0'):
- 1 = UxTX Idle state is '0'
- 0 = UxTX Idle state is '1'

If IrDA mode is enabled (i.e., IREN (UxMODE<12>) is '1'):
- 1 = IrDA encoded UxTX Idle state is '1'
- 0 = IrDA encoded UxTX Idle state is '0'

bit 12 **URXEN:** Receiver Enable bit
- 1 = UARTx receiver is enabled. UxRX pin is controlled by UARTx (if ON = 1)
- 0 = UARTx receiver is disabled. UxRX pin is ignored by the UARTx module. UxRX pin is controlled by the port.

bit 11 **UTXBRK:** Transmit Break bit
- 1 = Send Break on next transmission. Start bit followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
- 0 = Break transmission is disabled or completed

bit 10 **UTXEN:** Transmit Enable bit
- 1 = UARTx transmitter is enabled. UxTX pin is controlled by UARTx (if ON = 1)
- 0 = UARTx transmitter is disabled. Any pending transmission is aborted and buffer is reset. UxTX pin is controlled by the port.

bit 9 **UTXBF:** Transmit Buffer Full Status bit (read-only)
- 1 = Transmit buffer is full
- 0 = Transmit buffer is not full, at least one more character can be written


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**REGISTER 19-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)**

bit 8 **TRMT:** Transmit Shift Register is Empty bit (read-only)
1 = Transmit shift register is empty and transmit buffer is empty (the last transmission has completed)
0 = Transmit shift register is not empty, a transmission is in progress or queued in the transmit buffer

bit 7-6 **URXISEL<1:0>:** Receive Interrupt Mode Selection bit
11 = Reserved; do not use
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full (i.e., has 6 or more data characters)
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full (i.e., has 4 or more data characters)
00 =Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character)

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Data is being received

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit.
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and RSR to empty state.
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed

bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

## 19.2 Timing Diagrams

Figure 19-2 and Figure 19-3 illustrate typical receive and transmit timing for the UART module.

**FIGURE 19-2: UART RECEPTION**

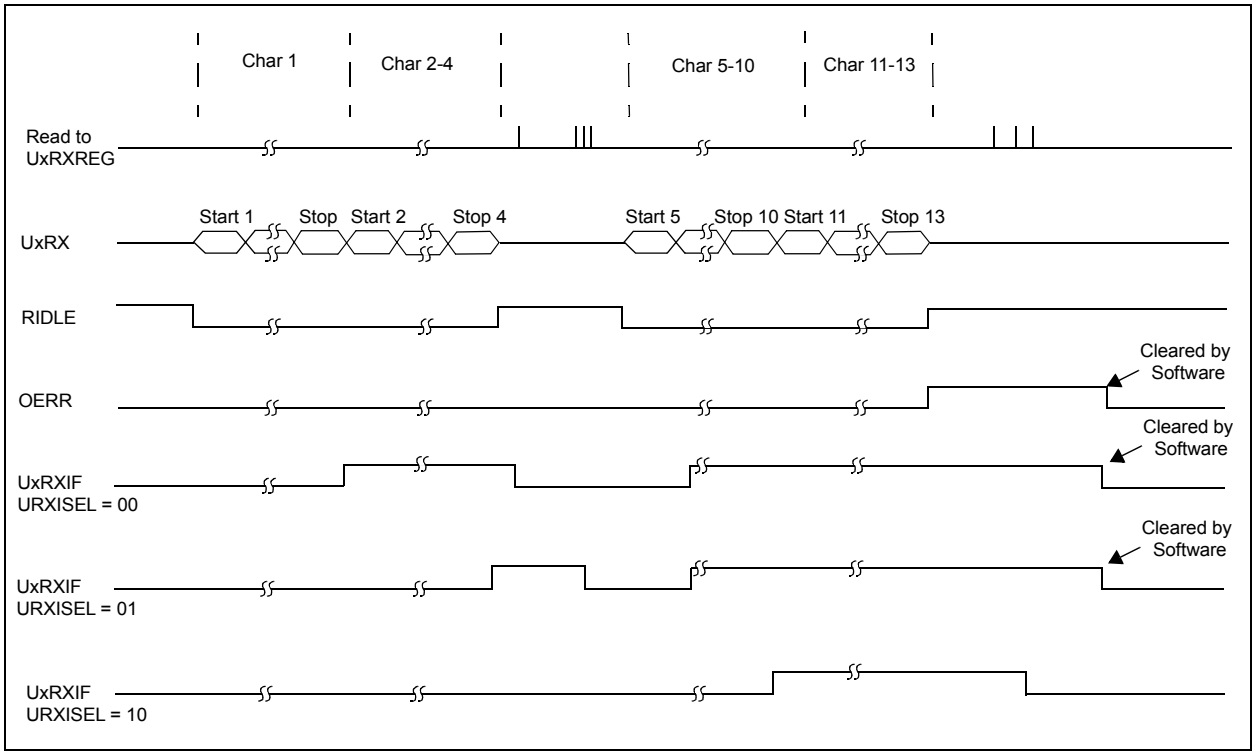
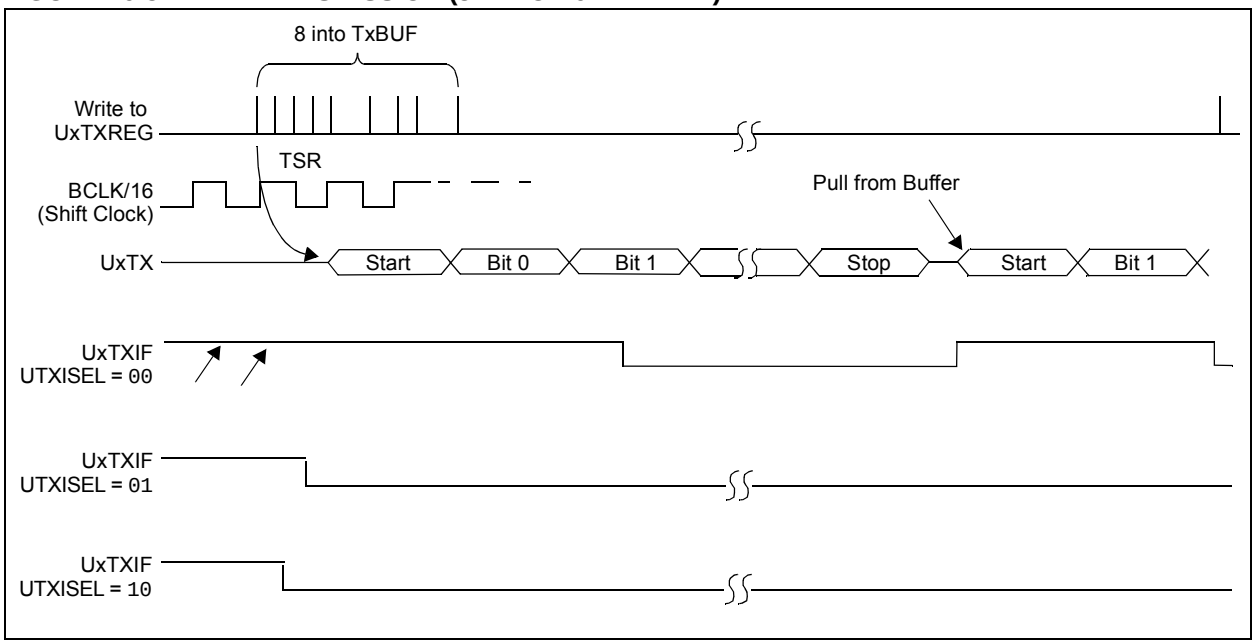



**FIGURE 19-3: TRANSMISSION (8-BIT OR 9-BIT DATA)**





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## 20.0 PARALLEL MASTER PORT (PMP)

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 13. "Parallel Master Port (PMP)"** (DS60001128) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

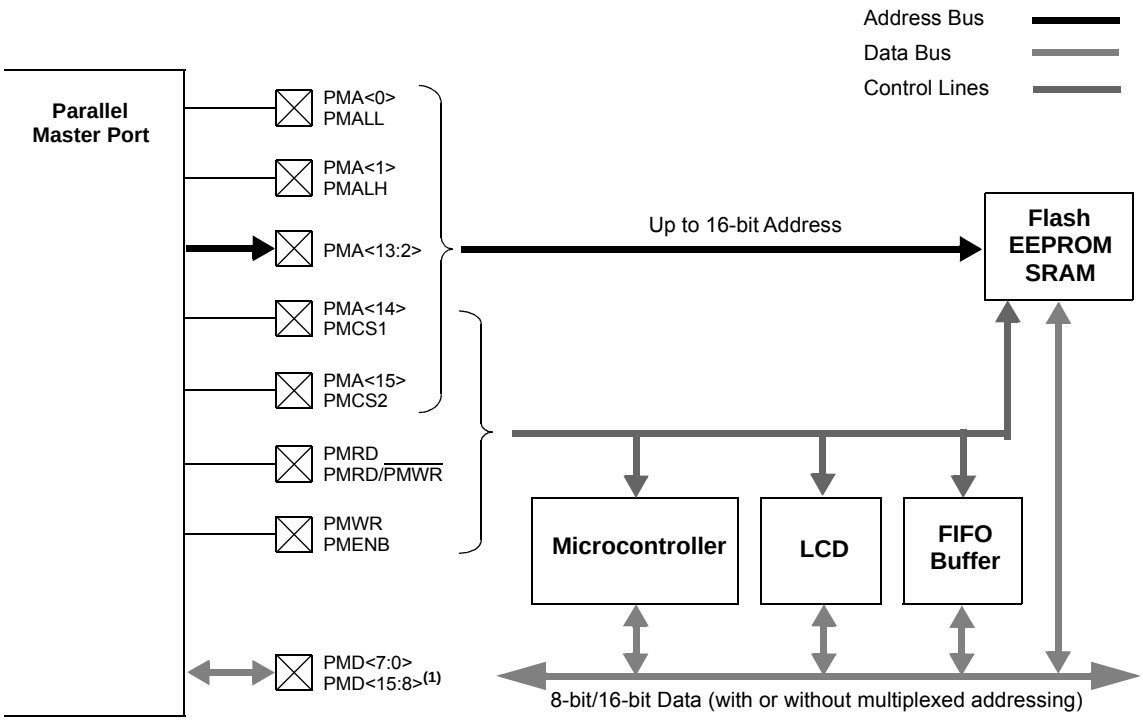
The PMP is a parallel 8-bit or 16-bit input/output module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable.

The following are the key features of the PMP module:

- 8-bit,16-bit interface
- Up to 16 programmable address lines
- Up to two Chip Select lines
- Programmable strobe options:
  - Individual read and write strobes, or
  - Read/write strobe with enable strobe
  - Selectable polarity
- Address auto-increment/auto-decrement
- Programmable address/data multiplexing
- Programmable polarity on control signals
- Parallel Slave Port support:
  - Legacy addressable
  - Address support
- Read and Write 4-byte deep auto-incrementing buffer
- Programmable Wait states
- Operate during CPU Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers
- Freeze option for in-circuit debugging

**Note:** On 64-pin devices, data pins PMD<15:8> are not available in 16-bit Master modes.

**FIGURE 20-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES**




**Note:** On 64-pin devices, data pins PMD<15:8> are not available in 16-bit Master modes.

## 20.1 Control Registers

**TABLE 20-1: PARALLEL MASTER PORT REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 7000 | PMCON | 31:16 | — | — | — | — | — | — | — | — | RDSTART | — | — | — | — | — | DUALBUF | — | 0000 |
| | | 15:0 | ON | — | SIDL | ADRMUX<1:0> | | PMPTTL | PTWREN | PTRDEN | CSF<1:0> | | ALP | CS2P | CS1P | — | WRSP | RDSP | 0000 |
| 7010 | PMMODE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BUSY | IRQM<1:0> | | INCM<1:0> | | MODE16 | MODE<1:0> | | WAITB<1:0> | | WAITM<3:0> | | | | WAITE<1:0> | | 0000 |
| 7020 | PMADDR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CS2 | CS1 | ADDR<13:0> | | | | | | | | | | | | | | 0000 |
| | | | ADDR15 | ADDR14 | | | | | | | | | | | | | | | 0000 |
| 7030 | PMDOUT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | DATAOUT<15:0> | | | | | | | | | | | | | | | | 0000 |
| 7040 | PMDIN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | DATAIN<15:0> | | | | | | | | | | | | | | | | 0000 |
| 7050 | PMAEN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PTEN<15:0> | | | | | | | | | | | | | | | | 0000 |
| 7060 | PMSTAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | IBF | IBOV | — | — | IB3F | IB2F | IB1F | IB0F | OBE | OBUF | — | — | OB3E | OB2E | OB1E | OB0E | BFBF |
| 7070 | PMWADDR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | WCS2 | WCS1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | | WADDR15 | WADDR14 | WADDR<13:0> | | | | | | | | | | | | | | 0000 |
| 7080 | PMRADDR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RCS2 | RCS1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | | RADDR15 | RADDR14 | RADDR<13:0> | | | | | | | | | | | | | | 0000 |
| 7090 | PMRDIN | 31:16 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | 15:0 | RDATAIN<15:0> | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.



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**REGISTER 20-1: PMCON: PARALLEL PORT CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | R/W-0, HC | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | U-0 |
| | RDSTART | — | — | — | — | — | DUALBUF | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ON(1) | — | SIDL | ADRMUX<1:0> | | PMPTTL | PTWREN | PTRDEN |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| | CSF<1:0>(2) | | ALP(2) | CS2P(2) | CS1P(2) | — | WRSP | RDSP |

| Legend: | HC = Hardware cleared | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **RDSTART:** Start a Read on the PMP Bus bit(3)
- 1 = Start a read cycle on the PMP bus
- 0 = No effect

This bit is cleared by hardware at the end of the read cycle when the BUSY bit (PMMODE<15>) = 0.

bit 22-18 **Unimplemented:** Read as '0'

bit 17 **DUALBUF:** Parallel Master Port Dual Read/Write Buffer Enable bit

This bit is only valid in Master mode.
- 1 = PMP uses separate registers for reads and writes
  Reads: PMRADDR and PMRDIN
  Writes: PMRWADDR and PMDOUT
- 0 = PMP uses legacy registers for reads and writes
  Reads/Writes: PMADDR and PMRDIN

bit 16 **Unimplemented:** Read as '0'

bit 15 **ON:** Parallel Master Port Enable bit(1)
- 1 = PMP enabled
- 0 = PMP disabled, no off-chip access performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when device enters Idle mode
- 0 = Continue module operation in Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
- 11 = Lower 8 bits of address are multiplexed on PMD<15:0> pins
- 10 = All 16 bits of address are multiplexed on PMD<7:0> pins
- 01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper bits are on PMA<15:8>
- 00 = Address and data appear on separate pins

bit 10 **PMPTTL:** PMP Module TTL Input Buffer Select bit
- 1 = PMP module uses TTL input buffers
- 0 = PMP module uses Schmitt Trigger input buffer

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
- 1 = PMWR/PMENB port enabled
- 0 = PMWR/PMENB port disabled

**Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

**2:** These bits have no effect when their corresponding pins are used as address lines.

**REGISTER 20-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)**

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
1 = PMRD/PMWR port enabled
0 = PMRD/PMWR port disabled

bit 7-6 **CSF<1:0>:** Chip Select Function bits(2)
11 = Reserved
10 = PMCS1 and PMCS2 function as Chip Select
01 = PMCS1 functions as address bit 14; PMCS2 functions as Chip Select
00 = PMCS1 and PMCS2 function as address bits 14 and 15, respectively

bit 5 **ALP:** Address Latch Polarity bit(2)
1 = Active-high (PMALL and PMALH)
0 = Active-low ($\overline{\text{PMALL}}$ and $\overline{\text{PMALH}}$)

bit 4 **CS2P:** Chip Select 0 Polarity bit(2)
1 = Active-high (PMCS2)
0 = Active-low ($\overline{\text{PMCS2}}$)

bit 3 **CS1P:** Chip Select 0 Polarity bit(2)
1 = Active-high (PMCS1)
0 = Active-low ($\overline{\text{PMCS1}}$)

bit 2 **Unimplemented:** Read as '0'

bit 1 **WRSP:** Write Strobe Polarity bit
For Slave Modes and Master mode 2 (MODE<1:0> = 00,01,10):
1 = Write strobe active-high (PMWR)
0 = Write strobe active-low ($\overline{\text{PMWR}}$)
For Master mode 1 (MODE<1:0> = 11):
1 = Enable strobe active-high (PMENB)
0 = Enable strobe active-low ($\overline{\text{PMENB}}$)

bit 0 **RDSP:** Read Strobe Polarity bit
For Slave modes and Master mode 2 (MODE<1:0> = 00,01,10):
1 = Read Strobe active-high (PMRD)
0 = Read Strobe active-low ($\overline{\text{PMRD}}$)
For Master mode 1 (MODE<1:0> = 11):
1 = Read/write strobe active-high (PMRD/$\overline{\text{PMWR}}$)
0 = Read/write strobe active-low ($\overline{\text{PMRD}}$/PMWR)

**Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

**2:** These bits have no effect when their corresponding pins are used as address lines.


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**REGISTER 20-2: PMMODE: PARALLEL PORT MODE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BUSY | IRQM<1:0> | | INCM<1:0> | | MODE16 | MODE<1:0> | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | WAITB<1:0>(1) | | WAITM<3:0>(1) | | | | WAITE<1:0>(1) | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **BUSY:** Busy bit (Master mode only)
- 1 = Port is busy
- 0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits
- 11 = Reserved, do not use
- 10 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> =11 (Addressable Slave mode only)
- 01 = Interrupt generated at the end of the read/write cycle
- 00 = No Interrupt generated

bit 12-11 **INCM<1:0>:** Increment Mode bits
- 11 = Slave mode read and write buffers auto-increment (MODE<1:0> = 00 only)
- 10 = Decrement ADDR<15:0> by 1 every read/write cycle(2)
- 01 = Increment ADDR<15:0> by 1 every read/write cycle(2)
- 00 = No increment or decrement of address

bit 10 **MODE16:** 8/16-bit Mode bit
- 1 = 16-bit mode: a read or write to the data register invokes a single 16-bit transfer
- 0 = 8-bit mode: a read or write to the data register invokes a single 8-bit transfer

bit 9-8 **MODE<1:0>:** Parallel Port Mode Select bits
- 11 = Master mode 1 (PMCSx, PMRD/PMWR, PMENB, PMA<x:0>, PMD<7:0> and PMD<8:15>(3))
- 10 = Master mode 2 (PMCSx, PMRD, PMWR, PMA<x:0>, PMD<7:0> and PMD<8:15>(3))
- 01 = Enhanced Slave mode, control signals (PMRD, PMWR, PMCS, PMD<7:0> and PMA<1:0>)
- 00 = Legacy Parallel Slave Port, control signals (PMRD, PMWR, PMCS and PMD<7:0>)

bit 7-6 **WAITB<1:0>:** Data Setup to Read/Write Strobe Wait States bits(1)
- 11 = Data wait of 4 TPB; multiplexed address phase of 4 TPB
- 10 = Data wait of 3 TPB; multiplexed address phase of 3 TPB
- 01 = Data wait of 2 TPB; multiplexed address phase of 2 TPB
- 00 = Data wait of 1 TPB; multiplexed address phase of 1 TPB (default)

**Note 1:** Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.

**2:** Address bits, A15 and A14, are not subject to automatic increment/decrement if configured as Chip Select CS2 and CS1.

**3:** These pins are active when MODE16 = 1 (16-bit mode).

**REGISTER 20-2: PMMODE: PARALLEL PORT MODE REGISTER (CONTINUED)**

bit 5-2 **WAITM<3:0>:** Data Read/Write Strobe Wait States bits(1)

1111 = Wait of 16 TPB
•
•
•
0001 = Wait of 2 TPB
0000 = Wait of 1 TPB (default)

bit 1-0 **WAITE<1:0>:** Data Hold After Read/Write Strobe Wait States bits(1)

11 = Wait of 4 TPB
10 = Wait of 3 TPB
01 = Wait of 2 TPB
00 = Wait of 1 TPB (default)

For Read operations:
11 = Wait of 3 TPB
10 = Wait of 2 TPB
01 = Wait of 1 TPB
00 = Wait of 0 TPB (default)

**Note 1:** Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.

**2:** Address bits, A15 and A14, are not subject to automatic increment/decrement if configured as Chip Select CS2 and CS1.

**3:** These pins are active when MODE16 = 1 (16-bit mode).


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**REGISTER 20-3: PMADDR: PARALLEL PORT ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CS2(1) | CS1(3) | ADDR<13:8> | | | | | |
| | ADDR15(2) | ADDR14(4) | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ADDR<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **CS2:** Chip Select 2 bit(1)
- 1 = Chip Select 2 is active
- 0 = Chip Select 2 is inactive

bit 15 **ADDR<15>:** Target Address bit 15(2)

bit 14 **CS1:** Chip Select 1 bit(3)
- 1 = Chip Select 1 is active
- 0 = Chip Select 1 is inactive

bit 14 **ADDR<14>:** Target Address bit 14(4)

bit 13-0 **ADDR<13:0>:** Address bits

**Note 1:** When the CSF<1:0> bits (PMCON<7:6>) = 10 or 01.
**2:** When the CSF<1:0> bits (PMCON<7:6>) = 00.
**3:** When the CSF<1:0> bits (PMCON<7:6>) = 10.
**4:** When the CSF<1:0> bits (PMCON<7:6>) = 00 or 01.

**Note:** If the DUALBUF bit (PMCON<17>) = 0, the bits in this register control both read and write target addressing. If the DUALBUF bit = 1, the bits in this register are not used. In this instance, use the PMRADDR register for Read operations and the PMWADDR register for Write operations.

**REGISTER 20-4: PMDOUT: PARALLEL PORT OUTPUT DATA REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DATAOUT<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DATAOUT<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **DATAOUT<15:0>:** Port Data Output bits

This register is used for Read operations in the Enhanced Parallel Slave mode and Write operations for Dual Buffer Master mode.

In Dual Buffer Master mode, the DUALBUF bit (PMPCON<17>) = 1, a write to the MSB triggers the transaction on the PMP port. When MODE16 = 1, MSB = DATAOUT<15:8>. When MODE16 = 0, MSB = DATAOUT<7:0>.

| **Note:** | In Master mode, a read will return the last value written to the register. In Slave mode, a read will return indeterminate results. |
|---|---|

**REGISTER 20-5: PMDIN: PARALLEL PORT INPUT DATA REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DATAIN<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DATAIN<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **DATAIN<15:0>:** Port Data Input bits

This register is used for both Parallel Master Port mode and Enhanced Parallel Slave mode.

In Parallel Master mode, a write to the MSB triggers the write transaction on the PMP port. Similarly, a read to the MSB triggers the read transaction on the PMP port.

When MODE16 = 1, MSB = DATAIN<15:8>. When MODE16 = 0, MSB = DATAIN<7:0>.

| **Note:** | This register is not used in Dual Buffer Master mode (i.e., DUALBUF bit (PMPCON<17>) = 1). |
|---|---|


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**REGISTER 20-6: PMAEN: PARALLEL PORT PIN ENABLE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PTEN<15:14>(1) | | PTEN<13:8> | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PTEN<7:2> | | | | | | PTEN<1:0>(2) | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Write '0'; ignore read

bit 15-14 **PTEN<15:14>:** PMCSx Address Port Enable bits
- 1 = PMA15 and PMA14 function as either PMA<15:14> or PMCS2 and PMCS1(1)
- 0 = PMA15 and PMA14 function as port I/O

bit 13-2 **PTEN<13:2>:** PMP Address Port Enable bits
- 1 = PMA<13:2> function as PMP address lines
- 0 = PMA<13:2> function as port I/O

bit 1-0 **PTEN<1:0>:** PMALH/PMALL Address Port Enable bits
- 1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL(2)
- 0 = PMA1 and PMA0 pads function as port I/O

**Note 1:** The use of these pins as PMA15/PMA14 or CS2/CS1 is selected by the CSF<1:0> bits (PMCON<7:6>).

**2:** The use of these pins as PMA1/PMA0 or PMALH/PMALL depends on the Address/Data Multiplex mode selected by the ADRMUX<1:0> bits in the PMCON register.

**REGISTER 20-7: PMSTAT: PARALLEL PORT STATUS REGISTER (SLAVE MODES ONLY)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R-0 | R/W-0, HSC | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
| | IBF | IBOV | — | — | IB3F | IB2F | IB1F | IB0F |
| 7:0 | R-1 | R/W-0, HSC | U-0 | U-0 | R-1 | R-1 | R-1 | R-1 |
| | OBE | OBUF | — | — | OB3E | OB2E | OB1E | OB0E |

| **Legend:** | HSC = Set by Hardware; Cleared by Software | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **IBF:** Input Buffer Full Status bit
- 1 = All writable input buffer registers are full
- 0 = Some or all of the writable input buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit
- 1 = A write attempt to a full input byte buffer occurred (must be cleared in software)
- 0 = No overflow occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IBxF:** Input Buffer 'x' Status Full bits
- 1 = Input Buffer contains data that has not been read (reading buffer will clear this bit)
- 0 = Input Buffer does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit
- 1 = All readable output buffer registers are empty
- 0 = Some or all of the readable output buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit
- 1 = A read occurred from an empty output byte buffer (must be cleared in software)
- 0 = No underflow occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OBxE:** Output Buffer 'x' Status Empty bits
- 1 = Output buffer is empty (writing data to the buffer will clear this bit)
- 0 = Output buffer contains data that has not been transmitted


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**REGISTER 20-8: PMWADDR: PARALLEL PORT WRITE ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | WCS2(1) | WCS1(3) | WADDR<13:8> | | | | | |
| | WADDR15(2) | WADDR14(4) | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | WADDR<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **WCS2:** Chip Select 2 bit(1)
- 1 = Chip Select 2 is active
- 0 = Chip Select 2 is inactive

bit 15 **WADDR<15>:** Target Address bit 15(2)

bit 14 **WCS1:** Chip Select 1 bit(3)
- 1 = Chip Select 1 is active
- 0 = Chip Select 1 is inactive

bit 14 **WADDR<14>:** Target Address bit 14(4)

bit 13-0 **WADDR<13:0>:** Address bits

**Note 1:** When the CSF<1:0> bits (PMCON<7:6>) = 10 or 01.
**2:** When the CSF<1:0> bits (PMCON<7:6>) = 00.
**3:** When the CSF<1:0> bits (PMCON<7:6>) = 10.
**4:** When the CSF<1:0> bits (PMCON<7:6>) = 00 or 01.

**Note:** This register is only used when the DUALBUF bit (PMCON<17>) is set to '1'.

**REGISTER 20-9: PMRADDR: PARALLEL PORT READ ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RCS2(1) | RCS1(3) | RADDR<13:8> | | | | | |
| | RADDR15(2) | RADDR14(4) | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RADDR<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **RCS2:** Chip Select 2 bit(1)
- 1 = Chip Select 2 is active
- 0 = Chip Select 2 is inactive (RADDR15 function is selected)

bit 15 **RADDR<15>:** Target Address bit 15(2)

bit 14 **RCS1:** Chip Select 1 bit(3)
- 1 = Chip Select 1 is active
- 0 = Chip Select 1 is inactive (RADDR14 function is selected)

bit 14 **RADDR<14>:** Target Address bit 14(4)

bit 13-0 **RADDR<13:0>:** Address bits

**Note 1:** When the CSF<1:0> bits (PMCON<7:6>) = 10 or 01.
**2:** When the CSF<1:0> bits (PMCON<7:6>) = 00.
**3:** When the CSF<1:0> bits (PMCON<7:6>) = 10.
**4:** When the CSF<1:0> bits (PMCON<7:6>) = 00 or 01.

**Note:** This register is only used when the DUALBUF bit (PMCON<17>) is set to '1'.


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**REGISTER 20-10: PMRDIN: PARALLEL PORT READ INPUT DATA REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RDATAIN<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RDATAIN<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **RDATAIN<15:0>:** Port Read Input Data bits

**Note:** This register is only used when the DUALBUF bit (PMCON<17>) is set to '1' and exclusively for reads. If the DUALBUF bit is '0', the PMDIN register (Register 20-5) is used for reads instead of PMRDIN.

**NOTES:**


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## 21.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

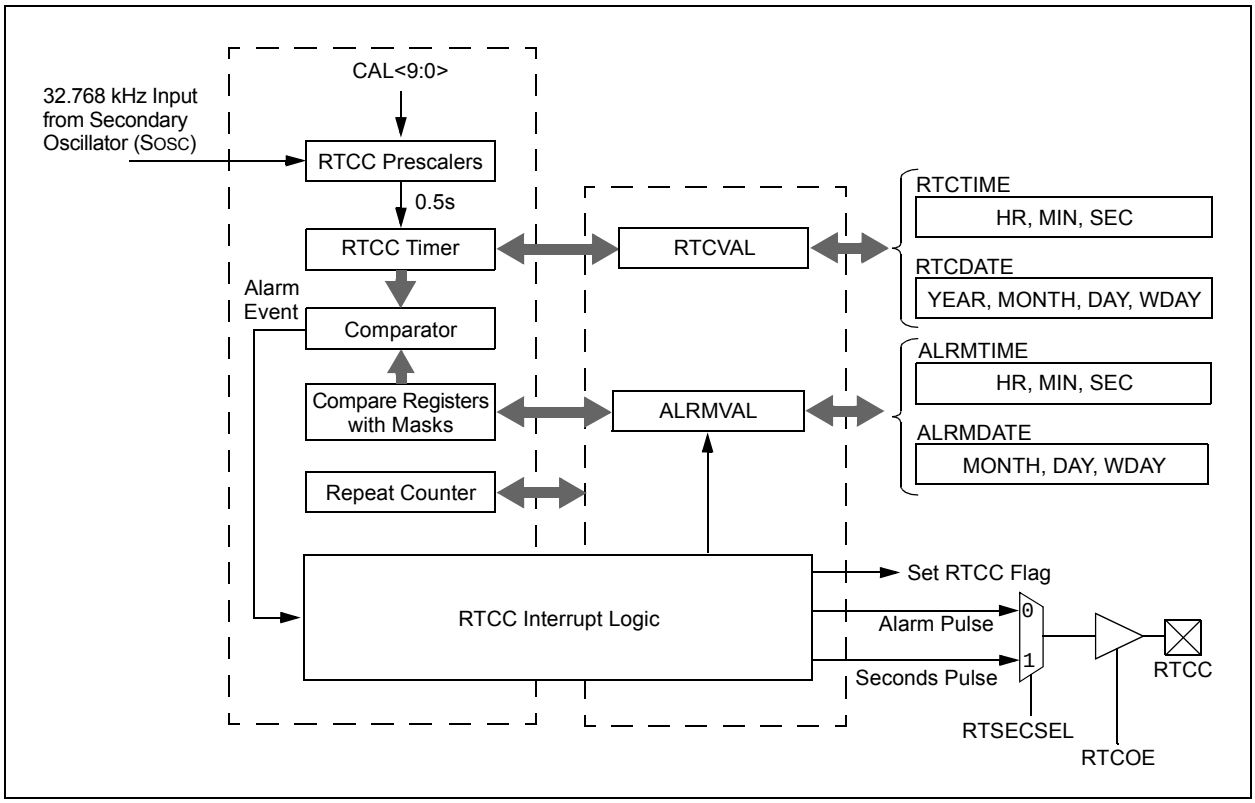
**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The PIC32 RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

The following are the key features of this module:

- Time: hours, minutes and seconds
- 24-hour format (military time)
- Visibility of one-half second period
- Provides calendar: Weekday, date, month and year
- Alarm intervals are configurable for half of a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month and one year
- Alarm repeat with decrementing counter
- Alarm with indefinite repeat: Chime
- Year range: 2000 to 2099
- Leap year correction
- BCD format for smaller firmware overhead
- Optimized for long-term battery operation
- Fractional second synchronization
- User calibration of the clock crystal frequency with auto-adjust
- Calibration range: ±0.66 seconds error per month
- Calibrates up to 260 ppm of crystal error
- Requirements: External 32.768 kHz clock crystal
- Alarm pulse or seconds clock output on RTCC pin

**FIGURE 21-1: RTCC BLOCK DIAGRAM**



## 21.1 Control Registers

**TABLE 21-1: RTCC REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0200 | RTCCON | 31:16 | — | — | — | — | — | — | CAL<9:0> | | | | | | | | | | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | RTSECSEL | RTCCLKON | — | — | RTCWREN | RTCSYNC | HALFSEC | RTCOE | 0000 |
| 0210 | RTCALRM | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ALRMEN | CHIME | PIV | ALRMSYNC | AMASK<3:0> | | | | ARPT<7:0> | | | | | | | | 0000 |
| 0220 | RTCTIME | 31:16 | HR10<3:0> | | | | HR01<3:0> | | | | MIN10<3:0> | | | | MIN01<3:0> | | | | xxxx |
| | | 15:0 | SEC10<3:0> | | | | SEC01<3:0> | | | | — | — | — | — | — | — | — | — | xx00 |
| 0230 | RTCDATE | 31:16 | YEAR10<3:0> | | | | YEAR01<3:0> | | | | MONTH10<3:0> | | | | MONTH01<3:0> | | | | xxxx |
| | | 15:0 | DAY10<3:0> | | | | DAY01<3:0> | | | | — | — | — | — | WDAY01<3:0> | | | | xx00 |
| 0240 | ALRMTIME | 31:16 | HR10<3:0> | | | | HR01<3:0> | | | | MIN10<3:0> | | | | MIN01<3:0> | | | | xxxx |
| | | 15:0 | SEC10<3:0> | | | | SEC01<3:0> | | | | — | — | — | — | — | — | — | — | xx00 |
| 0250 | ALRMDATE | 31:16 | — | — | — | — | — | — | — | — | MONTH10<3:0> | | | | MONTH01<3:0> | | | | 00xx |
| | | 15:0 | DAY10<3:0> | | | | DAY01<3:0> | | | | — | — | — | — | WDAY01<3:0> | | | | xx0x |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.



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**REGISTER 21-1: RTCCON: RTC CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | — | CAL<9:8> | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CAL<7:0> | | | | | | | |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ON(1,2) | — | SIDL | — | — | — | — | — |
| 7:0 | R/W-0 | R-0 | U-0 | U-0 | R/W-0 | R-0 | R-0 | R/W-0 |
| | RTSECSEL(3) | RTCCLKON | — | — | RTCWREN(4) | RTCSYNC | HALFSEC(5) | RTCOE |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-26 **Unimplemented:** Read as '0'

bit 25-16 **CAL<9:0>:** RTC Drift Calibration bits, which contain a signed 10-bit integer value
0111111111 = Maximum positive adjustment, adds 511 RTC clock pulses every one minute
•
•
•
0000000001 = Minimum positive adjustment, adds 1 RTC clock pulse every one minute
0000000000 = No adjustment
1111111111 = Minimum negative adjustment, subtracts 1 RTC clock pulse every one minute
•
•
•
1000000000 = Maximum negative adjustment, subtracts 512 clock pulses every one minute

bit 15 **ON:** RTCC On bit(1,2)
1 = RTCC module is enabled
0 = RTCC module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Disables the PBCLK to the RTCC when CPU enters in Idle mode
0 = Continue normal operation in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **RTSECSEL:** RTCC Seconds Clock Output Select bit(3)
1 = RTCC Seconds Clock is selected for the RTCC pin
0 = RTCC Alarm Pulse is selected for the RTCC pin

bit 6 **RTCCLKON:** RTCC Clock Enable Status bit
1 = RTCC Clock is actively running
0 = RTCC Clock is not running

bit 5-4 **Unimplemented:** Read as '0'

**Note 1:** The ON bit is only writable when RTCWREN = 1.
**2:** When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
**3:** Requires RTCOE = 1 (RTCCON<0>) for the output to be active.
**4:** The RTCWREN bit can be set only when the write sequence is enabled.
**5:** This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

**Note:** This register is reset only on a Power-on Reset (POR).

**REGISTER 21-1: RTCCON: RTC CONTROL REGISTER (CONTINUED)**

bit 3 **RTCWREN:** RTC Value Registers Write Enable bit(4)
- 1 = RTC Value registers can be written to by the user
- 0 = RTC Value registers are locked out from being written to by the user

bit 2 **RTCSYNC:** RTCC Value Registers Read Synchronization bit
- 1 = RTC Value registers can change while reading, due to a rollover ripple that results in an invalid data read If the register is read twice and results in the same data, the data can be assumed to be valid
- 0 = RTC Value registers can be read without concern about a rollover ripple

bit 1 **HALFSEC:** Half-Second Status bit(5)
- 1 = Second half period of a second
- 0 = First half period of a second

bit 0 **RTCOE:** RTCC Output Enable bit
- 1 = RTCC clock output enabled – clock presented onto an I/O
- 0 = RTCC clock output disabled

**Note 1:** The ON bit is only writable when RTCWREN = 1.

**2:** When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**3:** Requires RTCOE = 1 (RTCCON<0>) for the output to be active.

**4:** The RTCWREN bit can be set only when the write sequence is enabled.

**5:** This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

**Note:** This register is reset only on a Power-on Reset (POR).


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**REGISTER 21-2: RTCALRM: RTC ALARM CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ALRMEN(1,2) | CHIME(2) | PIV(2) | ALRMSYNC(3) | AMASK<3:0>(3) | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ARPT<7:0>(3) | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ALRMEN:** Alarm Enable bit(1,2)
- 1 = Alarm is enabled
- 0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit(2)
- 1 = Chime is enabled – ARPT<7:0> is allowed to rollover from 0x00 to 0xFF
- 0 = Chime is disabled – ARPT<7:0> stops once it reaches 0x00

bit 13 **PIV:** Alarm Pulse Initial Value bit(2)

When ALRMEN = 0, PIV is writable and determines the initial value of the Alarm Pulse.
When ALRMEN = 1, PIV is read-only and returns the state of the Alarm Pulse.

bit 12 **ALRMSYNC:** Alarm Sync bit(3)
- 1 = ARPT<7:0> and ALRMEN may change as a result of a half second rollover during a read. The ARPT must be read repeatedly until the same value is read twice. This must be done since multiple bits may be changing, which are then synchronized to the PB clock domain
- 0 = ARPT<7:0> and ALRMEN can be read without concerns of rollover because the prescaler is > 32 RTC clocks away from a half-second rollover

bit 11-8 **AMASK<3:0>:** Alarm Mask Configuration bits(3)
- 0000 = Every half-second
- 0001 = Every second
- 0010 = Every 10 seconds
- 0011 = Every minute
- 0100 = Every 10 minutes
- 0101 = Every hour
- 0110 = Once a day
- 0111 = Once a week
- 1000 = Once a month
- 1001 = Once a year (except when configured for February 29, once every four years)
- 1010 = Reserved; do not use
- 1011 = Reserved; do not use
- 11xx = Reserved; do not use

**Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

**2:** This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

**3:** This assumes a CPU read will execute in less than 32 PBCLKs.

**Note:** This register is reset only on a Power-on Reset (POR).

**REGISTER 21-2: RTCALRM: RTC ALARM CONTROL REGISTER (CONTINUED)**

bit 7-0 **ARPT<7:0>:** Alarm Repeat Counter Value bits(3)

11111111 =Alarm will trigger 256 times
•
•
•
00000000 =Alarm will trigger one time
The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = 1.

**Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

**2:** This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

**3:** This assumes a CPU read will execute in less than 32 PBCLKs.

| **Note:** | This register is reset only on a Power-on Reset (POR). |
|---|---|


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**REGISTER 21-3: RTCTIME: RTC TIME VALUE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | HR10<3:0> | | | | HR01<3:0> | | | |
| 23:16 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | MIN10<3:0> | | | | MIN01<3:0> | | | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | SEC10<3:0> | | | | SEC01<3:0> | | | |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-28 **HR10<3:0>:** Binary-Coded Decimal Value of Hours bits, 10s place digits; contains a value from 0 to 2

bit 27-24 **HR01<3:0>:** Binary-Coded Decimal Value of Hours bits, 1s place digit; contains a value from 0 to 9

bit 23-20 **MIN10<3:0>:** Binary-Coded Decimal Value of Minutes bits, 10s place digits; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>:** Binary-Coded Decimal Value of Minutes bits, 1s place digit; contains a value from 0 to 9

bit 15-12 **SEC10<3:0>:** Binary-Coded Decimal Value of Seconds bits, 10s place digits; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>:** Binary-Coded Decimal Value of Seconds bits, 1s place digit; contains a value from 0 to 9

bit 7-0 **Unimplemented:** Read as '0'

**Note:** This register is only writable when RTCWREN = 1 (RTCCON<3>).

**REGISTER 21-4: RTCDATE: RTC DATE VALUE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | YEAR10<3:0> | | | | YEAR01<3:0> | | | |
| 23:16 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | MONTH10<3:0> | | | | MONTH01<3:0> | | | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | DAY10<3:0> | | | | DAY01<3:0> | | | |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x |
| | — | — | — | — | WDAY01<3:0> | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-28 **YEAR10<3:0>:** Binary-Coded Decimal Value of Years bits, 10s place digits

bit 27-24 **YEAR01<3:0>:** Binary-Coded Decimal Value of Years bits, 1s place digit

bit 23-20 **MONTH10<3:0>:** Binary-Coded Decimal Value of Months bits, 10s place digits; contains a value of 0 or 1

bit 19-16 **MONTH01<3:0>:** Binary-Coded Decimal Value of Months bits, 1s place digit; contains a value from 0 to 9

bit 15-12 **DAY10<3:0>:** Binary-Coded Decimal Value of Days bits, 10s place digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary-Coded Decimal Value of Days bits, 1s place digit; contains a value from 0 to 9

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **WDAY01<3:0>:** Binary-Coded Decimal Value of Weekdays bits,1s place digit; contains a value from 0 to 6

**Note:** This register is only writable when RTCWREN = 1 (RTCCON<3>).


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**REGISTER 21-5: ALRMTIME: ALARM TIME VALUE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | HR10<3:0> | | | | HR01<3:0> | | | |
| 23:16 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | MIN10<3:0> | | | | MIN01<3:0> | | | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | SEC10<3:0> | | | | SEC01<3:0> | | | |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-28 **HR10<3:0>:** Binary Coded Decimal value of hours bits, 10s place digits; contains a value from 0 to 2

bit 27-24 **HR01<3:0>:** Binary Coded Decimal value of hours bits, 1s place digit; contains a value from 0 to 9

bit 23-20 **MIN10<3:0>:** Binary Coded Decimal value of minutes bits, 10s place digits; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>:** Binary Coded Decimal value of minutes bits, 1s place digit; contains a value from 0 to 9

bit 15-12 **SEC10<3:0>:** Binary Coded Decimal value of seconds bits, 10s place digits; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>:** Binary Coded Decimal value of seconds bits, 1s place digit; contains a value from 0 to 9

bit 7-0 **Unimplemented:** Read as '0'

**REGISTER 21-6: ALRMDATE: ALARM DATE VALUE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | MONTH10<3:0> | | | | MONTH01<3:0> | | | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | DAY10<1:0> | | | | DAY01<3:0> | | | |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x |
| | — | — | — | — | WDAY01<3:0> | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-24 **Unimplemented:** Read as '0'

bit 23-20 **MONTH10<3:0>:** Binary Coded Decimal value of months bits, 10s place digits; contains a value of 0 or 1

bit 19-16 **MONTH01<3:0>:** Binary Coded Decimal value of months bits, 1s place digit; contains a value from 0 to 9

bit 15-12 **DAY10<3:0>:** Binary Coded Decimal value of days bits, 10s place digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary Coded Decimal value of days bits, 1s place digit; contains a value from 0 to 9

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **WDAY01<3:0>:** Binary Coded Decimal value of weekdays bits, 1s place digit; contains a value from 0 to 6


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## 22.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

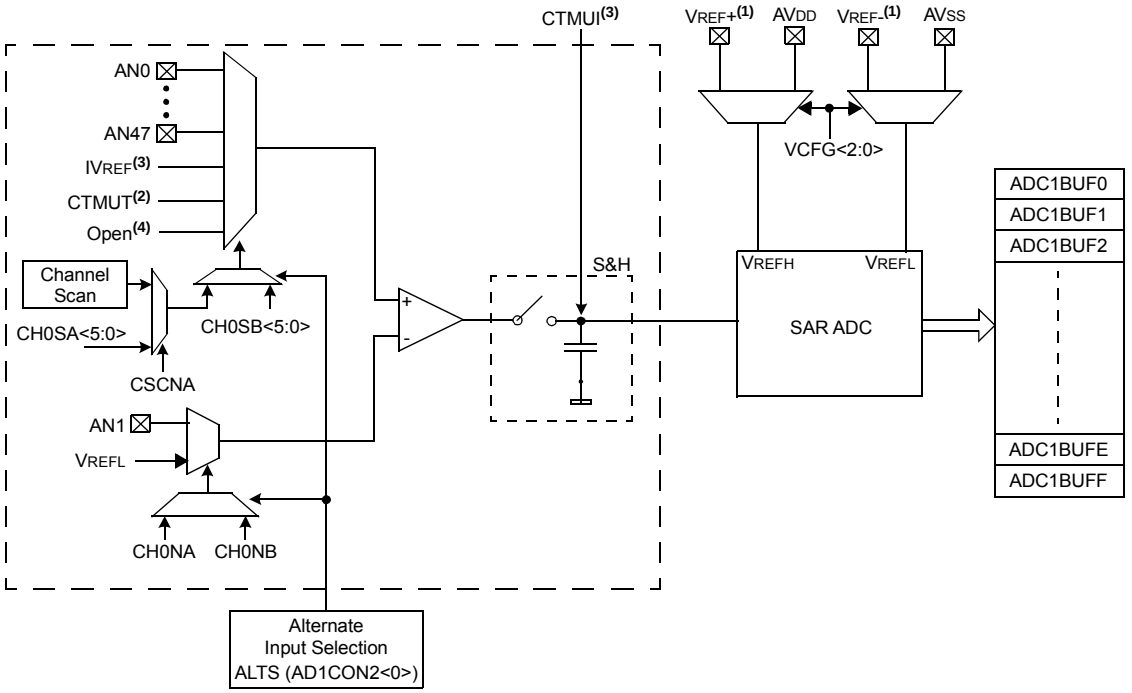
**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 17. "10-bit Analog-to-Digital Converter (ADC)"** (DS60001104) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The 10-bit Analog-to-Digital Converter (ADC) includes the following features:

- Successive Approximation Register (SAR) conversion
- Up to 1 Msps conversion speed
- Up to 48 analog input pins
- External voltage reference input pins
- One unipolar, differential Sample and Hold Amplifier (SHA)
- Automatic Channel Scan mode
- Selectable conversion trigger source
- 16-word conversion result buffer
- Selectable buffer fill modes
- Eight conversion result format options
- Operation during CPU Sleep and Idle modes

A block diagram of the 10-bit ADC is illustrated in Figure 22-1. The 10-bit ADC has up to 28 analog input pins, designated AN0-AN27. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins and may be common to other analog module references.

**FIGURE 22-1: ADC1 MODULE BLOCK DIAGRAM**



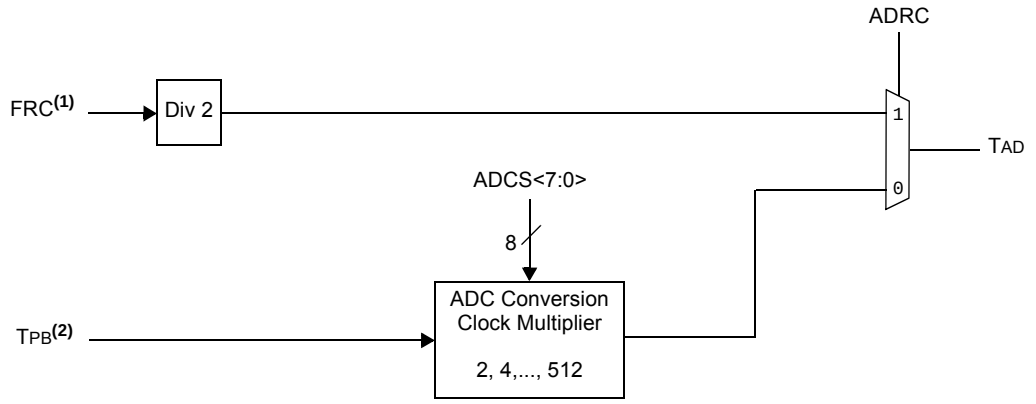

**Note 1:** VREF+ and VREF- inputs can be multiplexed with other analog inputs.

**2:** Connected to the CTMU temperature reference diode. See **Section 26.0 "Charge Time Measurement Unit (CTMU)"** for more information.

**3:** Internal precision 1.2V reference. See **Section 24.0 "Comparator"** for more information.

**4:** This selection is only used with CTMU capacitive and time measurement.

**FIGURE 22-2: ADC CONVERSION CLOCK PERIOD BLOCK DIAGRAM**




**Note 1:** See **Section 31.0 "40 MHz Electrical Characteristics"** for the exact FRC clock value.

**2:** Refer to Figure 8-1 in **Section 8.0 "Oscillator Configuration"** for more information.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## 22.1 Control Registers

**TABLE 22-1: ADC REGISTER MAP**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 9000 | AD1CON1(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | FORM<2:0> | | | SSRC<2:0> | | | CLRASAM | — | ASAM | SAMP | DONE | 0000 |
| 9010 | AD1CON2(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | VCFG<2:0> | | | OFFCAL | — | CSCNA | — | — | BUFS | — | SMPI<3:0> | | | | BUFM | ALTS | 0000 |
| 9020 | AD1CON3(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ADRC | — | — | SAMC<4:0> | | | | | ADCS<7:0> | | | | | | | | 0000 |
| 9040 | AD1CHS(1) | 31:16 | CH0NB | — | CH0SB<5:0>(2) | | | | | | CH0NA | — | CH0SA<5:0>(2) | | | | | | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 9050 | AD1CSSL(1,3) | 31:16 | CSSL31 | CSSL30 | CSSL29 | CSSL28 | CSSL27 | CSSL26 | CSSL25 | CSSL24 | CSSL23 | CSSL22 | CSSL21 | CSSL20 | CSSL19 | CSSL18 | CSSL17 | CSSL16 | 0000 |
| | | 15:0 | CSSL15 | CSSL14 | CSSL13 | CSSL12 | CSSL11 | CSSL10 | CSSL9 | CSSL8 | CSSL7 | CSSL6 | CSSL5 | CSSL4 | CSSL3 | CSSL2 | CSSL1 | CSSL0 | 0000 |
| 9060 | AD1CSSL2(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | CSSL50 | CSSL49 | CSSL48 | 0000 |
| | | 15:0 | CSSL47 | CSSL46 | CSSL45 | CSSL44 | CSSL43 | CSSL42 | CSSL41 | CSSL40 | CSSL39 | CSSL38 | CSSL37 | CSSL36 | CSSL35 | CSSL34 | CSSL33 | CSSL32 | 0000 |
| 9070 | ADC1BUF0 | 31:16 | ADC Result Word 0 (ADC1BUF0<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9080 | ADC1BUF1 | 31:16 | ADC Result Word 1 (ADC1BUF1<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9090 | ADC1BUF2 | 31:16 | ADC Result Word 2 (ADC1BUF2<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 90A0 | ADC1BUF3 | 31:16 | ADC Result Word 3 (ADC1BUF3<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 90B0 | ADC1BUF4 | 31:16 | ADC Result Word 4 (ADC1BUF4<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 90C0 | ADC1BUF5 | 31:16 | ADC Result Word 5 (ADC1BUF5<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 90D0 | ADC1BUF6 | 31:16 | ADC Result Word 6 (ADC1BUF6<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 90E0 | ADC1BUF7 | 31:16 | ADC Result Word 7 (ADC1BUF7<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 90F0 | ADC1BUF8 | 31:16 | ADC Result Word 8 (ADC1BUF8<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for details.

**2:** For 64-pin devices, the MSB of these bits is not available.

**3:** For 64-pin devices, only the CSSL30:CSSL0 bits are available.



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**TABLE 22-1: ADC REGISTER MAP (CONTINUED)**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 9100 | ADC1BUF9 | 31:16 | ADC Result Word 9 (ADC1BUF9<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9110 | ADC1BUFA | 31:16 | ADC Result Word A (ADC1BUFA<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9120 | ADC1BUFB | 31:16 | ADC Result Word B (ADC1BUFB<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9130 | ADC1BUFC | 31:16 | ADC Result Word C (ADC1BUFC<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9140 | ADC1BUFD | 31:16 | ADC Result Word D (ADC1BUFD<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9150 | ADC1BUFE | 31:16 | ADC Result Word E (ADC1BUFE<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9160 | ADC1BUFF | 31:16 | ADC Result Word F (ADC1BUFF<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for details.

**2:** For 64-pin devices, the MSB of these bits is not available.

**3:** For 64-pin devices, only the CSSL30:CSSL0 bits are available.



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**REGISTER 22-1: AD1CON1: ADC CONTROL REGISTER 1**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | ON(1) | — | SIDL | — | — | FORM<2:0> | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0, HSC | R/C-0, HSC |
| | SSRC<2:0> | | | CLRASAM | — | ASAM | SAMP(2) | DONE(3) |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** ADC Operating Mode bit(1)
- 1 = ADC module is operating
- 0 = ADC module is not operating

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when device enters Idle mode
- 0 = Continue module operation in Idle mode

bit 12-11 **Unimplemented:** Read as '0'

bit 10-8 **FORM<2:0>:** Data Output Format bits
- 011 = Signed Fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dd00 0000)
- 010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)
- 001 = Signed Integer 16-bit (DOUT = 0000 0000 0000 0000 ssss sssd dddd dddd)
- 000 = Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
- 111 = Signed Fractional 32-bit (DOUT = sddd dddd dd00 0000 0000 0000 0000)
- 110 = Fractional 32-bit (DOUT = dddd dddd dd00 0000 0000 0000 0000 0000)
- 101 = Signed Integer 32-bit (DOUT = ssss ssss ssss ssss ssss sssd dddd dddd)
- 100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

bit 7-5 **SSRC<2:0>:** Conversion Trigger Source Select bits
- 111 = Internal counter ends sampling and starts conversion (auto convert)
- 110 = Reserved
- 101 = Reserved
- 100 = Reserved
- 011 = CTMU ends sampling and starts conversion
- 010 = Timer 3 period match ends sampling and starts conversion
- 001 = Active transition on INT0 pin ends sampling and starts conversion
- 000 = Clearing SAMP bit ends sampling and starts conversion

**Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ 0, this bit is automatically cleared by hardware to end sampling and start conversion.

**3:** This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

**REGISTER 22-1: AD1CON1: ADC CONTROL REGISTER 1 (CONTINUED)**

bit 4 **CLRASAM:** Stop Conversion Sequence bit (when the first ADC interrupt is generated)
1 = Stop conversions when the first ADC interrupt is generated. Hardware clears the ASAM bit when the ADC interrupt is generated.
0 = Normal operation, buffer contents will be overwritten by the next conversion sequence

bit 3 **Unimplemented:** Read as '0'

bit 2 **ASAM:** ADC Sample Auto-Start bit
1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set.
0 = Sampling begins when SAMP bit is set

bit 1 **SAMP:** ADC Sample Enable bit(2)
1 = The ADC sample and hold amplifier is sampling
0 = The ADC sample/hold amplifier is holding
When ASAM = 0, writing '1' to this bit starts sampling.
When SSRC = 000, writing '0' to this bit will end sampling and start conversion.

bit 0 **DONE:** Analog-to-Digital Conversion Status bit(3)
1 = Analog-to-digital conversion is done
0 = Analog-to-digital conversion is not done or has not started
Clearing this bit will not affect any operation in progress.

**Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ 0, this bit is automatically cleared by hardware to end sampling and start conversion.

**3:** This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.


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**REGISTER 22-2: AD1CON2: ADC CONTROL REGISTER 2**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 |
| | VCFG<2:0> | | | OFFCAL | — | CSCNA | — | — |
| 7:0 | R-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BUFS | — | SMPI<3:0> | | | | BUFM | ALTS |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-13 **VCFG<2:0>:** Voltage Reference Configuration bits

| | VREFH | VREFL |
|---|---|---|
| 000 | AVDD | AVss |
| 001 | External VREF+ pin | AVSS |
| 010 | AVDD | External VREF- pin |
| 011 | External VREF+ pin | External VREF- pin |
| 1xx | AVDD | AVSS |

bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit
1 = Enable Offset Calibration mode
Positive and negative inputs of the sample and hold amplifier are connected to VREFL
0 = Disable Offset Calibration mode
The inputs to the sample and hold amplifier are controlled by AD1CHS or AD1CSSL

bit 11 **Unimplemented:** Read as '0'

bit 10 **CSCNA:** Input Scan Select bit
1 = Scan inputs
0 = Do not scan inputs

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit
Only valid when BUFM = 1.
1 = ADC is currently filling buffer 0x8-0xF, user should access data in 0x0-0x7
0 = ADC is currently filling buffer 0x0-0x7, user should access data in 0x8-0xF

bit 6 **Unimplemented:** Read as '0'

bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences Per Interrupt Selection bits
1111 = Interrupts at the completion of conversion for each 16th sample/convert sequence
1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence
•
•
•
0001 = Interrupts at the completion of conversion for each 2nd sample/convert sequence
0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **BUFM:** ADC Result Buffer Mode Select bit
1 = Buffer configured as two 8-word buffers, ADC1BUF7-ADC1BUF0, ADC1BUFF-ADCBUF8
0 = Buffer configured as one 16-word buffer ADC1BUFF-ADC1BUF0

bit 0 **ALTS:** Alternate Input Sample Mode Select bit
1 = Uses Sample A input multiplexer settings for first sample, then alternates between Sample B and Sample A input multiplexer settings for all subsequent samples
0 = Always use Sample A input multiplexer settings

**REGISTER 22-3: AD1CON3: ADC CONTROL REGISTER 3**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ADRC | — | — | SAMC<4:0>(1) | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W | R/W-0 |
| | ADCS<7:0>(2) | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ADRC:** ADC Conversion Clock Source bit
1 = Clock derived from FRC
0 = Clock derived from Peripheral Bus Clock (PBCLK)

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits(1)
11111 = 31 TAD
•
•
•
00001 = 1 TAD
00000 = 0 TAD (Not allowed)

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits(2)
11111111 =TPB • 2 • (ADCS<7:0> + 1) = 512 • TPB = TAD
•
•
•
00000001 =TPB • 2 • (ADCS<7:0> + 1) = 4 • TPB = TAD
00000000 =TPB • 2 • (ADCS<7:0> + 1) = 2 • TPB = TAD

**Note 1:** This bit is only used if the SSRC<2:0> bits (AD1CON1<7:5>) = 111.
**2:** This bit is not used if the ADRC bit (AD1CON3<15>) = 1.


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**REGISTER 22-4: AD1CHS: ADC INPUT SELECT REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CH0NB | — | CH0SB<5:0> | | | | | |
| 23:16 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CH0NA | — | CH0SA<5:0> | | | | | |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **CH0NB:** Negative Input Select bit for Sample B
1 = Channel 0 negative input is AN1
0 = Channel 0 negative input is VREFL

bit 30 **Unimplemented:** Read as '0'

bit 29-24 **CH0SB<5:0>:** Positive Input Select bits for Sample B
For 64-pin devices:
011110 = Channel 0 positive input is Open(1)
011101 = Channel 0 positive input is CTMU temperature sensor (CTMUT)(2)
011100 = Channel 0 positive input is IVREF(3)
011011 = Channel 0 positive input is AN27
•
•
•
000001 = Channel 0 positive input is AN1
000000 = Channel 0 positive input is AN0
For 100-pin devices:
110010 = Channel 0 positive input is Open(1)
110001 = Channel 0 positive input is CTMU temperature sensor (CTMUT)(2)
110000 = Channel 0 positive input is IVREF(3)
101111 = Channel 0 positive input is AN47
•
•
•
0000001 = Channel 0 positive input is AN1
0000000 = Channel 0 positive input is AN0

bit 23 **CH0NA:** Negative Input Select bit for Sample A Multiplexer Setting(3)
1 = Channel 0 negative input is AN1
0 = Channel 0 negative input is VREFL

bit 22 **Unimplemented:** Read as '0'

**Note 1:** This selection is only used with CTMU capacitive and time measurement.
**2:** See **Section 26.0 "Charge Time Measurement Unit (CTMU)"** for more information.
**3:** Internal precision 1.2V reference. See **Section 24.0 "Comparator"** for more information.

**REGISTER 22-4: AD1CHS: ADC INPUT SELECT REGISTER (CONTINUED)**

bit 21-16 **CH0SA<5:0>:** Positive Input Select bits for Sample A Multiplexer Setting

For 64-pin devices:

011110 = Channel 0 positive input is Open(1)
011101 = Channel 0 positive input is CTMU temperature sensor (CTMUT)(2)
011100 = Channel 0 positive input is IVREF(3)
011011 = Channel 0 positive input is AN27
•
•
•
000001 = Channel 0 positive input is AN1
000000 = Channel 0 positive input is AN0

For 100-pin devices:

110010 = Channel 0 positive input is Open(1)
110001 = Channel 0 positive input is CTMU temperature sensor (CTMUT)(2)
110000 = Channel 0 positive input is IVREF(3)
101111 = Channel 0 positive input is AN47
•
•
•
0000001 = Channel 0 positive input is AN1
0000000 = Channel 0 positive input is AN0

bit 15-0 **Unimplemented:** Read as '0'

**Note 1:** This selection is only used with CTMU capacitive and time measurement.
**2:** See **Section 26.0 "Charge Time Measurement Unit (CTMU)"** for more information.
**3:** Internal precision 1.2V reference. See **Section 24.0 "Comparator"** for more information.


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**REGISTER 22-5: AD1CSSL: ADC INPUT SCAN SELECT REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CSSL31(2) | CSSL30(1) | CSSL29(1) | CSSL28(1) | CSSL27 | CSSL26 | CSSL25 | CSSL24 |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CSSL23 | CSSL21 | CSSL21 | CSSL20 | CSSL19 | CSSL18 | CSSL17 | CSSL16 |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CSSL15 | CSSL14 | CSSL13 | CSSL12 | CSSL11 | CSSL10 | CSSL9 | CSSL8 |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CSSL7 | CSSL6 | CSSL5 | CSSL4 | CSSL3 | CSSL2 | CSSL1 | CSSL0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **CSSL<31:0>:** ADC Input Pin Scan Selection bits
1 = Select ANx for input scan; CSSLx = ANx, where 'x' = 0-31
0 = Skip ANx for input scan; CSSLx = ANx, where 'x' = 0-31

**Note 1:** For devices with 64 pins, CSSL28 selects IVREF (Band Gap) for scan; CSSL29 selects CTMU temperature diode for scan; and CSSL30 selects CTMU input for scan

**2:** On devices with less than 32 analog inputs, all CSSLx bits can be selected; however, inputs selected for scan without a corresponding input on the device will convert to VREFL.

**REGISTER 22-6: AD1CSSL2: ADC INPUT SCAN SELECT REGISTER 2**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | CSSL50(1) | CSSL49(1) | CSSL48(1) |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CSSL47 | CSSL46 | CSSL45 | CSSL44 | CSSL43 | CSSL42 | CSSL41 | CSSL40 |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CSSL39 | CSSL38 | CSSL37 | CSSL36 | CSSL35 | CSSL34 | CSSL33 | CSSL32 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-19 **Unimplemented:** Read as '0'

bit 18-0 **CSSL<50:32>:** ADC Input Pin Scan Selection bits
1 = Select ANx for input scan; CSSLx = ANx, where 'x' = 32-50
0 = Skip ANx for input scan; CSSLx = ANx, where 'x' = 32-50

**Note 1:** For devices with 100 or more pins, CSSL48 selects IVREF (Band Gap) for scan; CSSL49 selects CTMU temperature diode for scan; and CSSL50 selects CTMU input for scan

**Note:** The ANx inputs in this register only support devices with 100 or more pins.

**NOTES:**


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## 23.0 CONTROLLER AREA NETWORK (CAN)

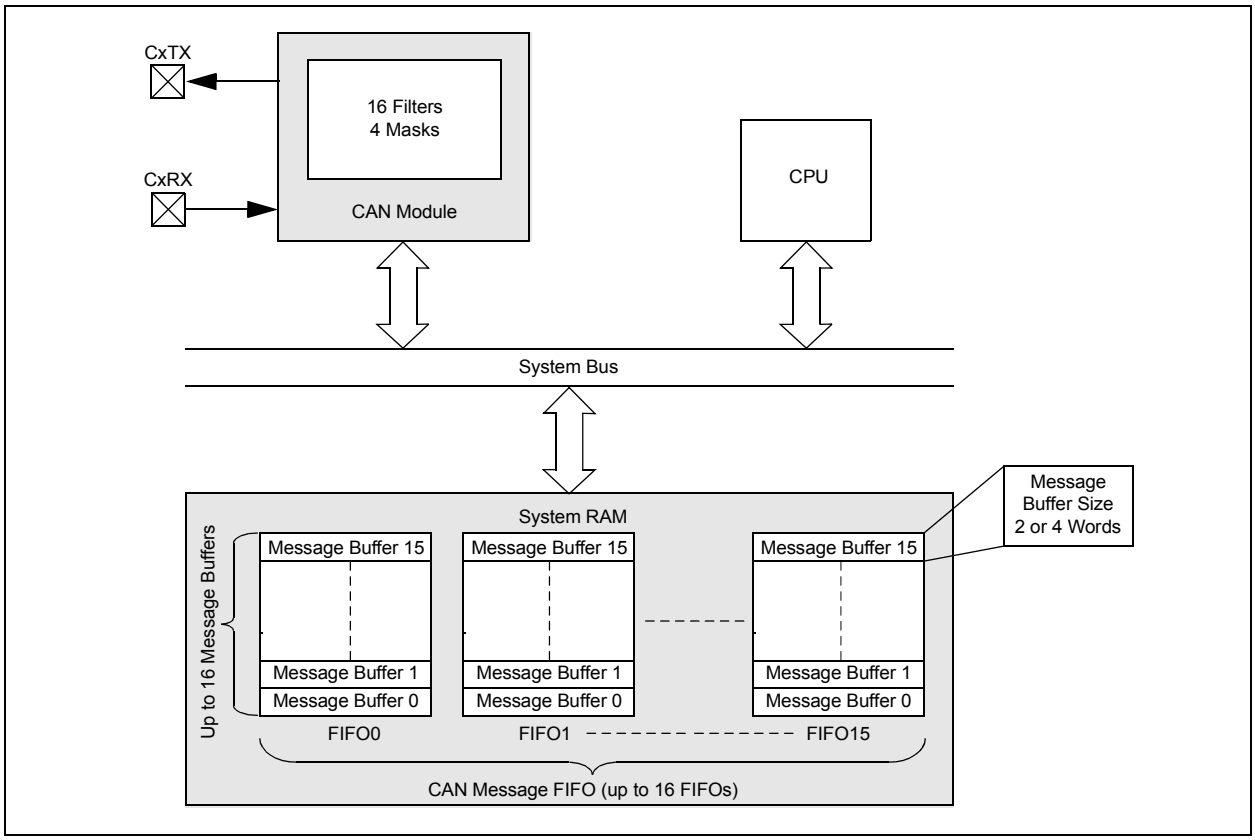
**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 34. "Controller Area Network (CAN)"** (DS60001154) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Controller Area Network (CAN) module supports the following key features:

- Standards Compliance:
  - Full CAN 2.0B compliance
  - Programmable bit rate up to 1 Mbps
- Message Reception and Transmission:
  - 16 message FIFOs
  - Each FIFO can have up to 16 messages for a total of 256 messages
  - FIFO can be a transmit message FIFO or a receive message FIFO
  - User-defined priority levels for message FIFOs used for transmission
  - 16 acceptance filters for message filtering
  - Four acceptance filter mask registers for message filtering
  - Automatic response to remote transmit request
  - DeviceNet™ addressing support
- Additional Features:
  - Loopback, Listen All Messages, and Listen Only modes for self-test, system diagnostics and bus monitoring
  - Low-power operating modes
  - CAN module is a bus master on the PIC32 system bus
  - Use of DMA is not required
  - Dedicated time-stamp timer
  - Dedicated DMA channels
  - Data-only Message Reception mode

Figure 23-1 illustrates the general structure of the CAN module.

**FIGURE 23-1: PIC32 CAN MODULE BLOCK DIAGRAM**



## 23.1 Control Registers

**TABLE 23-1: CAN1 REGISTER SUMMARY**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| B000 | C1CON | 31:16 | — | — | — | — | ABAT | REQOP<2:0> | | | OPMOD<2:0> | | | CANCAP | — | — | — | — | 0480 |
| | | 15:0 | ON | — | SIDLE | — | CANBUSY | — | — | — | — | — | — | DNCNT<4:0> | | | | | 0000 |
| B010 | C1CFG | 31:16 | — | — | — | — | — | — | — | — | — | WAKFIL | — | — | — | SEG2PH<2:0> | | | 0000 |
| | | 15:0 | SEG2PHTS | SAM | SEG1PH<2:0> | | | PRSEG<2:0> | | | SJW<1:0> | | BRP<5:0> | | | | | | 0000 |
| B020 | C1INT | 31:16 | IVRIE | WAKIE | CERRIE | SERRIE | RBOVIE | — | — | — | — | — | — | — | MODIE | CTMRIE | RBIE | TBIE | 0000 |
| | | 15:0 | IVRIF | WAKIF | CERRIF | SERRIF | RBOVIF | — | — | — | — | — | — | — | MODIF | CTMRIF | RBIF | TBIF | 0000 |
| B030 | C1VEC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | FILHIT<4:0> | | | | | — | ICODE<6:0> | | | | | | | 0040 |
| B040 | C1TREC | 31:16 | — | — | — | — | — | — | — | — | — | — | TXBO | TXBP | RXBP | TXWARN | RXWARN | EWARN | 0000 |
| | | 15:0 | TERRCNT<7:0> | | | | | | | | RERRCNT<7:0> | | | | | | | | 0000 |
| B050 | C1FSTAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | FIFOIP15 | FIFOIP14 | FIFOIP13 | FIFOIP12 | FIFOIP11 | FIFOIP10 | FIFOIP9 | FIFOIP8 | FIFOIP7 | FIFOIP6 | FIFOIP5 | FIFOIP4 | FIFOIP3 | FIFOIP2 | FIFOIP1 | FIFOIP0 | 0000 |
| B060 | C1RXOVF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RXOVF15 | RXOVF14 | RXOVF13 | RXOVF12 | RXOVF11 | RXOVF10 | RXOVF9 | RXOVF8 | RXOVF7 | RXOVF6 | RXOVF5 | RXOVF4 | RXOVF3 | RXOVF2 | RXOVF1 | RXOVF0 | 0000 |
| B070 | C1TMR | 31:16 | CANTS<15:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | CANTSPRE<15:0> | | | | | | | | | | | | | | | | 0000 |
| B080 | C1RXM0 | 31:16 | SID<10:0> | | | | | | | | | | | -— | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| B090 | C1RXM1 | 31:16 | SID<10:0> | | | | | | | | | | | -— | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| B0A0 | C1RXM2 | 31:16 | SID<10:0> | | | | | | | | | | | -— | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| B0B0 | C1RXM3 | 31:16 | SID<10:0> | | | | | | | | | | | -— | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| B0C0 | C1FLTCON0 | 31:16 | FLTEN3 | MSEL3<1:0> | | FSEL3<4:0> | | | | | FLTEN2 | MSEL2<1:0> | | FSEL2<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN1 | MSEL1<1:0> | | FSEL1<4:0> | | | | | FLTEN0 | MSEL0<1:0> | | FSEL0<4:0> | | | | | 0000 |
| B0D0 | C1FLTCON1 | 31:16 | FLTEN7 | MSEL7<1:0> | | FSEL7<4:0> | | | | | FLTEN6 | MSEL6<1:0> | | FSEL6<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN5 | MSEL5<1:0> | | FSEL5<4:0> | | | | | FLTEN4 | MSEL4<1:0> | | FSEL4<4:0> | | | | | 0000 |
| B0E0 | C1FLTCON2 | 31:16 | FLTEN11 | MSEL11<1:0> | | FSEL11<4:0> | | | | | FLTEN10 | MSEL10<1:0> | | FSEL10<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN9 | MSEL9<1:0> | | FSEL9<4:0> | | | | | FLTEN8 | MSEL8<1:0> | | FSEL8<4:0> | | | | | 0000 |
| B0F0 | C1FLTCON3 | 31:16 | FLTEN15 | MSEL15<1:0> | | FSEL15<4:0> | | | | | FLTEN14 | MSEL14<1:0> | | FSEL14<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN13 | MSEL13<1:0> | | FSEL13<4:0> | | | | | FLTEN12 | MSEL12<1:0> | | FSEL12<4:0> | | | | | 0000 |
| B140 | C1RXFn (n = 0-15) | 31:16 | SID<10:0> | | | | | | | | | | | -— | EXID | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.



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**TABLE 23-1: CAN1 REGISTER SUMMARY (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| B340 | C1FIFOBA | 31:16 | C1FIFOBA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| B350 | C1FIFOCONn (n = 0-15) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | FSIZE<4:0> | | | | | 0000 |
| | | 15:0 | — | FRESET | UINC | DONLY | — | — | — | — | TXEN | TXABAT | TXLARB | TXERR | TXREQ | RTREN | TXPRI<1:0> | | 0000 |
| B360 | C1FIFOINTn (n = 0-15) | 31:16 | — | — | — | — | — | TXNFULLIE | TXHALFIE | TXEMPTYIE | — | — | — | — | RXOVFLIE | RXFULLIE | RXHALFIE | RXN EMPTYIE | 0000 |
| | | 15:0 | — | — | — | — | — | TXNFULLIF | TXHALFIF | TXEMPTYIF | — | — | — | — | RXOVFLIF | RXFULLIF | RXHALFIF | RXN EMPTYIF | 0000 |
| B370 | C1FIFOUAn (n = 0-15) | 31:16 | C1FIFOUA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| B380 | C1FIFOCIn (n = 0-15) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | C1FIFOCIn<4:0> | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

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**REGISTER 23-1: C1CON: CAN MODULE CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | S/HC-0 | R/W-1 | R/W-0 | R/W-0 |
| | — | — | — | — | ABAT | REQOP<2:0> | | |
| 23:16 | R-1 | R-0 | R-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
| | OPMOD<2:0> | | | CANCAP | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | R-0 | U-0 | U-0 | U-0 |
| | ON(1) | — | SIDLE | — | CANBUSY | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | DNCNT<4:0> | | | | |

| Legend: | HC = Hardware Clear | S = Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **ABAT:** Abort All Pending Transmissions bit
1 = Signal all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions aborted

bit 26-24 **REQOP<2:0>:** Request Operation Mode bits
111 = Set Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Set Configuration mode
011 = Set Listen Only mode
010 = Set Loopback mode
001 = Set Disable mode
000 = Set Normal Operation mode

bit 23-21 **OPMOD<2:0>:** Operation Mode Status bits
111 = Module is in Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal Operation mode

bit 20 **CANCAP:** CAN Message Receive Time Stamp Timer Capture Enable bit
1 = CANTMR value is stored on valid message reception and is stored with the message
0 = Disable CAN message receive time stamp timer capture and stop CANTMR to conserve power

bit 19-16 **Unimplemented:** Read as '0'

bit 15 **ON:** CAN On bit(1)
1 = CAN module is enabled
0 = CAN module is disabled

bit 14 **Unimplemented:** Read as '0'

**Note 1:** If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.


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**REGISTER 23-1: C1CON: CAN MODULE CONTROL REGISTER (CONTINUED)**

bit 13 **SIDLE:** CAN Stop in Idle bit
1 = CAN Stops operation when system enters Idle mode
0 = CAN continues operation when system enters Idle mode

bit 12 **Unimplemented:** Read as '0'

bit 11 **CANBUSY:** CAN Module is Busy bit
1 = The CAN module is active
0 = The CAN module is completely disabled

bit 10-5 **Unimplemented:** Read as '0'

bit 4-0 **DNCNT<4:0>:** Device Net Filter Bit Number bits
10011-11111 = Invalid Selection (compare up to 18-bits of data with EID)
10010 = Compare up to data byte 2 bit 6 with EID17 (C1RXFn<17>)
•
•
•
00001 = Compare up to data byte 0 bit 7 with EID0 (C1RXFn<0>)
00000 = Do not compare data bytes

**Note 1:** If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

**REGISTER 23-2: C1CFG: CAN BAUD RATE CONFIGURATION REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | WAKFIL | — | — | — | SEG2PH<2:0>(1,4) | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SEG2PHTS(1) | SAM(2) | SEG1PH<2:0> | | | PRSEG<2:0> | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SJW<1:0>(3) | | BRP<5:0> | | | | | |

| Legend: | HC = Hardware Clear | S = Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-23 **Unimplemented:** Read as '0'

bit 22 **WAKFIL:** CAN Bus Line Filter Enable bit
1 = Use CAN bus line filter for wake-up
0 = CAN bus line filter is not used for wake-up

bit 21-19 **Unimplemented:** Read as '0'

bit 18-16 **SEG2PH<2:0>:** Phase Buffer Segment 2 bits(1,4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 15 **SEG2PHTS:** Phase Segment 2 Time Select bit(1)
1 = Freely programmable
0 = Maximum of SEG1PH or Information Processing Time, whichever is greater

bit 14 **SAM:** Sample of the CAN Bus Line bit(2)
1 = Bus line is sampled three times at the sample point
0 = Bus line is sampled once at the sample point

bit 13-11 **SEG1PH<2:0>:** Phase Buffer Segment 1 bits(4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

**Note 1:** SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.
**2:** 3 Time bit sampling is not allowed for BRP < 2.
**3:** SJW ≤ SEG2PH.
**4:** The Time Quanta per bit must be greater than 7 (that is, TQBIT > 7).

**Note:** This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (C1CON<23:21>) = 100).


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**REGISTER 23-2: C1CFG: CAN BAUD RATE CONFIGURATION REGISTER (CONTINUED)**

bit 10-8 **PRSEG<2:0>:** Propagation Time Segment bits(4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 7-6 **SJW<1:0>:** Synchronization Jump Width bits(3)
11 = Length is 4 x TQ
10 = Length is 3 x TQ
01 = Length is 2 x TQ
00 = Length is 1 x TQ

bit 5-0 **BRP<5:0>:** Baud Rate Prescaler bits
111111 = TQ = (2 x 64)/SYSCLK
111110 = TQ = (2 x 63)/SYSCLK
•
•
•
000001 = TQ = (2 x 2)/SYSCLK
000000 = TQ = (2 x 1)/SYSCLK

**Note 1:** SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.
**2:** 3 Time bit sampling is not allowed for BRP < 2.
**3:** SJW ≤ SEG2PH.
**4:** The Time Quanta per bit must be greater than 7 (that is, TQBIT > 7).

**Note:** This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (C1CON<23:21>) = 100).

**REGISTER 23-3: C1INT: CAN INTERRUPT REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
| | IVRIE | WAKIE | CERRIE | SERRIE | RBOVIE | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | MODIE | CTMRIE | RBIE | TBIE |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
| | IVRIF | WAKIF | CERRIF | SERRIF(1) | RBOVIF | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | MODIF | CTMRIF | RBIF | TBIF |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **IVRIE:** Invalid Message Received Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 30 **WAKIE:** CAN Bus Activity Wake-up Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 29 **CERRIE:** CAN Bus Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 28 **SERRIE:** System Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 27 **RBOVIE:** Receive Buffer Overflow Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 26-20 **Unimplemented:** Read as '0'

bit 19 **MODIE:** Mode Change Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 18 **CTMRIE:** CAN Timestamp Timer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 17 **RBIE:** Receive Buffer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 16 **TBIE:** Transmit Buffer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 15 **IVRIF:** Invalid Message Received Interrupt Flag bit
1 = An invalid messages interrupt has occurred
0 = An invalid message interrupt has not occurred

**Note 1:** This bit can only be cleared by turning the CAN module Off and On by clearing or setting the ON bit (C1CON<15>).


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**REGISTER 23-3: C1INT: CAN INTERRUPT REGISTER (CONTINUED)**

bit 14 **WAKIF:** CAN Bus Activity Wake-up Interrupt Flag bit
1 = A bus wake-up activity interrupt has occurred
0 = A bus wake-up activity interrupt has not occurred

bit 13 **CERRIF:** CAN Bus Error Interrupt Flag bit
1 = A CAN bus error has occurred
0 = A CAN bus error has not occurred

bit 12 **SERRIF:** System Error Interrupt Flag bit(1)
1 = A system error occurred (typically an illegal address was presented to the system bus)
0 = A system error has not occurred

bit 11 **RBOVIF:** Receive Buffer Overflow Interrupt Flag bit
1 = A receive buffer overflow has occurred
0 = A receive buffer overflow has not occurred

bit 10-4 **Unimplemented:** Read as '0'

bit 3 **MODIF:** CAN Mode Change Interrupt Flag bit
1 = A CAN module mode change has occurred (OPMOD<2:0> has changed to reflect REQOP)
0 = A CAN module mode change has not occurred

bit 2 **CTMRIF:** CAN Timer Overflow Interrupt Flag bit
1 = A CAN timer (CANTMR) overflow has occurred
0 = A CAN timer (CANTMR) overflow has not occurred

bit 1 **RBIF:** Receive Buffer Interrupt Flag bit
1 = A receive buffer interrupt is pending
0 = A receive buffer interrupt is not pending

bit 0 **TBIF:** Transmit Buffer Interrupt Flag bit
1 = A transmit buffer interrupt is pending
0 = A transmit buffer interrupt is not pending

**Note 1:** This bit can only be cleared by turning the CAN module Off and On by clearing or setting the ON bit (C1CON<15>).

**REGISTER 23-4: C1VEC: CAN INTERRUPT CODE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | — | — | — | FILHIT<4:0> | | | | |
| 7:0 | U-0 | R-1 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | — | ICODE<6:0>(1) | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-13 **Unimplemented:** Read as '0'

bit 12-8 **FILHIT<4:0>:** Filter Hit Number bit

11111 = Reserved
•
•
•
10000 = Reserved
01111 = Filter 15
•
•
•
00000 = Filter 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **ICODE<6:0>:** Interrupt Flag Code bits(1)

1111111 = Reserved
•
•
•
1001001 = Reserved
1001000 = Invalid message received (IVRIF)
1000111 = CAN module mode change (MODIF)
1000110 = CAN timestamp timer (CTMRIF)
1000101 = Bus bandwidth error (SERRIF)
1000100 = Address error interrupt (SERRIF)
1000011 = Receive FIFO overflow interrupt (RBOVIF)
1000010 = Wake-up interrupt (WAKIF)
1000001 = Error Interrupt (CERRIF)
1000000 = No interrupt
0111111 = Reserved
•
•
•
0010000 = Reserved
0001111 = FIFO15 Interrupt (C1FSTAT<15> set)
•
•
•
0000000 = FIFO0 Interrupt (C1FSTAT<0> set)

**Note 1:** These bits are only updated for enabled interrupts.


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**REGISTER 23-5: C1TREC: CAN TRANSMIT/RECEIVE ERROR COUNT REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | — | — | TXBO | TXBP | RXBP | TXWARN | RXWARN | EWARN |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | TERRCNT<7:0> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | RERRCNT<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-22 **Unimplemented:** Read as '0'

bit 21 **TXBO:** Transmitter in Error State Bus OFF (TERRCNT ≥ 256)

bit 20 **TXBP:** Transmitter in Error State Bus Passive (TERRCNT ≥ 128)

bit 19 **RXBP:** Receiver in Error State Bus Passive (RERRCNT ≥ 128)

bit 18 **TXWARN:** Transmitter in Error State Warning (128 > TERRCNT ≥ 96)

bit 17 **RXWARN:** Receiver in Error State Warning (128 > RERRCNT ≥ 96)

bit 16 **EWARN:** Transmitter or Receiver is in Error State Warning

bit 15-8 **TERRCNT<7:0>:** Transmit Error Counter

bit 7-0 **RERRCNT<7:0>:** Receive Error Counter

**REGISTER 23-6: C1FSTAT: CAN FIFO STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | FIFOIP15 | FIFOIP14 | FIFOIP13 | FIFOIP12 | FIFOIP11 | FIFOIP10 | FIFOIP9 | FIFOIP8 |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | FIFOIP7 | FIFOIP6 | FIFOIP5 | FIFOIP4 | FIFOIP3 | FIFOIP2 | FIFOIP1 | FIFOIP0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **FIFOIP<15:0>:** FIFOx Interrupt Pending bits

1 = One or more enabled FIFO interrupts are pending

0 = No FIFO interrupts are pending

**REGISTER 23-7: C1RXOVF: CAN RECEIVE FIFO OVERFLOW STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | RXOVF15 | RXOVF14 | RXOVF13 | RXOVF12 | RXOVF11 | RXOVF10 | RXOVF9 | RXOVF8 |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | RXOVF7 | RXOVF6 | RXOVF5 | RXOVF4 | RXOVF3 | RXOVF2 | RXOVF1 | RXOVF0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **RXOVF<15:0>:** FIFOx Receive Overflow Interrupt Pending bit
1 = FIFO has overflowed
0 = FIFO has not overflowed

**REGISTER 23-8: C1TMR: CAN TIMER REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CANTS<15:8> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CANTS<7:0> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CANTSPRE<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CANTSPRE<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **CANTS<15:0>:** CAN Time Stamp Timer bits
This is a free-running timer that increments every CANTSPRE system clocks when the CANCAP bit (C1CON<20>) is set.

bit 15-0 **CANTSPRE<15:0>:** CAN Time Stamp Timer Prescaler bits
1111 1111 1111 1111 = CAN time stamp timer (CANTS) increments every 65,535 system clocks
•
•
•
0000 0000 0000 0000 = CAN time stamp timer (CANTS) increments every system clock

**Note 1:** C1TMR will be paused when CANCAP = 0.
**2:** The C1TMR prescaler count will be reset on any write to C1TMR (CANTSPRE will be unaffected).


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**REGISTER 23-9: C1RXMn: CAN ACCEPTANCE FILTER MASK 'n' REGISTER (n = 0, 1, 2 OR 3)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SID<10:3> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| | SID<2:0> | | | — | MIDE | — | EID<17:16> | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | EID<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | EID<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-21 **SID<10:0>:** Standard Identifier bits
1 = Include the SIDx bit in filter comparison
0 = The SIDx bit is a 'don't care' in filter operation

bit 20 **Unimplemented:** Read as '0'

bit 19 **MIDE:** Identifier Receive Mode bit
1 = Match only message types (standard/extended address) that correspond to the EXID bit in filter
0 = Match either standard or extended address message if filters match (that is, if (Filter SID) = (Message SID) or if (FILTER SID/EID) = (Message SID/EID))

bit 18 **Unimplemented:** Read as '0'

bit 17-0 **EID<17:0>:** Extended Identifier bits
1 = Include the EIDx bit in filter comparison
0 = The EIDx bit is a 'don't care' in filter operation

**Note:** This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (C1CON<23:21>) = 100).

**REGISTER 23-10: C1FLTCON0: CAN FILTER CONTROL REGISTER 0**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN3 | MSEL3<1:0> | | FSEL3<4:0> | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN2 | MSEL2<1:0> | | FSEL2<4:0> | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN1 | MSEL1<1:0> | | FSEL1<4:0> | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN0 | MSEL0<1:0> | | FSEL0<4:0> | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **FLTEN3:** Filter 3 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL3<1:0>:** Filter 3 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL3<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN2:** Filter 2 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL2<1:0>:** Filter 2 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.


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**REGISTER 23-10: C1FLTCON0: CAN FILTER CONTROL REGISTER 0 (CONTINUED)**

bit 20-16 **FSEL2<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 15 **FLTEN1:** Filter 1 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL1<1:0>:** Filter 1 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL1<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN0:** Filter 0 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL0<1:0>:** Filter 0 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL0<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

**REGISTER 23-11: C1FLTCON1: CAN FILTER CONTROL REGISTER 1**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN7 | MSEL7<1:0> | | FSEL7<4:0> | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN6 | MSEL6<1:0> | | FSEL6<4:0> | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN5 | MSEL5<1:0> | | FSEL5<4:0> | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN4 | MSEL4<1:0> | | FSEL4<4:0> | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **FLTEN7:** Filter 7 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL7<1:0>:** Filter 7 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL7<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN6:** Filter 6 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL6<1:0>:** Filter 6 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.


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**REGISTER 23-11: C1FLTCON1: CAN FILTER CONTROL REGISTER 1 (CONTINUED)**

bit 20-16 **FSEL6<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 15 **FLTEN5:** Filter 17 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL5<1:0>:** Filter 5 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL5<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN4:** Filter 4 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL4<1:0>:** Filter 4 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL4<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

**REGISTER 23-12: C1FLTCON2: CAN FILTER CONTROL REGISTER 2**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN11 | MSEL11<1:0> | | FSEL11<4:0> | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN10 | MSEL10<1:0> | | FSEL10<4:0> | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN9 | MSEL9<1:0> | | FSEL9<4:0> | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN8 | MSEL8<1:0> | | FSEL8<4:0> | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **FLTEN11:** Filter 11 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL11<1:0>:** Filter 11 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL11<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN10:** Filter 10 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL10<1:0>:** Filter 10 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.


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**REGISTER 23-12: C1FLTCON2: CAN FILTER CONTROL REGISTER 2 (CONTINUED)**

bit 20-16 **FSEL10<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 15 **FLTEN9:** Filter 9 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL9<1:0>:** Filter 9 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL9<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN8:** Filter 8 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL8<1:0>:** Filter 8 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL8<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

**REGISTER 23-13: C1FLTCON3: CAN FILTER CONTROL REGISTER 3**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN15 | MSEL15<1:0> | | FSEL15<4:0> | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN14 | MSEL14<1:0> | | FSEL14<4:0> | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN13 | MSEL13<1:0> | | FSEL13<4:0> | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN12 | MSEL12<1:0> | | FSEL12<4:0> | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **FLTEN15:** Filter 15 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL15<1:0>:** Filter 15 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL15<4:0>:** FIFO Selection bits
11111 = Reserved
•
•
•
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
•
•
•
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN14:** Filter 14 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL14<1:0>:** Filter 14 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.


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**REGISTER 23-13: C1FLTCON3: CAN FILTER CONTROL REGISTER 3 (CONTINUED)**

bit 20-16 **FSEL14<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 15 **FLTEN13:** Filter 13 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL13<1:0>:** Filter 13 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL13<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN12:** Filter 12 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL12<1:0>:** Filter 12 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL12<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

**REGISTER 23-14: C1RXFn: CAN ACCEPTANCE FILTER 'n' REGISTER ('n' = 0 THROUGH 15)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | SID<10:3> | | | | | | | |
| 23:16 | R/W-x | R/W-x | R/W-x | U-0 | R/W-0 | U-0 | R/W-x | R/W-x |
| | SID<2:0> | | | — | EXID | — | EID<17:16> | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | EID<15:8> | | | | | | | |
| 7:0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | EID<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-21 **SID<10:0>:** Standard Identifier bits
1 = Message address bit SIDx must be '1' to match filter
0 = Message address bit SIDx must be '0' to match filter

bit 20 **Unimplemented:** Read as '0'

bit 19 **EXID:** Extended Identifier Enable bits
1 = Match only messages with extended identifier addresses
0 = Match only messages with standard identifier addresses

bit 18 **Unimplemented:** Read as '0'

bit 17-0 **EID<17:0>:** Extended Identifier bits
1 = Message address bit EIDx must be '1' to match filter
0 = Message address bit EIDx must be '0' to match filter

**Note:** This register can only be modified when the filter is disabled (FLTENn = 0).


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**REGISTER 23-15: C1FIFOBA: CAN MESSAGE BUFFER BASE ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | C1FIFOBA<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | C1FIFOBA<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | C1FIFOBA<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0(1) | R-0(1) |
| | C1FIFOBA<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **C1FIFOBA<31:0>:** CAN FIFO Base Address bits

These bits define the base address of all message buffers. Individual message buffers are located based on the size of the previous message buffers. This address is a physical address. Bits <1:0> are read-only and read as '0', forcing the messages to be 32-bit word-aligned in device RAM.

**Note 1:** This bit is unimplemented and will always read '0', which forces word-alignment of messages.

**Note:** This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (C1CON<23:21>) = 100).

**REGISTER 23-16: C1FIFOCONn: CAN FIFO CONTROL REGISTER 'n' ('n' = 0 THROUGH 15)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | FSIZE<4:0>(1) | | | | |
| 15:8 | U-0 | S/HC-0 | S/HC-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
| | — | FRESET | UINC | DONLY(1) | — | — | — | — |
| 7:0 | R/W-0 | R-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TXEN | TXABAT(2) | TXLARB(3) | TXERR(3) | TXREQ | RTREN | TXPR<1:0> | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-21 **Unimplemented:** Read as '0'

bit 20-16 **FSIZE<4:0>:** FIFO Size bits(1)

11111 = Reserved
.
.
.
10000 = Reserved
01111 = FIFO is 16 messages deep
.
.
.
00000 = FIFO is 1 message deep

bit 15 **Unimplemented:** Read as '0'

bit 14 **FRESET:** FIFO Reset bits

1 = FIFO will be reset when bit is set, cleared by hardware when FIFO is reset. After setting, the user should poll whether this bit is clear before taking any action.
0 = No effect

bit 13 **UINC:** Increment Head/Tail bit

TXEN = 1: (FIFO configured as a Transmit FIFO)
When this bit is set the FIFO head will increment by a single message
TXEN = 0: (FIFO configured as a Receive FIFO)
When this bit is set the FIFO tail will increment by a single message

bit 12 **DONLY:** Store Message Data Only bit(1)

TXEN = 1: (FIFO configured as a Transmit FIFO)
This bit is not used and has no effect.
TXEN = 0: (FIFO configured as a Receive FIFO)
1 = Only data bytes will be stored in the FIFO
0 = Full message is stored, including identifier

bit 11-8 **Unimplemented:** Read as '0'

**Note 1:** These bits can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> bits (C1CON<23:21>) = 100).

**2:** This bit is updated when a message completes (or aborts) or when the FIFO is reset.

**3:** This bit is reset on any read of this register or when the FIFO is reset.


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**REGISTER 23-16: C1FIFOCONn: CAN FIFO CONTROL REGISTER 'n' ('n' = 0 THROUGH 15)**

bit 7 **TXEN:** TX/RX Buffer Selection bit
1 = FIFO is a Transmit FIFO
0 = FIFO is a Receive FIFO

bit 6 **TXABAT:** Message Aborted bit(2)
1 = Message was aborted
0 = Message completed successfully

bit 5 **TXLARB:** Message Lost Arbitration bit(3)
1 = Message lost arbitration while being sent
0 = Message did not lose arbitration while being sent

bit 4 **TXERR:** Error Detected During Transmission bit(3)
1 = A bus error occured while the message was being sent
0 = A bus error did not occur while the message was being sent

bit 3 **TXREQ:** Message Send Request
TXEN = 1: (FIFO configured as a Transmit FIFO)
Setting this bit to '1' requests sending a message.
The bit will automatically clear when all the messages queued in the FIFO are successfully sent.
Clearing the bit to '0' while set ('1') will request a message abort.
TXEN = 0: (FIFO configured as a receive FIFO)
This bit has no effect.

bit 2 **RTREN:** Auto RTR Enable bit
1 = When a remote transmit is received, TXREQ will be set
0 = When a remote transmit is received, TXREQ will be unaffected

bit 1-0 **TXPR<1:0>:** Message Transmit Priority bits
11 = Highest message priority
10 = High intermediate message priority
01 = Low intermediate message priority
00 = Lowest message priority

**Note 1:** These bits can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> bits (C1CON<23:21>) = 100).
**2:** This bit is updated when a message completes (or aborts) or when the FIFO is reset.
**3:** This bit is reset on any read of this register or when the FIFO is reset.

**REGISTER 23-17: C1FIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' ('n' = 0 THROUGH 15)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | TXNFULLIE | TXHALFIE | TXEMPTYIE |
| 23:16 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | RXOVFLIE | RXFULLIE | RXHALFIE | RXNEMPTYIE |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 |
| | — | — | — | — | — | TXNFULLIF(1) | TXHALFIF | TXEMPTYIF(1) |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R-0 | R-0 | R-0 |
| | — | — | — | — | RXOVFLIF | RXFULLIF(1) | RXHALFIF(1) | RXNEMPTYIF(1) |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **TXNFULLIE:** Transmit FIFO Not Full Interrupt Enable bit
1 = Interrupt enabled for FIFO not full
0 = Interrupt disabled for FIFO not full

bit 25 **TXHALFIE:** Transmit FIFO Half Full Interrupt Enable bit
1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 24 **TXEMPTYIE:** Transmit FIFO Empty Interrupt Enable bit
1 = Interrupt enabled for FIFO empty
0 = Interrupt disabled for FIFO empty

bit 23-20 **Unimplemented:** Read as '0'

bit 19 **RXOVFLIE:** Overflow Interrupt Enable bit
1 = Interrupt enabled for overflow event
0 = Interrupt disabled for overflow event

bit 18 **RXFULLIE:** Full Interrupt Enable bit
1 = Interrupt enabled for FIFO full
0 = Interrupt disabled for FIFO full

bit 17 **RXHALFIE:** FIFO Half Full Interrupt Enable bit
1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 16 **RXNEMPTYIE:** Empty Interrupt Enable bit
1 = Interrupt enabled for FIFO not empty
0 = Interrupt disabled for FIFO not empty

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **TXNFULLIF:** Transmit FIFO Not Full Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is not full
0 = FIFO is full
TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

**Note 1:** This bit is read-only and reflects the status of the FIFO.


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**REGISTER 23-17: C1FIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' ('n' = 0 THROUGH 15)**

bit 9 **TXHALFIF:** FIFO Transmit FIFO Half Empty Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is ≤ half full
0 = FIFO is > half full
TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

bit 8 **TXEMPTYIF:** Transmit FIFO Empty Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is empty
0 = FIFO is not empty, at least 1 message queued to be transmitted
TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **RXOVFLIF:** Receive FIFO Overflow Interrupt Flag bit
TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'
TXEN = 0: (FIFO configured as a receive buffer)
1 = Overflow event has occurred
0 = No overflow event occured

bit 2 **RXFULLIF:** Receive FIFO Full Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'
TXEN = 0: (FIFO configured as a receive buffer)
1 = FIFO is full
0 = FIFO is not full

bit 1 **RXHALFIF:** Receive FIFO Half Full Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'
TXEN = 0: (FIFO configured as a receive buffer)
1 = FIFO is ≥ half full
0 = FIFO is < half full

bit 0 **RXNEMPTYIF:** Receive Buffer Not Empty Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'
TXEN = 0: (FIFO configured as a receive buffer)
1 = FIFO is not empty, has at least 1 message
0 = FIFO is empty

**Note 1:** This bit is read-only and reflects the status of the FIFO.

**REGISTER 23-18: C1FIFOUAn: CAN FIFO USER ADDRESS REGISTER 'n' ('n' = 0 THROUGH 15)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
| | C1FIFOUAn<31:24> | | | | | | | |
| 23:16 | R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
| | C1FIFOUAn<23:16> | | | | | | | |
| 15:8 | R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
| | C1FIFOUAn<15:8> | | | | | | | |
| 7:0 | R-x | R-x | R-x | R-x | R-x | R-x | R-0(1) | R-0(1) |
| | C1FIFOUAn<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **C1FIFOUAn<31:0>:** CAN FIFO User Address bits

TXEN = 1: (FIFO configured as a transmit buffer)

A read of this register will return the address where the next message is to be written (FIFO head).

TXEN = 0: (FIFO configured as a receive buffer)

A read of this register will return the address where the next message is to be read (FIFO tail).

**Note 1:** This bit will always read '0', which forces byte-alignment of messages.

**Note:** This register is not guaranteed to read correctly in Configuration mode, and should only be accessed when the module is not in Configuration mode.

**REGISTER 23-19: C1FIFOCIn: CAN MODULE MESSAGE INDEX REGISTER 'n' ('n' = 0 THROUGH 15)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | — | — | — | C1FIFOCIn<4:0> | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-5 **Unimplemented:** Read as '0'

bit 4-0 **C1FIFOCIn<4:0>:** CAN Side FIFO Message Index bits

TXEN = 1: (FIFO configured as a transmit buffer)
A read of this register will return an index to the message that the FIFO will next attempt to transmit.

TXEN = 0: (FIFO configured as a receive buffer)
A read of this register will return an index to the message that the FIFO will use to save the next message.


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## 24.0 COMPARATOR

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. "Comparator"** (DS60001110) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

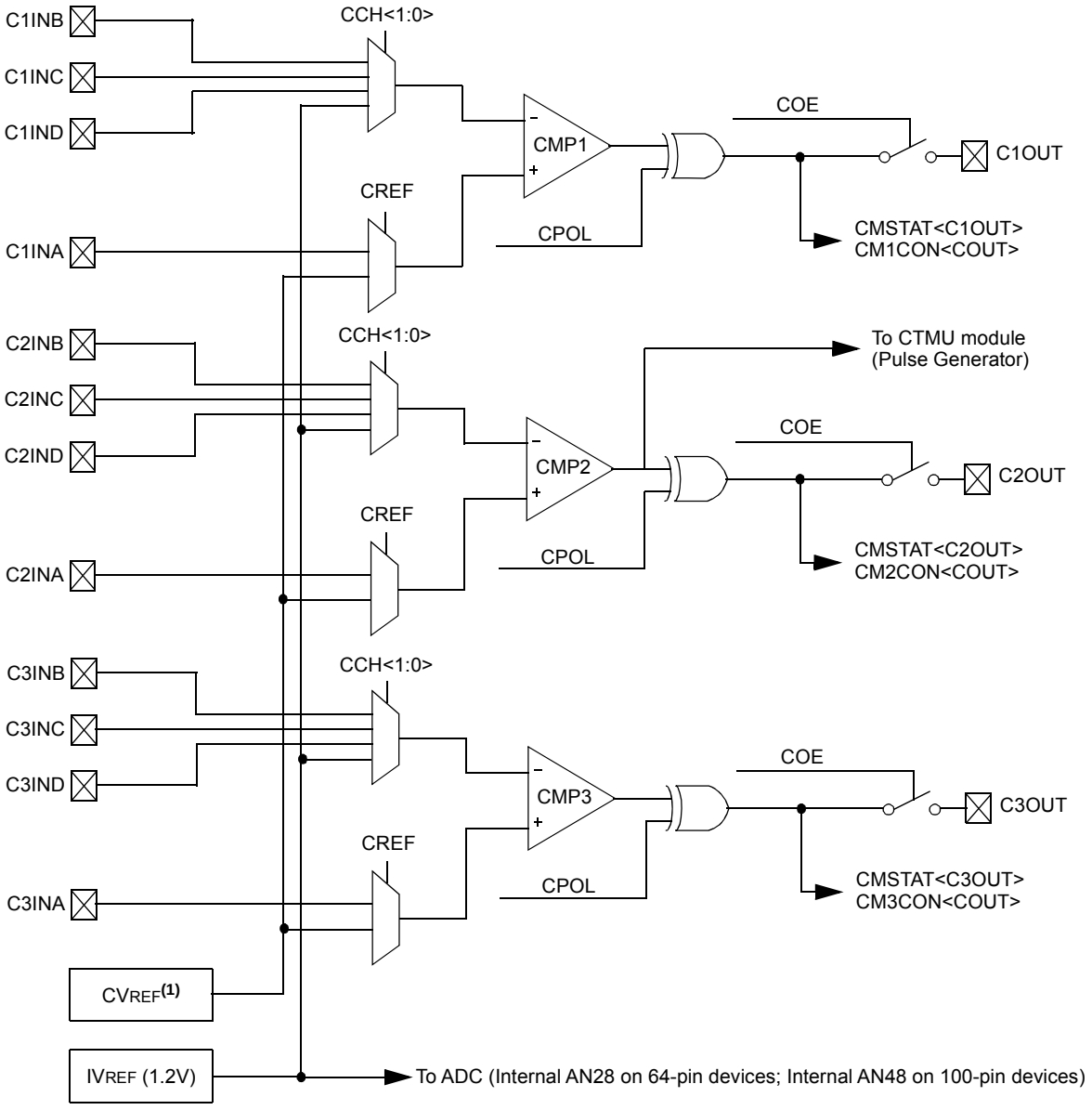
The Analog Comparator module contains three comparators that can be configured in a variety of ways.

The following are the key features of this module:

- Selectable inputs available include:
  - Analog inputs multiplexed with I/O pins
  - On-chip internal absolute voltage reference (IVREF)
  - Comparator voltage reference (CVREF)
- Outputs can be inverted
- Selectable interrupt generation

A block diagram of the comparator module is provided in Figure 24-1.

**FIGURE 24-1: COMPARATOR BLOCK DIAGRAM**




**Note 1:** Internally connected. See **Section 25.0 "Comparator Voltage Reference (CVREF)"** for more information.

## 24.1 Control Registers

**TABLE 24-1: COMPARATOR REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| A000 | CM1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | COE | CPOL | — | — | — | — | COUT | EVPOL<1:0> | | — | CREF | — | — | CCH<1:0> | | E1C3 |
| A010 | CM2CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | COE | CPOL | — | — | — | — | COUT | EVPOL<1:0> | | — | CREF | — | — | CCH<1:0> | | E1C3 |
| A020 | CM3CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | COE | CPOL | — | — | — | — | COUT | EVPOL<1:0> | | — | CREF | — | — | CCH<1:0> | | E1C3 |
| A060 | CMSTAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | SIDL | — | — | — | — | — | — | — | — | — | — | C3OUT | C2OUT | C1OUT | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.



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**REGISTER 24-1: CMxCON: COMPARATOR CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | R-0 |
| | ON(1) | COE | CPOL(2) | — | — | — | — | COUT |
| 7:0 | R/W-1 | R/W-1 | U-0 | R/W-0 | U-0 | U-0 | R/W-1 | R/W-1 |
| | EVPOL<1:0> | | — | CREF | — | — | CCH<1:0> | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator ON bit(1)
- 1 = Module is enabled. Setting this bit does not affect the other bits in this register
- 0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register

bit 14 **COE:** Comparator Output Enable bit
- 1 = Comparator output is driven on the output CxOUT pin
- 0 = Comparator output is not driven on the output CxOUT pin

bit 13 **CPOL:** Comparator Output Inversion bit(2)
- 1 = Output is inverted
- 0 = Output is not inverted

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **COUT:** Comparator Output bit
- 1 = Output of the Comparator is a '1'
- 0 = Output of the Comparator is a '0'

bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits
- 11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output
- 10 = Comparator interrupt is generated on a high-to-low transition of the comparator output
- 01 = Comparator interrupt is generated on a low-to-high transition of the comparator output
- 00 = Comparator interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Positive Input Configure bit
- 1 = Comparator non-inverting input is connected to the internal CVREF
- 0 = Comparator non-inverting input is connected to the CXINA pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Negative Input Select bits for Comparator
- 11 = Comparator inverting input is connected to the IVREF
- 10 = Comparator inverting input is connected to the CxIND pin
- 01 = Comparator inverting input is connected to the CxINC pin
- 00 = Comparator inverting input is connected to the CxINB pin

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

**REGISTER 24-2: CMSTAT: COMPARATOR STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | SIDL | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 |
| | — | — | — | — | — | C3OUT | C2OUT | C1OUT |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in IDLE Control bit
- 1 = All Comparator modules are disabled in IDLE mode
- 0 = All Comparator modules continue to operate in the IDLE mode

bit 12-3 **Unimplemented:** Read as '0'

bit 2 **C3OUT:** Comparator Output bit
- 1 = Output of Comparator 3 is a '1'
- 0 = Output of Comparator 3 is a '0'

bit 1 **C2OUT:** Comparator Output bit
- 1 = Output of Comparator 2 is a '1'
- 0 = Output of Comparator 2 is a '0'

bit 0 **C1OUT:** Comparator Output bit
- 1 = Output of Comparator 1 is a '1'
- 0 = Output of Comparator 1 is a '0'


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## 25.0 COMPARATOR VOLTAGE REFERENCE (CVREF)

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 20. "Comparator Voltage Reference (CVREF)"** (DS60001109) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

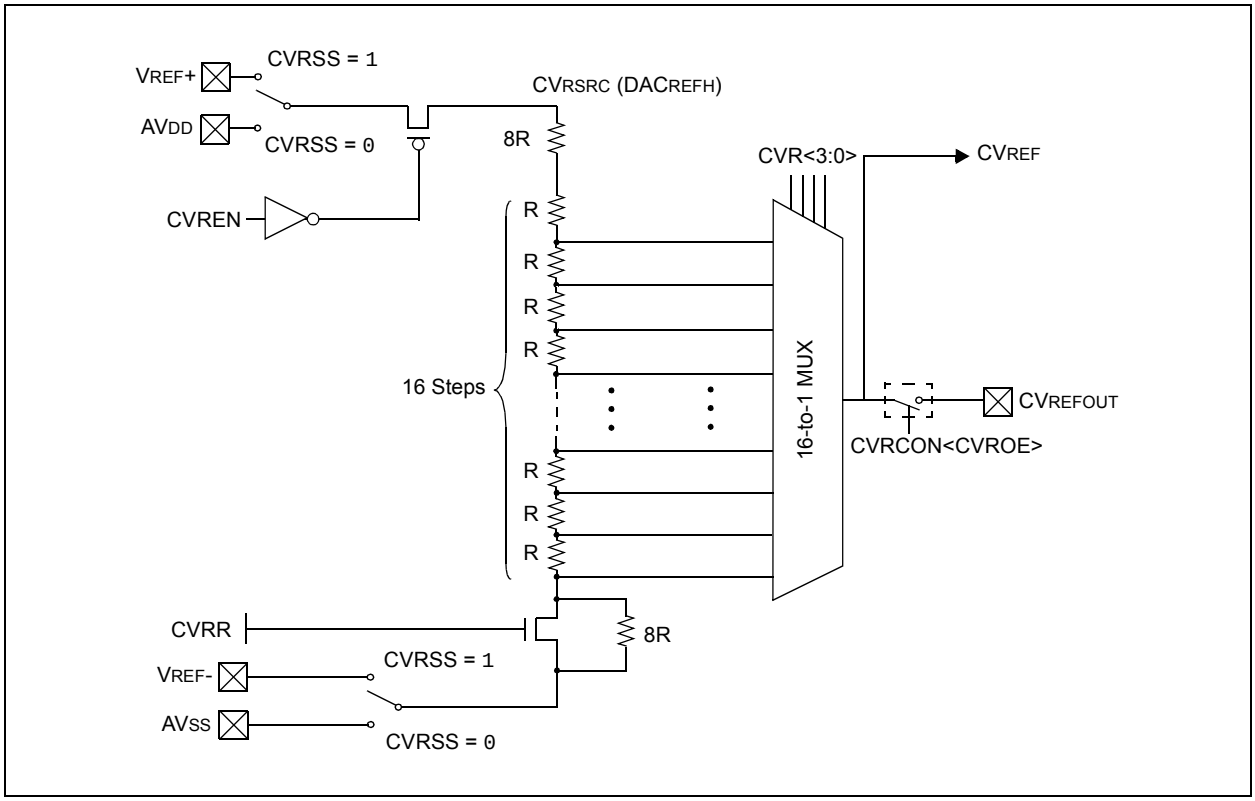
The CVREF module is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them.

A block diagram of the module is illustrated in Figure 25-1. The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDD/VSS or an external voltage reference. The CVREF output is available for the comparators and typically available for pin output.

The CVREF module has the following features:

- High and low range selection
- Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- Output can be connected to a pin

**FIGURE 25-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM**



## 25.1 Control Registers

**TABLE 25-1: COMPARATOR VOLTAGE REFERENCE REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 9800 | CVRCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | — | — | — | — | — | — | — | CVROE | CVRR | CVRSS | CVR<3:0> | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** The register in this table has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.



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**REGISTER 25-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ON(1) | — | — | — | — | — | — | — |
| 7:0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | CVROE | CVRR | CVRSS | CVR<3:0> | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator Voltage Reference On bit(1)
- 1 = Module is enabled
  Setting this bit does not affect other bits in the register.
- 0 = Module is disabled and does not consume current
  Clearing this bit does not affect the other bits in the register.

bit 14-7 **Unimplemented:** Read as '0'

bit 6 **CVROE:** $CV_{REFOUT}$ Enable bit
- 1 = Voltage level is output on $CV_{REFOUT}$ pin
- 0 = Voltage level is disconnected from $CV_{REFOUT}$ pin

bit 5 **CVRR:** $CV_{REF}$ Range Selection bit
- 1 = 0 to 0.625 $CV_{RSRC}$, with $CV_{RSRC}/24$ step size
- 0 = 0.25 $CV_{RSRC}$ to 0.719 $CV_{RSRC}$, with $CV_{RSRC}/32$ step size

bit 4 **CVRSS:** $CV_{REF}$ Source Selection bit
- 1 = Comparator voltage reference source, $CV_{RSRC} = (V_{REF+}) – (V_{REF-})$
- 0 = Comparator voltage reference source, $CV_{RSRC} = AV_{DD} – AV_{SS}$

bit 3-0 **CVR<3:0>:** $CV_{REF}$ Value Selection $0 \leq CVR<3:0> \leq 15$ bits

When CVRR = 1:
$CV_{REF} = (CVR<3:0>/24) \bullet (CV_{RSRC})$

When CVRR = 0:
$CV_{REF} = 1/4 \bullet (CV_{RSRC}) + (CVR<3:0>/32) \bullet (CV_{RSRC})$

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**NOTES:**


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## 26.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 37. "Charge Time Measurement Unit (CTMU)"** (DS60001167) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

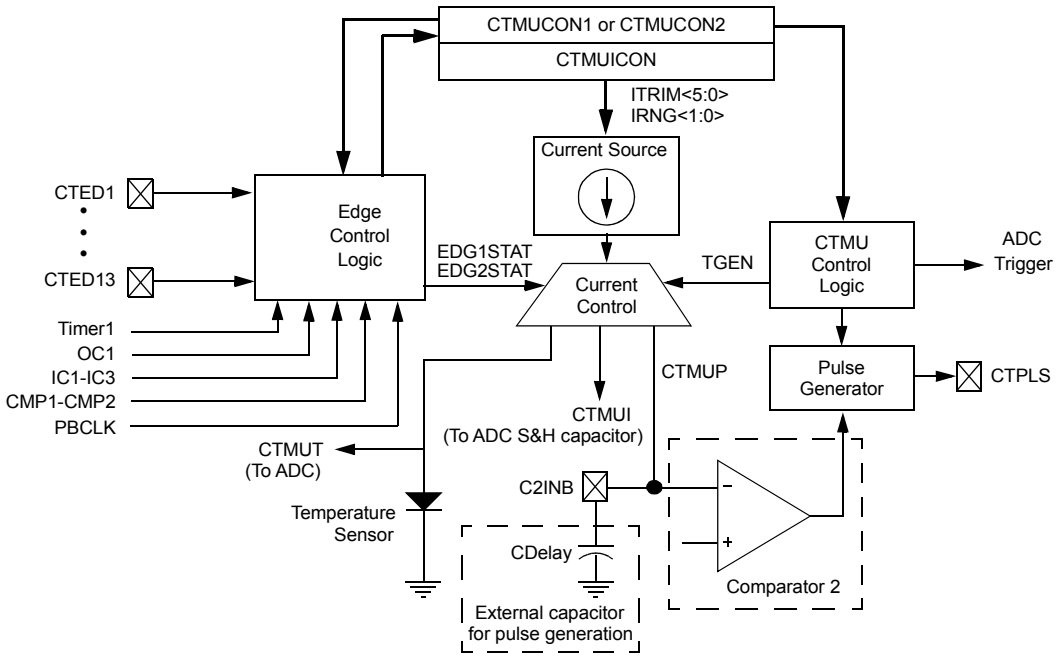
The Charge Time Measurement Unit (CTMU) is a flexible analog module that has a configurable current source with a digital configuration circuit built around it. The CTMU can be used for differential time measurement between pulse sources and can be used for generating an asynchronous pulse. By working with other on-chip analog modules, the CTMU can be used for high resolution time measurement, measure capacitance, measure relative changes in capacitance or generate output pulses with a specific time delay. The CTMU is ideal for interfacing with capacitive-based sensors.

The CTMU module includes the following key features:

- Up to 13 channels available for capacitive or time measurement input
- On-chip precision current source
- 16-edge input trigger sources
- Selection of edge or level-sensitive inputs
- Polarity control for each edge source
- Control of edge sequence
- Control of response to edges
- High precision time measurement
- Time delay of external or internal signal asynchronous to system clock
- Integrated temperature sensing diode
- Control of current source during auto-sampling
- Four current source ranges
- Time measurement resolution of one nanosecond

A block diagram of the CTMU is shown in Figure 26-1.

**FIGURE 26-1: CTMU BLOCK DIAGRAM**




| Current Control Selection | TGEN | EDG1STAT, EDG2STAT |
|---|---|---|
| CTMUT | 0 | EDG1STAT = EDG2STAT |
| CTMUI | 0 | EDG1STAT ≠ EDG2STAT |
| CTMUP | 1 | EDG1STAT ≠ EDG2STAT |
| No Connect | 1 | EDG1STAT = EDG2STAT |

## 26.1 Control Registers

**TABLE 26-1: CTMU REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| A200 | CTMUCON | 31:16 | EDG1MOD | EDG1POL | EDG1SEL<3:0> | | | | EDG2STAT | EDG1STAT | EDG2MOD | EDG2POL | EDG2SEL<3:0> | | | | — | — | 0000 |
| | | 15:0 | ON | — | CTMUSIDL | TGEN | EDGEN | EDGSEQEN | IDISSEN | CTTRIG | ITRIM<5:0> | | | | | | IRNG<1:0> | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.



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**REGISTER 26-1: CTMUCON: CTMU CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | EDG1MOD | EDG1POL | EDG1SEL<3:0> | | | | EDG2STAT | EDG1STAT |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
| | EDG2MOD | EDG2POL | EDG2SEL<3:0> | | | | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ON | — | CTMUSIDL | TGEN(1) | EDGEN | EDGSEQEN | IDISSEN(2) | CTTRIG |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ITRIM<5:0> | | | | | | IRNG<1:0> | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **EDG1MOD:** Edge 1 Edge Sampling Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 30 **EDG1POL:** Edge 1 Polarity Select bit
1 = Edge 1 programmed for a positive edge response
0 = Edge 1 programmed for a negative edge response

bit 29-26 **EDG1SEL<3:0>:** Edge 1 Source Select bits
1111 = IC4 Capture Event is selected
1110 = C2OUT pin is selected
1101 = C1OUT pin is selected
1100 = IC3 Capture Event is selected
1011 = IC2 Capture Event is selected
1010 = IC1 Capture Event is selected
1001 = CTED8 pin is selected
1000 = CTED7 pin is selected
0111 = CTED6 pin is selected
0110 = CTED5 pin is selected
0101 = CTED4 pin is selected
0100 = CTED3 pin is selected
0011 = CTED1 pin is selected
0010 = CTED2 pin is selected
0001 = OC1 Compare Event is selected
0000 = Timer1 Event is selected

bit 25 **EDG2STAT:** Edge 2 Status bit
Indicates the status of Edge 2 and can be written to control edge source
1 = Edge 2 has occurred
0 = Edge 2 has not occurred

**Note 1:** When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.

**2:** The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

**3:** Refer to the CTMU Current Source Specifications (Table 31-41) in **Section 31.0 "40 MHz Electrical Characteristics"** for current values.

**4:** This bit setting is not available for the CTMU temperature diode.

**REGISTER 26-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)**

bit 24 **EDG1STAT:** Edge 1 Status bit
Indicates the status of Edge 1 and can be written to control edge source
1 = Edge 1 has occurred
0 = Edge 1 has not occurred

bit 23 **EDG2MOD:** Edge 2 Edge Sampling Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 22 **EDG2POL:** Edge 2 Polarity Select bit
1 = Edge 2 programmed for a positive edge response
0 = Edge 2 programmed for a negative edge response

bit 21-18 **EDG2SEL<3:0>:** Edge 2 Source Select bits
1111 = IC4 Capture Event is selected
1110 = C2OUT pin is selected
1101 = C1OUT pin is selected
1100 = PBCLK clock is selected
1011 = IC3 Capture Event is selected
1010 = IC2 Capture Event is selected
1001 = IC1 Capture Event is selected
1000 = CTED13 pin is selected
0111 = CTED12 pin is selected
0110 = CTED11 pin is selected
0101 = CTED10 pin is selected
0100 = CTED9 pin is selected
0011 = CTED1 pin is selected
0010 = CTED2 pin is selected
0001 = OC1 Compare Event is selected
0000 = Timer1 Event is selected

bit 17-16 **Unimplemented:** Read as '0'

bit 15 **ON:** ON Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **CTMUSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12 **TGEN:** Time Generation Enable bit(1)
1 = Enables edge delay generation
0 = Disables edge delay generation

bit 11 **EDGEN:** Edge Enable bit
1 = Edges are not blocked
0 = Edges are blocked

**Note 1:** When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.

**2:** The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

**3:** Refer to the CTMU Current Source Specifications (Table 31-41) in **Section 31.0 "40 MHz Electrical Characteristics"** for current values.

**4:** This bit setting is not available for the CTMU temperature diode.


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**REGISTER 26-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)**

bit 10 **EDGSEQEN:** Edge Sequence Enable bit
1 = Edge 1 must occur before Edge 2 can occur
0 = No edge sequence is needed

bit 9 **IDISSEN:** Analog Current Source Control bit(2)
1 = Analog current source output is grounded
0 = Analog current source output is not grounded

bit 8 **CTTRIG:** Trigger Control bit
1 = Trigger output is enabled
0 = Trigger output is disabled

bit 7-2 **ITRIM<5:0>:** Current Source Trim bits
011111 = Maximum positive change from nominal current
011110
•
•
•
000001 = Minimum positive change from nominal current
000000 = Nominal current output specified by IRNG<1:0>
111111 = Minimum negative change from nominal current
•
•
•
100010
100001 = Maximum negative change from nominal current

bit 1-0 **IRNG<1:0>:** Current Range Select bits(3)
11 = 100 times base current
10 = 10 times base current
01 = Base current level
00 = 1000 times base current(4)

**Note 1:** When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.

**2:** The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

**3:** Refer to the CTMU Current Source Specifications (Table 31-41) in **Section 31.0 "40 MHz Electrical Characteristics"** for current values.

**4:** This bit setting is not available for the CTMU temperature diode.

**NOTES:**


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## 27.0 POWER-SAVING FEATURES

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Features"** (DS60001130) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

This section describes power-saving features for the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. These PIC32 devices offer a total of nine methods and modes, organized into two categories, that allow the user to balance power consumption with device performance. In all of the methods and modes described in this section, power-saving is controlled by software.

## 27.1 Power Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the PBCLK and by individually disabling modules. These methods are grouped into the following categories:

- FRC Run mode: the CPU is clocked from the FRC clock source with or without postscalers.
- LPRC Run mode: the CPU is clocked from the LPRC clock source.
- SOSC Run mode: the CPU is clocked from the SOSC clock source.

In addition, the Peripheral Bus Scaling mode is available where peripherals are clocked at the programmable fraction of the CPU clock (SYSCLK).

## 27.2 CPU Halted Methods

The device supports two power-saving modes, Sleep and Idle, both of which Halt the clock to the CPU. These modes operate with all clock sources, as listed below:

- POSC Idle mode: the system clock is derived from the POSC. The system clock source continues to operate. Peripherals continue to operate, but can optionally be individually disabled.
- FRC Idle mode: the system clock is derived from the FRC with or without postscalers. Peripherals continue to operate, but can optionally be individually disabled.
- SOSC Idle mode: the system clock is derived from the SOSC. Peripherals continue to operate, but can optionally be individually disabled.
- LPRC Idle mode: the system clock is derived from the LPRC. Peripherals continue to operate, but can optionally be individually disabled. This is the lowest power mode for the device with a clock running.
- Sleep mode: the CPU, the system clock source and any peripherals that operate from the system clock source are Halted. Some peripherals can operate in Sleep using specific clock sources. This is the lowest power mode for the device.

## 27.3 Power-Saving Operation

Peripherals and the CPU can be Halted or disabled to further reduce power consumption.

### 27.3.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device power-saving operating modes. The CPU and most peripherals are Halted. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep.

Sleep mode includes the following characteristics:

- The CPU is Halted.
- The system clock source is typically shutdown. See **Section 27.3.3 "Peripheral Bus Scaling Method"** for specific information.
- There can be a wake-up delay based on the oscillator selection.
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode.
- The BOR circuit remains operative during Sleep mode.
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode.
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC, Timer1 and Input Capture).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep.
- The USB module can override the disabling of the Posc or FRC. Refer to the USB section for specific details.
- Modules can be individually disabled by software prior to entering Sleep in order to further reduce consumption.

The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset
- On a WDT time-out

If the interrupt priority is lower than or equal to the current priority, the CPU will remain Halted, but the PBCLK will start running and the device will enter into Idle mode.

### 27.3.2 IDLE MODE

In Idle mode, the CPU is Halted but the System Clock (SYSCLK) source is still enabled. This allows peripherals to continue operation when the CPU is Halted. Peripherals can be individually configured to Halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

**Note 1:** Changing the PBCLK divider ratio requires recalculation of peripheral timing. For example, assume the UART is configured for 9600 baud with a PB clock ratio of 1:1 and a POSC of 8 MHz. When the PB clock divisor of 1:2 is used, the input frequency to the baud clock is cut in half; therefore, the baud rate is reduced to 1/2 its former value. Due to numeric truncation in calculations (such as the baud rate divisor), the actual baud rate may be a tiny percentage different than expected. For this reason, any timing calculation required for a peripheral should be performed with the new PB clock frequency instead of scaling the previous value based on a change in the PB divisor ratio.

**2:** Oscillator start-up and PLL lock delays are applied when switching to a clock source that was disabled and that uses a crystal and/or the PLL. For example, assume the clock source is switched from POSC to LPRC just prior to entering Sleep in order to save power. No oscillator start-up delay would be applied when exiting Idle. However, when switching back to POSC, the appropriate PLL and/or oscillator start-up/lock delays would be applied.

The device enters Idle mode when the SLPEN bit (OSCCON<4>) is clear and a `WAIT` instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than or equal to current priority of the CPU, the CPU will remain Halted and the device will remain in Idle mode.
- On any form of device Reset
- On a WDT time-out interrupt

### 27.3.3 PERIPHERAL BUS SCALING METHOD

Most of the peripherals on the device are clocked using the PBCLK. The peripheral bus can be scaled relative to the SYSCLK to minimize the dynamic power consumed by the peripherals. The PBCLK divisor is controlled by PBDIV<1:0> (OSCCON<20:19>), allowing SYSCLK to PBCLK ratios of 1:1, 1:2, 1:4 and 1:8. All peripherals using PBCLK are affected when the divisor is changed. Peripherals such as the USB, Interrupt Controller, DMA, and the bus matrix are clocked directly from SYSCLK. As a result, they are not affected by PBCLK divisor changes.

Changing the PBCLK divisor affects:

- The CPU to peripheral access latency. The CPU has to wait for next PBCLK edge for a read to complete. In 1:8 mode, this results in a latency of one to seven SYSCLKs.
- The power consumption of the peripherals. Power consumption is directly proportional to the frequency at which the peripherals are clocked. The greater the divisor, the lower the power consumed by the peripherals.

To minimize dynamic power, the PB divisor should be chosen to run the peripherals at the lowest frequency that provides acceptable system performance. When selecting a PBCLK divider, peripheral clock requirements, such as baud rate accuracy, should be taken into account. For example, the UART peripheral may not be able to achieve all baud rate values at some PBCLK divider depending on the SYSCLK value.


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## 27.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default). See Table 27-1 for more information.

| **Note:** | Disabling a peripheral module while it's ON bit is set, may result in undefined behavior. The ON bit for the associated peripheral module must be cleared prior to disable a module via the PMDx bits. |
|---|---|

**TABLE 27-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS**

| Peripheral(1) | PMDx bit Name(1) | Register Name and Bit Location |
|---|---|---|
| ADC1 | AD1MD | PMD1<0> |
| CTMU | CTMUMD | PMD1<8> |
| Comparator Voltage Reference | CVRMD | PMD1<12> |
| Comparator 1 | CMP1MD | PMD2<0> |
| Comparator 2 | CMP2MD | PMD2<1> |
| Comparator 3 | CMP3MD | PMD2<2> |
| Input Capture 1 | IC1MD | PMD3<0> |
| Input Capture 2 | IC2MD | PMD3<1> |
| Input Capture 3 | IC3MD | PMD3<2> |
| Input Capture 4 | IC4MD | PMD3<3> |
| Input Capture 5 | IC5MD | PMD3<4> |
| Output Compare 1 | OC1MD | PMD3<16> |
| Output Compare 2 | OC2MD | PMD3<17> |
| Output Compare 3 | OC3MD | PMD3<18> |
| Output Compare 4 | OC4MD | PMD3<19> |
| Output Compare 5 | OC5MD | PMD3<20> |
| Timer1 | T1MD | PMD4<0> |
| Timer2 | T2MD | PMD4<1> |
| Timer3 | T3MD | PMD4<2> |
| Timer4 | T4MD | PMD4<3> |
| Timer5 | T5MD | PMD4<4> |
| UART1 | U1MD | PMD5<0> |
| UART2 | U2MD | PMD5<1> |
| UART3 | U3MD | PMD5<2> |
| UART4 | U4MD | PMD5<3> |
| UART5 | U5MD | PMD5<4> |
| SPI1 | SPI1MD | PMD5<8> |
| SPI2 | SPI2MD | PMD5<9> |
| SPI3 | SPI3MD | PMD5<10> |
| SPI4 | SPI4MD | PMD5<11> |
| I2C1 | I2C1MD | PMD5<16> |
| I2C2 | I2C2MD | PMD5<17> |
| USB(2) | USBMD | PMD5<24> |
| CAN | CAN1MD | PMD5<28> |
| RTCC | RTCCMD | PMD6<0> |
| Reference Clock Output | REFOMD | PMD6<1> |
| PMP | PMPMD | PMD6<16> |

**Note 1:** Not all modules and associated PMDx bits are available on all devices. See **TABLE 1: "PIC32MX1XX/2XX/5XX 64/100-pin Controller Family Features"** for the list of available peripherals.

**2:** Module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

### 27.4.1 CONTROLLING CONFIGURATION CHANGES

Because peripherals can be disabled during run time, some restrictions on disabling peripherals are needed to prevent accidental configuration changes. PIC32 devices include two features to prevent alterations to enabled or disabled peripherals:

- Control register lock sequence
- Configuration bit select lock

#### 27.4.1.1 Control Register Lock

Under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the PMDLOCK Configuration bit (CFGCON<12>). Setting PMDLOCK prevents writes to the control registers; clearing PMDLOCK allows writes.

To set or clear PMDLOCK, an unlock sequence must be executed. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

#### 27.4.1.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the PMDx registers. The PMDL1WAY Configuration bit (DEVCFG3<28>) blocks the PMDLOCK bit from being cleared after it has been set once. If PMDLOCK remains set, the register unlock procedure does not execute, and the peripheral pin select control registers cannot be written to. The only way to clear the bit and re-enable PMD functionality is to perform a device Reset.


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**TABLE 27-2: PERIPHERAL MODULE DISABLE REGISTER SUMMARY**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets(1) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| F240 | PMD1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | CVRMD | — | — | — | CTMUMD | — | — | — | — | — | — | — | AD1MD | 0000 |
| F250 | PMD2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | CMP3MD | CMP2MD | CMP1MD | 0000 |
| F260 | PMD3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | OC5MD | OC4MD | OC3MD | OC2MD | OC1MD | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | IC5MD | IC4MD | IC3MD | IC2MD | IC1MD | 0000 |
| F270 | PMD4 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | T5MD | T4MD | T3MD | T2MD | T1MD | 0000 |
| F280 | PMD5 | 31:16 | — | — | — | CAN1MD | — | — | — | USBMD(1) | — | — | — | — | — | — | I2C1MD | I2C1MD | 0000 |
| | | 15:0 | — | — | — | — | SPI4MD | SPI3MD | SPI2MD | SPI1MD | — | — | — | U5MD | U4MD | U3MD | U2MD | U1MD | 0000 |
| F290 | PMD6 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | PMPMD | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | REFOMD | RTCCMD | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This bit is only available on devices with a USB module.

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**NOTES:**


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## 28.0 SPECIAL FEATURES

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. "Watchdog Timer and Power-up Timer"** (DS60001114), **Section 32. "Configuration"** (DS60001124) and **Section 33. "Programming and Diagnostics"** (DS60001129) in the *"PIC32 Family Reference Manual"*, which are available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX1XX/2XX/5XX 64/100-pin devices include several features intended to maximize application flexibility and reliability and minimize cost through elimination of external components. These are:

- Flexible device configuration
- Watchdog Timer (WDT)
- Joint Test Action Group (JTAG) interface
- In-Circuit Serial Programming™ (ICSP™)

### 28.1 Configuration Bits

The Configuration bits can be programmed using the following registers to select various device configurations.

- DEVCFG0: Device Configuration Word 0
- DEVCFG1: Device Configuration Word 1
- DEVCFG2: Device Configuration Word 2
- DEVCFG3: Device Configuration Word 3
- CFGCON: Configuration Control Register

In addition, the DEVID register (Register 28-6) provides device and revision information.

## 28.2 Registers

### TABLE 28-1: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

| Virtual Address (BFC0_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0BF0 | DEVCFG3 | 31:16 | FVBUSONIO | FUSBIDIO | IOL1WAY | PMDL1WAY | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| | | 15:0 | USERID<15:0> | | | | | | | | | | | | | | | | xxxx |
| 0BF4 | DEVCFG2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | FPLLODIV<2:0> | | | xxxx |
| | | 15:0 | UPLLEN(1) | — | — | — | — | UPLLIDIV<2:0>(1) | | | — | FPLLMUL<2:0> | | | — | FPLLIDIV<2:0> | | | xxxx |
| 0BF8 | DEVCFG1 | 31:16 | — | — | — | — | — | — | FWDTWINSZ<1:0> | | FWDTEN | WINDIS | — | WDTPS<4:0> | | | | | xxxx |
| | | 15:0 | FCKSM<1:0> | | FPBDIV<1:0> | | — | OSCIOFNC | POSCMOD<1:0> | | IESO | — | FSOSCEN | — | — | FNOSC<2:0> | | | xxxx |
| 0BFC | DEVCFG0 | 31:16 | — | — | — | CP | — | — | — | BWP | — | — | — | — | PWP<9:6> | | | | xxxx |
| | | 15:0 | PWP<5:0> | | | | — | — | — | — | — | — | — | ICESEL<1:0> | | JTAGEN | DEBUG<1:0> | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This bit is only available on devices with a USB module.

### TABLE 28-2: DEVICE AND REVISION ID SUMMARY

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets(1) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| F200 | CFGCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | IOLOCK | PMDLOCK | — | — | — | — | — | — | — | — | JTAGEN | TROEN(2) | — | TDOEN | 000B |
| F220 | DEVID | 31:16 | VER<3:0> | | | | DEVID<27:16> | | | | | | | | | | | | xxxx |
| | | 15:0 | DEVID<15:0> | | | | | | | | | | | | | | | | xxxx |
| F230 | SYSKEY(3) | 31:16 | SYSKEY<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Reset values are dependent on the device.

**2:** This bit is not available on 64-pin devices.



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**REGISTER 28-1: DEVCFG0: DEVICE CONFIGURATION WORD 0**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | r-0 | r-1 | r-1 | R/P | r-1 | r-1 | r-1 | R/P |
| | — | — | — | CP | — | — | — | BWP |
| 23:16 | r-1 | r-1 | r-1 | r-1 | R/P | R/P | R/P | R/P |
| | — | — | — | — | PWP<9:6> | | | |
| 15:8 | R/P | R/P | R/P | R/P | R/P | R/P | r-1 | r-1 |
| | PWP<5:0> | | | | | | — | — |
| 7:0 | r-1 | r-1 | r-1 | R/P | R/P | R/P | R/P | R/P |
| | — | — | — | ICESEL<1:0> | | JTAGEN(1) | DEBUG<1:0> | |

| **Legend:** | r = Reserved bit | P = Programmable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **Reserved:** Write '0'

bit 30-29 **Reserved:** Write '1'

bit 28 **CP:** Code-Protect bit

Prevents boot and program Flash memory from being read or modified by an external programming device.
1 = Protection is disabled
0 = Protection is enabled

bit 27-25 **Reserved:** Write '1'

bit 24 **BWP:** Boot Flash Write-Protect bit

Prevents boot Flash memory from being modified during code execution.
1 = Boot Flash is writable
0 = Boot Flash is not writable

bit 23-20 **Reserved:** Write '1'

**Note 1:** This bit sets the value for the JTAGEN bit in the CFGCON register.

**REGISTER 28-1: DEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)**

bit 19-10 **PWP<9:0>:** Program Flash Write-Protect bits

Prevents selected program Flash memory pages from being modified during code execution. The PWP bits represent the one's compliment of the number of write protected program Flash memory pages.

1111111111 = Disabled
1111111110 = Memory below 0x0400 address is write-protected
1111111101 = Memory below 0x0800 address is write-protected
1111111100 = Memory below 0x0C00 address is write-protected
1111111011 = Memory below 0x1000 (4K) address is write-protected
1111111010 = Memory below 0x1400 address is write-protected
1111111001 = Memory below 0x1800 address is write-protected
1111111000 = Memory below 0x1C00 address is write-protected
1111110111 = Memory below 0x2000 (8K) address is write-protected
1111110110 = Memory below 0x2400 address is write-protected
1111110101 = Memory below 0x2800 address is write-protected
1111110100 = Memory below 0x2C00 address is write-protected
1111110011 = Memory below 0x3000 address is write-protected
1111110010 = Memory below 0x3400 address is write-protected
1111110001 = Memory below 0x3800 address is write-protected
1111110000 = Memory below 0x3C00 address is write-protected
1111101111 = Memory below 0x4000 (16K) address is write-protected
.
.
.
1110111111 = Memory below 0x10000 (64K) address is write-protected
.
.
.
1101111111 = Memory below 0x20000 (128K) address is write-protected
.
.
.
1011111111 = Memory below 0x40000 (256K) address is write-protected
.
.
.
0111111111 = Memory below 0x80000 (512K) address is write-protected
.
.
.
0000000000 = All possible memory is write-protected

**Note:** These bits are effective only if Boot Flash is also protected by clearing the BWP bit (DEVCFG0<24>).

bit 9-5 **Reserved:** Write '1'

bit 4-3 **ICESEL<1:0>:** In-Circuit Emulator/Debugger Communication Channel Select bits

11 = PGEC1/PGED1 pair is used
10 = PGEC2/PGED2 pair is used
01 = PGEC3/PGED3 pair is used
00 = Reserved

bit 2 **JTAGEN:** JTAG Enable bit(1)

1 = JTAG is enabled
0 = JTAG is disabled

bit 1-0 **DEBUG<1:0>:** Background Debugger Enable bits (forced to '11' if code-protect is enabled)

1x = Debugger is disabled
0x = Debugger is enabled

**Note 1:** This bit sets the value for the JTAGEN bit in the CFGCON register.


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**REGISTER 28-2: DEVCFG1: DEVICE CONFIGURATION WORD 1**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | R/P | R/P |
| | — | — | — | — | — | — | FWDTWINSZ<1:0> | |
| 23:16 | R/P | R/P | r-1 | R/P | R/P | R/P | R/P | R/P |
| | FWDTEN | WINDIS | — | WDTPS<4:0> | | | | |
| 15:8 | R/P | R/P | R/P | R/P | r-1 | R/P | R/P | R/P |
| | FCKSM<1:0> | | FPBDIV<1:0> | | — | OSCIOFNC | POSCMOD<1:0> | |
| 7:0 | R/P | r-1 | R/P | r-1 | r-1 | R/P | R/P | R/P |
| | IESO | — | FSOSCEN | — | — | FNOSC<2:0> | | |

| **Legend:** | r = Reserved bit | P = Programmable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-26 **Reserved:** Write '1'

bit 25-24 **FWDTWINSZ:** Watchdog Timer Window Size bits
11 = Window size is 25%
10 = Window size is 37.5%
01 = Window size is 50%
00 = Window size is 75%

bit 23 **FWDTEN:** Watchdog Timer Enable bit
1 = Watchdog Timer is enabled and cannot be disabled by software
0 = Watchdog Timer is not enabled; it can be enabled in software

bit 22 **WINDIS:** Watchdog Timer Window Enable bit
1 = Watchdog Timer is in non-Window mode
0 = Watchdog Timer is in Window mode

bit 21 **Reserved:** Write '1'

bit 20-16 **WDTPS<4:0>:** Watchdog Timer Postscale Select bits
10100 = 1:1048576
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1
All other combinations not shown result in operation = 10100

**Note 1:** Do not disable the POSC (POSCMOD = 11) when using this oscillator source.

**REGISTER 28-2: DEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)**

bit 15-14 **FCKSM<1:0>:** Clock Switching and Monitor Selection Configuration bits
- 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
- 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
- 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

bit 13-12 **FPBDIV<1:0>:** Peripheral Bus Clock Divisor Default Value bits
- 11 = PBCLK is SYSCLK divided by 8
- 10 = PBCLK is SYSCLK divided by 4
- 01 = PBCLK is SYSCLK divided by 2
- 00 = PBCLK is SYSCLK divided by 1

bit 11 **Reserved:** Write '1'

bit 10 **OSCIOFNC:** CLKO Enable Configuration bit
- 1 = CLKO output disabled
- 0 = CLKO output signal active on the OSCO pin; Primary Oscillator must be disabled or configured for the External Clock mode (EC) for the CLKO to be active (POSCMOD<1:0> = 11 or 00)

bit 9-8 **POSCMOD<1:0>:** Primary Oscillator Configuration bits
- 11 = Primary Oscillator disabled
- 10 = HS Oscillator mode selected
- 01 = XT Oscillator mode selected
- 00 = External Clock mode selected

bit 7 **IESO:** Internal External Switchover bit
- 1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)
- 0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)

bit 6 **Reserved:** Write '1'

bit 5 **FSOSCEN:** Secondary Oscillator Enable bit
- 1 = Enable Secondary Oscillator
- 0 = Disable Secondary Oscillator

bit 4-3 **Reserved:** Write '1'

bit 2-0 **FNOSC<2:0>:** Oscillator Selection bits
- 111 = Fast RC Oscillator with divide-by-N (FRCDIV)
- 110 = FRCDIV16 Fast RC Oscillator with fixed divide-by-16 postscaler
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator (POSC) with PLL module (XT+PLL, HS+PLL, EC+PLL)
- 010 = Primary Oscillator (XT, HS, EC)(1)
- 001 = Fast RC Oscillator with divide-by-N with PLL module (FRCDIV+PLL)
- 000 = Fast RC Oscillator (FRC)

**Note 1:** Do not disable the POSC (POSCMOD = 11) when using this oscillator source.


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**REGISTER 28-3: DEVCFG2: DEVICE CONFIGURATION WORD 2**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | — | — | — | — | — | — | — | — |
| 23:16 | r-1 | r-1 | r-1 | r-1 | r-1 | R/P | R/P | R/P |
| | — | — | — | — | — | FPLLODIV<2:0> | | |
| 15:8 | R/P | r-1 | r-1 | r-1 | r-1 | R/P | R/P | R/P |
| | UPLLEN(1) | — | — | — | — | UPLLIDIV<2:0>(1) | | |
| 7:0 | r-1 | R/P-1 | R/P | R/P-1 | r-1 | R/P | R/P | R/P |
| | — | FPLLMUL<2:0> | | | — | FPLLIDIV<2:0> | | |

| Legend: | r = Reserved bit | P = Programmable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-19 **Reserved:** Write '1'

bit 18-16 **FPLLODIV<2:0>:** Default PLL Output Divisor bits
- 111 = PLL output divided by 256
- 110 = PLL output divided by 64
- 101 = PLL output divided by 32
- 100 = PLL output divided by 16
- 011 = PLL output divided by 8
- 010 = PLL output divided by 4
- 001 = PLL output divided by 2
- 000 = PLL output divided by 1

bit 15 **UPLLEN:** USB PLL Enable bit(1)
- 1 = Disable and bypass USB PLL
- 0 = Enable USB PLL

bit 14-11 **Reserved:** Write '1'

bit 10-8 **UPLLIDIV<2:0>:** USB PLL Input Divider bits(1)
- 111 = 12x divider
- 110 = 10x divider
- 101 = 6x divider
- 100 = 5x divider
- 011 = 4x divider
- 010 = 3x divider
- 010 = 3x divider
- 001 = 2x divider
- 000 = 1x divider

bit 7 **Reserved:** Write '1'

bit 6-4 **FPLLMUL<2:0>:** PLL Multiplier bits
- 111 = 24x multiplier
- 110 = 21x multiplier
- 101 = 20x multiplier
- 100 = 19x multiplier
- 011 = 18x multiplier
- 010 = 17x multiplier
- 001 = 16x multiplier
- 000 = 15x multiplier

bit 3 **Reserved:** Write '1'

**Note 1:** This bit is available on PIC32MX2XX/5XX devices only.

**REGISTER 28-3: DEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)**

bit 2-0 **FPLLIDIV<2:0>:** PLL Input Divider bits

111 = 12x divider
110 = 10x divider
101 = 6x divider
100 = 5x divider
011 = 4x divider
010 = 3x divider
001 = 2x divider
000 = 1x divider

**Note 1:** This bit is available on PIC32MX2XX/5XX devices only.


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**REGISTER 28-4: DEVCFG3: DEVICE CONFIGURATION WORD 3**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/P | R/P | R/P | R/P | U-0 | U-0 | U-0 | U-0 |
| | FVBUSONIO | FUSBIDIO | IOL1WAY | PMDL1WAY | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/P | R/P | R/P | R/P | R/P | R/P | R/P | R/P |
| | USERID<15:8> | | | | | | | |
| 7:0 | R/P | R/P | R/P | R/P | R/P | R/P | R/P | R/P |
| | USERID<7:0> | | | | | | | |

| **Legend:** | r = Reserved bit | P = Programmable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **FVBUSONIO:** USB VBUS_ON Selection bit
1 = VBUSON pin is controlled by the USB module
0 = VBUSON pin is controlled by the port function

bit 30 **FUSBIDIO:** USB USBID Selection bit
1 = USBID pin is controlled by the USB module
0 = USBID pin is controlled by the port function

bit 29 **IOL1WAY:** Peripheral Pin Select Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 28 **PMDL1WAY:** Peripheral Module Disable Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 27-16 **Unimplemented:** Read as '0'

bit 15-0 **USERID<15:0>:** This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG

**REGISTER 28-5: CFGCON: CONFIGURATION CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | IOLOCK(1) | PMDLOCK(1) | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-1 |
| | — | — | — | — | JTAGEN | — | — | TDOEN |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-14 **Unimplemented:** Read as '0'

bit 13 **IOLOCK:** Peripheral Pin Select Lock bit(1)
- 1 = Peripheral Pin Select is locked. Writes to PPS registers is not allowed
- 0 = Peripheral Pin Select is not locked. Writes to PPS registers is allowed

bit 12 **PMDLOCK:** Peripheral Module Disable bit(1)
- 1 = Peripheral module is locked. Writes to PMD registers is not allowed
- 0 = Peripheral module is not locked. Writes to PMD registers is allowed

bit 11-4 **Unimplemented:** Read as '0'

bit 3 **JTAGEN:** JTAG Port Enable bit
- 1 = Enable the JTAG port
- 0 = Disable the JTAG port

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **TDOEN:** TDO Enable for 2-Wire JTAG
- 1 = 2-wire JTAG protocol uses TDO
- 0 = 2-wire JTAG protocol does not use TDO

**Note 1:** To change this bit, the unlock sequence must be performed. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.


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**REGISTER 28-6: DEVID: DEVICE AND REVISION ID REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R | R | R | R | R | R | R | R |
| | VER<3:0>(1) | | | | DEVID<27:24>(1) | | | |
| 23:16 | R | R | R | R | R | R | R | R |
| | DEVID<23:16>(1) | | | | | | | |
| 15:8 | R | R | R | R | R | R | R | R |
| | DEVID<15:8>(1) | | | | | | | |
| 7:0 | R | R | R | R | R | R | R | R |
| | DEVID<7:0>(1) | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-28 **VER<3:0>:** Revision Identifier bits(1)

bit 27-0 **DEVID<27:0>:** Device ID(1)

**Note 1:** See the *"PIC32 Flash Programming Specification"* (DS60001145) for a list of Revision and Device ID values.

## 28.3 On-Chip Voltage Regulator

All PIC32MX1XX/2XX/5XX 64/100-pin devices' core and digital logic are designed to operate at a nominal 1.8V. To simplify system designs, most devices in the PIC32MX1XX/2XX/5XX 64/100-pin family incorporate an on-chip regulator providing the required core logic voltage from VDD.

A low-ESR capacitor (such as tantalum) must be connected to the VCAP pin (see Figure 28-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in **Section 31.1 "DC Characteristics"**.

| | |
|---|---|
| **Note:** | It is important that the low-ESR capacitor is placed as close as possible to the VCAP pin. |

### 28.3.1 HIGH VOLTAGE DETECT (HVD)

The HVD module monitors the core voltage at the VCAP pin. If a voltage above the required level is detected on VCAP, the I/O pins are disabled and the device is held in Reset as long as the HVD condition persists. See parameter HV10 (VHVD) in Table 31-11 in **Section 31.1 "DC Characteristics"** for more information.

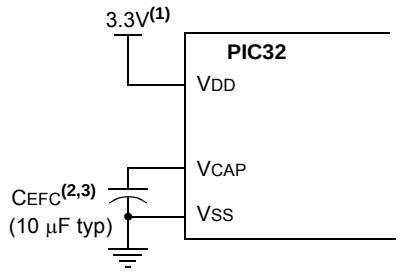
### 28.3.2 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

### 28.3.3 ON-CHIP REGULATOR AND BOR

PIC32MX1XX/2XX/5XX 64/100-pin devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in **Section 31.1 "DC Characteristics"**.

**FIGURE 28-1: CONNECTIONS FOR THE ON-CHIP REGULATOR**




**Note 1:** These are typical operating voltages. Refer to **Section 31.1 "DC Characteristics"** for the full operating ranges of VDD.
**2:** It is important that the low-ESR capacitor is placed as close as possible to the VCAP pin.
**3:** The typical voltage on the VCAP pin is 1.8V.

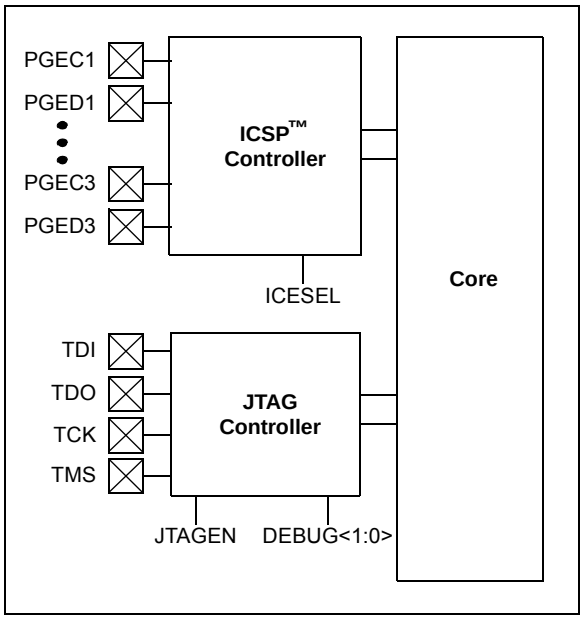
## 28.4 Programming and Diagnostics

PIC32MX1XX/2XX/5XX 64/100-pin devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming™ (ICSP™) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32 devices incorporate two programming and diagnostic modules that provide a range of functions to the application developer.

**FIGURE 28-2: BLOCK DIAGRAM OF PROGRAMMING, DEBUGGING AND TRACE PORTS**





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## 29.0 INSTRUCTION SET

The PIC32MX1XX/2XX/5XX 64/100-pin family instruction set complies with the MIPS32® Release 2 instruction set architecture. The PIC32 device family does not support the following features:

- Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

**Note:** Refer to *"MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set"* at www.imgtec.com for more information.

**NOTES:**


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## 30.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

### 30.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

## 30.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

## 30.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

## 30.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

## 30.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility


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## 30.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

## 30.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

## 30.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

## 30.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

## 30.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at $V_{DDMIN}$ and $V_{DDMAX}$ for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

## 30.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

## 30.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®


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## 31.0 40 MHz ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MX1XX/2XX/5XX 64/100-pin Family electrical characteristics for devices that operate at 40 MHz. Refer to **Section 32.0 "50 MHz Electrical Characteristics"** for additional specifications for operations at higher frequency. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MX1XX/2XX/5XX 64/100-pin Family devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

### Absolute Maximum Ratings

**(See Note 1)**

| | |
|---|---|
| Ambient temperature under bias | -40°C to +105°C |
| Storage temperature | -65°C to +150°C |
| Voltage on $V_{DD}$ with respect to $V_{SS}$ | -0.3V to +4.0V |
| Voltage on any pin that is not 5V tolerant, with respect to $V_{SS}$ **(Note 3)** | -0.3V to ($V_{DD}$ + 0.3V) |
| Voltage on any 5V tolerant pin with respect to $V_{SS}$ when $V_{DD} \geq 2.3V$ **(Note 3)** | -0.3V to +5.5V |
| Voltage on any 5V tolerant pin with respect to $V_{SS}$ when $V_{DD} < 2.3V$ **(Note 3)** | -0.3V to +3.6V |
| Voltage on D+ or D- pin with respect to $V_{USB3V3}$ | -0.3V to ($V_{USB3V3}$ + 0.3V) |
| Voltage on $V_{BUS}$ with respect to $V_{SS}$ | -0.3V to +5.5V |
| Maximum current out of $V_{SS}$ pin(s) | 300 mA |
| Maximum current into $V_{DD}$ pin(s) **(Note 2)** | 300 mA |
| Maximum output current sunk by any I/O pin | 15 mA |
| Maximum output current sourced by any I/O pin | 15 mA |
| Maximum current sunk by all ports | 200 mA |
| Maximum current sourced by all ports **(Note 2)** | 200 mA |

**Note 1:** Stresses above those listed under **"Absolute Maximum Ratings"** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**2:** Maximum allowable current is a function of device maximum power dissipation (see Table 31-2).

**3:** See the **"Device Pin Tables"** section for the 5V tolerant pins.

## 31.1 DC Characteristics

**TABLE 31-1: OPERATING MIPS VS. VOLTAGE**

| Characteristic | VDD Range (in Volts)(1) | Temp. Range (in °C) | Max. Frequency |
|---|---|---|---|
| | | | PIC32MX1XX/2XX/5XX 64/100-pin Family |
| DC5 | VBOR-3.6V | -40°C to +105°C | 40 MHz |

**Note 1:** Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 31-10 for BOR values.

**TABLE 31-2: THERMAL OPERATING CONDITIONS**

| Rating | Symbol | Min. | Typical | Max. | Unit |
|---|---|---|---|---|---|
| **Industrial Temperature Devices** | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +125 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +85 | °C |
| **V-temp Temperature Devices** | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +140 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +105 | °C |
| Power Dissipation:<br>Internal Chip Power Dissipation:<br>PINT = VDD x (IDD – S IOH)<br>I/O Pin Power Dissipation:<br>I/O = S (({VDD – VOH} x IOH) + S (VOL x IOL)) | PD | PINT + PI/O | | | W |
| Maximum Allowed Power Dissipation | PDMAX | (TJ – TA)/θJA | | | W |

**TABLE 31-3: THERMAL PACKAGING CHARACTERISTICS**

| Characteristics | Symbol | Typical | Max. | Unit | Notes |
|---|---|---|---|---|---|
| Package Thermal Resistance, 64-pin QFN | θJA | 28 | — | °C/W | **1** |
| Package Thermal Resistance, 64-pin TQFP, 10 mm x 10 mm | θJA | 55 | — | °C/W | **1** |
| Package Thermal Resistance, 100-pin TQFP, 12 mm x 12 mm | θJA | 52 | — | °C/W | **1** |
| Package Thermal Resistance, 100-pin TQFP, 14 mm x 14 mm | θJA | 50 | — | °C/W | **1** |

**Note 1:** Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.


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**TABLE 31-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **Operating Voltage** | | | | | | | |
| DC10 | VDD | **Supply Voltage (Note 2)** | 2.3 | — | 3.6 | V | — |
| DC12 | VDR | **RAM Data Retention Voltage (Note 1)** | 1.75 | — | — | V | — |
| DC16 | VPOR | **VDD Start Voltage** to Ensure Internal Power-on Reset Signal | 1.75 | — | 2.1 | V | — |
| DC17 | SVDD | **VDD Rise Rate** to Ensure Internal Power-on Reset Signal | 0.00005 | — | 0.115 | V/μs | — |

**Note 1:** This is the limit to which VDD can be lowered without losing RAM data.

**2:** Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 31-10 for BOR values.

**TABLE 31-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | |
|---|---|---|---|---|---|
| **Parameter No.** | **Typical(3)** | **Max.** | **Units** | **Conditions** | |
| **Operating Current (IDD) (Notes 1, 2, 5)** | | | | | |
| DC20 | 2 | 8 | mA | 4 MHz **(Note 4)** | |
| DC21 | 7 | 13 | mA | 10 MHz | |
| DC22 | 10 | 18 | mA | 20 MHz **(Note 4)** | |
| DC23 | 15 | 25 | mA | 30 MHz **(Note 4)** | |
| DC24 | 20 | 32 | mA | 40 MHz | |
| DC25 | 180 | 250 | µA | +25ºC, 3.3V | LPRC (31 kHz) **(Note 4)** |

**Note 1:** A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

**2:** The test conditions for IDD measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU, Program Flash, and SRAM data memory are operational, SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- CPU executing `while(1)` statement from Flash
- RTCC and JTAG are disabled

**3:** Data in the "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

**4:** This parameter is characterized, but not tested in manufacturing.

**5:** IPD electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.


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**TABLE 31-6: DC CHARACTERISTICS: IDLE CURRENT ($I_{IDLE}$)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | |
|---|---|---|---|---|---|---|
| **Parameter No.** | **Typical(2)** | **Max.** | **Units** | **Conditions** | | |
| **Idle Current ($I_{IDLE}$): Core Off, Clock on Base Current (Notes 1, 4)** | | | | | | |
| DC30a | 1.5 | 5 | mA | 4 MHz **(Note 3)** | | |
| DC31a | 3 | 8 | mA | 10 MHz | | |
| DC32a | 5 | 12 | mA | 20 MHz **(Note 3)** | | |
| DC33a | 6.5 | 15 | mA | 30 MHz **(Note 3)** | | |
| DC34a | 8 | 20 | mA | 40 MHz | | |
| DC37a | 75 | 100 | µA | -40°C | 3.3V | LPRC (31 kHz) **(Note 3)** |
| DC37b | 180 | 250 | µA | +25°C | | |
| DC37c | 280 | 380 | µA | +85°C | | |

**Note 1:** The test conditions for $I_{IDLE}$ current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Idle mode (CPU core Halted), and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to $V_{SS}$
- $\overline{MCLR}$ = $V_{DD}$
- RTCC and JTAG are disabled

**2:** Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** This parameter is characterized, but not tested in manufacturing.

**4:** $I_{IDLE}$ electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.

**TABLE 31-7: DC CHARACTERISTICS: POWER-DOWN CURRENT ($I_{PD}$)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | |
|---|---|---|---|---|---|
| **Param. No.** | **Typical(2)** | **Max.** | **Units** | **Conditions** | |
| **Power-Down Current ($I_{PD}$) (Notes 1, 5)** | | | | | |
| DC40k | 33 | 78 | μA | -40°C | Base Power-Down Current |
| DC40l | 49 | 78 | μA | +25°C | |
| DC40n | 281 | 450 | μA | +85°C | |
| DC40m | 559 | 895 | μA | +105ºC | |
| **Module Differential Current** | | | | | |
| DC41e | 10 | 25 | μA | 3.6V | Watchdog Timer Current: $\Delta I_{WDT}$ **(Note 3)** |
| DC42e | 29 | 50 | μA | 3.6V | RTCC + Timer1 w/32 kHz Crystal: $\Delta I_{RTCC}$ **(Note 3)** |
| DC43d | 1000 | 1300 | μA | 3.6V | ADC: $\Delta I_{ADC}$ **(Notes 3,4)** |

**Note 1:** The test conditions for $I_{PD}$ current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Sleep mode, and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is set
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to $V_{SS}$
- $\overline{MCLR}$ = $V_{DD}$
- RTCC and JTAG are disabled

**2:** Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base $I_{PD}$ current.

**4:** Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.

**5:** $I_{PD}$ electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.


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**TABLE 31-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| | VIL | **Input Low Voltage** | | | | | |
| DI10 | | I/O Pins with PMP | VSS | — | 0.15 VDD | V | |
| | | I/O Pins | VSS | — | 0.2 VDD | V | |
| DI18 | | SDAx, SCLx | VSS | — | 0.3 VDD | V | SMBus disabled **(Note 4)** |
| DI19 | | SDAx, SCLx | VSS | — | 0.8 | V | SMBus enabled **(Note 4)** |
| | VIH | **Input High Voltage** | | | | | |
| DI20 | | I/O Pins not 5V-tolerant(5) | 0.65 VDD | — | VDD | V | **(Note 4,6)** |
| | | I/O Pins 5V-tolerant with PMP(5) | 0.25 VDD + 0.8V | — | 5.5 | V | **(Note 4,6)** |
| | | I/O Pins 5V-tolerant(5) | 0.65 VDD | — | 5.5 | V | |
| DI28 | | SDAx, SCLx | 0.65 VDD | — | 5.5 | V | SMBus disabled **(Note 4,6)** |
| DI29 | | SDAx, SCLx | 2.1 | — | 5.5 | V | SMBus enabled, 2.3V ≤ VPIN ≤ 5.5 **(Note 4,6)** |
| DI30 | ICNPU | **Change Notification Pull-up Current** | — | -200 | -50 | µA | VDD = 3.3V, VPIN = VSS **(Note 3,6)** |
| DI31 | ICNPD | **Change Notification Pull-down Current(4)** | 50 | 200 | — | µA | VDD = 3.3V, VPIN = VDD |
| | IIL | **Input Leakage Current (Note 3)** | | | | | |
| DI50 | | I/O Ports | — | — | ±1 | µA | VSS ≤ VPIN ≤ VDD, Pin at high-impedance |
| DI51 | | Analog Input Pins | — | — | ±1 | µA | VSS ≤ VPIN ≤ VDD, Pin at high-impedance |
| DI55 | | $\overline{\text{MCLR}}$(2) | — | — | ±1 | µA | VSS ≤ VPIN ≤ VDD |
| DI56 | | OSC1 | — | — | ±1 | µA | VSS ≤ VPIN ≤ VDD, XT and HS modes |

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Negative current is defined as current sourced by the pin.

**4:** This parameter is characterized, but not tested in manufacturing.

**5:** See the **"Device Pin Tables"** section for the 5V-tolerant pins.

**6:** The VIH specifications are only in relation to externally applied inputs, and not with respect to the user-selectable internal pull-ups. External open drain input signals utilizing the internal pull-ups of the PIC32 device are guaranteed to be recognized only as a logic "high" internally to the PIC32 device, provided that the external load does not exceed the minimum value of ICNPU. For External "input" logic inputs that require a pull-up source, to guarantee the minimum VIH of those components, it is recommended to use an external pull-up resistor rather than the internal pull-ups of the PIC32 device.

**TABLE 31-9: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| DO10 | VOL | **Output Low Voltage**<br>I/O Pins:<br>4x Sink Driver Pins - All I/O output pins not defined as 8x Sink Driver pins | — | — | 0.4 | V | IOL ≤ 9 mA, VDD = 3.3V |
| | | **Output Low Voltage**<br>I/O Pins:<br>8x Sink Driver Pins - RB14, RC15, RD2, RD10, RD15, RF6, RF13, RG6 | — | — | 0.4 | V | IOL ≤ 15 mA, VDD = 3.3V |
| DO20 | VOH | **Output High Voltage**<br>I/O Pins:<br>4x Source Driver Pins - All I/O output pins not defined as 8x Source Driver pins | 2.4 | — | — | V | IOH ≥ -10 mA, VDD = 3.3V |
| | | **Output High Voltage**<br>I/O Pins:<br>8x Source Driver Pins - RB14, RC15, RD2, RD10, RD15, RF6, RF13, RG6 | 2.4 | — | — | V | IOH ≥ -15 mA, VDD = 3.3V |
| DO20A | VOH1 | **Output High Voltage**<br>I/O Pins:<br>4x Source Driver Pins - All I/O output pins not defined as 8x Sink Driver pins | 1.5(1) | — | — | V | IOH ≥ -14 mA, VDD = 3.3V |
| | | | 2.0(1) | — | — | | IOH ≥ -12 mA, VDD = 3.3V |
| | | | 3.0(1) | — | — | | IOH ≥ -7 mA, VDD = 3.3V |
| | | **Output High Voltage**<br>I/O Pins:<br>8x Source Driver Pins - RB14, RC15, RD2, RD10, RD15, RF6, RF13, RG6 | 1.5(1) | — | — | V | IOH ≥ -22 mA, VDD = 3.3V |
| | | | 2.0(1) | — | — | | IOH ≥ -18 mA, VDD = 3.3V |
| | | | 3.0(1) | — | — | | IOH ≥ -10 mA, VDD = 3.3V |

**Note 1:** Parameters are characterized, but not tested.


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**TABLE 31-10: ELECTRICAL CHARACTERISTICS: BOR**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.(1)** | **Typical** | **Max.** | **Units** | **Conditions** |
| BO10 | VBOR | BOR Event on VDD transition high-to-low(2) | 2.0 | — | 2.3 | V | — |

**Note 1:** Parameters are for design guidance only and are not tested in manufacturing.

**2:** Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN.

**TABLE 31-11: ELECTRICAL CHARACTERISTICS: HVD**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.(1)** | **Symbol** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| HV10 | VHVD | High Voltage Detect on VCAP pin | — | 2.5 | — | V | — |

**Note 1:** Parameters are for design guidance only and are not tested in manufacturing.

**TABLE 31-12: DC CHARACTERISTICS: PROGRAM MEMORY**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| | | **Program Flash Memory(3)** | | | | | |
| D130 | EP | Cell Endurance | 20,000 | — | — | E/W | — |
| D131 | VPR | VDD for Read | 2.3 | — | 3.6 | V | — |
| D132 | VPEW | VDD for Erase or Write | 2.3 | — | 3.6 | V | — |
| D134 | TRETD | Characteristic Retention | 20 | — | — | Year | Provided no other specifications are violated |
| D135 | IDDP | Supply Current during Programming | — | 10 | — | mA | — |
| | TWW | Word Write Cycle Time | — | 411 | — | FRC Cycles | See **Note 4** |
| D136 | TRW | Row Write Cycle Time | — | 6675 | — | FRC Cycles | See **Note 2,4** |
| D137 | TPE | Page Erase Cycle Time | — | 20011 | — | FRC Cycles | See **Note 4** |
| | TCE | Chip Erase Cycle Time | — | 80180 | — | FRC Cycles | See **Note 4** |

**Note 1:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated.

**2:** The minimum SYSCLK for row programming is 4 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

**3:** Refer to the *“PIC32 Flash Programming Specification”* (DS60001145) for operating conditions during programming and erase cycles.

**4:** This parameter depends on FRC accuracy (See Table 31-19) and FRC tuning values (See Register 8-2).


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**TABLE 31-13: COMPARATOR SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions (see Note 4): 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typ.** | **Max.** | **Units** | **Comments** |
| D300 | VIOFF | Input Offset Voltage | — | ±7.5 | ±25 | mV | AVDD = VDD,<br>AVSS = VSS |
| D301 | VICM(2) | Input Common Mode Voltage | 0 | — | VDD | V | AVDD = VDD,<br>AVSS = VSS |
| D302 | CMRR(2) | Common Mode Rejection Ratio | 55 | — | — | dB | Max VICM = (VDD - 1)V |
| D303 | TRESP(1,2) | Response Time | — | 150 | 400 | ns | AVDD = VDD,<br>AVSS = VSS |
| D304 | ON2OV(2) | Comparator Enabled to Output Valid | — | — | 10 | μs | Comparator module is configured before setting the comparator ON bit |
| D305 | IVREF | Internal Voltage Reference | 1.14 | 1.2 | 1.26 | V | — |

**Note 1:** Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

**2:** These parameters are characterized but not tested.

**3:** Settling time measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but not tested in manufacturing.

**4:** The Comparator module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

**TABLE 31-14: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typ.** | **Max.** | **Units** | **Comments** |
| D312 | TSET | Internal 4-bit DAC Comparator Reference Settling time. | — | — | 10 | µs | See **Note 1** |
| D313 | DACREFH | CVREF Input Voltage Reference Range | AVSS | — | AVDD | V | CVRSRC with CVRSS = 0 |
| | | | VREF- | — | VREF+ | V | CVRSRC with CVRSS = 1 |
| D314 | DVREF | CVREF Programmable Output Range | 0 | — | 0.625 x DACREFH | V | 0 to 0.625 DACREFH with DACREFH/24 step size |
| | | | 0.25 x DACREFH | — | 0.719 x DACREFH | V | 0.25 x DACREFH to 0.719 DACREFH with DACREFH/32 step size |
| D315 | DACRES | Resolution | — | — | DACREFH/24 | | CVRCON<CVRR> = 1 |
| | | | — | — | DACREFH/32 | | CVRCON<CVRR> = 0 |
| D316 | DACACC | Absolute Accuracy(2) | — | — | 1/4 | LSB | DACREFH/24, CVRCON<CVRR> = 1 |
| | | | — | — | 1/2 | LSB | DACREFH/32, CVRCON<CVRR> = 0 |

**Note 1:** Settling time was measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but is not tested in manufacturing.

**2:** These parameters are characterized but not tested.

**TABLE 31-15: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Comments** |
| D321 | CEFC | External Filter Capacitor Value | 8 | 10 | — | µF | Capacitor must be low series resistance (≤ 3 ohm). Typical voltage on the VCAP pin is 1.8V. |


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## 31.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX1XX/2XX/5XX 64/100-pin AC characteristics and timing parameters.

**FIGURE 31-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS**

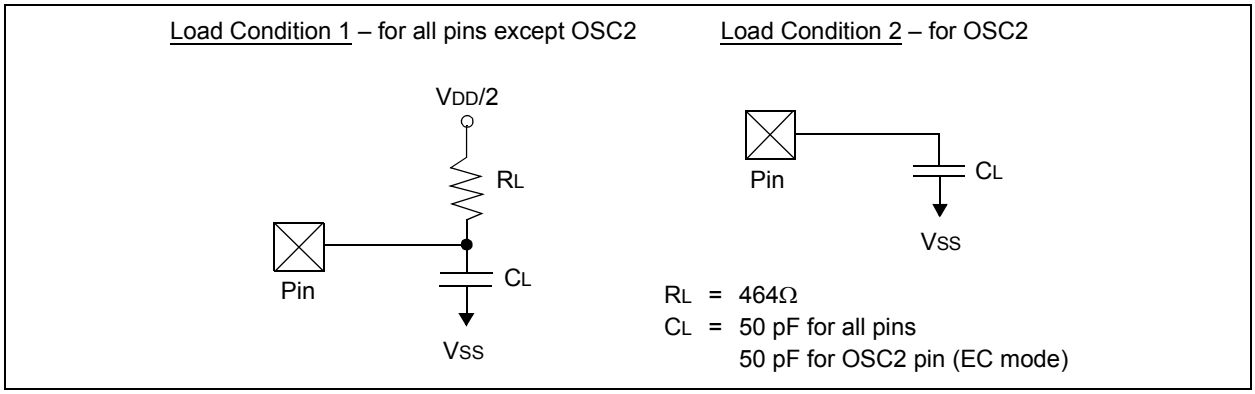


**TABLE 31-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| DO50 | COSCO | OSC2 pin | — | — | 15 | pF | In XT and HS modes when an external crystal is used to drive OSC1 |
| DO50a | CSOSC | SOSCI/SOSCO pins | — | 33 | — | pF | Epson P/N: MC-306 32.7680K-A0:ROHS |
| DO56 | CIO | All I/O pins and OSC2 | — | — | 50 | pF | EC mode |
| DO58 | CB | SCLx, SDAx | — | — | 400 | pF | In $I^2C$ mode |

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**FIGURE 31-2: EXTERNAL CLOCK TIMING**

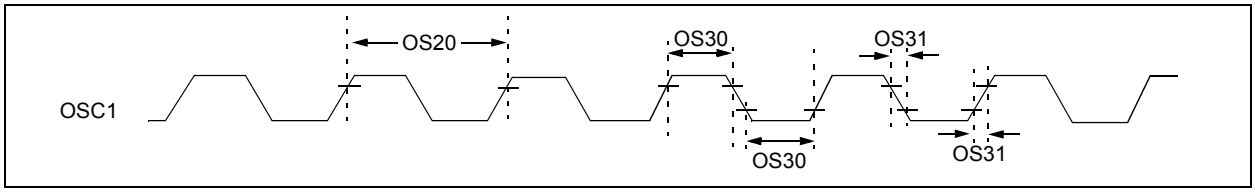

**TABLE 31-17: EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| OS10 | FOSC | External CLKI Frequency (External clocks allowed only in EC and ECPLL modes) | DC<br>4 | —<br>— | 40<br>40 | MHz<br>MHz | EC **(Note 4)**<br>ECPLL **(Note 3)** |
| OS11 | | Oscillator Crystal Frequency | 3 | — | 10 | MHz | XT **(Note 4)** |
| OS12 | | | 4 | — | 10 | MHz | XTPLL **(Notes 3,4)** |
| OS13 | | | 10 | — | 25 | MHz | HS **(Note 5)** |
| OS14 | | | 10 | — | 25 | MHz | HSPLL **(Notes 3,4)** |
| OS15 | | | 32 | 32.768 | 100 | kHz | SOSC **(Note 4)** |
| OS20 | TOSC | TOSC = 1/FOSC = TCY **(Note 2)** | — | — | — | — | See parameter OS10 for FOSC value |
| OS30 | TOSL, TOSH | External Clock In (OSC1) High or Low Time | 0.45 x TOSC | — | — | ns | EC **(Note 4)** |
| OS31 | TOSR, TOSF | External Clock In (OSC1) Rise or Fall Time | — | — | 0.05 x TOSC | ns | EC **(Note 4)** |
| OS40 | TOST | Oscillator Start-up Timer Period (Only applies to HS, HSPLL, XT, XTPLL and SOSC Clock Oscillator modes) | — | 1024 | — | TOSC | **(Note 4)** |
| OS41 | TFSCM | Primary Clock Fail Safe Time-out Period | — | 2 | — | ms | **(Note 4)** |
| OS42 | GM | External Oscillator Transconductance (Primary Oscillator only) | — | 12 | — | mA/V | VDD = 3.3V, TA = +25°C **(Note 4)** |

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are characterized but are not tested.

**2:** Instruction cycle period (TCY) equals the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin.

**3:** PLL input requirements: 4 MHz ≤ FPLLIN ≤ 5 MHz (use PLL prescaler to reduce FOSC). This parameter is characterized, but tested at 10 MHz only at manufacturing.

**4:** This parameter is characterized, but not tested in manufacturing.


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**TABLE 31-18: PLL CLOCK TIMING SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| OS50 | FPLLI | PLL Voltage Controlled Oscillator (VCO) Input Frequency Range | 3.92 | — | 5 | MHz | ECPLL, HSPLL, XTPLL, FRCPLL modes |
| OS51 | FSYS | On-Chip VCO System Frequency | 60 | — | 120 | MHz | — |
| OS52 | TLOCK | PLL Start-up Time (Lock Time) | — | — | 2 | ms | — |
| OS53 | DCLK | CLKO Stability(2) (Period Jitter or Cumulative) | -0.25 | — | +0.25 | % | Measured over 100 ms period |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter \quad \frac{D_{CLK}}{\sqrt{\frac{SYSCLK}{CommunicationClock}}}$$

For example, if SYSCLK = 40 MHz and SPI bit rate = 20 MHz, the effective jitter is as follows:

$$EffectiveJitter \quad \frac{D_{CLK}}{\sqrt{\frac{40}{20}}} \quad \frac{D_{CLK}}{1.41}$$

**TABLE 31-19: INTERNAL FRC ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| **Internal FRC Accuracy @ 8.00 MHz(1)** | | | | | | |
| F20a | FRC | -0.9 | — | +0.9 | % | -40°C ≤ TA ≤ +85°C |
| F20b | FRC | -2 | — | +2 | % | -40°C ≤ TA ≤ +105°C |

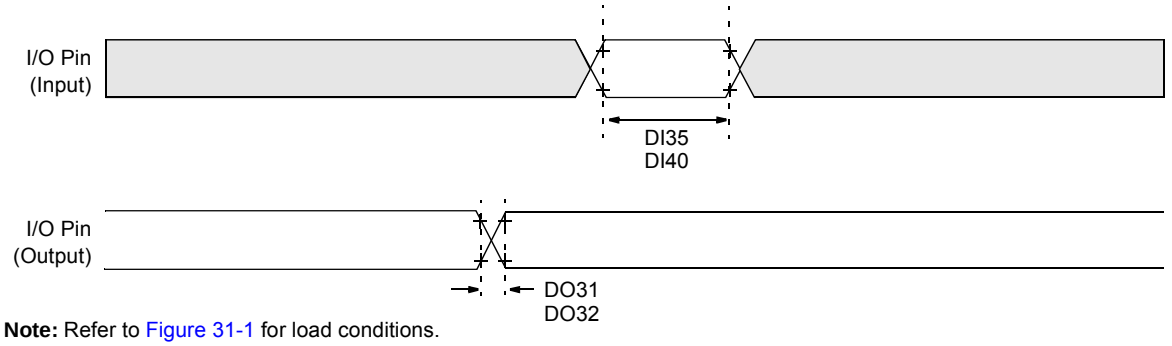
**Note 1:** Frequency calibrated at 25°C and 3.3V. The TUN bits can be used to compensate for temperature drift.

**TABLE 31-20: INTERNAL LPRC ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| **LPRC @ 31.25 kHz(1)** | | | | | | |
| F21 | LPRC | -15 | — | +15 | % | — |

**Note 1:** Change of LPRC frequency as VDD changes.

**FIGURE 31-3: I/O TIMING CHARACTERISTICS**




**Note:** Refer to Figure 31-1 for load conditions.

**TABLE 31-21: I/O TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(2)** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| DO31 | TIOR | Port Output Rise Time | — | 5 | 15 | ns | VDD < 2.5V |
| | | | — | 5 | 10 | ns | VDD > 2.5V |
| DO32 | TIOF | Port Output Fall Time | — | 5 | 15 | ns | VDD < 2.5V |
| | | | — | 5 | 10 | ns | VDD > 2.5V |
| DI35 | TINP | INTx Pin High or Low Time | 10 | — | — | ns | — |
| DI40 | TRBP | CNx High or Low Time (input) | 2 | — | — | TSYSCLK | — |

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

**2:** This parameter is characterized, but not tested in manufacturing.


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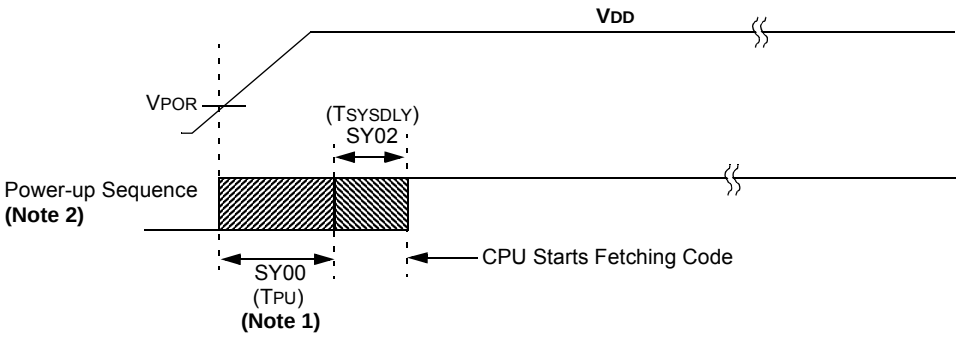
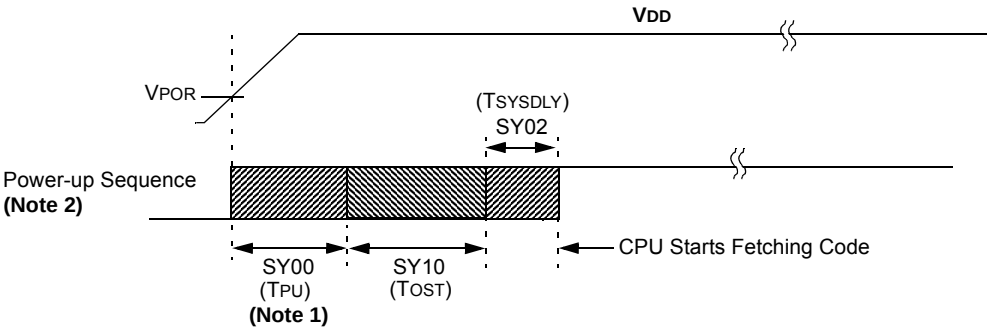
**FIGURE 31-4: POWER-ON RESET TIMING CHARACTERISTICS**

**Internal Voltage Regulator Enabled**
**Clock Sources = (FRC, FRCDIV, FRCDIV16, FRCPLL, EC, ECPLL and LPRC)**




**Internal Voltage Regulator Enabled**
**Clock Sources = (HS, HSPLL, XT, XTPLL and SOSC)**




**Note 1:** The power-up period will be extended if the power-up sequence completes before the device exits from BOR ($V_{DD} < V_{DDMIN}$).

**2:** Includes interval voltage regulator stabilization delay.

**FIGURE 31-5: EXTERNAL RESET TIMING CHARACTERISTICS**

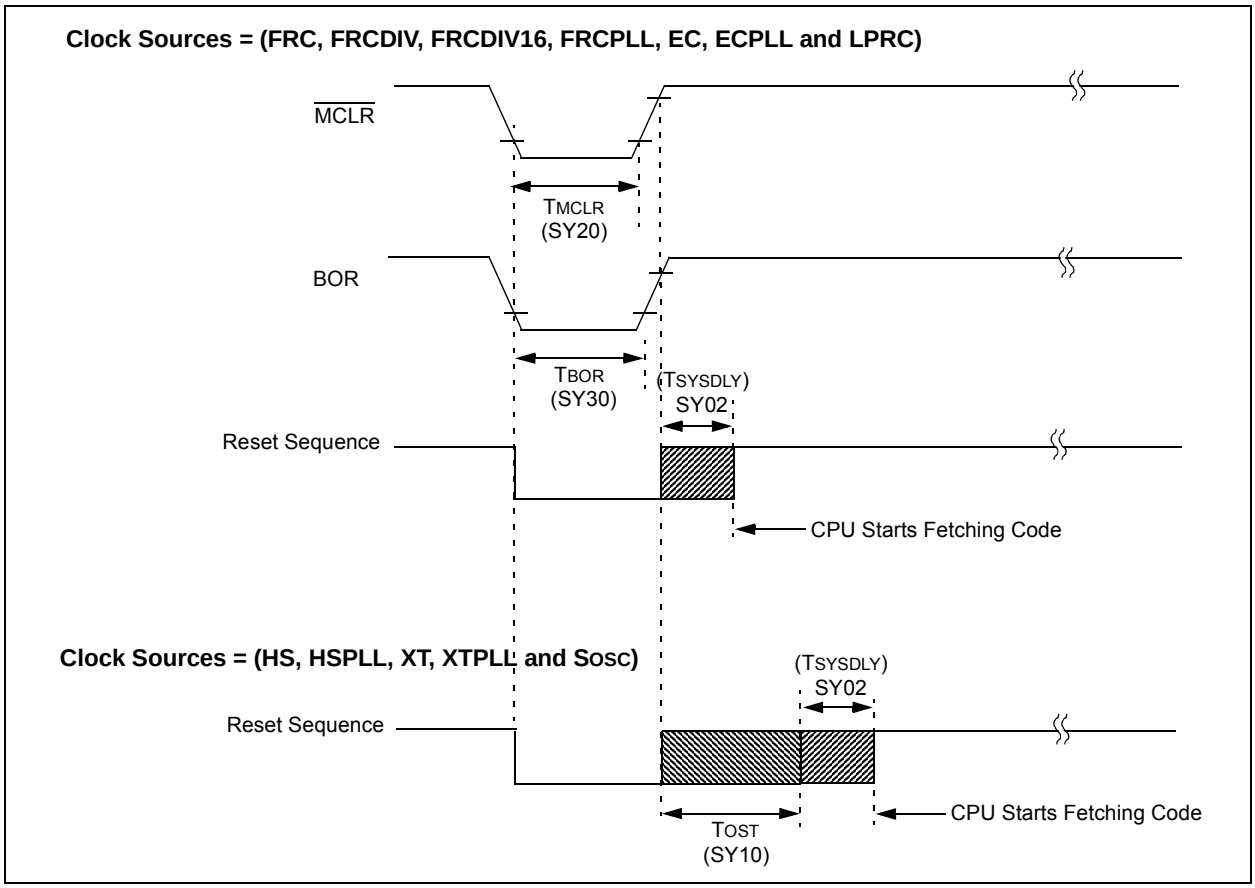



**TABLE 31-22: RESETS TIMING**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| SY00 | TPU | Power-up Period<br>Internal Voltage Regulator Enabled | — | 400 | 600 | μs | — |
| SY02 | TSYSDLY | System Delay Period:<br>Time Required to Reload Device Configuration Fuses plus SYSCLK Delay before First instruction is Fetched. | — | 1 μs + 8 SYSCLK cycles | — | — | — |
| SY20 | TMCLR | $\overline{\text{MCLR}}$ Pulse Width (low) | 2 | — | — | μs | — |
| SY30 | TBOR | BOR Pulse Width (low) | — | 1 | — | μs | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Characterized by design but not tested.


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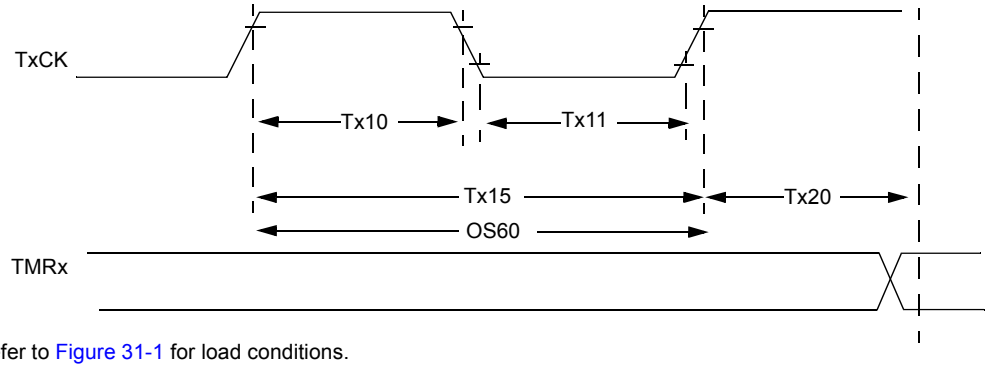
**FIGURE 31-6: TIMER1, 2, 3, 4, 5 EXTERNAL CLOCK TIMING CHARACTERISTICS**




**Note:** Refer to Figure 31-1 for load conditions.

**TABLE 31-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS**

| **AC CHARACTERISTICS(1)** | | | | **Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(2)** | | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| TA10 | TTXH | TxCK High Time | Synchronous, with prescaler | [(12.5 ns or 1 TPB)/N] + 25 ns | — | — | ns | Must also meet parameter TA15 |
| | | | Asynchronous, with prescaler | 10 | — | — | ns | — |
| TA11 | TTXL | TxCK Low Time | Synchronous, with prescaler | [(12.5 ns or 1 TPB)/N] + 25 ns | — | — | ns | Must also meet parameter TA15 |
| | | | Asynchronous, with prescaler | 10 | — | — | ns | — |
| TA15 | TTXP | TxCK Input Period | Synchronous, with prescaler | [(Greater of 25 ns or 2 TPB)/N] + 30 ns | — | — | ns | VDD > 2.7V |
| | | | | [(Greater of 25 ns or 2 TPB)/N] + 50 ns | — | — | ns | VDD < 2.7V |
| | | | Asynchronous, with prescaler | 20 | — | — | ns | VDD > 2.7V **(Note 3)** |
| | | | | 50 | — | — | ns | VDD < 2.7V **(Note 3)** |
| OS60 | FT1 | SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting the TCS (T1CON<1>) bit) | | 32 | — | 100 | kHz | — |
| TA20 | TCKEXTMRL | Delay from External TxCK Clock Edge to Timer Increment | | — | | 1 | TPB | — |

**Note 1:** Timer1 is a Type A timer.

**2:** This parameter is characterized, but not tested in manufacturing.

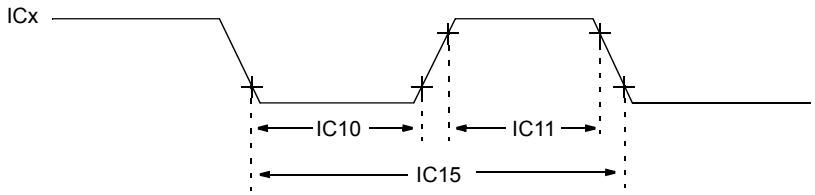
**3:** N = Prescale Value (1, 8, 64, 256).

**TABLE 31-24: TIMER2, 3, 4, 5 EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | | **Min.** | **Max.** | **Units** | **Conditions** | |
| TB10 | TTXH | TxCK High Time | Synchronous, with prescaler | [(12.5 ns or 1 TPB)/N] + 25 ns | — | ns | Must also meet parameter TB15 | N = prescale value (1, 2, 4, 8, 16, 32, 64, 256) |
| TB11 | TTXL | TxCK Low Time | Synchronous, with prescaler | [(12.5 ns or 1 TPB)/N] + 25 ns | — | ns | Must also meet parameter TB15 | |
| TB15 | TTXP | TxCK Input Period | Synchronous, with prescaler | [(Greater of [(25 ns or 2 TPB)/N] + 30 ns | — | ns | VDD > 2.7V | |
| | | | | [(Greater of [(25 ns or 2 TPB)/N] + 50 ns | — | ns | VDD < 2.7V | |
| TB20 | TCKEXTMRL | Delay from External TxCK Clock Edge to Timer Increment | | — | 1 | TPB | — | |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**FIGURE 31-7: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 31-1 for load conditions.

**TABLE 31-25: INPUT CAPTURE MODULE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Max.** | **Units** | **Conditions** | |
| IC10 | TCCL | ICx Input Low Time | [(12.5 ns or 1 TPB)/N] + 25 ns | — | ns | Must also meet parameter IC15. | N = prescale value (1, 4, 16) |
| IC11 | TCCH | ICx Input High Time | [(12.5 ns or 1 TPB)/N] + 25 ns | — | ns | Must also meet parameter IC15. | |
| IC15 | TCCP | ICx Input Period | [(25 ns or 2 TPB)/N] + 50 ns | — | ns | — | |

**Note 1:** These parameters are characterized, but not tested in manufacturing.


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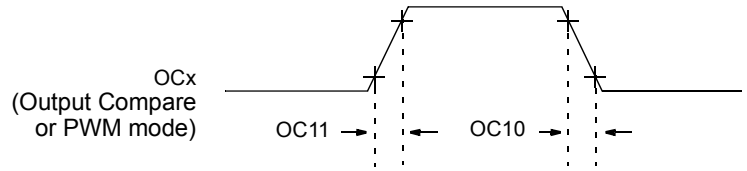
**FIGURE 31-8: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 31-1 for load conditions.

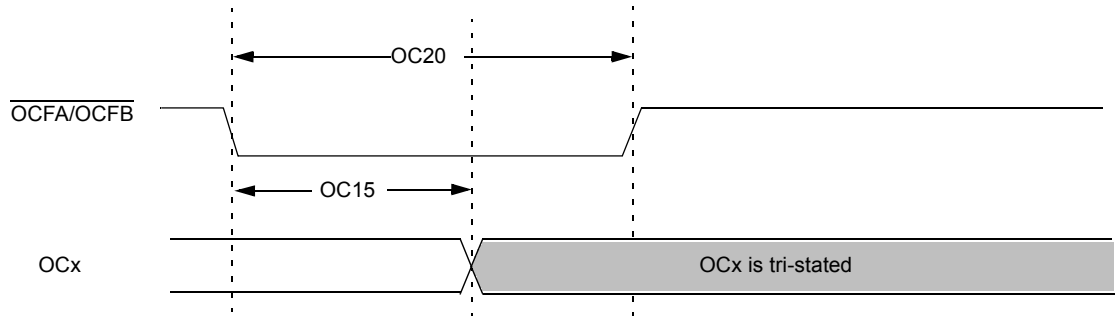
**TABLE 31-26: OUTPUT COMPARE MODULE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| OC10 | TccF | OCx Output Fall Time | — | — | — | ns | See parameter DO32 |
| OC11 | TccR | OCx Output Rise Time | — | — | — | ns | See parameter DO31 |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**FIGURE 31-9: OCx/PWM MODULE TIMING CHARACTERISTICS**




**Note:** Refer to Figure 31-1 for load conditions.

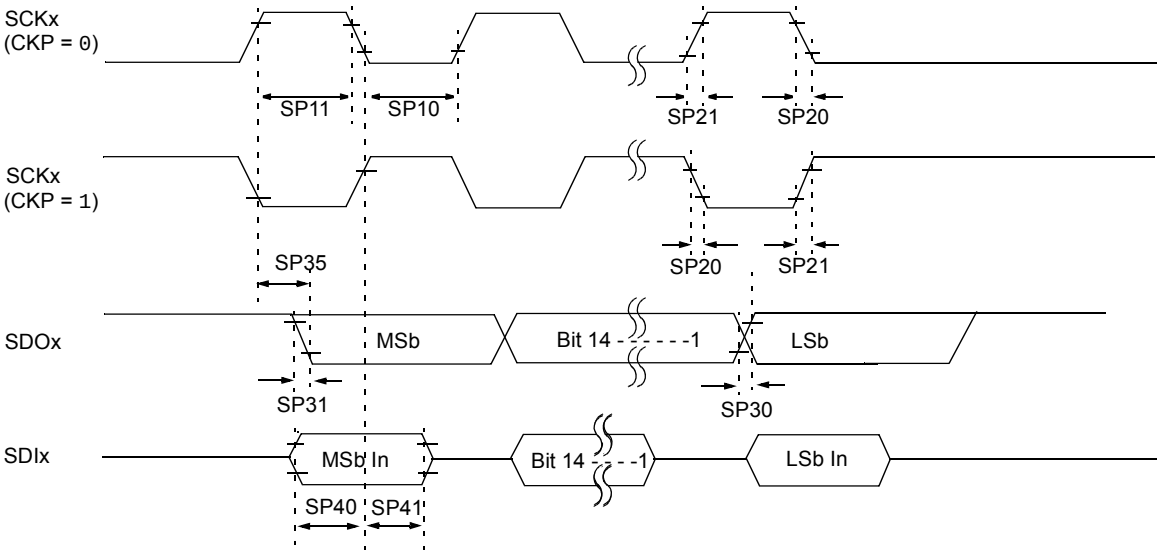
**TABLE 31-27: SIMPLE OCx/PWM MODE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristics(1)** | **Min** | **Typical(2)** | **Max** | **Units** | **Conditions** |
| OC15 | TFD | Fault Input to PWM I/O Change | — | — | 50 | ns | — |
| OC20 | TFLT | Fault Input Pulse Width | 50 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**FIGURE 31-10: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 31-1 for load conditions.

**TABLE 31-28: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | TscL | SCKx Output Low Time **(Note 3)** | Tsck/2 | — | — | ns | — |
| SP11 | TscH | SCKx Output High Time **(Note 3)** | Tsck/2 | — | — | ns | — |
| SP20 | TscF | SCKx Output Fall Time **(Note 4)** | — | — | — | ns | See parameter DO32 |
| SP21 | TscR | SCKx Output Rise Time **(Note 4)** | — | — | — | ns | See parameter DO31 |
| SP30 | TdoF | SDOx Data Output Fall Time **(Note 4)** | — | — | — | ns | See parameter DO32 |
| SP31 | TdoR | SDOx Data Output Rise Time **(Note 4)** | — | — | — | ns | See parameter DO31 |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 15 | ns | VDD > 2.7V |
| | | | — | — | 20 | ns | VDD < 2.7V |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 50 ns. Therefore, the clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.


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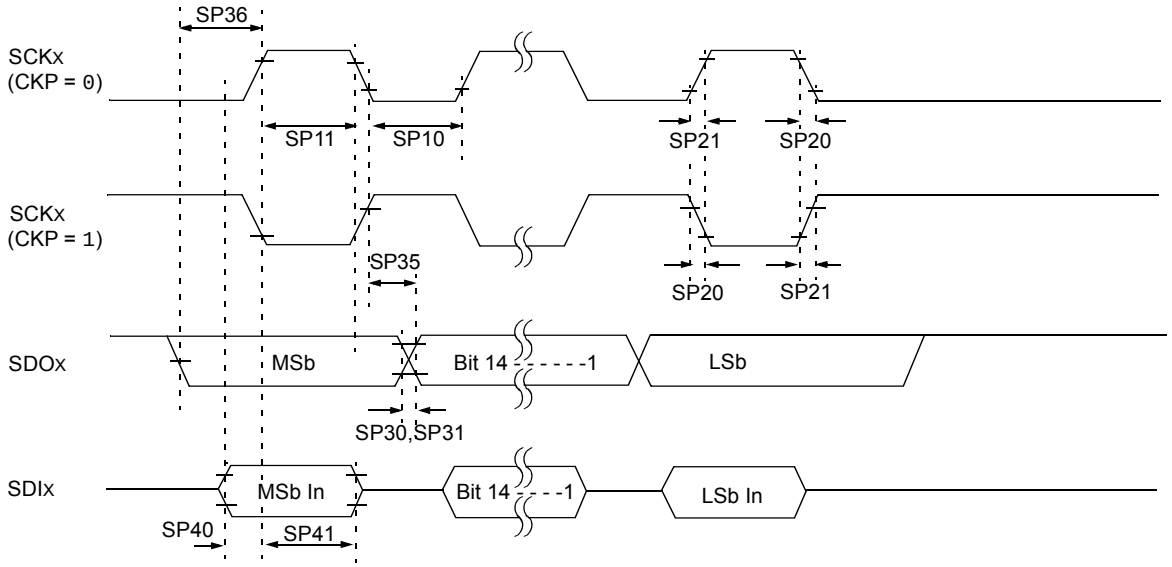
**FIGURE 31-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 31-1 for load conditions.

**TABLE 31-29: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | TscL | SCKx Output Low Time **(Note 3)** | Tsck/2 | — | — | ns | — |
| SP11 | TscH | SCKx Output High Time **(Note 3)** | Tsck/2 | — | — | ns | — |
| SP20 | TscF | SCKx Output Fall Time **(Note 4)** | — | — | — | ns | See parameter DO32 |
| SP21 | TscR | SCKx Output Rise Time **(Note 4)** | — | — | — | ns | See parameter DO31 |
| SP30 | TdoF | SDOx Data Output Fall Time **(Note 4)** | — | — | — | ns | See parameter DO32 |
| SP31 | TdoR | SDOx Data Output Rise Time **(Note 4)** | — | — | — | ns | See parameter DO31 |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 15 | ns | VDD > 2.7V |
| | | | — | — | 20 | ns | VDD < 2.7V |
| SP36 | TdoV2sc, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 15 | — | — | ns | — |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 15 | — | — | ns | VDD > 2.7V |
| | | | 20 | — | — | ns | VDD < 2.7V |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 15 | — | — | ns | VDD > 2.7V |
| | | | 20 | — | — | ns | VDD < 2.7V |

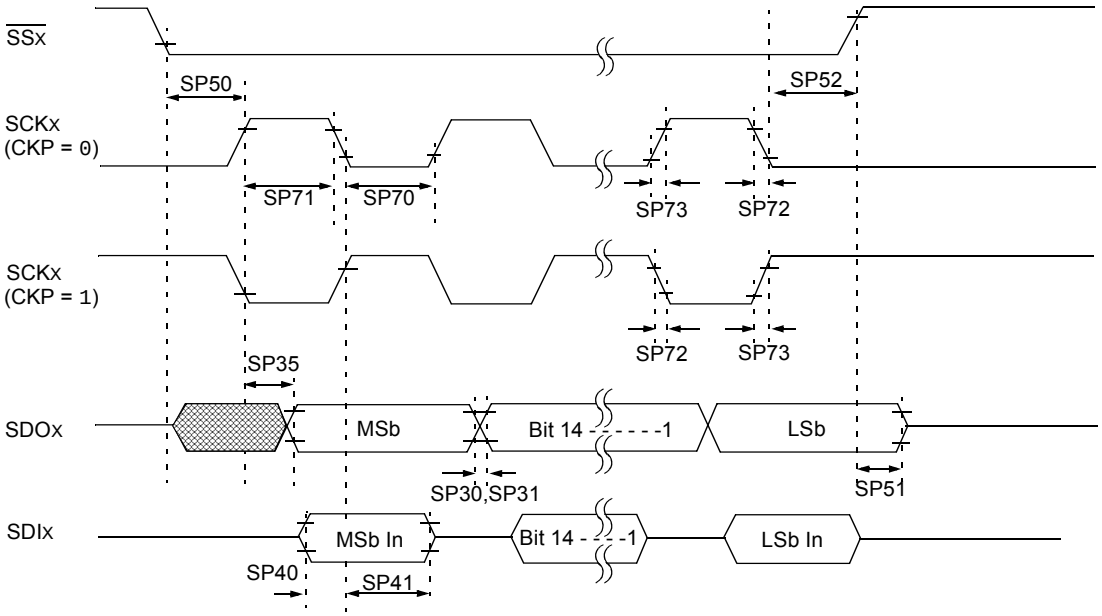
**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 50 ns. Therefore, the clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

**FIGURE 31-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 31-1 for load conditions.

**TABLE 31-30: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | TscL | SCKx Input Low Time **(Note 3)** | Tsck/2 | — | — | ns | — |
| SP71 | TscH | SCKx Input High Time **(Note 3)** | Tsck/2 | — | — | ns | — |
| SP72 | TscF | SCKx Input Fall Time | — | — | — | ns | See parameter DO32 |
| SP73 | TscR | SCKx Input Rise Time | — | — | — | ns | See parameter DO31 |
| SP30 | TdoF | SDOx Data Output Fall Time **(Note 4)** | — | — | — | ns | See parameter DO32 |
| SP31 | TdoR | SDOx Data Output Rise Time **(Note 4)** | — | — | — | ns | See parameter DO31 |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 15 | ns | VDD > 2.7V |
| | | | — | — | 20 | ns | VDD < 2.7V |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP50 | TssL2scH, TssL2scL | $\overline{SSx}$ ↓ to SCKx ↑ or SCKx Input | 175 | — | — | ns | — |
| SP51 | TssH2doZ | $\overline{SSx}$ ↑ to SDOx Output High-Impedance **(Note 3)** | 5 | — | 25 | ns | — |
| SP52 | TscH2ssH TscL2ssH | $\overline{SSx}$ after SCKx Edge | Tsck + 20 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 50 ns.

**4:** Assumes 50 pF load on all SPIx pins.


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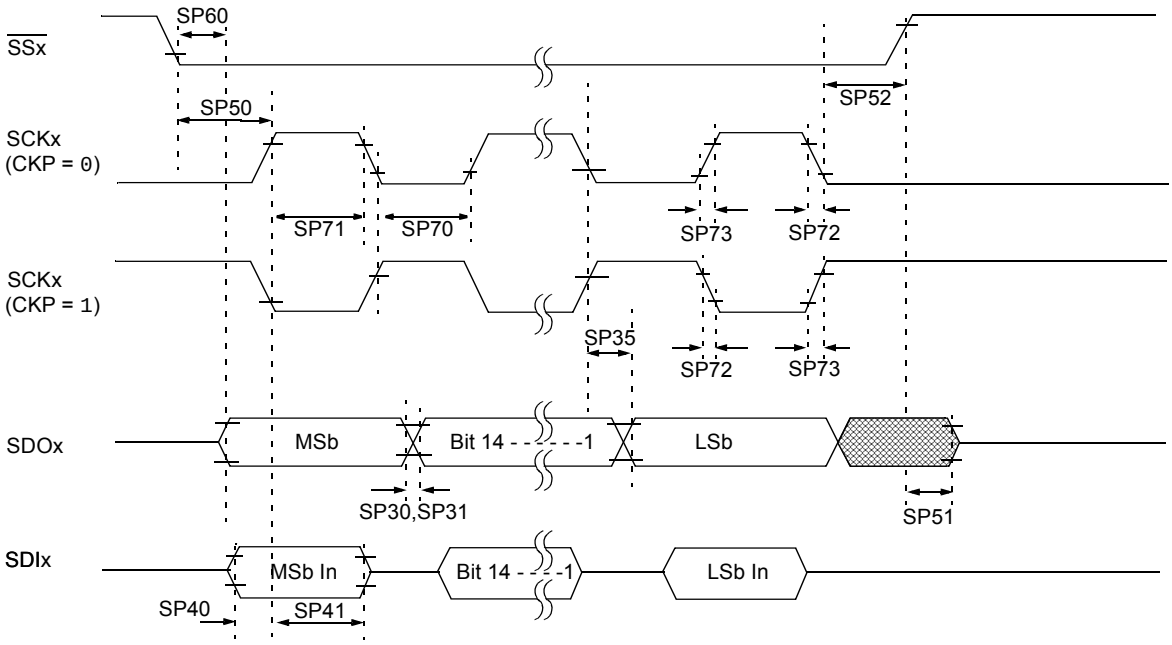
**FIGURE 31-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 31-1 for load conditions.

**TABLE 31-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | TscL | SCKx Input Low Time **(Note 3)** | Tsck/2 | — | — | ns | — |
| SP71 | TscH | SCKx Input High Time **(Note 3)** | Tsck/2 | — | — | ns | — |
| SP72 | TscF | SCKx Input Fall Time | — | 5 | 10 | ns | — |
| SP73 | TscR | SCKx Input Rise Time | — | 5 | 10 | ns | — |
| SP30 | TdoF | SDOx Data Output Fall Time **(Note 4)** | — | — | — | ns | See parameter DO32 |
| SP31 | TdoR | SDOx Data Output Rise Time **(Note 4)** | — | — | — | ns | See parameter DO31 |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 20 | ns | VDD > 2.7V |
| | | | — | — | 30 | ns | VDD < 2.7V |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP50 | TssL2scH, TssL2scL | $\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input | 175 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 50 ns.

**4:** Assumes 50 pF load on all SPIx pins.

**TABLE 31-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| SP51 | TssH2doZ | $\overline{SSx}$ ↑ to SDOx Output High-Impedance **(Note 4)** | 5 | — | 25 | ns | — |
| SP52 | TscH2ssH<br>TscL2ssH | $\overline{SSx}$ ↑ after SCKx Edge | Tsck + 20 | — | — | ns | — |
| SP60 | TssL2doV | SDOx Data Output Valid after $\overline{SSx}$ Edge | — | — | 25 | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 50 ns.

**4:** Assumes 50 pF load on all SPIx pins.


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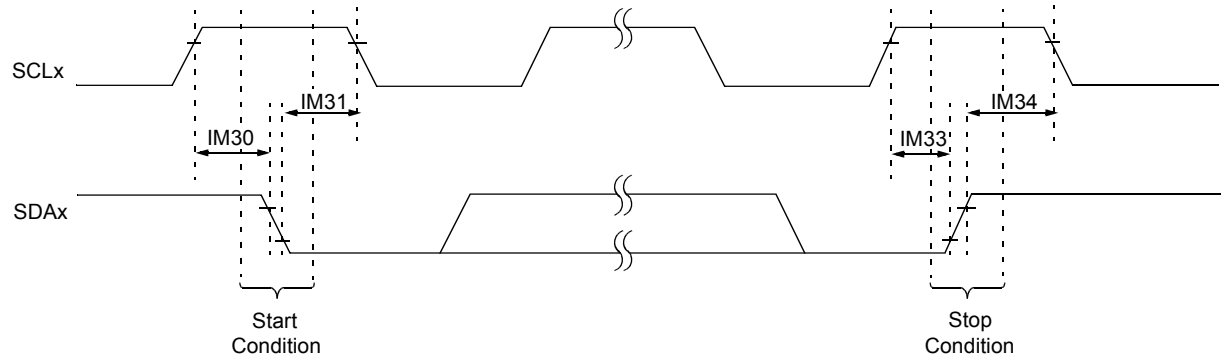
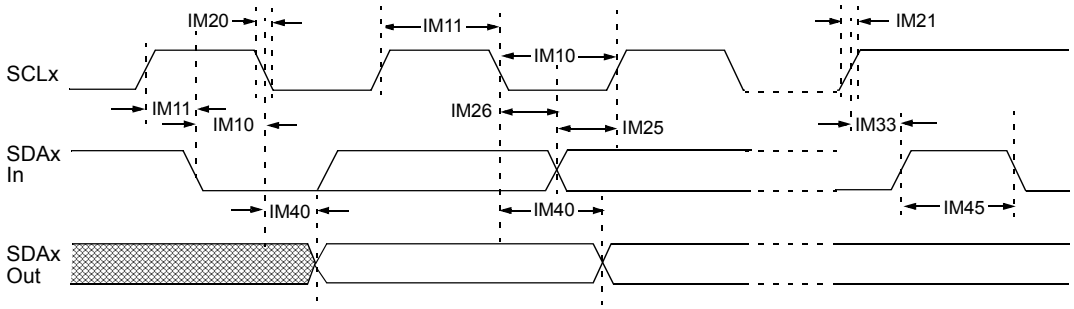
**FIGURE 31-14: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)**




**Note:** Refer to Figure 31-1 for load conditions.

**FIGURE 31-15: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)**




**Note:** Refer to Figure 31-1 for load conditions.

**TABLE 31-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | | **Min.(1)** | **Max.** | **Units** | **Conditions** |
| IM10 | TLO:SCL | Clock Low Time | 100 kHz mode | TPB * (BRG + 2) | — | µs | — |
| | | | 400 kHz mode | TPB * (BRG + 2) | — | µs | — |
| | | | 1 MHz mode **(Note 2)** | TPB * (BRG + 2) | — | µs | — |
| IM11 | THI:SCL | Clock High Time | 100 kHz mode | TPB * (BRG + 2) | — | µs | — |
| | | | 400 kHz mode | TPB * (BRG + 2) | — | µs | — |
| | | | 1 MHz mode **(Note 2)** | TPB * (BRG + 2) | — | µs | — |
| IM20 | TF:SCL | SDAx and SCLx Fall Time | 100 kHz mode | — | 300 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode **(Note 2)** | — | 100 | ns | |
| IM21 | TR:SCL | SDAx and SCLx Rise Time | 100 kHz mode | — | 1000 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode **(Note 2)** | — | 300 | ns | |
| IM25 | TSU:DAT | Data Input Setup Time | 100 kHz mode | 250 | — | ns | — |
| | | | 400 kHz mode | 100 | — | ns | |
| | | | 1 MHz mode **(Note 2)** | 100 | — | ns | |
| IM26 | THD:DAT | Data Input Hold Time | 100 kHz mode | 0 | — | µs | — |
| | | | 400 kHz mode | 0 | 0.9 | µs | |
| | | | 1 MHz mode **(Note 2)** | 0 | 0.3 | µs | |
| IM30 | TSU:STA | Start Condition Setup Time | 100 kHz mode | TPB * (BRG + 2) | — | µs | Only relevant for Repeated Start condition |
| | | | 400 kHz mode | TPB * (BRG + 2) | — | µs | |
| | | | 1 MHz mode **(Note 2)** | TPB * (BRG + 2) | — | µs | |
| IM31 | THD:STA | Start Condition Hold Time | 100 kHz mode | TPB * (BRG + 2) | — | µs | After this period, the first clock pulse is generated |
| | | | 400 kHz mode | TPB * (BRG + 2) | — | µs | |
| | | | 1 MHz mode **(Note 2)** | TPB * (BRG + 2) | — | µs | |
| IM33 | TSU:STO | Stop Condition Setup Time | 100 kHz mode | TPB * (BRG + 2) | — | µs | — |
| | | | 400 kHz mode | TPB * (BRG + 2) | — | µs | |
| | | | 1 MHz mode **(Note 2)** | TPB * (BRG + 2) | — | µs | |
| IM34 | THD:STO | Stop Condition Hold Time | 100 kHz mode | TPB * (BRG + 2) | — | ns | — |
| | | | 400 kHz mode | TPB * (BRG + 2) | — | ns | |
| | | | 1 MHz mode **(Note 2)** | TPB * (BRG + 2) | — | ns | |

**Note 1:** BRG is the value of the $I^2C$ Baud Rate Generator.

**2:** Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

**3:** The typical value for this parameter is 104 ns.


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**TABLE 31-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE) (CONTINUED)**

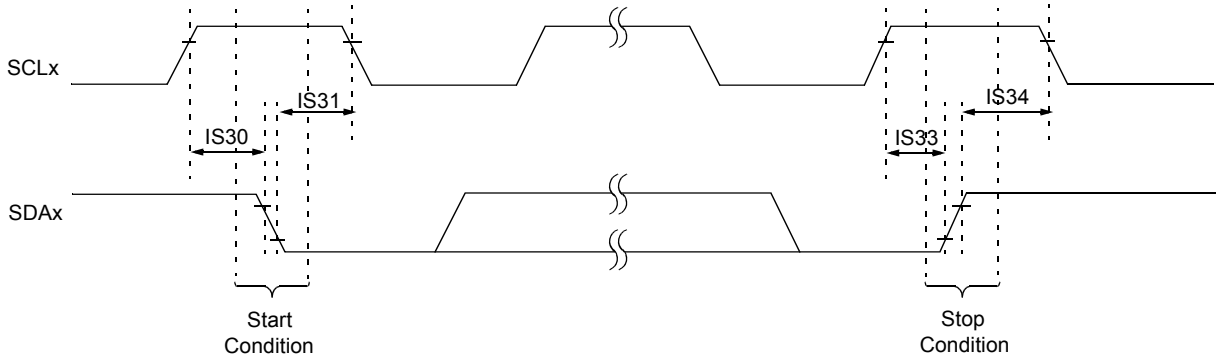
| AC CHARACTERISTICS | | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | | **Min.(1)** | **Max.** | **Units** | **Conditions** |
| IM40 | TAA:SCL | Output Valid from Clock | 100 kHz mode | — | 3500 | ns | — |
| | | | 400 kHz mode | — | 1000 | ns | — |
| | | | 1 MHz mode **(Note 2)** | — | 350 | ns | — |
| IM45 | TBF:SDA | Bus Free Time | 100 kHz mode | 4.7 | — | μs | The amount of time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | μs | |
| | | | 1 MHz mode **(Note 2)** | 0.5 | — | μs | |
| IM50 | CB | Bus Capacitive Loading | | — | 400 | pF | — |
| IM51 | TPGD | Pulse Gobbler Delay | | 52 | 312 | ns | See **Note 3** |

**Note 1:** BRG is the value of the $I^2C$ Baud Rate Generator.

**2:** Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

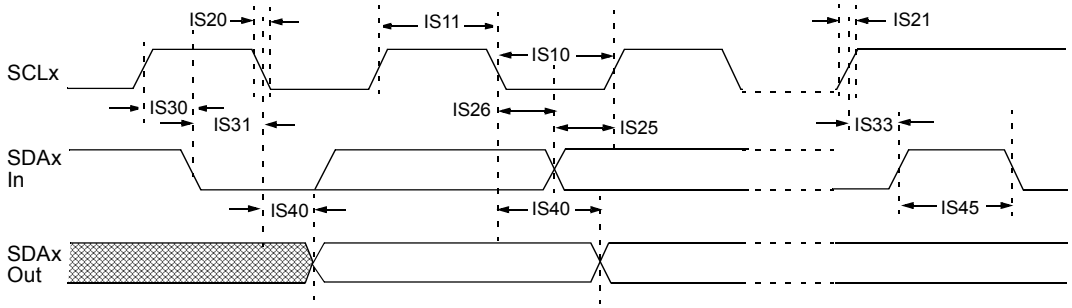
**3:** The typical value for this parameter is 104 ns.

**FIGURE 31-16: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)**




**Note:** Refer to Figure 31-1 for load conditions.

**FIGURE 31-17: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)**




**Note:** Refer to Figure 31-1 for load conditions.


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**TABLE 31-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | | **Min.** | **Max.** | **Units** | **Conditions** |
| IS10 | TLO:SCL | Clock Low Time | 100 kHz mode | 4.7 | — | μs | PBCLK must operate at a minimum of 800 kHz |
| | | | 400 kHz mode | 1.3 | — | μs | PBCLK must operate at a minimum of 3.2 MHz |
| | | | 1 MHz mode **(Note 1)** | 0.5 | — | μs | — |
| IS11 | THI:SCL | Clock High Time | 100 kHz mode | 4.0 | — | μs | PBCLK must operate at a minimum of 800 kHz |
| | | | 400 kHz mode | 0.6 | — | μs | PBCLK must operate at a minimum of 3.2 MHz |
| | | | 1 MHz mode **(Note 1)** | 0.5 | — | μs | — |
| IS20 | TF:SCL | SDAx and SCLx Fall Time | 100 kHz mode | — | 300 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode **(Note 1)** | — | 100 | ns | |
| IS21 | TR:SCL | SDAx and SCLx Rise Time | 100 kHz mode | — | 1000 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode **(Note 1)** | — | 300 | ns | |
| IS25 | TSU:DAT | Data Input Setup Time | 100 kHz mode | 250 | — | ns | — |
| | | | 400 kHz mode | 100 | — | ns | |
| | | | 1 MHz mode **(Note 1)** | 100 | — | ns | |
| IS26 | THD:DAT | Data Input Hold Time | 100 kHz mode | 0 | — | ns | — |
| | | | 400 kHz mode | 0 | 0.9 | μs | |
| | | | 1 MHz mode **(Note 1)** | 0 | 0.3 | μs | |
| IS30 | TSU:STA | Start Condition Setup Time | 100 kHz mode | 4700 | — | ns | Only relevant for Repeated Start condition |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1 MHz mode **(Note 1)** | 250 | — | ns | |
| IS31 | THD:STA | Start Condition Hold Time | 100 kHz mode | 4000 | — | ns | After this period, the first clock pulse is generated |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1 MHz mode **(Note 1)** | 250 | — | ns | |
| IS33 | TSU:STO | Stop Condition Setup Time | 100 kHz mode | 4000 | — | ns | — |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1 MHz mode **(Note 1)** | 600 | — | ns | |

**Note 1:** Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

**TABLE 31-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE) (CONTINUED)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | | **Min.** | **Max.** | **Units** | **Conditions** |
| IS34 | THD:STO | Stop Condition Hold Time | 100 kHz mode | 4000 | — | ns | — |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1 MHz mode **(Note 1)** | 250 | | ns | |
| IS40 | TAA:SCL | Output Valid from Clock | 100 kHz mode | 0 | 3500 | ns | — |
| | | | 400 kHz mode | 0 | 1000 | ns | |
| | | | 1 MHz mode **(Note 1)** | 0 | 350 | ns | |
| IS45 | TBF:SDA | Bus Free Time | 100 kHz mode | 4.7 | — | µs | The amount of time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | µs | |
| | | | 1 MHz mode **(Note 1)** | 0.5 | — | µs | |
| IS50 | CB | Bus Capacitive Loading | | — | 400 | pF | — |

**Note 1:** Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).


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**TABLE 31-34: ADC MODULE SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions (see Note 5): 2.5V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| **Device Supply** | | | | | | | |
| AD01 | AVDD | Module VDD Supply | Greater of VDD – 0.3 or 2.5 | — | Lesser of VDD + 0.3 or 3.6 | V | — |
| AD02 | AVSS | Module VSS Supply | VSS | — | AVDD | V | **(Note 1)** |
| **Reference Inputs** | | | | | | | |
| AD05<br>AD05a | VREFH | Reference Voltage High | AVSS + 2.0<br>2.5 | —<br>— | AVDD<br>3.6 | V<br>V | **(Note 1)**<br>VREFH = AVDD **(Note 3)** |
| AD06 | VREFL | Reference Voltage Low | AVSS | — | VREFH – 2.0 | V | **(Note 1)** |
| AD07 | VREF | Absolute Reference Voltage (VREFH – VREFL) | 2.0 | — | AVDD | V | **(Note 3)** |
| AD08<br>AD08a | IREF | Current Drain | —<br>— | 250<br>— | 400<br>3 | µA<br>µA | ADC operating<br>ADC off |
| **Analog Input** | | | | | | | |
| AD12 | VINH-VINL | Full-Scale Input Span | VREFL | — | VREFH | V | — |
| AD13 | VINL | Absolute VINL Input Voltage | AVSS – 0.3 | — | AVDD/2 | V | — |
| AD14 | VIN | Absolute Input Voltage | AVSS – 0.3 | — | AVDD + 0.3 | V | — |
| AD15 | — | Leakage Current | — | ±0.001 | ±0.610 | µA | VINL = AVSS = VREFL = 0V,<br>AVDD = VREFH = 3.3V<br>Source Impedance = 10 kΩ |
| AD17 | RIN | Recommended Impedance of Analog Voltage Source | — | — | 5k | Ω | **(Note 1)** |
| **ADC Accuracy – Measurements with External VREF+/VREF-** | | | | | | | |
| AD20c | Nr | Resolution | 10 data bits | | | bits | — |
| AD21c | INL | Integral Non-linearity | > -1 | — | < 1 | LSb | VINL = AVSS = VREFL = 0V,<br>AVDD = VREFH = 3.3V |
| AD22c | DNL | Differential Non-linearity | > -1 | — | < 1 | LSb | VINL = AVSS = VREFL = 0V,<br>AVDD = VREFH = 3.3V<br>**(Note 2)** |
| AD23c | GERR | Gain Error | > -1 | — | < 1 | LSb | VINL = AVSS = VREFL = 0V,<br>AVDD = VREFH = 3.3V |
| AD24c | EOFF | Offset Error | > -1 | — | < 1 | Lsb | VINL = AVSS = 0V,<br>AVDD = 3.3V |
| AD25c | — | Monotonicity | — | — | — | — | Guaranteed |

**Note 1:** These parameters are not characterized or tested in manufacturing.

**2:** With no missing codes.

**3:** These parameters are characterized, but not tested in manufacturing.

**4:** Characterized with a 1 kHz sine wave.

**5:** The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

**TABLE 31-34: ADC MODULE SPECIFICATIONS (CONTINUED)**

| AC CHARACTERISTICS | | | Standard Operating Conditions (see Note 5): 2.5V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| **ADC Accuracy – Measurements with Internal VREF+/VREF-** | | | | | | | |
| AD20d | Nr | Resolution | 10 data bits | | | bits | **(Note 3)** |
| AD21d | INL | Integral Non-linearity | > -1 | — | < 1 | LSb | VINL = AVSS = 0V, AVDD = 2.5V to 3.6V **(Note 3)** |
| AD22d | DNL | Differential Non-linearity | > -1 | — | < 1 | LSb | VINL = AVSS = 0V, AVDD = 2.5V to 3.6V **(Notes 2,3)** |
| AD23d | GERR | Gain Error | > -4 | — | < 4 | LSb | VINL = AVSS = 0V, AVDD = 2.5V to 3.6V **(Note 3)** |
| AD24d | EOFF | Offset Error | > -2 | — | < 2 | Lsb | VINL = AVSS = 0V, AVDD = 2.5V to 3.6V **(Note 3)** |
| AD25d | — | Monotonicity | — | — | — | — | Guaranteed |
| **Dynamic Performance** | | | | | | | |
| AD32b | SINAD | Signal to Noise and Distortion | 55 | 58.5 | — | dB | **(Notes 3,4)** |
| AD34b | ENOB | Effective Number of bits | 9.0 | 9.5 | — | bits | **(Notes 3,4)** |

**Note 1:** These parameters are not characterized or tested in manufacturing.

**2:** With no missing codes.

**3:** These parameters are characterized, but not tested in manufacturing.

**4:** Characterized with a 1 kHz sine wave.

**5:** The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.


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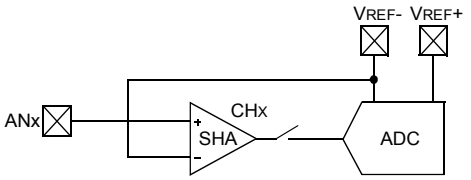
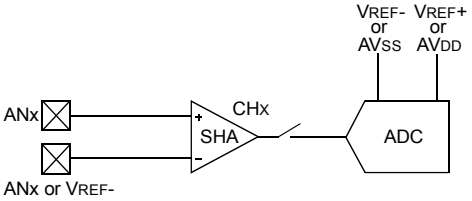
**TABLE 31-35: 10-BIT CONVERSION RATE PARAMETERS**

| AC CHARACTERISTICS(2) | | | Standard Operating Conditions (see Note 3): 2.5V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | |
|---|---|---|---|---|---|
| **ADC Speed** | **TAD Min.** | **Sampling Time Min.** | **RS Max.** | **VDD** | **ADC Channels Configuration** |
| 1 Msps to 400 ksps(1) | 65 ns | 132 ns | 500Ω | 3.0V to 3.6V |  |
| Up to 400 ksps | 200 ns | 200 ns | 5.0 kΩ | 2.5V to 3.6V |  |

**Note 1:** External VREF- and VREF+ pins must be used for correct operation.

**2:** These parameters are characterized, but not tested in manufacturing.

**3:** The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

**TABLE 31-36: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions (see Note 4): 2.5V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| **Clock Parameters** | | | | | | | |
| AD50 | TAD | ADC Clock Period(2) | 65 | — | — | ns | See Table 31-35 |
| **Conversion Rate** | | | | | | | |
| AD55 | TCONV | Conversion Time | — | 12 TAD | — | — | — |
| AD56 | FCNV | Throughput Rate (Sampling Speed) | — | — | 1000 | ksps | AVDD = 3.0V to 3.6V |
| | | | — | — | 400 | ksps | AVDD = 2.5V to 3.6V |
| AD57 | TSAMP | Sample Time | 1 TAD | — | — | — | TSAMP must be ≥ 132 ns |
| **Timing Parameters** | | | | | | | |
| AD60 | TPCS | Conversion Start from Sample Trigger(3) | — | 1.0 TAD | — | — | Auto-Convert Trigger (SSRC<2:0> = 111) not selected |
| AD61 | TPSS | Sample Start from Setting Sample (SAMP) bit | 0.5 TAD | — | 1.5 TAD | — | — |
| AD62 | TCSS | Conversion Completion to Sample Start (ASAM = 1)(3) | — | 0.5 TAD | — | — | — |
| AD63 | TDPU | Time to Stabilize Analog Stage from ADC Off to ADC On(3) | — | — | 2 | μs | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

**3:** Characterized by design but not tested.

**4:** The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.


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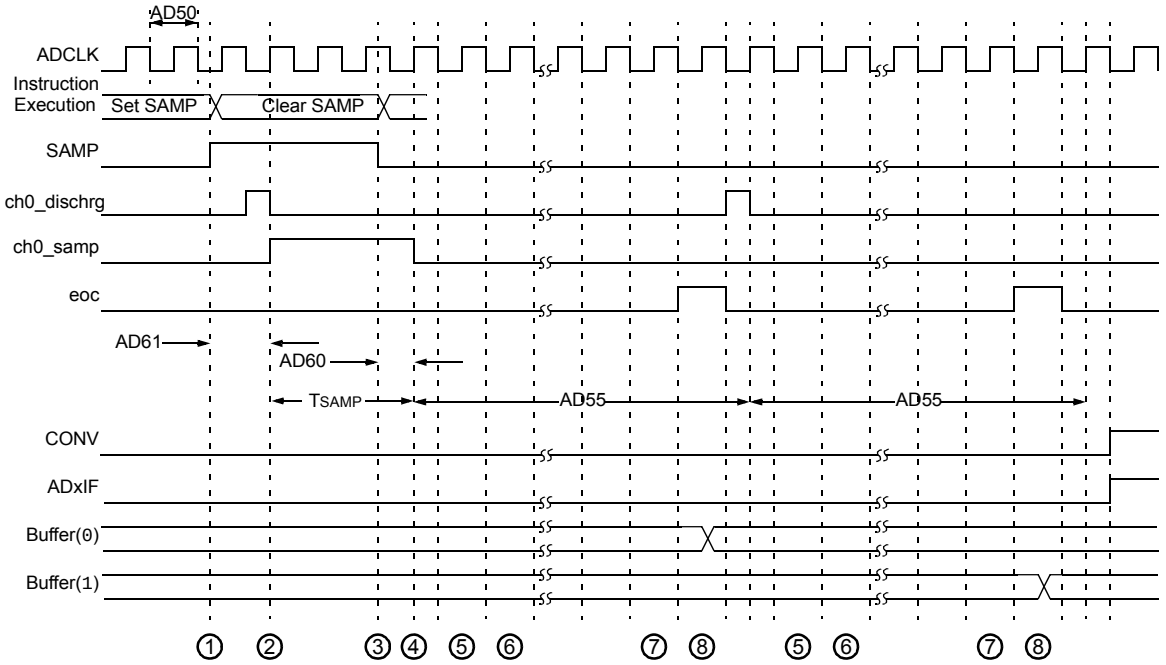
**FIGURE 31-18: ANALOG-TO-DIGITAL CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (ASAM = 0, SSRC<2:0> = 000)**




(1) – Software sets ADxCON. SAMP to start sampling.

(2) – Sampling starts after discharge period. TSAMP is described in **Section 17. "10-bit Analog-to-Digital Converter (ADC)"** (DS60001104) in the *"PIC32 Family Reference Manual"*.

(3) – Software clears ADxCON. SAMP to start conversion.

(4) – Sampling ends, conversion sequence starts.

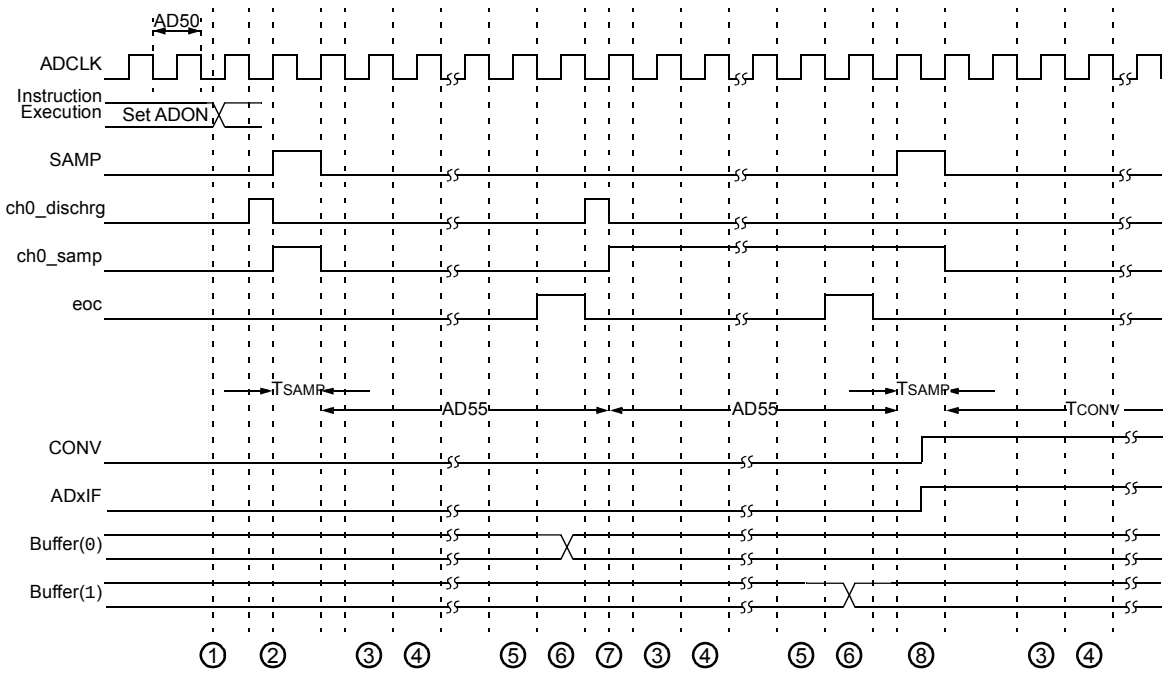
(5) – Convert bit 9.

(6) – Convert bit 8.

(7) – Convert bit 0.

(8) – One TAD for end of conversion.

**FIGURE 31-19: ANALOG-TO-DIGITAL CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (ASAM = 1, SSRC<2:0> = 111, SAMC<4:0> = 00001)**




(1) – Software sets ADxCON. ADON to start AD operation.

(2) – Sampling starts after discharge period. TSAMP is described in **Section 17. "10-bit Analog-to-Digital Converter (ADC)"** (DS60001104).

(3) – Convert bit 9.

(4) – Convert bit 8.

(5) – Convert bit 0.

(6) – One TAD for end of conversion.

(7) – Begin conversion of next channel.

(8) – Sample for time specified by SAMC<4:0>.


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**FIGURE 31-20: PARALLEL SLAVE PORT TIMING**

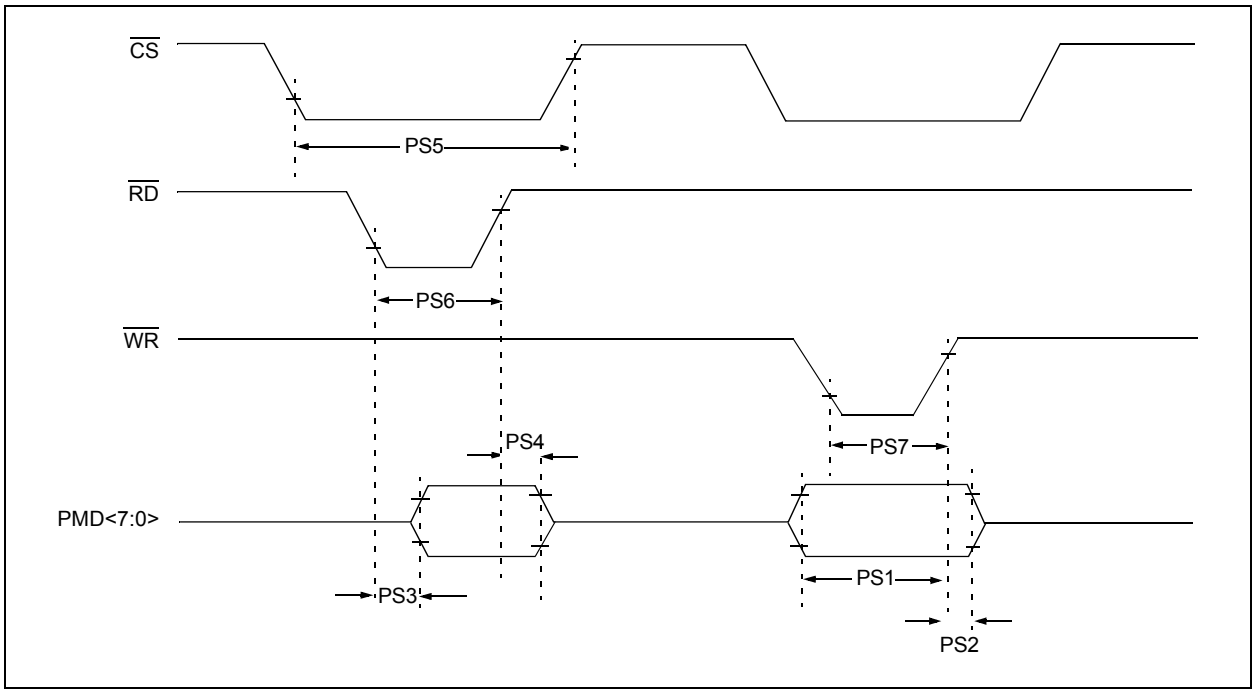

**TABLE 31-37: PARALLEL SLAVE PORT REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param.No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| PS1 | TdtV2wrH | Data In Valid before $\overline{WR}$ or $\overline{CS}$ Inactive (setup time) | 20 | — | — | ns | — |
| PS2 | TwrH2dtI | $\overline{WR}$ or $\overline{CS}$ Inactive to Data-In Invalid (hold time) | 40 | — | — | ns | — |
| PS3 | TrdL2dtV | $\overline{RD}$ and $\overline{CS}$ Active to Data-Out Valid | — | — | 60 | ns | — |
| PS4 | TrdH2dtI | $\overline{RD}$ Active or $\overline{CS}$ Inactive to Data-Out Invalid | 0 | — | 10 | ns | — |
| PS5 | Tcs | $\overline{CS}$ Active Time | TPB + 40 | — | — | ns | — |
| PS6 | TWR | $\overline{WR}$ Active Time | TPB + 25 | — | — | ns | — |
| PS7 | TRD | $\overline{RD}$ Active Time | TPB + 25 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**FIGURE 31-21: PARALLEL MASTER PORT READ TIMING DIAGRAM**

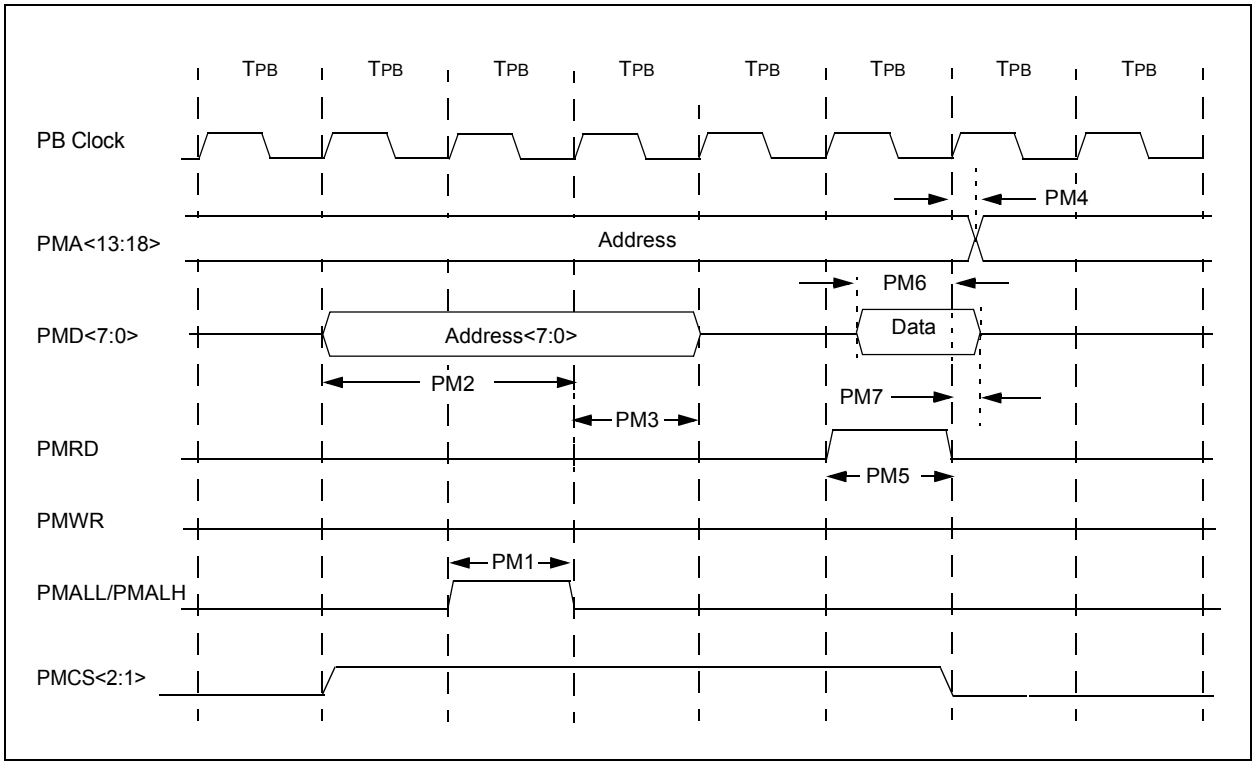



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**TABLE 31-38: PARALLEL MASTER PORT READ TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| PM1 | TLAT | PMALL/PMALH Pulse Width | — | 1 TPB | — | — | — |
| PM2 | TADSU | Address Out Valid to PMALL/ PMALH Invalid (address setup time) | — | 2 TPB | — | — | — |
| PM3 | TADHOLD | PMALL/PMALH Invalid to Address Out Invalid (address hold time) | — | 1 TPB | — | — | — |
| PM4 | TAHOLD | PMRD Inactive to Address Out Invalid (address hold time) | 5 | — | — | ns | — |
| PM5 | TRD | PMRD Pulse Width | — | 1 TPB | — | — | — |
| PM6 | TDSU | PMRD or PMENB Active to Data In Valid (data setup time) | 15 | — | — | ns | — |
| PM7 | TDHOLD | PMRD or PMENB Inactive to Data In Invalid (data hold time) | — | 80 | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**FIGURE 31-22: PARALLEL MASTER PORT WRITE TIMING DIAGRAM**

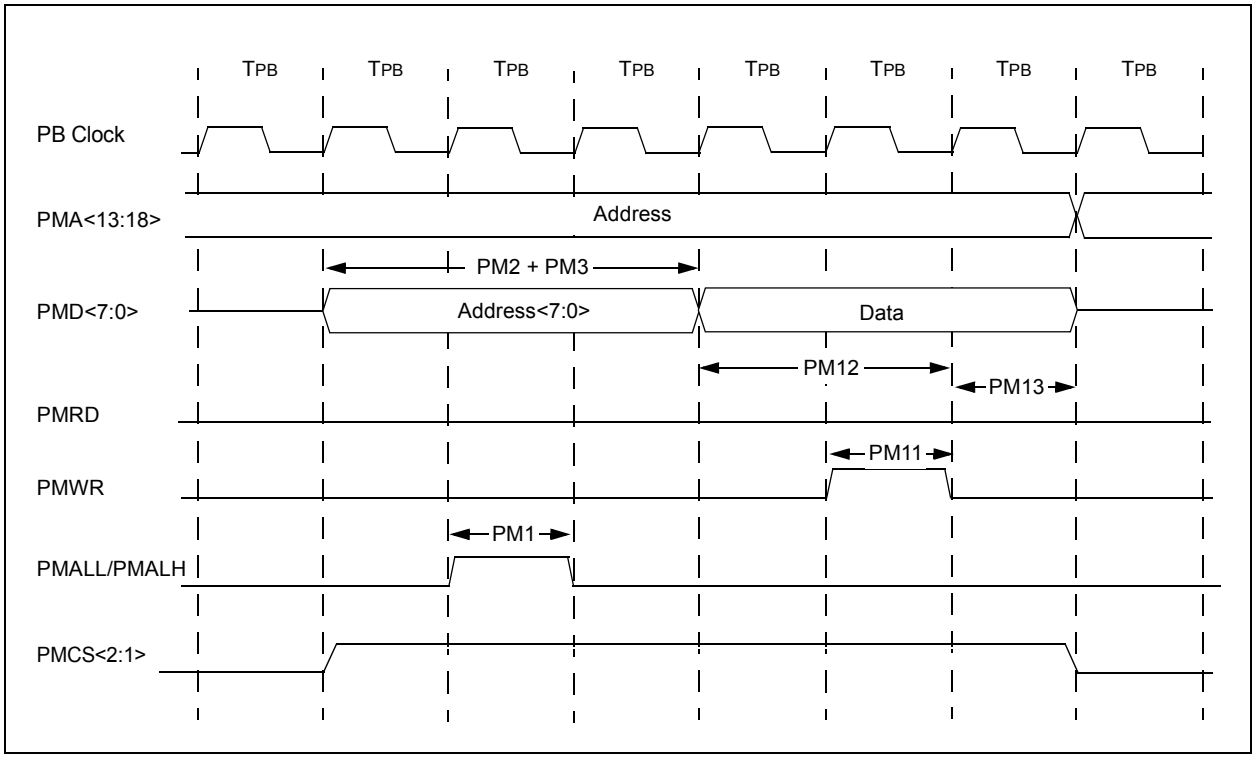

**TABLE 31-39: PARALLEL MASTER PORT WRITE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| PM11 | TWR | PMWR Pulse Width | — | 1 TPB | — | — | — |
| PM12 | TDVSU | Data Out Valid before PMWR or PMENB goes Inactive (data setup time) | — | 2 TPB | — | — | — |
| PM13 | TDVHOLD | PMWR or PMEMB Invalid to Data Out Invalid (data hold time) | — | 1 TPB | — | — | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**TABLE 31-40: OTG ELECTRICAL SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| USB313 | VUSB3V3 | USB Voltage | 3.0 | — | 3.6 | V | Voltage on VUSB3V3 must be in this range for proper USB operation |
| USB315 | VILUSB | Input Low Voltage for USB Buffer | — | — | 0.8 | V | — |
| USB316 | VIHUSB | Input High Voltage for USB Buffer | 2.0 | — | — | V | — |
| USB318 | VDIFS | Differential Input Sensitivity | — | — | 0.2 | V | The difference between D+ and D- must exceed this value while VCM is met |
| USB319 | VCM | Differential Common Mode Range | 0.8 | — | 2.5 | V | — |
| USB320 | ZOUT | Driver Output Impedance | 28.0 | — | 44.0 | Ω | — |
| USB321 | VOL | Voltage Output Low | 0.0 | — | 0.3 | V | 1.425 kΩ load connected to VUSB3V3 |
| USB322 | VOH | Voltage Output High | 2.8 | — | 3.6 | V | 1.425 kΩ load connected to ground |

**Note 1:** These parameters are characterized, but not tested in manufacturing.


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**TABLE 31-41: CTMU CURRENT SOURCE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions (see Note 3):2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **CTMU CURRENT SOURCE** | | | | | | | |
| CTMUI1 | IOUT1 | Base Range(1) | — | 0.55 | — | µA | CTMUCON<9:8> = 01 |
| CTMUI2 | IOUT2 | 10x Range(1) | — | 5.5 | — | µA | CTMUCON<9:8> = 10 |
| CTMUI3 | IOUT3 | 100x Range(1) | — | 55 | — | µA | CTMUCON<9:8> = 11 |
| CTMUI4 | IOUT4 | 1000x Range(1) | — | 550 | — | µA | CTMUCON<9:8> = 00 |
| CTMUFV1 | VF | Temperature Diode Forward Voltage(1,2) | — | 0.598 | — | V | TA = +25ºC, CTMUCON<9:8> = 01 |
| | | | — | 0.658 | — | V | TA = +25ºC, CTMUCON<9:8> = 10 |
| | | | — | 0.721 | — | V | TA = +25ºC, CTMUCON<9:8> = 11 |
| CTMUFV2 | VFVR | Temperature Diode Rate of Change(1,2) | — | -1.92 | — | mV/ºC | CTMUCON<9:8> = 01 |
| | | | — | -1.74 | — | mV/ºC | CTMUCON<9:8> = 10 |
| | | | — | -1.56 | — | mV/ºC | CTMUCON<9:8> = 11 |

**Note 1:** Nominal value at center point of current trim range (CTMUCON<15:10> = 000000).

**2:** Parameters are characterized but not tested in manufacturing. Measurements taken with the following conditions:

- VREF+ = AVDD = 3.3V
- ADC module configured for conversion speed of 500 ksps
- All PMD bits are cleared (PMDx = 0)
- Executing a while(1) statement
- Device operating from the FRC with no PLL

**3:** The CTMU module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

**FIGURE 31-23: EJTAG TIMING CHARACTERISTICS**

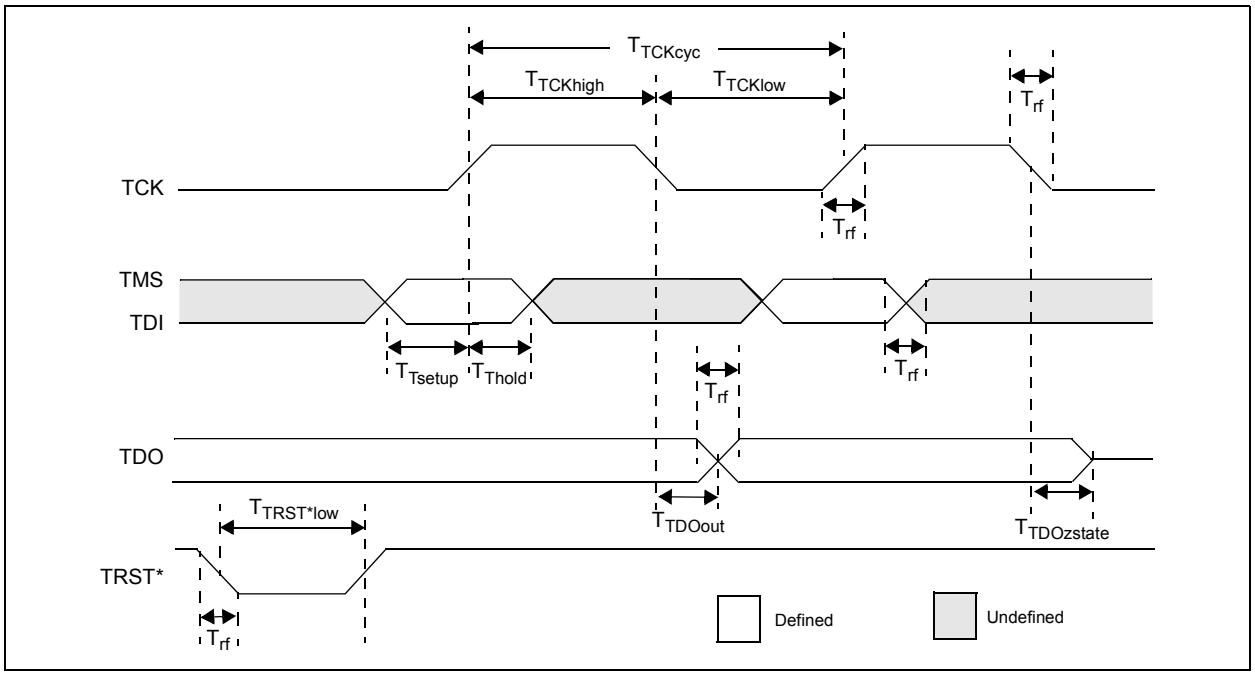


**TABLE 31-42: EJTAG TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Description(1)** | **Min.** | **Max.** | **Units** | **Conditions** |
| EJ1 | TTCKCYC | TCK Cycle Time | 25 | — | ns | — |
| EJ2 | TTCKHIGH | TCK High Time | 10 | — | ns | — |
| EJ3 | TTCKLOW | TCK Low Time | 10 | — | ns | — |
| EJ4 | TTSETUP | TAP Signals Setup Time Before Rising TCK | 5 | — | ns | — |
| EJ5 | TTHOLD | TAP Signals Hold Time After Rising TCK | 3 | — | ns | — |
| EJ6 | TTDOOUT | TDO Output Delay Time from Falling TCK | — | 5 | ns | — |
| EJ7 | TTDOZSTATE | TDO 3-State Delay Time from Falling TCK | — | 5 | ns | — |
| EJ8 | TTRSTLOW | TRST Low Time | 25 | — | ns | — |
| EJ9 | TRF | TAP Signals Rise/Fall Time, All Input and Output | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.


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## 32.0 50 MHz ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MX1XX/2XX/5XX 64/100-pin Family electrical characteristics for devices operating at 50 MHz.

The specifications for 50 MHz are identical to those shown in **Section 31.0 "40 MHz Electrical Characteristics"**, with the exception of the parameters listed in this chapter.

Parameters in this chapter begin with the letter "M", which denotes 50 MHz operation. For example, parameter DC29a in **Section 31.0 "40 MHz Electrical Characteristics"**, is the up to 40 MHz operation equivalent for MDC29a.

Absolute maximum ratings for the PIC32MX1XX/2XX/5XX 64/100-pin Family 50 MHz devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

### Absolute Maximum Ratings

**(See Note 1)**

Ambient temperature under bias ..... -40°C to +85°C
Storage temperature ..... -65°C to +150°C
Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to $V_{SS}$ **(Note 3)** ..... -0.3V to ($V_{DD}$ + 0.3V)
Voltage on any 5V tolerant pin with respect to $V_{SS}$ when $V_{DD} \geq 2.3V$ **(Note 3)** ..... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to $V_{SS}$ when $V_{DD} < 2.3V$ **(Note 3)** ..... -0.3V to +3.6V
Voltage on D+ or D- pin with respect to $V_{USB3V3}$ ..... -0.3V to ($V_{USB3V3}$ + 0.3V)
Voltage on $V_{BUS}$ with respect to $V_{SS}$ ..... -0.3V to +5.5V
Maximum current out of $V_{SS}$ pin(s) ..... 300 mA
Maximum current into $V_{DD}$ pin(s) **(Note 2)** ..... 300 mA
Maximum output current sunk by any I/O pin ..... 15 mA
Maximum output current sourced by any I/O pin ..... 15 mA
Maximum current sunk by all ports ..... 200 mA
Maximum current sourced by all ports **(Note 2)** ..... 200 mA

**Note 1:** Stresses above those listed under **"Absolute Maximum Ratings"** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**2:** Maximum allowable current is a function of device maximum power dissipation (see Table 32-2).

**3:** See the **"Device Pin Tables"** section for the 5V tolerant pins.

## 32.1 DC Characteristics

**TABLE 32-1: OPERATING MIPS VS. VOLTAGE**

| Characteristic | VDD Range (in Volts)(1) | Temp. Range (in °C) | Max. Frequency |
|---|---|---|---|
| | | | PIC32MX1XX/2XX/5XX 64/100-pin Family |
| MDC5 | VBOR-3.6V | -40°C to +85°C | 50 MHz |

**Note 1:** Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 31-10 for BOR values.

**TABLE 32-2: DC CHARACTERISTICS: OPERATING CURRENT (IDD)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | |
|---|---|---|---|---|
| Parameter No. | Typical(3) | Max. | Units | Conditions |
| **Operating Current (IDD) (Note 1, 2)** | | | | |
| MDC24 | 25 | 40 | mA | 50 MHz |

**Note 1:** A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

**2:** The test conditions for IDD measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU, Program Flash, and SRAM data memory are operational, SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- CPU executing `while(1)` statement from Flash

**3:** RTCC and JTAG are disabled

**4:** Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.


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**TABLE 32-3: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | |
|---|---|---|---|---|
| **Parameter No.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| **Idle Current (IIDLE): Core Off, Clock on Base Current (Note 1)** | | | | |
| MDC34a | 9.5 | 24 | mA | 50 MHz |

**Note 1:** The test conditions for IIDLE current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Idle mode (CPU core Halted), and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- RTCC and JTAG are disabled

**2:** Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**TABLE 32-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | |
|---|---|---|---|---|---|
| **Param. No.** | **Typical(2)** | **Max.** | **Units** | **Conditions** | |
| **Power-Down Current (IPD) (Note 1)** | | | | | |
| MDC40k | 50 | 150 | µA | -40°C | Base Power-Down Current |
| MDC40n | 250 | 650 | µA | +85°C | |
| **Module Differential Current** | | | | | |
| MDC41e | 15 | 55 | µA | 3.6V | Watchdog Timer Current: ΔIWDT **(Note 3)** |
| MDC42e | 34 | 55 | µA | 3.6V | RTCC + Timer1 w/32 kHz Crystal: ΔIRTCC **(Note 3)** |
| MDC43d | 1100 | 1800 | µA | 3.6V | ADC: ΔIADC **(Notes 3,4)** |

**Note 1:** The test conditions for IPD current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Sleep mode, and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is set
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- RTCC and JTAG are disabled

**2:** Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

**4:** Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.

## 32.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX1XX/2XX/5XX 64/100-pin AC characteristics and timing parameters.

**TABLE 32-5: EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| MOS10 | FOSC | External CLKI Frequency<br>(External clocks allowed only in EC and ECPLL modes) | DC<br>4 | —<br>— | 50<br>50 | MHz<br>MHz | EC **(Note 2)**<br>ECPLL **(Note 1)** |

**Note 1:** PLL input requirements: 4 MHz ≤ FPLLIN ≤ 5 MHz (use PLL prescaler to reduce Fosc). This parameter is characterized, but tested at 10 MHz only at manufacturing.

**2:** This parameter is characterized, but not tested in manufacturing.

**TABLE 32-6: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| MSP10 | TscL | SCKx Output Low Time **(Note 1,2)** | TSCK/2 | — | — | ns | — |
| MSP11 | TscH | SCKx Output High Time **(Note 1,2)** | TSCK/2 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

**TABLE 32-7: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| MSP10 | TscL | SCKx Output Low Time **(Note 1,2)** | TSCK/2 | — | — | ns | — |
| MSP11 | TscH | SCKx Output High Time **(Note 1,2)** | TSCK/2 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.


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**TABLE 32-8: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| MSP70 | TscL | SCKx Input Low Time **(Note 1,2)** | Tsck/2 | — | — | ns | — |
| MSP71 | TscH | SCKx Input High Time **(Note 1,2)** | Tsck/2 | — | — | ns | — |
| MSP51 | TssH2doZ | $\overline{SSx}$ ↑ to SDOx Output High-Impedance **(Note 2)** | 5 | — | 25 | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** The minimum clock period for SCKx is 40 ns.

**TABLE 32-9: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| SP70 | TscL | SCKx Input Low Time **(Note 1,2)** | Tsck/2 | — | — | ns | — |
| SP71 | TscH | SCKx Input High Time **(Note 1,2)** | Tsck/2 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** The minimum clock period for SCKx is 40 ns.

**NOTES:**


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## 33.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

**Note:** The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

**FIGURE 33-1: VOH – 4x DRIVER PINS**

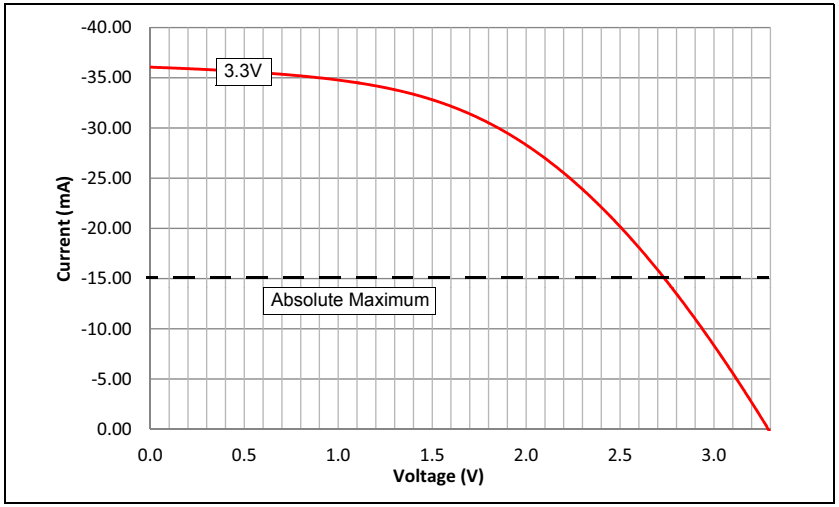


**FIGURE 33-2: VOH – 8x DRIVER PINS**

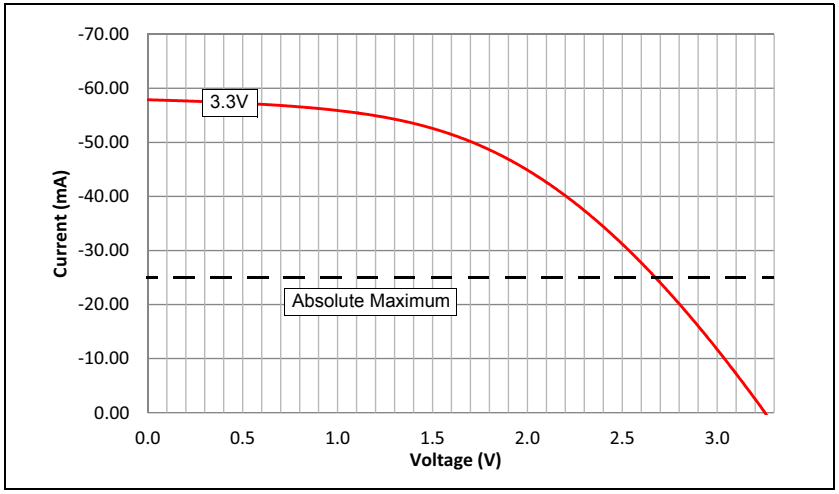


**FIGURE 33-3: VOL – 4x DRIVER PINS**

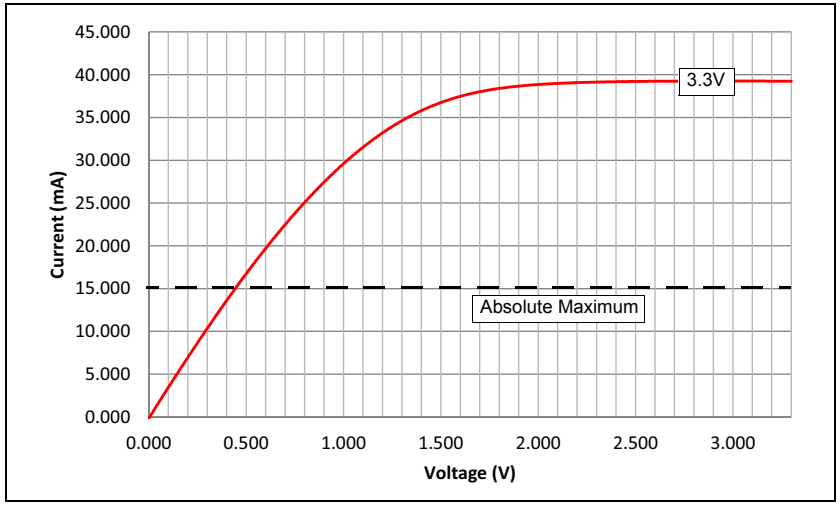


**FIGURE 33-4: VOL – 8x DRIVER PINS**

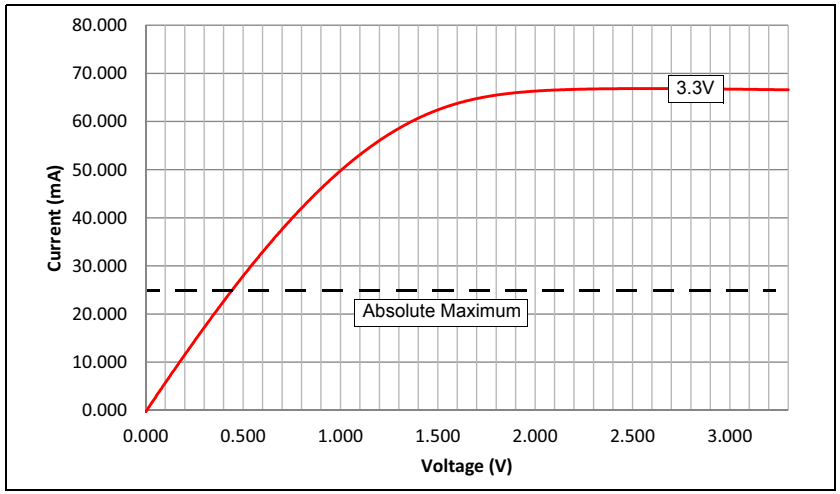


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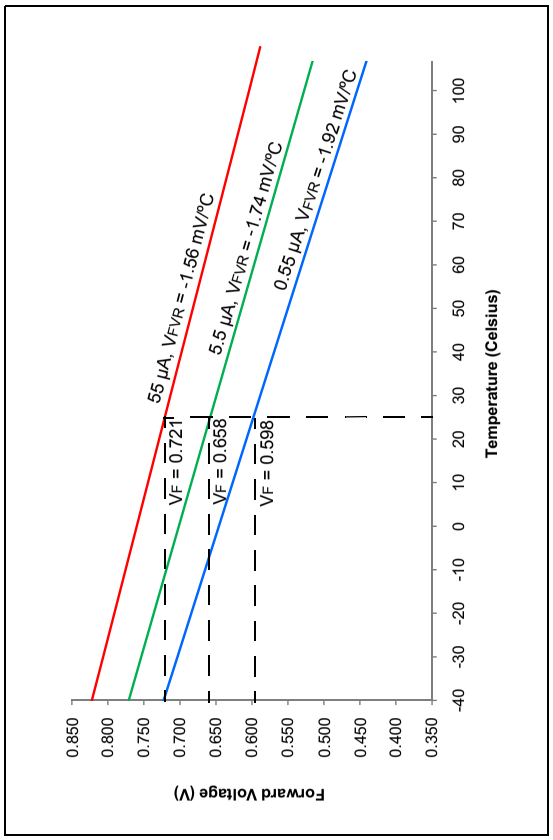
**FIGURE 33-5: TYPICAL CTMU TEMPERATURE DIODE FORWARD VOLTAGE**





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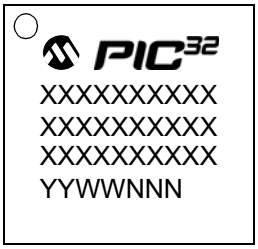
## 34.0 PACKAGING INFORMATION

### 34.1 Package Marking Information

64-Lead TQFP (10x10x1 mm)

Example

64-Lead QFN (9x9x0.9 mm)




Example

100-Lead TQFP (14x14x1 mm)

Example

100-Lead TQFP (12x12x1 mm)

Example

| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

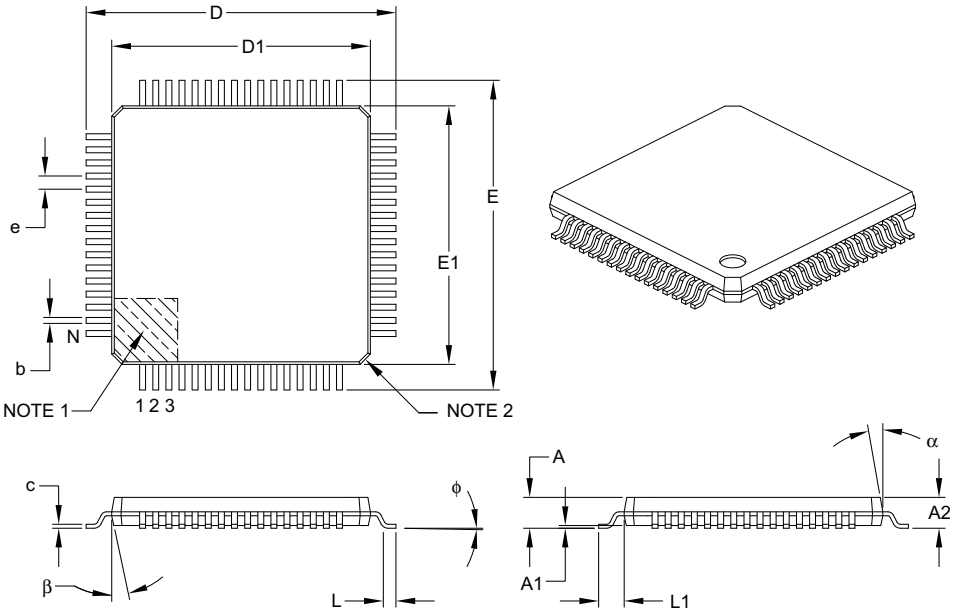
**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## 34.2 Package Details

The following sections give the technical details of the packages.

### 64-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 64 | |
| Lead Pitch | e | | 0.50 BSC | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | ϕ | 0° | 3.5° | 7° |
| Overall Width | E | | 12.00 BSC | |
| Overall Length | D | | 12.00 BSC | |
| Molded Package Width | E1 | | 10.00 BSC | |
| Molded Package Length | D1 | | 10.00 BSC | |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.17 | 0.22 | 0.27 |
| Mold Draft Angle Top | α | 11° | 12° | 13° |
| Mold Draft Angle Bottom | β | 11° | 12° | 13° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085B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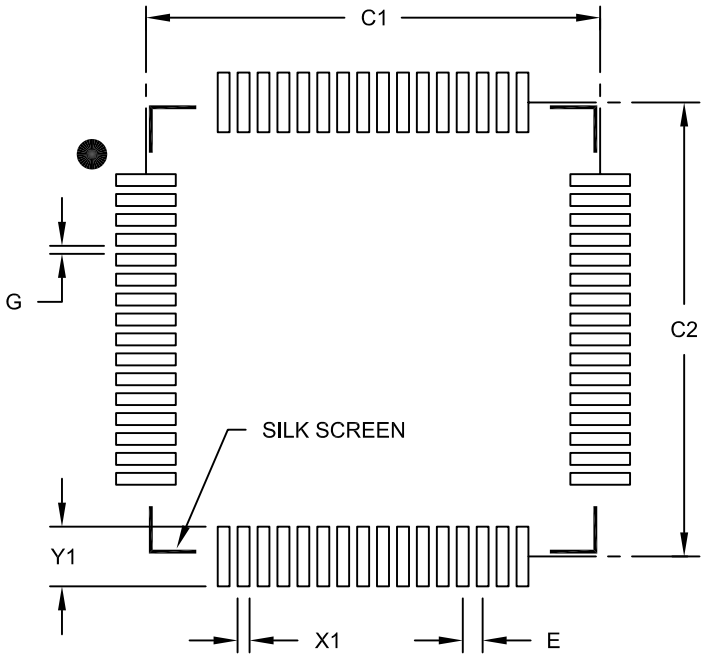
64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Contact Pad Spacing | C1 | | 11.40 | |
| Contact Pad Spacing | C2 | | 11.40 | |
| Contact Pad Width (X64) | X1 | | | 0.30 |
| Contact Pad Length (X64) | Y1 | | | 1.50 |
| Distance Between Pads | G | 0.20 | | |

Notes:

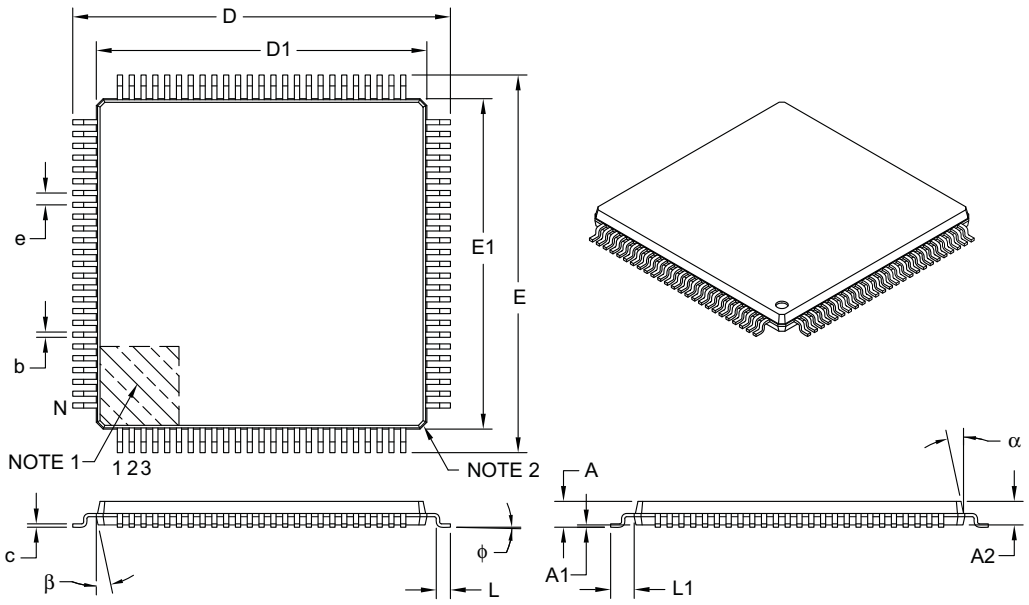
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085B

### 100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 100 | |
| Lead Pitch | e | | 0.50 BSC | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | ϕ | 0° | 3.5° | 7° |
| Overall Width | E | | 16.00 BSC | |
| Overall Length | D | | 16.00 BSC | |
| Molded Package Width | E1 | | 14.00 BSC | |
| Molded Package Length | D1 | | 14.00 BSC | |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.17 | 0.22 | 0.27 |
| Mold Draft Angle Top | α | 11° | 12° | 13° |
| Mold Draft Angle Bottom | β | 11° | 12° | 13° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-110B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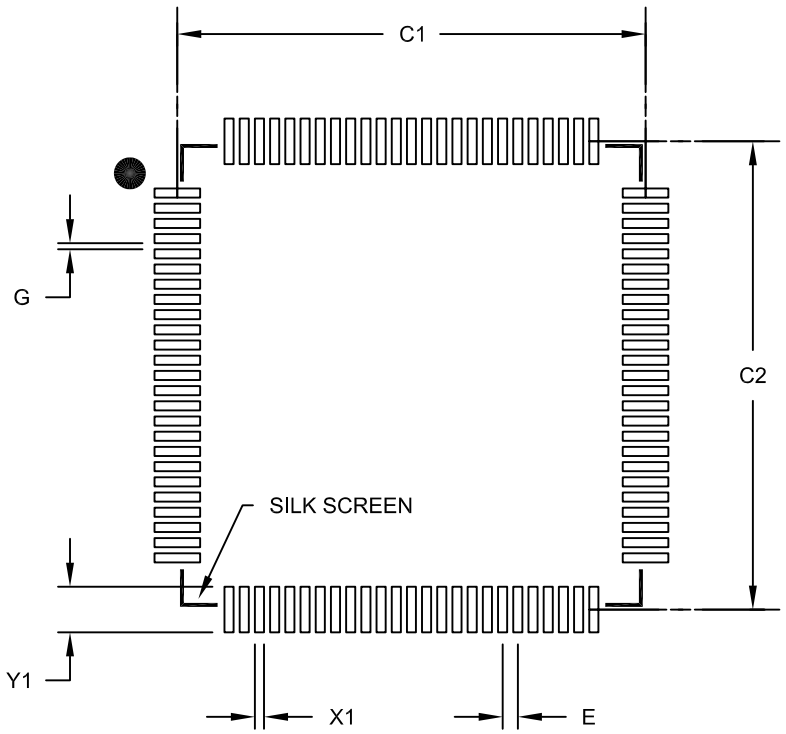
100-Lead Plastic Thin Quad Flatpack (PF) - 14x14x1 mm Body 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Contact Pad Spacing | C1 | | 15.40 | |
| Contact Pad Spacing | C2 | | 15.40 | |
| Contact Pad Width (X100) | X1 | | | 0.30 |
| Contact Pad Length (X100) | Y1 | | | 1.50 |
| Distance Between Pads | G | 0.20 | | |

Notes:

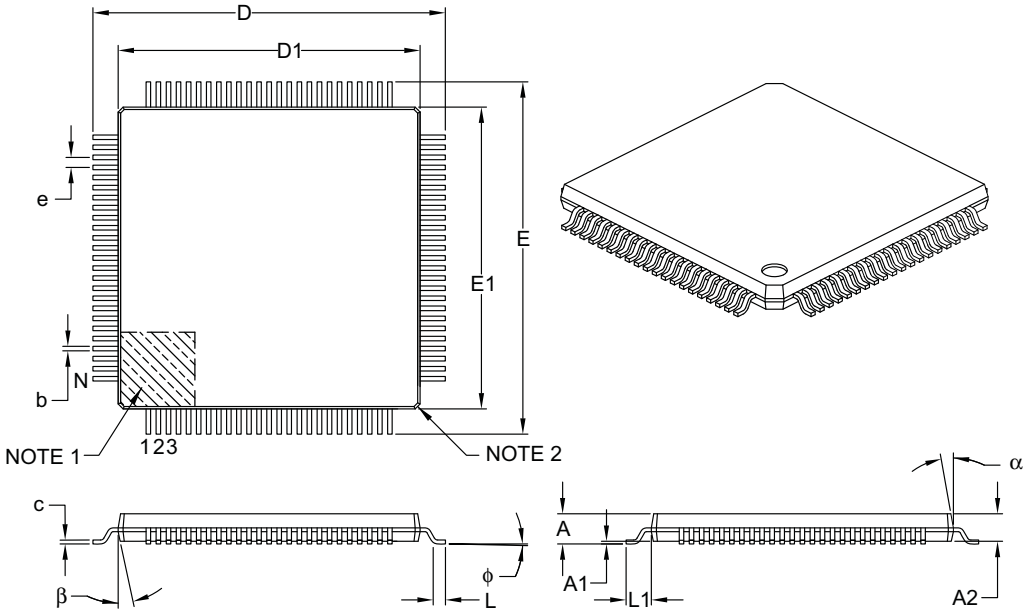
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2110B

### 100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 100 | |
| Lead Pitch | e | | 0.40 BSC | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | ϕ | 0° | 3.5° | 7° |
| Overall Width | E | | 14.00 BSC | |
| Overall Length | D | | 14.00 BSC | |
| Molded Package Width | E1 | | 12.00 BSC | |
| Molded Package Length | D1 | | 12.00 BSC | |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.13 | 0.18 | 0.23 |
| Mold Draft Angle Top | α | 11° | 12° | 13° |
| Mold Draft Angle Bottom | β | 11° | 12° | 13° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B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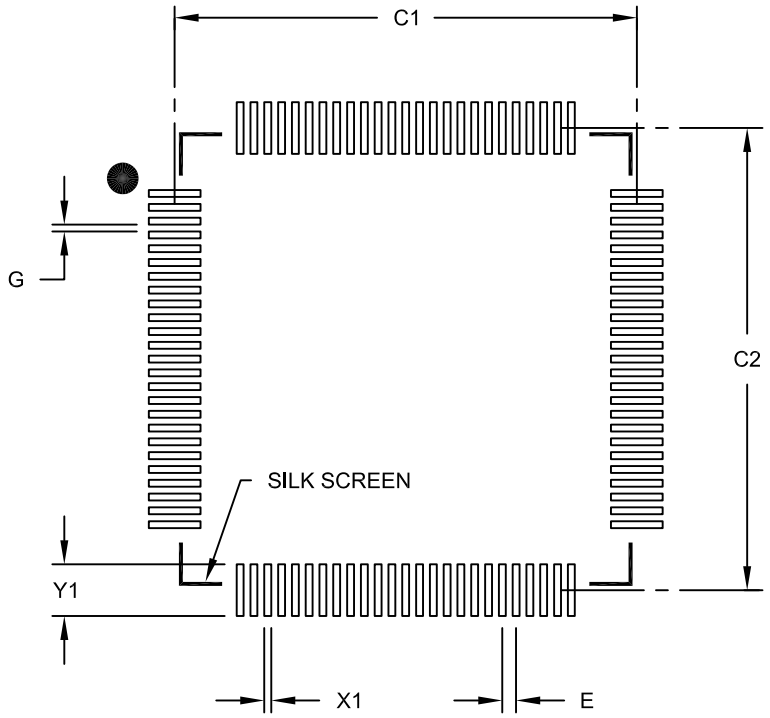
100-Lead Plastic Thin Quad Flatpack (PT)-12x12x1mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.40 BSC | |
| Contact Pad Spacing | C1 | | 13.40 | |
| Contact Pad Spacing | C2 | | 13.40 | |
| Contact Pad Width (X100) | X1 | | | 0.20 |
| Contact Pad Length (X100) | Y1 | | | 1.50 |
| Distance Between Pads | G | 0.20 | | |

Notes:

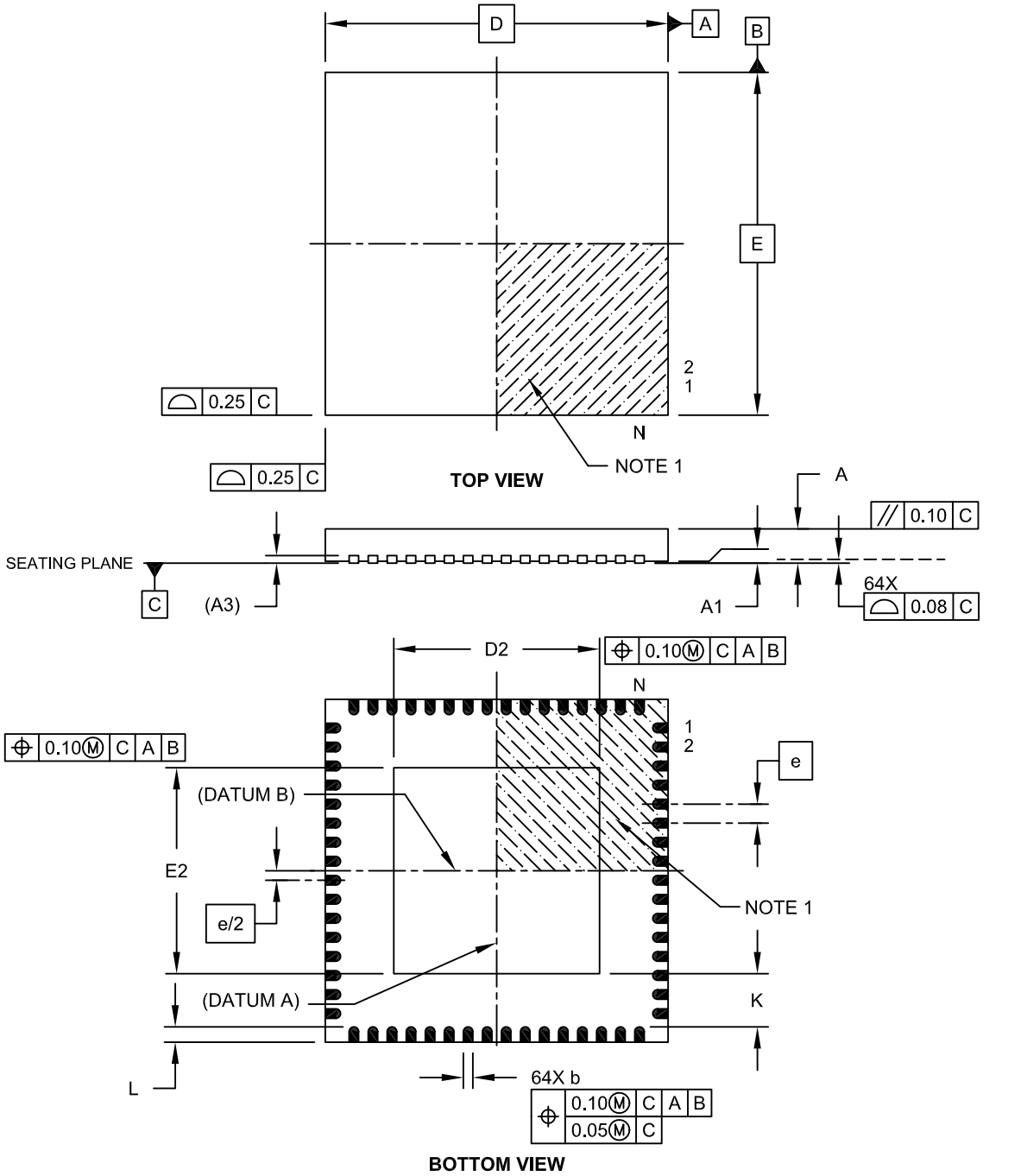
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2100B

**64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-154A Sheet 1 of 2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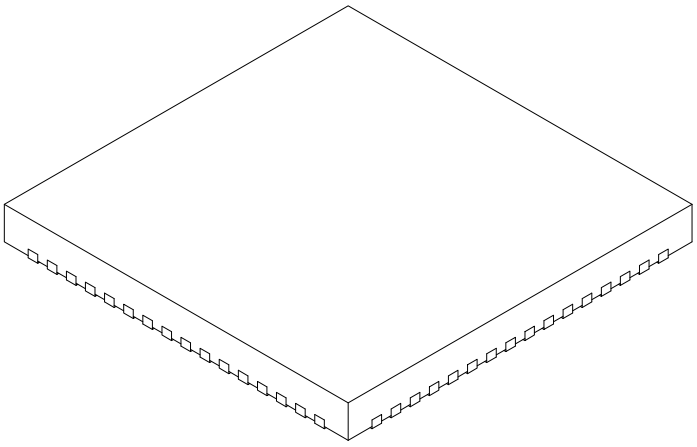
**64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 64 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 9.00 BSC | |
| Exposed Pad Width | E2 | 5.30 | 5.40 | 5.50 |
| Overall Length | D | | 9.00 BSC | |
| Exposed Pad Length | D2 | 5.30 | 5.40 | 5.50 |
| Contact Width | b | 0.20 | 0.25 | 0.30 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

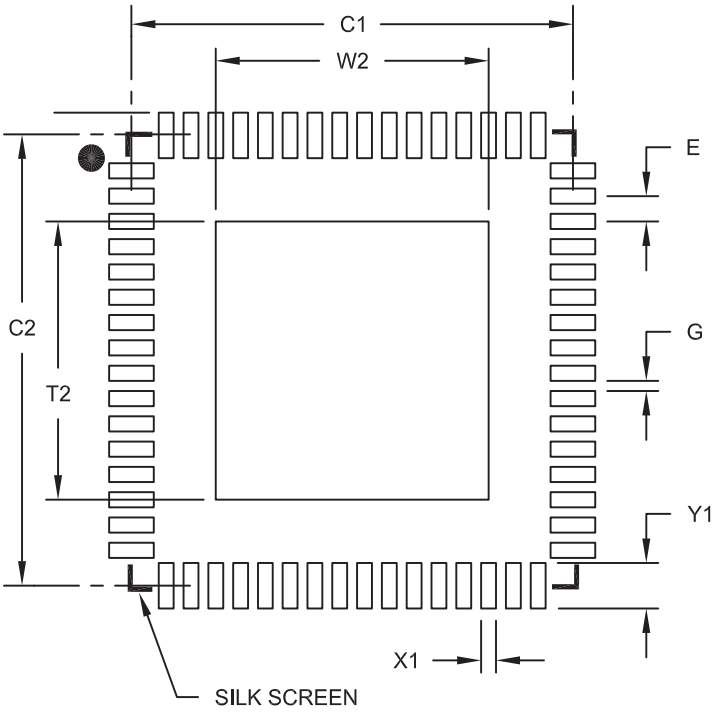
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-154A Sheet 2 of 2

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length and 5.40x5.40mm Exposed Pad

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.50 BSC | | |
| Optional Center Pad Width | W2 | | | 5.50 |
| Optional Center Pad Length | T2 | | | 5.50 |
| Contact Pad Spacing | C1 | | 8.90 | |
| Contact Pad Spacing | C2 | | 8.90 | |
| Contact Pad Width (X64) | X1 | | | 0.30 |
| Contact Pad Length (X64) | Y1 | | | 0.85 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2154A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# APPENDIX A: REVISION HISTORY

## Revision A (July 2014)

This is the initial released version of the document.

## Revision B (September 2014)

This revision includes the following major changes, which are referenced by their respective chapter in Table A-1.

In addition, minor updates to text and formatting were incorporated throughout the document.

**TABLE A-1: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **1.0 "Device Overview"** | Added the USBOEN pin to the Pinout I/O Descriptions (see Table 1-1). |
| **2.0 "Guidelines for Getting Started with 32-bit MCUs"** | Updated the Primary Oscillator loading capacitor calculations (see **2.8.1 "Crystal Oscillator Design Consideration"**).<br>Added **2.11 "Considerations When Interfacing to Remotely Powered Circuits"** |
| **10.0 "USB On-The-Go (OTG)"** | Updated the UOEMON bit definitions (see Register 10-20). |
| **31.0 "40 MHz Electrical Characteristics"** | Updated DC Characteristics I/O Pin Input Specification parameters DI30 and DI31 (see Table 31-8). |

## Revision C (November 2014)

This revision includes the following major changes, which are referenced by their respective chapter in Table A-2.

In addition, minor updates to text and formatting were incorporated throughout the document.

**TABLE A-2: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **20.0 "Parallel Master Port (PMP)"** | Added the RDSTART bit to the Parallel Port Control Register (see Table 20-1 and Register 20-1). |
| **31.0 "40 MHz Electrical Characteristics"** | Updated the $I_{DD}$ Operating Current DC Characteristics (see Table 31-5).<br>Updated the $I_{IDLE}$ Idle Current DC Characteristics (see Table 31-6).<br>Updated the $I_{PD}$ Power Down Current DC Characteristics (see Table 31-7).<br>Updated the Internal FRC Accuracy (see Table 31-19). |
| **32.0 "50 MHz Electrical Characteristics"** | Updated the $I_{DD}$ Operating Current DC Characteristics (see Table 32-2).<br>Updated the $I_{IDLE}$ Idle Current DC Characteristics (see Table 32-3).<br>Updated the $I_{PD}$ Power Down Current DC Characteristics (see Table 32-4). |

## Revision D (April 2016)

This revision includes the following major changes, which are referenced by their respective chapter in Table A-2.

**TABLE A-3: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **1.0 "Device Overview"** | Removed the USBOEN pin and all trace-related pins from the Pinout I/O Descriptions (see Table 1-1). |
| **2.0 "Guidelines for Getting Started with 32-bit MCUs"** | **Section 2.7 "Trace"** was removed.<br>**Section 2.10 "Sosc Design Recommendation"** was removed. |
| **3.0 "CPU"** | References to the Shadow Register Set (SRS), which is not supported by PIC32MX1XX/2XX/5XX 64/100-pin Family devices, were removed from **3.1 "Features"**, **3.2.1 "Execution Unit"**, and Coprocessor 0 Registers (Table 3-2). |
| **4.0 "Memory Organization"** | The SFR Memory Map was added (see Table 4-1). |
| **5.0 "Interrupt Controller"** | The Single Vector Shadow Register Set (SSO) bit (INTCON<16>) was removed (see Register 5-1). |
| **10.0 "USB On-The-Go (OTG)"** | The UOEMON bit (U1CNFG1<6>) was removed (see Register 10-20). |
| **23.0 "Controller Area Network (CAN)"** | The CAN features (number of messages and FIFOs) were updated.<br>The PIC32 CAN Block Diagram was updated (see Figure 23-1).<br>The following registers were updated:<br>• C1FSTAT (see Register 23-6)<br>• C1RXOVF (see Register 23-7)<br>• C1RXFn (see Register 23-14)<br>• C1FIFOCONn (see Register 23-16)<br>• C1FIFOINTn (see Register 23-17)<br>• C1FIFOUAn (see Register 23-18)<br>• C1FIFOCIn (see Register 23-19)<br>The C1FLTCON4 through C1FLTCON7 registers were removed. |
| **28.0 "Special Features"** | The virtual addresses for the Device Configuration Word registers were updated (see Table 28-1). |
| **31.0 "40 MHz Electrical Characteristics"** | The EJTAG Timing Characteristics diagram was updated (see Figure 31-23). |


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### Revision E (October 2017)

In this revision, the Preliminary status was removed.

**NOTES:**


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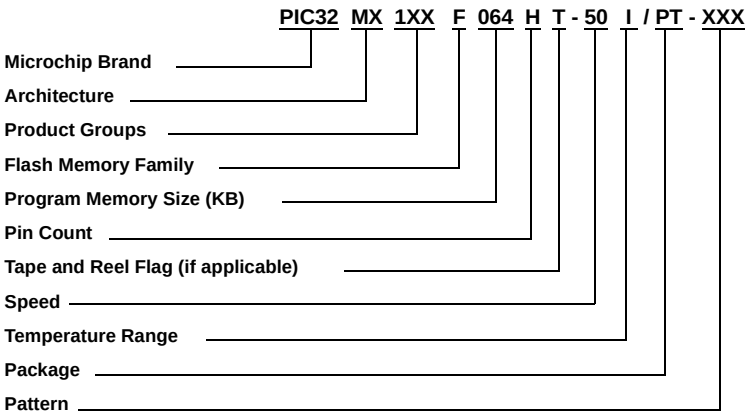


**Example:**

PIC32MX170F512H-50I/PT:
General Purpose PIC32, 32-bit RISC MCU,
512 KB program memory,
64-pin, Industrial temperature,
TQFP package.

**Flash Memory Family**

| | |
|---|---|
| Architecture | MX = 32-bit RISC MCU core |
| Product Groups | 1XX = General Purpose microcontroller family<br>2XX = USB microcontroller family<br>5XX = USB and CAN microcontroller family |
| Flash Memory Family | F = Flash program memory |
| Program Memory Size | 064 = 64 KB<br>128 = 128 KB<br>256 = 256 KB<br>512 = 512 KB |
| Pin Count | H = 64-pin<br>L = 100-pin |
| Speed | = 40 MHz (blank, no marking on package)<br>50 = 50 MHz |
| Temperature Range | I = -40°C to +85°C (Industrial)<br>V = -40°C to +105°C (V-Temp) |
| Package | PT = 64-Lead (10x10x1 mm) TQFP (Thin Quad Flatpack)<br>PT = 100-Lead (12x12x1 mm) TQFP (Thin Quad Flatpack)<br>PF = 100-Lead (14x14x1 mm) TQFP (Thin Quad Flatpack)<br>MR = 64-Lead (9x9x0.9 mm) QFN (Plastic Quad Flat) |
| Pattern | Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise)<br>ES = Engineering Sample |

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