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FDG6332C

20V N & P-Channel PowerTrench® MOSFETs

General Description

The N & P-Channel MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive TSSOP-8 and SSOP-6 packages are impractical.

Applications

- DC/DC converter
- Load switch
- · LCD display inverter

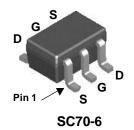
Features

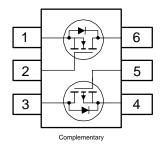
• Q1 0.7 A, 20V. $R_{DS(ON)} = 300 \ m\Omega \ @ \ V_{GS} = 4.5 \ V$

 $R_{DS(ON)}$ = 400 m Ω @ V_{GS} = 2.5 V

• Q2 -0.6 A, -20V. $R_{DS(ON)} = 420$ m Ω @ $V_{GS} = -4.5$ V $R_{DS(ON)} = 630$ m Ω @ $V_{GS} = -2.5$ V

- Low gate charge
- High performance trench technology for extremely low R_{DS(ON)}
- SC70-6 package: small footprint (51% smaller than SSOT-6); low profile (1mm thick)





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Q1	Q2	Units	
V_{DSS}	Drain-Source Voltage	20	-20	V	
V _{GSS}	Gate-Source Voltage	±12	±12	V	
I _D	Drain Current — Continuous (Note 1)		0.7	-0.6	Α
	- Pulsed		2.1	-2	
P _D	Power Dissipation for Single Operation	0	W		
T _J , T _{STG}	Operating and Storage Junction Temperature Range -55 to +150				°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1)	415	°C/W
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Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.32 FDG6332C		7"	8mm	3000 units

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units		
Off Char	acteristics				I.		I.	I.
BV _{DSS}	Drain-Source Breakdown Volta	ge	$V_{GS} = 0 \text{ V}, \qquad I_D = 250 \mu\text{A} \ V_{GS} = 0 \text{ V}, \qquad I_D = -250 \mu\text{A}$	Q1 Q2	20 -20			V
<u>ΔBV_{DSS}</u> ΔT _J	Breakdown Voltage Temperatur Coefficient	re	$I_D = 250 \mu\text{A}, \text{Ref. to } 25^{\circ}\text{C}$ $I_D = -250 \mu\text{A}, \text{Ref. to } 25^{\circ}\text{C}$		14 –14		mV/°C	
I _{DSS}	Zero Gate Voltage Drain Currer	nt	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V} $ Q1 $V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$ Q2				1 –1	μΑ
I _{GSSF} /I _{GSSR}	Gate-Body Leakage, Forward		$V_{GS} = \pm 12 \text{ V}, V_{DS} = 0 \text{ V}$				±100	nA
I _{GSSF} /I _{GSSR}	Gate–Body Leakage, Reverse		$V_{GS} = \pm 12V$, $V_{DS} = 0 V$				±100	nA
On Char	acteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage Q1		$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	0.6	1.1	1.5	V	
,	_	Q2	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$		-0.6	-1.2	-1.5	
$\Delta V_{GS(th)}$	Gate Threshold Voltage	Q1	I _D = 250 μA,Ref. To 25°C			-2.8		mV/°C
ΔT_J	Temperature Coefficient	Q2	$I_D = -250 \mu\text{A}, \text{Ref. to } 25^{\circ}\text{C}$			3		, \
R _{DS(on)}	Static Drain-Source	Q1	$V_{GS} = 4.5 \text{ V}, I_D = 0.7 \text{ A}$			180	300	mΩ
	On–Resistance		$V_{GS} = 2.5 \text{ V}, I_{D} = 0.6 \text{ A}$	-		293	400	
			$V_{GS} = 4.5 \text{ V}, I_D = 0.7 \text{A}, T_J = 12$	25°C		247	442	
		Q2	$V_{GS} = -4.5 \text{ V}, I_D = -0.6 \text{ A}$			300	420	
			$V_{GS} = -2.5 \text{ V}, I_D = -0.5 \text{ A}$ $V_{GS} = -4.5 \text{ V}, I_D = -0.6 \text{ A}, T_J = 1$	25°€		470 400	630 700	
~	Famurand Transport division as		$V_{DS} = 5 \text{ V}$ $I_D = 0.7 \text{ A}$		1	700		
g fs	Forward Transconductance	Q1				2.8		S
	Q		$V_{DS} = -5 \text{ V}$ $I_{D} = -0.6 \text{A}$		1.8			
I _{D(on)}	On–State Drain Current	Q1	$V_{GS} = 4.5 \text{ V}, V_{DS} = 5 \text{ V}$		1			Α
		Q2	$V_{GS} = -4.5 \text{ V}, \ V_{DS} = -5 \text{ V}$		-2			
Dynamic	: Characteristics							
C _{iss} Input Capacitance		Q1	V _{DS} =10 V, V _{GS} = 0 V, f=1.0M	Hz		113		pF
100		Q2	V _{DS} =-10 V, V _{GS} = 0 V, f=1.0			114		'
Coss	Output Capacitance		V _{DS} =10 V, V _{GS} = 0 V, f=1.0M		34		pF	
-033		Q1 Q2	V _{DS} =-10 V, V _{GS} = 0 V, f=1.0			24		Ρ.
C _{rss}	Reverse Transfer Capacitance	Q1	$V_{DS}=10 \text{ V}, V_{GS}=0 \text{ V}, f=1.0\text{M}$		16		pF	
Orss	Neverse Transfer Capacitance	Q2	V_{DS} =-10 V, V $_{GS}$ = 0 V, f=1.0N		9		pΓ	
		Q2	VDS- 10 V, V GS- 0 V, I-1.01	VII IZ		9		
Switchin	g Characteristics (Note 2)	1	1		П	1	П	
$t_{d(on)}$	Turn-On Delay Time	Q1	For Q1 :			5	10	ns
		Q2	$V_{DS} = 10 \text{ V}, I_{D} = 1 \text{ A}$			5.5	11	
t _r	Turn-On Rise Time	Q1	V_{GS} = 4.5 V, R_{GEN} = 6 Ω			7	15	ns
		Q2	For Q2 :			14	25	
$t_{d(off)}$	Turn-Off Delay Time	Q1	$V_{DS} = -10 \text{ V}, I_{D} = -1 \text{ A}$			9	18	ns
		Q2	V_{GS} = -4.5 V, R_{GEN} = 6 Ω			6	12	
t _f	Turn-Off Fall Time	Q1	_			1.5	3	ns
		Q2				1.7	3.4	
Q_g	Total Gate Charge	Q1	For Q1 :			1.1	1.5	nC
		Q2	$V_{DS} = 10 \text{ V}, I_{D} = 0.7 \text{ A}$			1.4	2	
Q_{gs}	Gate-Source Charge	Q1	$V_{GS} = 4.5 \text{ V}, R_{GEN} = 6 \Omega$			0.24		nC
		Q2	For Q2 : V _{DS} =-10 V, I _D = -0.6 A			0.3		
Q_{gd}	Gate-Drain Charge	Q1	$V_{GS} = -4.5 \text{ V}, R_{GEN} = 6 \Omega$			0.3		nC
		Q2	. 32			0.4		

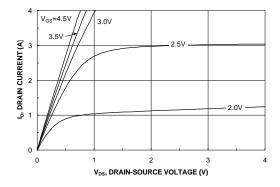
Electrical Characteristics T_A = 25°C unless otherwise noted **Symbol Parameter Test Conditions** Min Тур Max Units **Drain-Source Diode Characteristics and Maximum Ratings** Maximum Continuous Drain-Source Diode Forward Current Q1 0.25 Α I_S Q2 -0.25 $V_{GS} = 0 \text{ V}, I_{S} = 0.25 \text{ A}$ $V_{\text{SD}} \\$ Drain-Source Diode Forward (Note 2) 0.74 1.2 $V_{GS} = 0 \text{ V}, I_{S} = -0.25 \text{ A}$ (Note 2) -0.77 -1.2

Notes:

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

^{1.} R_{0JA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{0JC} is guaranteed by design while R_{0JA} is determined by the user's board design. R_{0JA} = 415°C/W when mounted on a minimum pad of FR-4 PCB in a still air environment.

Typical Characteristics: N-Channel



NORMALIZED

NORMALIZED

NOS = 2.5V

NOS = 2.5V

NOS = 2.5V

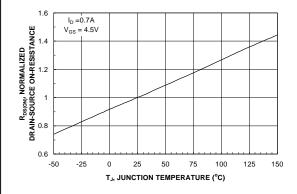
NOS = 2.5V

A.5V

1.8

Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.



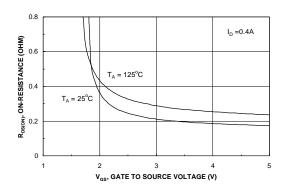
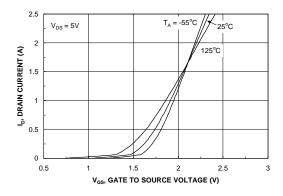


Figure 3. On-Resistance Variation with Temperature.

Figure 4. On-Resistance Variation with Gate-to-Source Voltage.



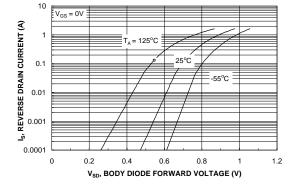
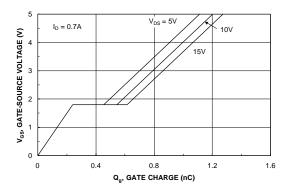


Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: N-Channel



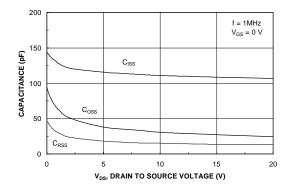
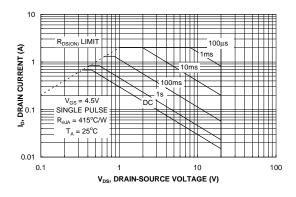


Figure 7. Gate Charge Characteristics.

Figure 8. Capacitance Characteristics.



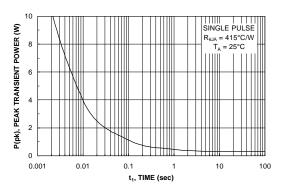


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: P-Channel

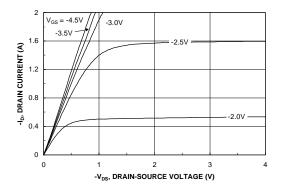


Figure 11. On-Region Characteristics.

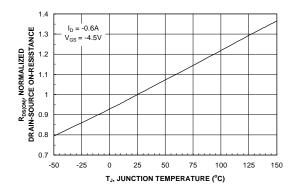


Figure 13. On-Resistance Variation with Temperature.

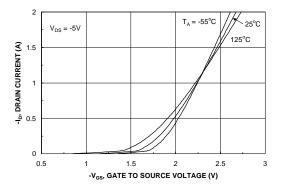


Figure 15. Transfer Characteristics.

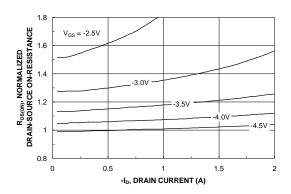


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

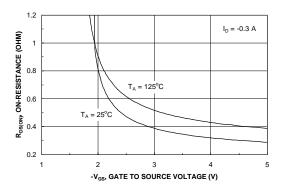


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

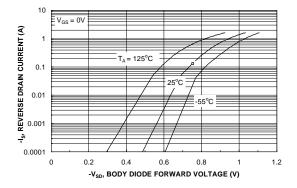
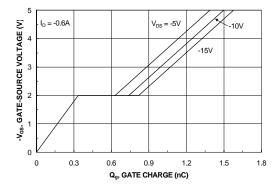


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: P-Channel



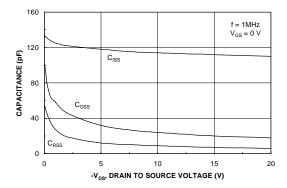


Figure 17. Gate Charge Characteristics.

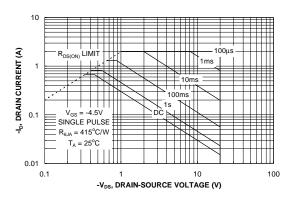


Figure 18. Capacitance Characteristics.

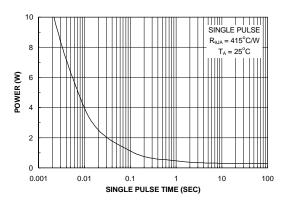


Figure 19. Maximum Safe Operating Area.



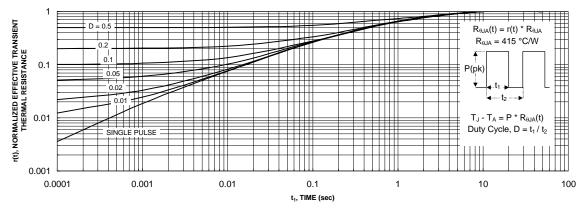


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1. Transient thermal response will change depending on the circuit board design.





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Deminition of Terms		
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