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February 2007

# FDB8447L 40V N-Channel PowerTrench MOSFET 40V, 50A, $8.5 m\Omega$

### **Features**

- Max  $r_{DS(on)}$  = 8.5m $\Omega$  at  $V_{GS}$  = 10V,  $I_D$  = 14A
- Max  $r_{DS(on)}$  = 11m $\Omega$  at  $V_{GS}$  = 4.5V,  $I_D$  = 11A
- Fast Switching
- RoHS Compliant

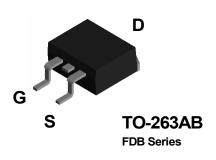


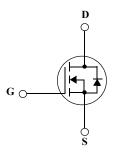
### **General Description**

This N-Channel MOSFET has been produced using Fairchild Semiconductor's proprietary PowerTrench<sup>®</sup> technology to deliver low  $r_{DS(on)}$  and optimized BV<sub>DSS</sub> capability to offer superior performance benefit in the application.

### **Application**

- Inverter
- Power Supplies





### MOSFET Maximum Ratings $T_C = 25$ °C unless otherwise noted

Symbol	Parameter			Ratings	Units
$V_{DS}$	Drain to Source Voltage			40	V
$V_{GS}$	Gate to Source Voltage			±20	V
	Drain Current -Continuous (Package limited)	T <sub>C</sub> = 25°C		50	
	-Continuous (Silicon limited)	T <sub>C</sub> = 25°C	(Note 1)	66	٨
'D	-Continuous	T <sub>A</sub> = 25°C	(Note 1a)	15	Α
	-Pulsed			100	
E <sub>AS</sub>	Drain-Source Avalanche Energy		(Note 3)	153	mJ
В	Power Dissipation	T <sub>C</sub> = 25°C		60	W
$P_{D}$	Power Dissipation		(Note 1a)	3.1	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	ge		-55 to +150	°C

### **Thermal Characteristics**

$R_{\thetaJC}$	Thermal Resistance, Junction to Case	(Note 1)	2.1	°C/W
R <sub>e.IA</sub>	Thermal Resistance, Junction to Ambient	(Note 1a)	40	C/VV

### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB8447L	FDB8447L	TO-263AB	330mm	24mm	800 units

### **Electrical Characteristics** $T_J = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, referenced to 25°C		35		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 32V, V_{GS} = 0V$			1	μΑ
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20V, V_{GS} = 0V$			±100	nA

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		-5		mV/°C
		V <sub>GS</sub> = 10V, I <sub>D</sub> = 14A		7.4	8.5	
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 4.5V, I_D = 11A$		8.7	11.0	mΩ
	V <sub>GS</sub> = 10V, I <sub>D</sub> = 14A, T <sub>J</sub> =125°C		10.8	12.4		
$g_{FS}$	Forward Transconductance	V <sub>DS</sub> = 5V, I <sub>D</sub> = 14A		58		S

### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V = 20V V = 0V	1970	2620	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 20V, V_{GS} = 0V,$ f = 1MHz	250	335	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 111112	150	225	pF
$R_a$	Gate Resistance	f = 1MHz	1.0		Ω

### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time			11	20	ns
t <sub>r</sub>	Rise Time	$V_{DD} = 20V, I_{D} = 14A$ $V_{GS} = 10V, R_{GEN} = 6\Omega$		6	12	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			28	45	ns
t <sub>f</sub>	Fall Time			4	10	ns
$Q_{g(TOT)}$	Total Gate Charge, V <sub>GS</sub> = 10V			37	52	nC
$Q_{g(TOT)}$	Total Gate Charge, V <sub>GS</sub> = 5V	V <sub>DD</sub> =20V, I <sub>D</sub> = 14A V <sub>GS</sub> = 10V		20	28	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	V <sub>GS</sub> = 10V		6		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			7		nC

### **Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 14A (Note 2)		8.0	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 14A, di/dt = 100A/μs		28	42	ns
Q <sub>rr</sub>	Reverse Recovery Charge			24	36	nC

Re<sub>0.0.C</sub> is guaranteed by design while R<sub>0.0.C</sub> is determined by the user's board design.

a. 40°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper

b. 62.5°C/W when mounted on a minimum pad.

<sup>2:</sup> Pulse Test: Pulse Width < 300 $\mu$ s, Duty cycle < 2.0%. 3: Starting T<sub>J</sub> = 25°C, L = 1mH, I<sub>AS</sub> = 17.5A, V<sub>DD</sub> = 40V, V<sub>GS</sub> = 10V.

### Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

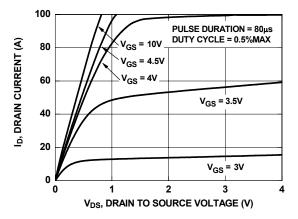


Figure 1. On Region Characteristics

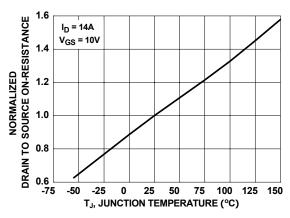


Figure 3. Normalized On Resistance vs Junction Temperature

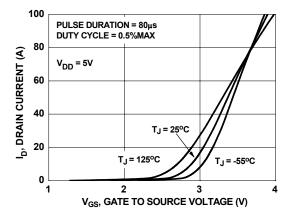


Figure 5. Transfer Characteristics

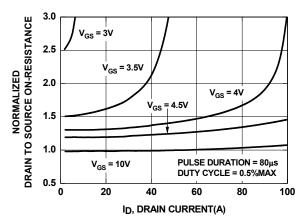


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

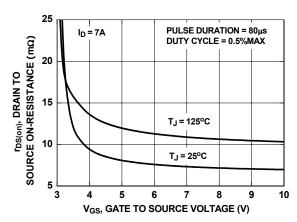


Figure 4. On-Resistance vs Gate to Source Voltage

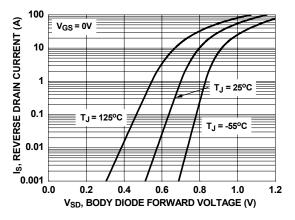


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

### **Typical Characteristics** $T_J = 25^{\circ}C$ unless otherwise noted

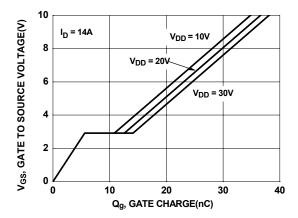


Figure 7. Gate Charge Characteristics

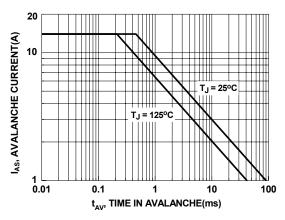


Figure 9. Unclamped Inductive Switching Capability

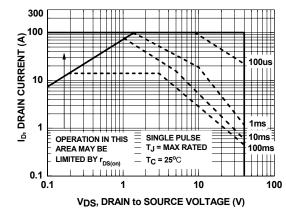


Figure 11. Forward Bias Safe Operating Area

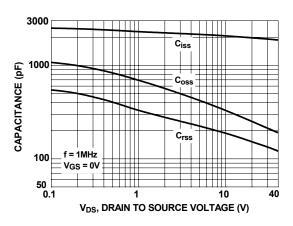


Figure 8. Capacitance vs Drain to Source Voltage

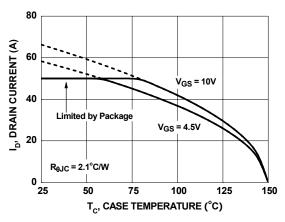


Figure 10. Maximum Continuous Drain Current vs Case Temperature

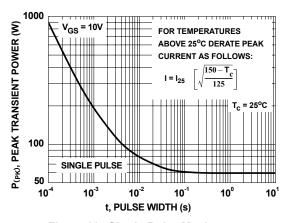


Figure 12. Single Pulse Maximum Power Dissipation

### Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

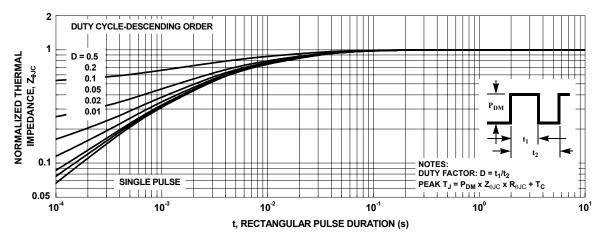


Figure 13. Transient Thermal Response Curve





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