

# TPS40305EVM-488

The TPS40305EVM-488 evaluation module (EVM) is a synchronous buck converter providing a fixed 1.8-V output at up to 10A from a 12-V input bus. The EVM is designed to start-up from a single supply; so, no additional bias voltage is required for start-up. The module uses the TPS40305 high performance, mid-input voltage synchronous buck controller and TI's NexFET™ high performance MOSFETs.

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## 1 Description

The TPS40305EVM-488 is designed to use a regulated 12-V (8V – 14V) bus voltage to provide a regulated 1.8-V output at up to 10A of load current. The TPS40305EVM-488 is designed to demonstrate the TPS40305 controller and TI NexFETs in a typical 12-V bus to low-voltage application while providing a number of non-invasive test points to evaluate the performance of the TPS40305 and TI NexFETs in a given application.

### 1.1 Applications

- High-current, low-voltage FPGA or microcontroller core supplies
- High-current point of load modules
- Telecommunications equipment
- Computer peripherals

### 1.2 Features

- 8-V to 14-V input voltage rating
- 1.8-V  $\pm$  2% output voltage rating
- 10-A steady state load current
- 1.2-MHz switching frequency
- Simple access to IC features including Power Good, Enable, Soft-Start and Error Amplifier
- Convenient test points for simple, non-invasive measurements of converter performance

## 2 TPS40305EVM-488 Electrical Performance Specifications

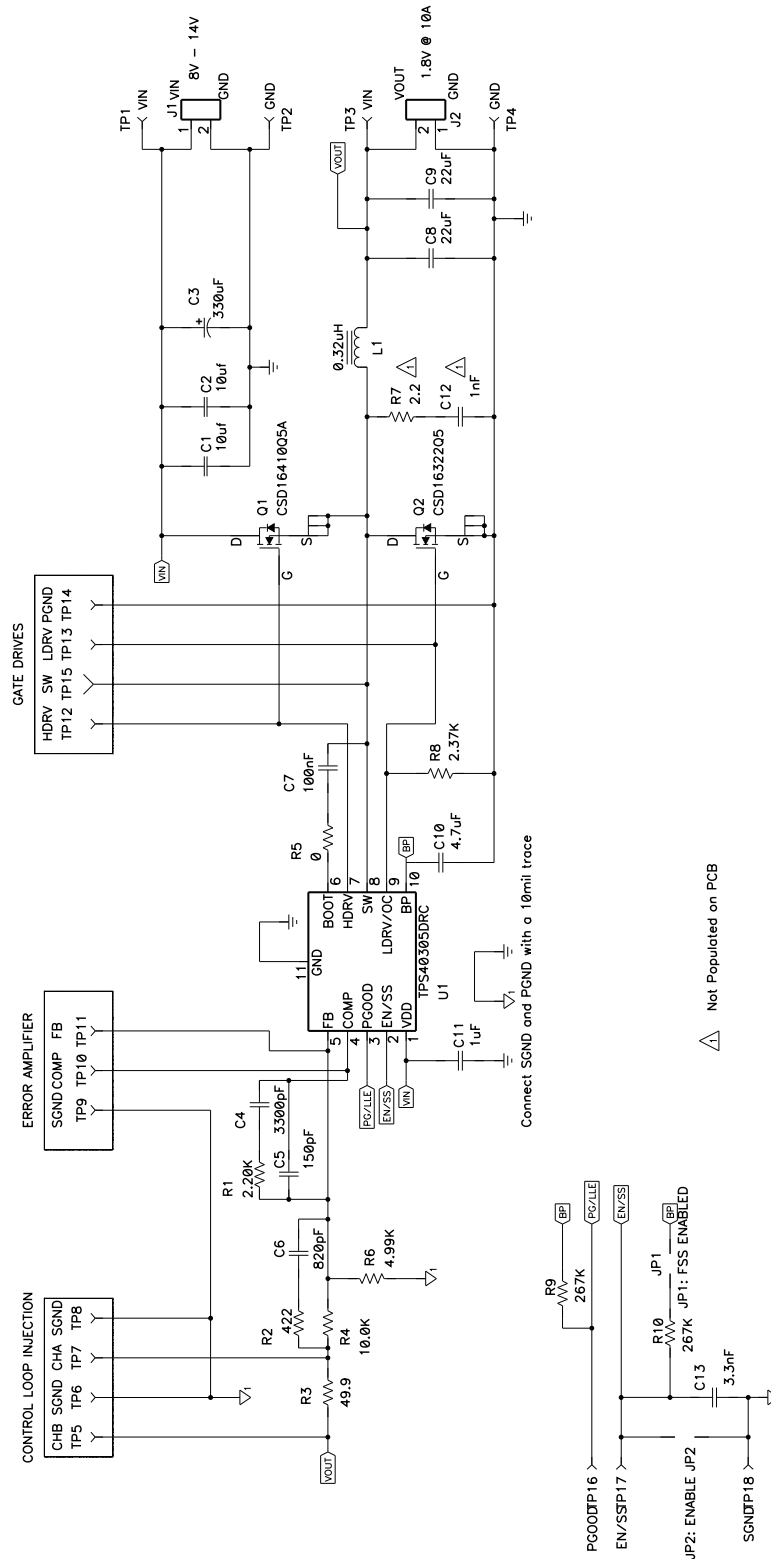
**Table 1. TPS40305EVM-488 Electrical and Performance Specifications**

Parameter		Notes and Conditions	Min	Typ	Max	Unit
<b>Inputs Characteristics</b>						
$V_{IN}$	Input voltage		8	12	14	V
$I_{IN}$	Input current	$V_{IN} = 12V, I_{OUT} = 10A$	–	1.7	2.00	A
	No load input current	$V_{IN} = 12V, I_{OUT} = 0A$	–	47	60	mA
$V_{IN\_UVLO}$	Input UVLO	$I_{OUT} = 10A$		3.0		V
<b>Outputs Characteristics</b>						
$V_{OUT1}$	Output voltage 1	$V_{IN} = 12V, I_{OUT} = 10A$	1.76	1.8	1.84	V
	Line regulation	$V_{IN} = 8V \text{ to } 14V$	–	–	0.5%	
	Load regulation	$I_{OUT} = 0A \text{ to } 10A$	–	–	0.5%	
$V_{OUT\_ripple}$	Output voltage ripple	$V_{IN} = 12V, I_{OUT} = 10A$	–	–	24	mVpp
$I_{OUT1}$	Output current 1	$V_{IN} = 8V \text{ to } 14V$	0		10	A
<b>Systems Characteristics</b>						
$F_{SW}$	Switching frequency		1000	1200	1400	kHz

**Table 1. TPS40305EVM-488 Electrical and Performance Specifications (continued)**

Parameter		Notes and Conditions	Min	Typ	Max	Unit
$\eta_{pk}$	Peak efficiency	$V_{IN} = 12V$	–	88%	–	
$\eta$	Full load efficiency	$V_{IN} = 12V, I_{OUT} = 10A$	–	86%	–	

3 TPS40305EVM-488 Schematic



For reference only, See Section 8 for specific values

Figure 1. TPS40305EVM-488 Schematic

## 4 Connector and Test Point Descriptions

### 4.1 Enable Jumper (JP2)

The TPS40305EVM-488 is designed with a Disable Jumper (JP2) using a 0.1" spacing header and shunt. Installing a shunt in the JP2 position connects the EN/SS pin to GND, discharges the soft-start capacitor, and disables the TPS40305 controller. This forces the output into a high-impedance state (approximately 15kΩ to GND).

### 4.2 Frequency Spread Spectrum – FSS Jumper (JP1)

The TPS40305EVM-488 is designed with a FSS Enable Jumper (JP1) using a 0.1" spacing header and shunt. Installing a shunt in the JP1 position connects the EN/SS pin to BP via a 267-kΩ resistor (R10) to enable Frequency Spread Spectrum.

Frequency Spread Spectrum modulates the switching frequency to  $\pm 10\%$  of the nominal value at 30kHz to reduce EMI at the switching frequency and its harmonics, however there may be a 30-kHz component to the output ripple (see [Figure 10](#)).

The TPS40305EVM-488 does not dynamically monitor the JP1 status for programming FSS. The TPS40305EVM-488 must be disabled via JP2 or powered down by reducing VIN to less than 3.0V to remove or install JP1.

### 4.3 Test Point Descriptions

**Table 2. Test Point Description**

Test Point	Label	Use	Section
TP1	VIN	Measurement test point for input voltage	4.3.1
TP2	GND	Ground test point for input voltage	4.3.1
TP3	VOUT	Measurement test point for output voltage	4.3.1
TP4	GND	Ground test point for output voltage	4.3.2
TP5	CHB	Measurement test point for channel B of loop response	4.3.3
TP6	SGND	Ground test point for channel B of loop response	4.3.3
TP7	CHA	Measurement test point for channel A of loop response	4.3.3
TP8	SGND	Ground test point for channel A of loop response	4.3.3
TP9	SGND	Ground test point for error amplifier measurements	4.3.4
TP10	COMP	Measurement test point for error amplifier output voltage	4.3.4
TP11	FB	Measurement test point for error amplifier input voltage	4.3.4
TP12	HDRV	Measurement test point for high-side gate driver voltage	4.3.5
TP13	LDRV	Measurement test point for low-side gate driver voltage	4.3.5
TP14	PGND	Ground test point for switch node and gate drive voltages	4.3.5
TP15	SW	Measurement test point for switch node voltage	4.3.5
TP16	PGOOD	Measurement test point for power good	4.3.6
TP17	EN/SS	Measurement test point for enable / soft-start	4.3.7
TP18	SGND	Ground test point for power good and enable / soft-start	4.3.6 and 4.3.7

#### 4.3.1 Input Voltage Monitoring (TP1 and TP2)

The TPS40305EVM-488 provides two test points for measuring the input voltage applied to the module. This allows the user to measure the actual input module voltage without losses from input cables and connectors. All input voltage measurements should be made between TP1 and TP2. To use TP1 and TP2, connect a voltmeter positive input to TP1 and input terminal to TP2.

### 4.3.2 Output Voltage Monitoring (TP3 and TP4)

The TPS40305EVM-488 provides two test points for measuring the output voltage generated by the module. This allows the user to measure the actual module output voltage without losses from input cables and connectors. All input voltage measurements should be made between TP3 and TP4. To use TP3 and TP4, connect a voltmeter positive input to TP3 and negative input to TP4.

### 4.3.3 Loop Response Testing (TP5, TP6, TP7, TP8, and R3)

The TPS40305EVM-488 provides four test points (2 signal and 2 ground) for measuring the control loop frequency response. This allows the user to measure the actual module loop response without modifying the evaluation board. A transformer isolated signal up to 30mV can be injected between TP5 and TP7. The injected signal amplitude can be measured by the AC coupled amplitude at CHA (TP7) and the resulting output voltage deviation can be measured at CHB (TP5). See [Figure 4](#) for additional detail.

### 4.3.4 Error Amplifier Voltage Monitoring (TP9, TP10, and TP11)

The TPS40305EVM-488 provides three test points for measuring the error amplifier input and output voltages. This allows the user to directly measure the feedback and control voltages of the TPS40305 controller. The control voltage (TP10) can also be used to measure the Control to Output or Power Stage frequency response or Output to Control or Error Amplifier frequency response. See Section 5.5 for additional details.

### 4.3.5 Switching Waveform Monitoring (TP12, TP13, TP14, and TP15)

The TPS40305EVM-488 provides three test points and a local power ground for measuring the switching waveforms of the module power stage. This allows the user to monitor actual switching waveforms during operation. TP15 is a 0.040" square pad of exposed PCB copper to minimize EMI radiation from the high transient voltages on the switch node. Switching waveform measurements should be made using Power Ground (TP14) as the ground reference for more accurate measurements.

### 4.3.6 Power Good Voltage Monitoring (TP16 and TP18)

The TPS40305EVM-488 provides a test point and local ground for measuring the power good output voltage. A 100-k $\Omega$  resistor pull-up to BP (R9) is included to allow the Power Good signal to be monitored without requiring an external pull-up. For true open-drain operation with no pull-up, remove R9. With R9 removed, TP16 can be connected to TP17 of another TPS40305EVM-488 to provide sequential start-up of the two TPS40305EVM-488 converters.

### 4.3.7 Enable and Soft-Start Voltage Monitoring (TP17 and TP18)

The TPS40305EVM-488 provides a test point and local ground for measuring the Enable and Soft-Start voltage. TP17 and TP18 or JP2 can be used to provide an external enable signal. Due to the nature of the Soft-Start function, the external signal must be open-collector or open-drain without pull-up.

## 5 Test Set Up

### 5.1 Equipment

#### 5.1.1 Voltage Source

$V_{IN}$  — The input voltage source ( $V_{IN}$ ) shall be a 0V – 15V variable dc source capable of supplying 2.5A<sub>dc</sub>

#### 5.1.2 Meters

A1: — Input current meter. 0A<sub>dc</sub> – 2.5A<sub>dc</sub> ammeter

V1: — Input voltage meter. 0V – 15V voltmeter

V2: — Output voltage meter. 0V – 2V voltmeter

### 5.1.3 Loads

LOAD1: — Output load. Electronic load set for constant current or constant resistance capable of 0Adc – 10Adc at 1.8Vdc

### 5.1.4 Oscilloscope

For Output Voltage Ripple: — Oscilloscope shall be an analog or digital oscilloscope set for ac coupled measurement with 20-MHz bandwidth limiting. Use 20mV / division vertical resolution, 200ns/division horizontal resolution.

For Switching Waveforms: — Oscilloscope shall be an analog or digital oscilloscope set for dc coupled measurement with 20-MHz bandwidth limiting. Use 2V/division or 5V/division vertical resolution and 200ns/division horizontal resolution.

### 5.1.5 Recommended Wire Gauge

VIN to J1: — The connection between the source voltage (VIN) and J1 of TPS40305EVM-488 can carry as much as 2.5Adc of current. The minimum recommended wire size is AWG #16 with the total length of wire less than 2 feet (1 foot input, 1 foot return).

J2 to LOAD1: — The connection between the source voltage (VIN) and J1 of TPS40305EVM-488 can carry as much as 10Adc of current. The minimum recommended wire size is AWG #14 with the total length of wire less than 2 feet (1 foot input, 1 foot return).

### 5.1.6 Other

FAN: — The TPS40305EVM-488 evaluation module includes components that can get hot to the touch when operating. Because this evaluation module is not enclosed to allow probing of circuit nodes, a small fan capable of 200lfm – 400lfm is recommended to reduce component temperatures when operating.

## 5.2 Equipment Setup

Shown in [Figure 2](#) is the basic test set up recommended to evaluate the TPS40305EVM-488. Note that although the return for J1 and JP2 are the same system ground, the connections should remain separate as shown in [Figure 2](#).

### 5.2.1 Procedure

1. Working at an ESD workstation, make sure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
2. Prior to connecting the DC input source,  $V_{IN}$ , it is advisable to limit the source current from  $V_{IN}$  to 3.0A maximum. Make sure  $V_{IN}$  is initially set to 0V and connected as shown in [Figure 2](#).
3. Connect VIN to J1 as shown in [Figure 2](#).
4. Connect ammeter A1 between VIN and J1 as shown in [Figure 2](#).
5. Connect voltmeter V1 to TP1 and TP2 as shown in [Figure 2](#).
6. Connect voltmeter V2 to TP3 and TP4 as shown in [Figure 2](#).
7. Connect oscilloscope probes to desired test points per [Table 2](#).
8. Place fan as shown in [Figure 2](#) and turn on making sure to blow air directly across the evaluation module.

5.2.2 Diagram

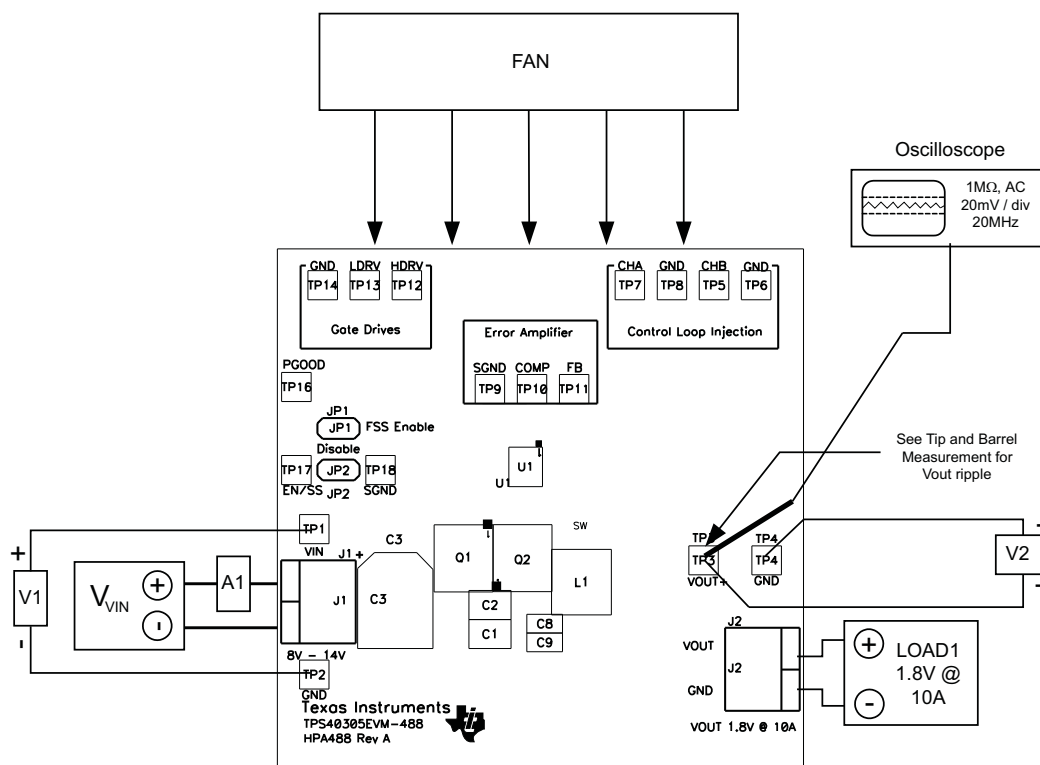


Figure 2. TPS40305EVM-488 Recommended Test Set-Up

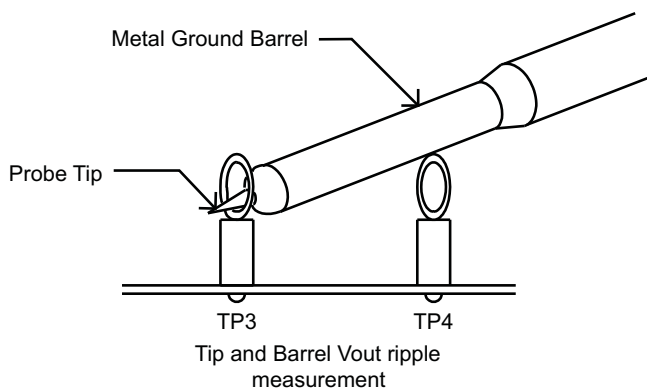


Figure 3. Output Ripple Measurement – Tip and Barrel using TP3 and TP4



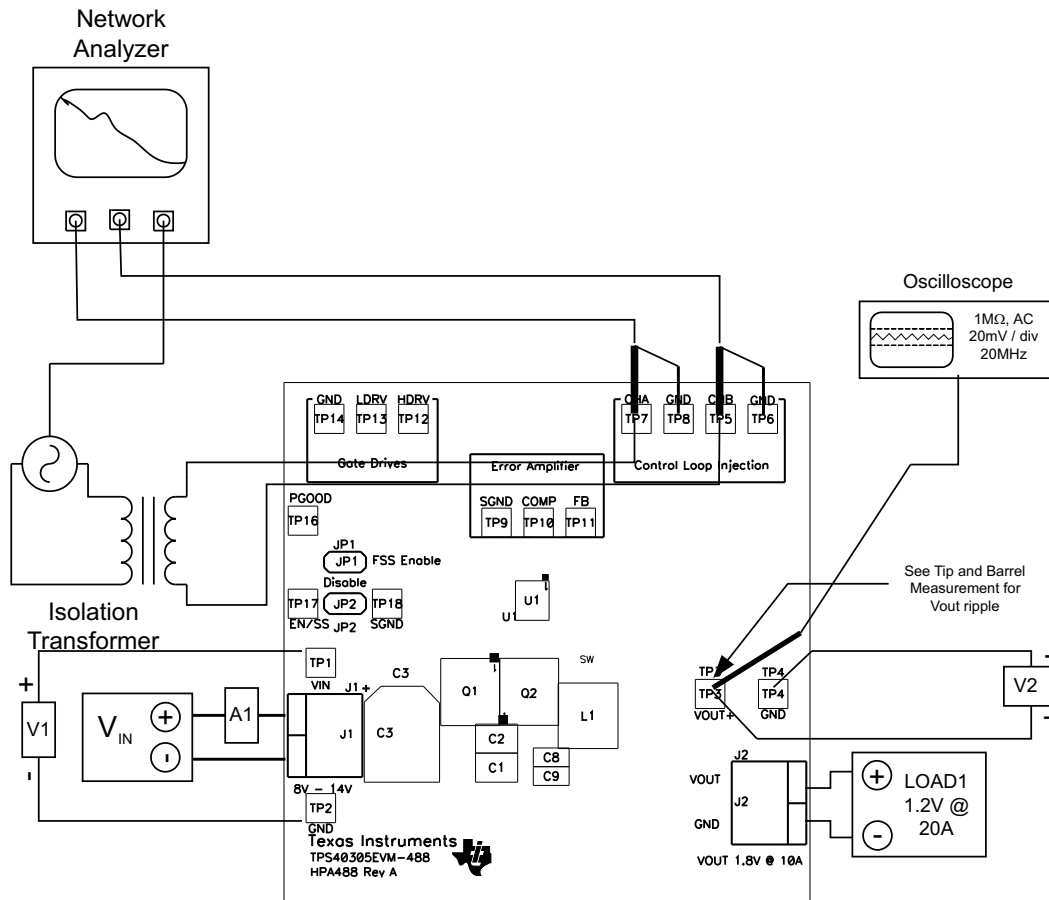


Figure 4. Control Loop Measurement Setup

### 5.3 Start Up/Shut Down Procedure

1. Verify shunt position for JP1 for desired FSS status per section 4.1.2
2. Remove shunt from JP2 location if present
3. Increase VIN from 0Vdc to 12Vdc
4. Vary LOAD1 from 0Adc to 10Adc
5. Vary VIN from 8V to 14V
6. Decrease VIN to 0V
7. Decrease LOAD1 to 0A

### 5.4 Output Ripple Voltage Measurement Procedure

1. Follow section 5.3 Start-Up / Shut-Down Procedure steps 1 – 5 to set VIN and LOAD1 to the desired operating condition
2. Connect oscilloscope probe with exposed metal barrel to TP3 and TP4 per Figure 3
3. Set oscilloscope per oscilloscope for output voltage ripple measurement in section 5.1.4
4. Follow section 5.3 Start-Up / Shut-Down Procedure steps 6 and 7 to power down

### 5.5 Control Loop Gain and Phase Measurement Procedure

1. Follow section 5.3 Start-Up / Shut-Down Procedure steps 1 – 5 to set VIN and LOAD1 to desired operating condition
  - (a) If JP1 is installed (FSS enabled), loop response data about the modulation frequency (30kHz) may be affected

2. Connect a 1-kHz – 1-MHz isolation transformer to TP5 and TP7 as shown in [Figure 4](#)
  3. Connect input signal amplitude measurement probe (channel A) to TP7 as shown in [Figure 4](#)
  4. Connect output signal amplitude measurement probe (channel B) to TP5 as shown in [Figure 4](#)
  5. Connect ground lead of channel A and channel B to TP6 and TP8 as shown in [Figure 4](#)
  6. Inject 30mV or less signal across R3 through isolation transformer
  7. Sweep frequency from 1kHz to 1MHz with 10-Hz or lower post filter
- $$20 \times \text{LOG} \left( \frac{\text{Channel B}}{\text{Channel A}} \right)$$
8. Control loop gain can be measured by
  9. Control loop phase can be measured by the phase difference between channel A and channel B
  10. Control to output response (power stage transfer function) can be measured by connecting channel A probe to TP10 (COMP) and channel B probe to TP5 (CHB)
  11. Output to control response (compensated error amplifier transfer function) can be measured by connecting channel A probe to TP7 (CHA) and channel B probe to TP10 (COMP)
  12. Follow section 5.3 Start-Up / Shut-Down Procedure steps 6 and 7 to power down

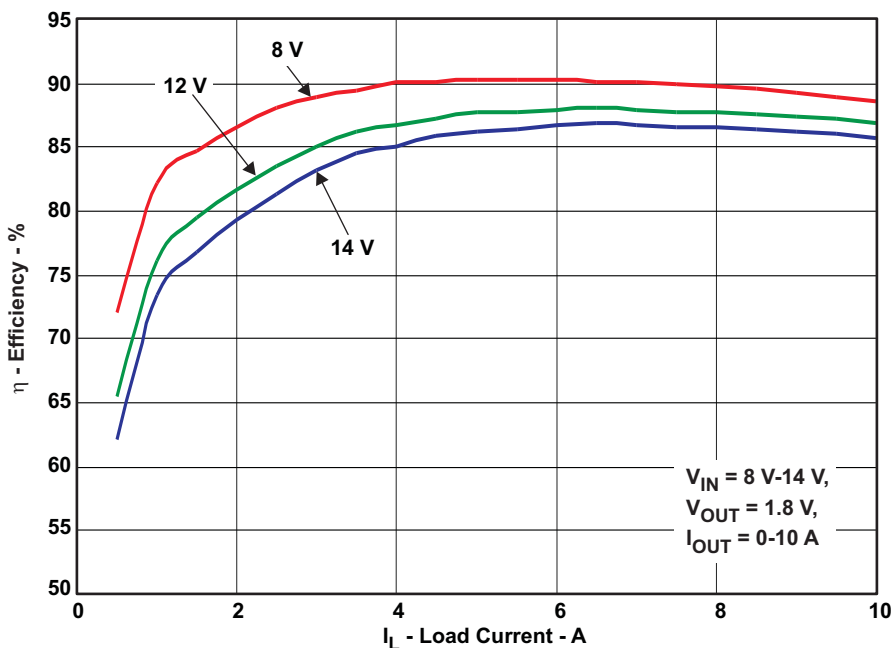
## 5.6 Equipment Shutdown

1. Shut down oscilloscope
2. Shut down LOAD1
3. Shut down VIN
4. Shut down fan

## 6 TPS40305EVM-488 Test Data

[Figure 5](#) through [Figure 11](#) present typical performance curves for the TPS40305EVM-488. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

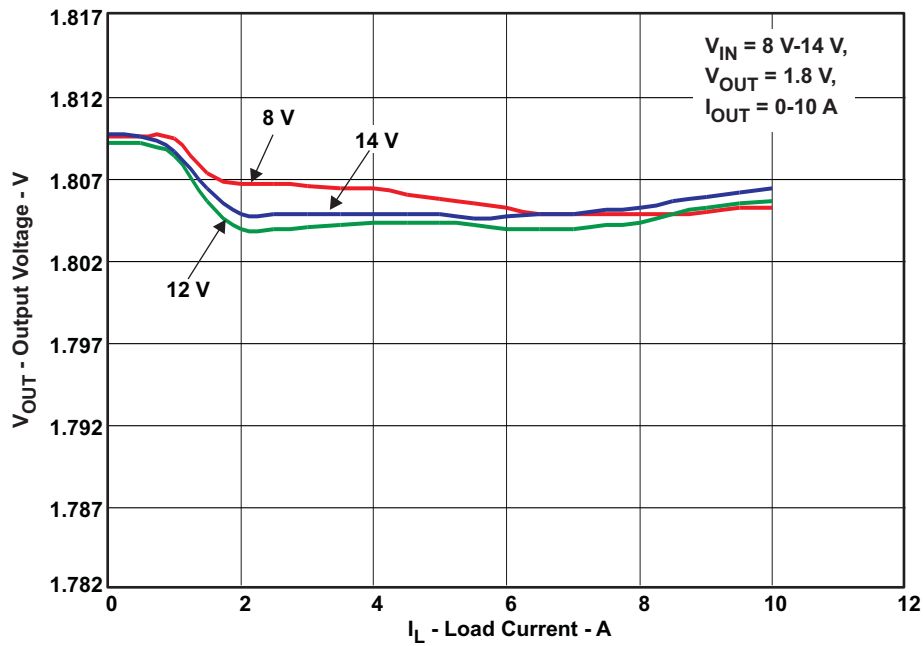
### 6.1 Efficiency



$V_{IN} = 8.0\text{V} - 14\text{V}$ ,  $V_{OUT} = 1.8\text{V}$ ,  $I_{OUT} = 0\text{A} - 10\text{A}$

**Figure 5. TPS40305EVM-488 Efficiency vs Load Current**

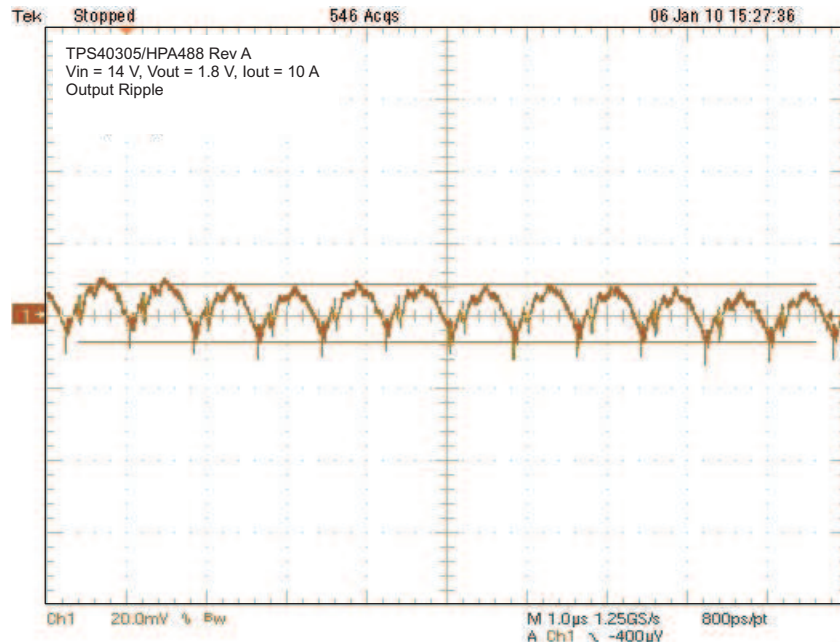
### 6.2 Line and Load Regulation



$V_{IN} = 8.0V - 14V$ ,  $V_{OUT} = 1.8V$ ,  $I_{OUT} = 0A - 10A$

Figure 6. TPS40305EVM-488 Output Voltage vs Load Current

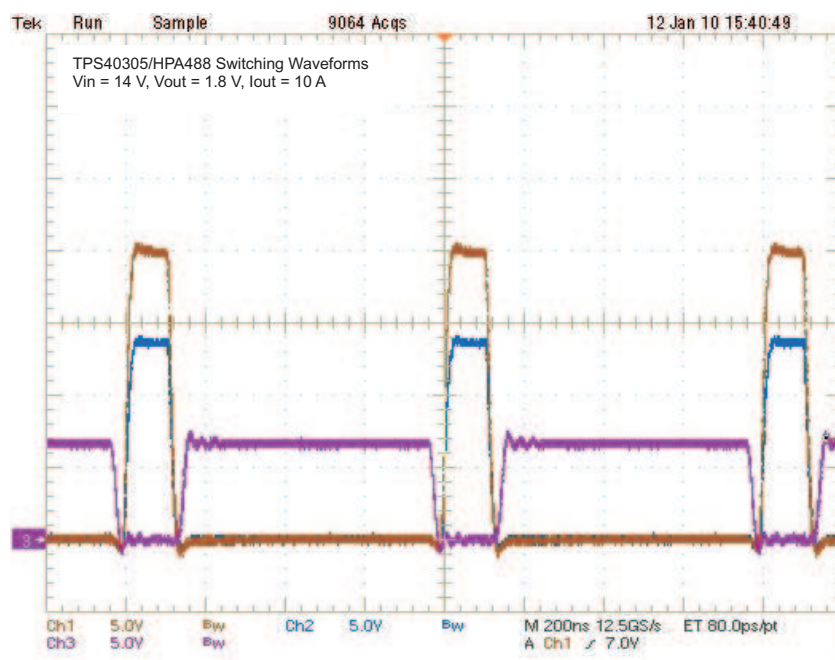
### 6.3 Output Voltage Ripple



$V_{IN} = 14V$ ,  $V_{OUT} = 1.8V$ ,  $I_{OUT} = 10A$

Figure 7. TPS40305EVM-488 Output Voltage Ripple

## 6.4 Switch Node

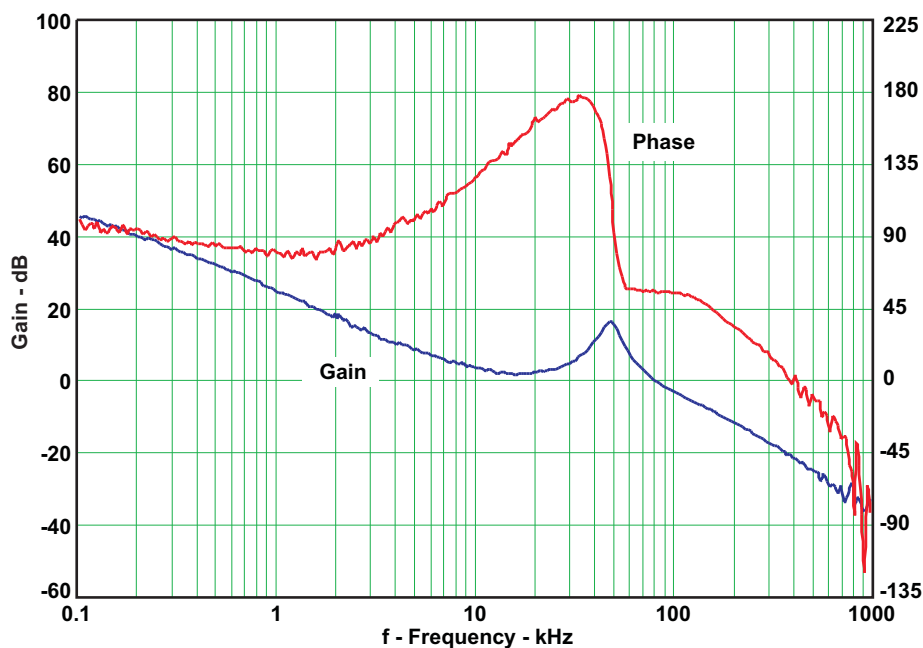


$V_{IN} = 12V$ ,  $V_{OUT} = 1.8V$ ,  $I_{OUT} = 10A$

Ch1: TP12 (HDRV), Ch2:13 TP (SW), Ch3: TP14 (LDRV)

**Figure 8. TPS40305EVM-488 Switching Waveforms**

## 6.5 Control Loop Bode Diagram



$V_{IN} = 14V$ ,  $V_{OUT} = 1.8V$ ,  $I_{OUT} = 10A$ , Bandwidth: 83kHz, Phase Margin: 55°

**Figure 9. TPS40305EVM-488 Gain and Phase vs. Frequency**

## 6.6 Additional Waveforms

### 6.6.1 Output Ripple with Frequency Spread Spectrum (FSS) Enabled

Frequency Spread Spectrum varies the output switching frequency. This change in switching frequency can produce a small change in the output voltage at the modulation frequency. Figure 10 shows the approximately 50mV modulation of the output voltage generated when Frequency Spread Spectrum is enabled.

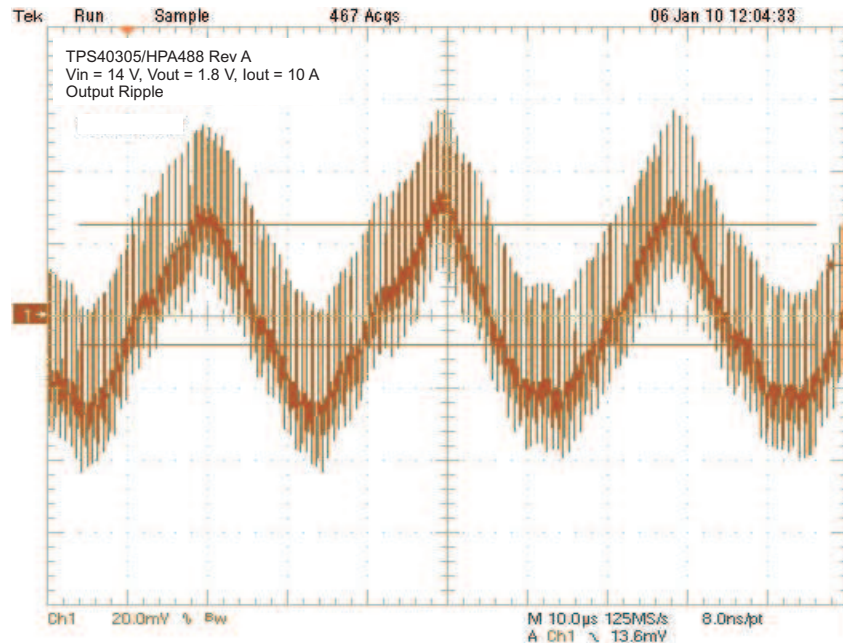


Figure 10. TPS40305EVM-488 Output Ripple with FSS Enabled

## 7 TPS40305EVM-488 Assembly Drawings and Layout

The following figures (Figure 11 through Figure 16) show the design of the TPS40305EVM-488 printed circuit board. The EVM has been designed using a 4-layer, 2oz. copper-clad circuit board 2.5" × 2.5" with all populated components on the top to allow the user to easily view, probe and evaluate the TPS40305 control IC in a practical double-sided application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space constrained systems.

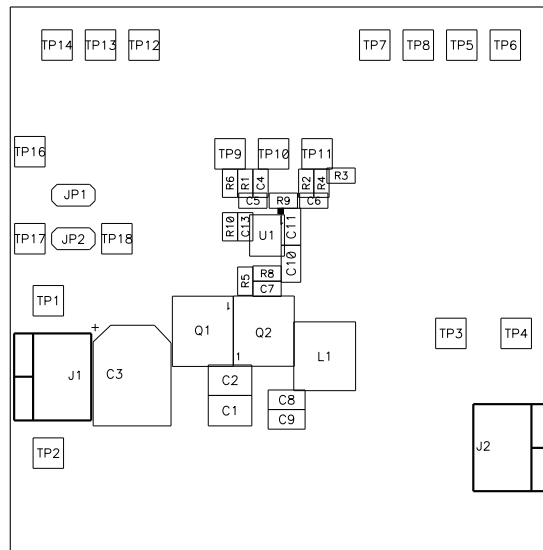


Figure 11. TPS40305EVM-488 Top Component Placement (Top View)

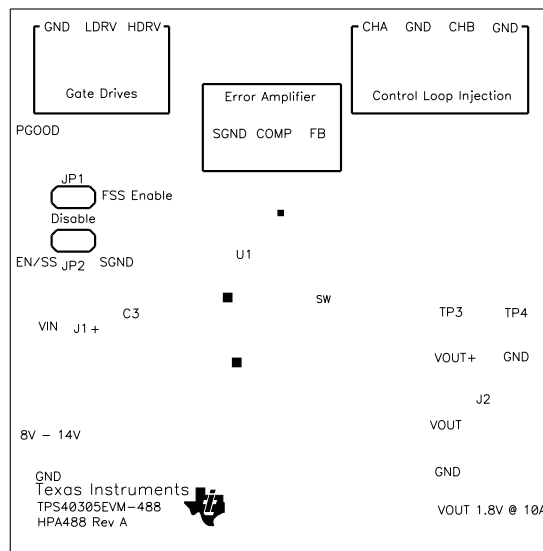


Figure 12. TPS40305EVM-488 Silk Screen (Top View)

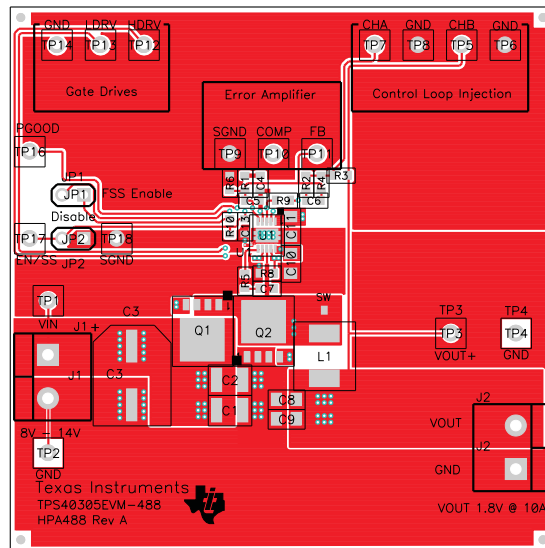


Figure 13. TPS40305EVM-488 Top Copper (Top View)

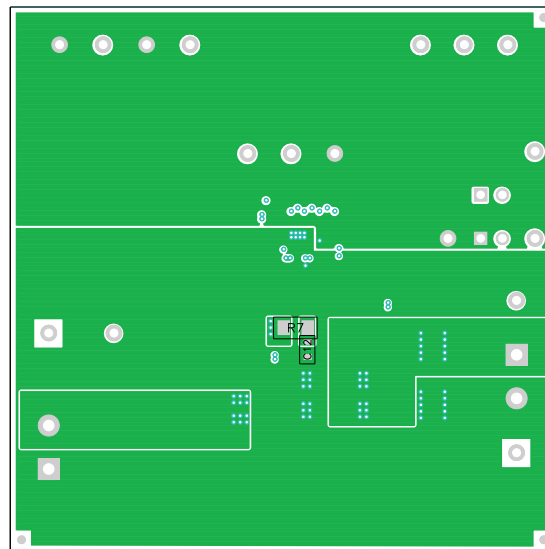
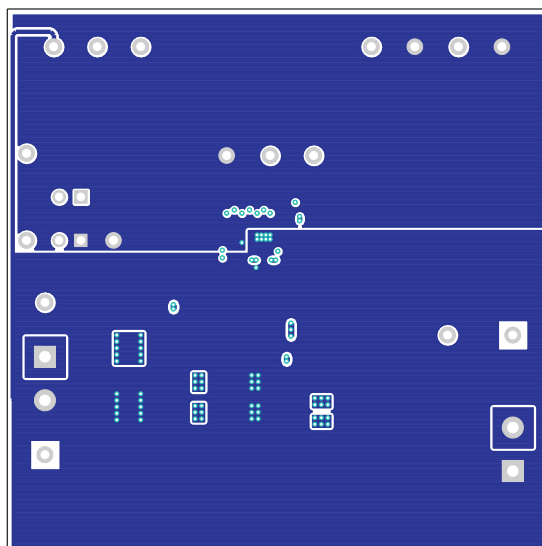
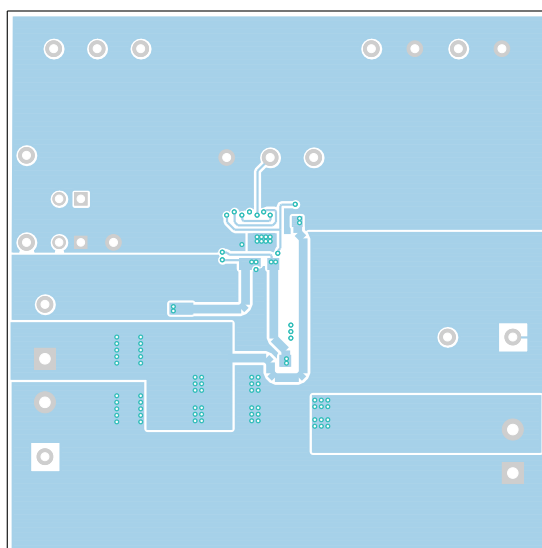


Figure 14. TPS40305EVM-488 Bottom Copper (Top View)


**Figure 15. TPS40305EVM-488 Internal 1 (X-Ray Top View)**

**Figure 16. TPS40305EVM-488 Internal 2 (X-Ray Top View)**

## 8 TPS40305EVM-488 Bill of Materials

**Table 3. TPS40305EVM-488 Bill of Materials**

QTY	RefDes	Value	Description	Size	Part Number	MFR
2	C1, C2	10 $\mu$ F	Capacitor, Ceramic, 25V, X7R, 10%	1210	Std	Std
1	C10	4.7 $\mu$ F	Capacitor, Ceramic, 10V, X7R, 20%	0805	Std	Std
1	C11	1 $\mu$ F	Capacitor, Ceramic, 25V, X7R, 20%	0805	Std	Std
0	C12	1nF	Capacitor, Ceramic, 25V, X5R, 20%	0603	Std	Std
1	C13	3.3nF	Capacitor, Ceramic, 10V, X7R, 20%	0603	Std	Std
1	C3	330 $\mu$ F	Capacitor, Aluminum, 25V, $\pm$ 20%, 160m $\Omega$	0.328 x 0.390 inch	EEEFK1E331P	Panasonic
1	C4	3300pF	Capacitor, Ceramic, 25V, X7R, 10%	0603	Std	Std
1	C5	150pF	Capacitor, Ceramic, 25V, X7R, 10%	0603	Std	Std



**Table 3. TPS40305EVM-488 Bill of Materials (continued)**

QTY	RefDes	Value	Description	Size	Part Number	MFR
1	C6	820pF	Capacitor, Ceramic, 25V, X7R, 10%	0603	Std	Std
1	C7	100nF	Capacitor, Ceramic, 16V, X7R, 20%	0603	Std	Std
2	C8, C9	22µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	Std	Std
2	J1, J2	ED120/2DS	Terminal Block, 2-pin, 15-A, 5.1mm	0.40 x 0.35 inch	ED120/2DS	OST
2	JP1, JP2	PEC02SAAN	Header, 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
1	L1	0.32µH	Inductor, SMT, 17A	0.268 x 0.268 inch	PG0083.401NLT	Pulse
1	Q1*	CSD16410Q5A	MOSFET, N-Chan, 25V, 59A, 9.6mΩ	QFN-8 POWER	CSD16410Q5A	TI
1	Q2*	CSD16322Q5	MOSFET, N-Chan, 25V, 97A, 4.5mΩ	QFN-8 POWER	CSD16322Q5	TI
1	R1	2.20kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	422Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	49.9Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	10.0kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	0Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	4.99kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R7	2.2Ω	Resistor, Chip, 1/8W, 5%	1206	Std	Std
1	R8	2.37kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R9, R10	267kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	TP1, TP3	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
0	TP15	None	Test Point, SM, 2x3mm	0.118 x 0.079 inch		
6	TP2, TP4, TP6, TP8, TP9, TP18	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
9	TP5, TP7, TP10– TP14, TP16, TP17	5002	Test Point, White, Thru Hole Color Keyed	0.100 x 0.100 inch	5002	Keystone
1	U1*	TPS40305DRC	IC, 3V – 20V sync. 600kHz Buck Controller w/ LLE and FSS	DRC10	TPS40305DRC	TI

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## EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 8 V to 14 V and the output voltage range of 1.8 V  $\pm$  2%.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85° C. The EVM is designed to operate properly with certain components above 85° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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