QPB9015

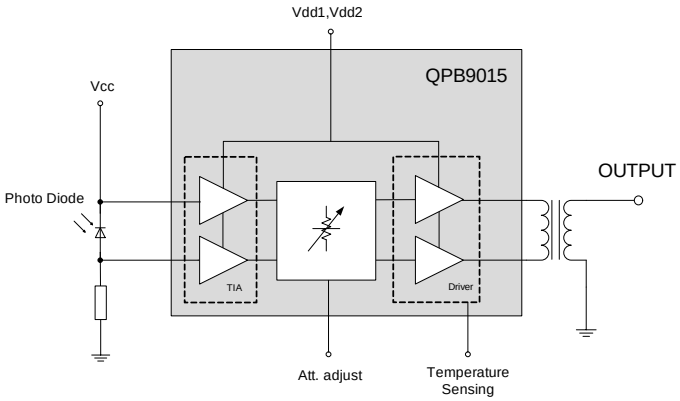
xPON Video Receiver with integrated VCA

28 pin, 11.0 mm x 11.0 mm x 1.375 mm package

Product Description

The QPB9015 is a video receiver integrated circuit (IC) which provides a low noise analog interface to optical access triplexer modules used in single family ONTs in fiber to the premise (FTTP) applications. The QPB9015 exhibits low input noise and distortion to meet critical FTTP link requirements. QPB9015 employs an integrated voltage controlled attenuator that provides, with external control circuitry, automatic gain control to maintain a constant +19 to +23 dBmV / channel output to insure consistent video quality.

Functional Block Diagram



Product Features

- 45 – 1218 MHz Operational Bandwidth
- Efficient Power Consumption: 1.5 W
- Low Noise: 3.5 pA / √Hz Equivalent Input Noise Current (EINC)
- Linearity: -65 dBc CSO and -66 dBc CTB at +22 dBmV RF Output per Channel (79-NTSC Equivalent Channels)
- Integrated VCA, 25 dB Attenuation Range
- Temperature Sensing Feature

Applications

xPON RF Overlay Video Receiver for FTTX Triplexer-Equipped Optical Network Termination (ONT) and RFoG Network Interface Unit (NIU)

Ordering Information

Part No.	Description
QPB9015SB	Sample bag 5 pcs
QPB9015SQ	Sample bag 25 pcs
QPB9015SR	7” Reel with 100 pcs
QPB9015TR7	7” Reel with 250 pcs
QPB9015TR13	13” Reel with 750 pcs
QPB9015PCBA-410	Fully assembled Evaluation Board

Absolute Maximum Ratings

Parameter	Value / Range
Detector Bias over-voltage (Vcc)	+15 V
DC Supply over-voltage (Vdd1,Vdd2, Vc, MODE)	+6V
Storage Temperature	−40 to 100 °C
Operating Mounting Base Temperature	−40 to 85 °C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Detector Bias Voltage (Vcc)	+11.4	+12	+12.6	V
DC Supply Voltage (Vdd1,Vdd2)	+4.5	+5	+5.5	V
Operating Mounting Base Temperature	-40		+85	°C

Electrical specifications are measured at specified test conditions in application circuit. Specifications are not guaranteed over all recommended operating conditions.

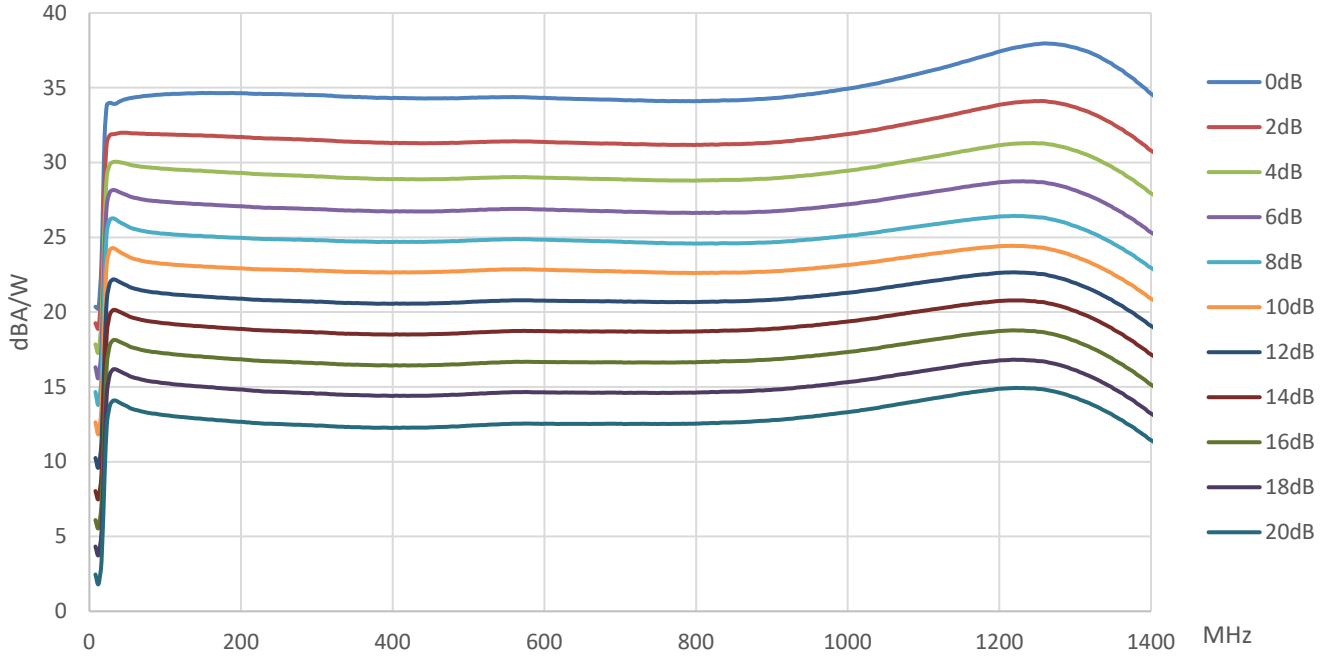
Electrical Specifications – tested in evaluation circuit

Parameter	Conditions (Vcc=12V, Vdd1=Vdd2=5V, TMB=30°C, ZL=75Ω, ATT=0…20dB)	Min	Typ	Max	Units
Supply Current (I_{DD})	Steady state operation, current draw during attenuation state transitions is higher.		300		mA
Frequency Range		45		1218	MHz
Spectral sensitivity [1]	0dBm optical input, 1310nm	900			V/W
Gain (O/E)	1218MHz, ATT=0dB		37		dBA/W
Gain Slope [2]	45MHz to 1218MHz		1		dB
Gain Flatness [3]	45MHz to 1218MHz		2		dB
Output Return Loss (S22)	45MHz to 1218MHz		-15		dB
Equivalent Input Noise (EINC)	45MHz to 1218MHz, ATT=0dB		3.5		pA/ √Hz
Optical Input Power				+2	dBm
CSO	Source: 79 NTSC analog channels (55.25 to 547.25MHz), flat, OMI = 2.82%/ch;		-65		dBc
CTB	DUT: +2 dBm optical input power, attenuator set to RFOUT = +22 dBmV per channel		-66		dBc
Voltage Control Range, Positive Attenuation Slope	MODE Pin Logic High: Control voltage Vc=5V is lowest insertion loss	0	0…3	5	V
Voltage Control Range, Negative Attenuation Slope	MODE Pin Logic Low: Control voltage Vc=0V is lowest insertion loss	0	0…3	5	V
MODE Pin Logic Low				0.4	V
MODE Pin Logic High		1			V
Attenuator Range			0…25		dB
Thermal Resistance	T_{REF} taken at +85 °C from backside of PCB under the QPB9015		26.5		K/W

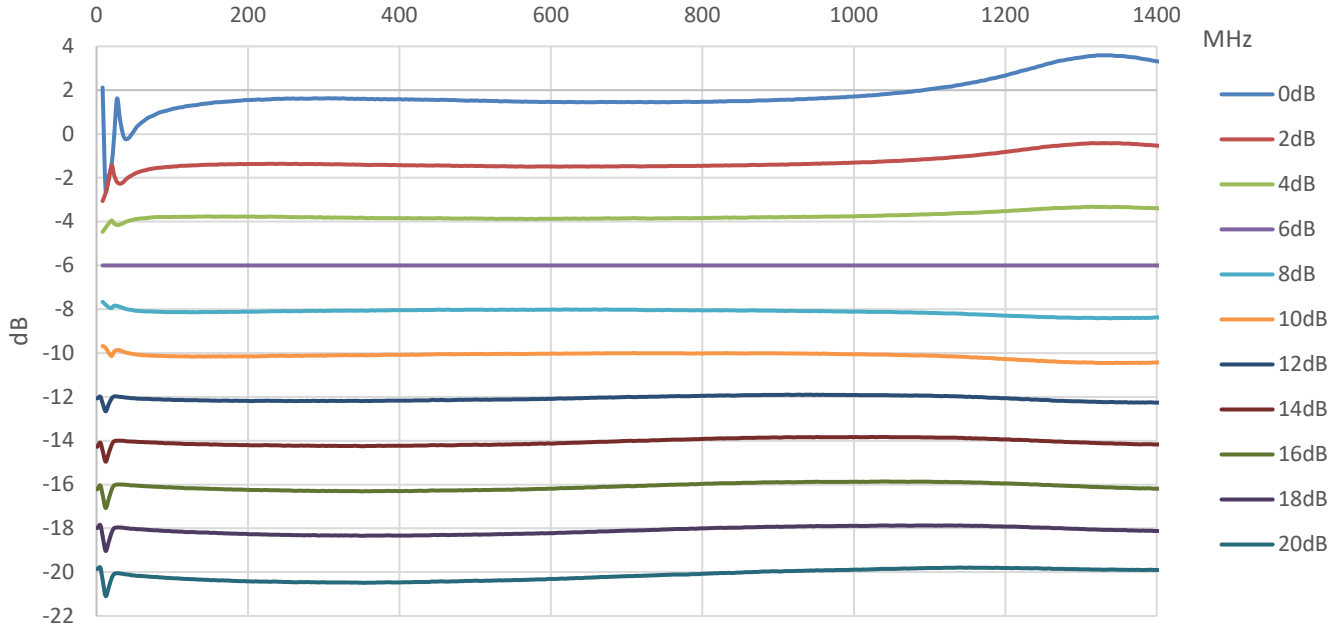
1. Measured between OPS pin and GND on evaluation board.
2. The slope is defined as the difference between the gain at start frequency and the gain at stop frequency.
3. Measured as sum of positive and negative deviation from a straight line between gain at start frequency and gain at stop frequency.

Composite Second Order (CSO) - The CSO parameter (both sum and difference products) is defined by ANSI/SCTE 6.
Composite Triple Beat (CTB) The CTB parameter is defined by ANSI/SCTE 6.

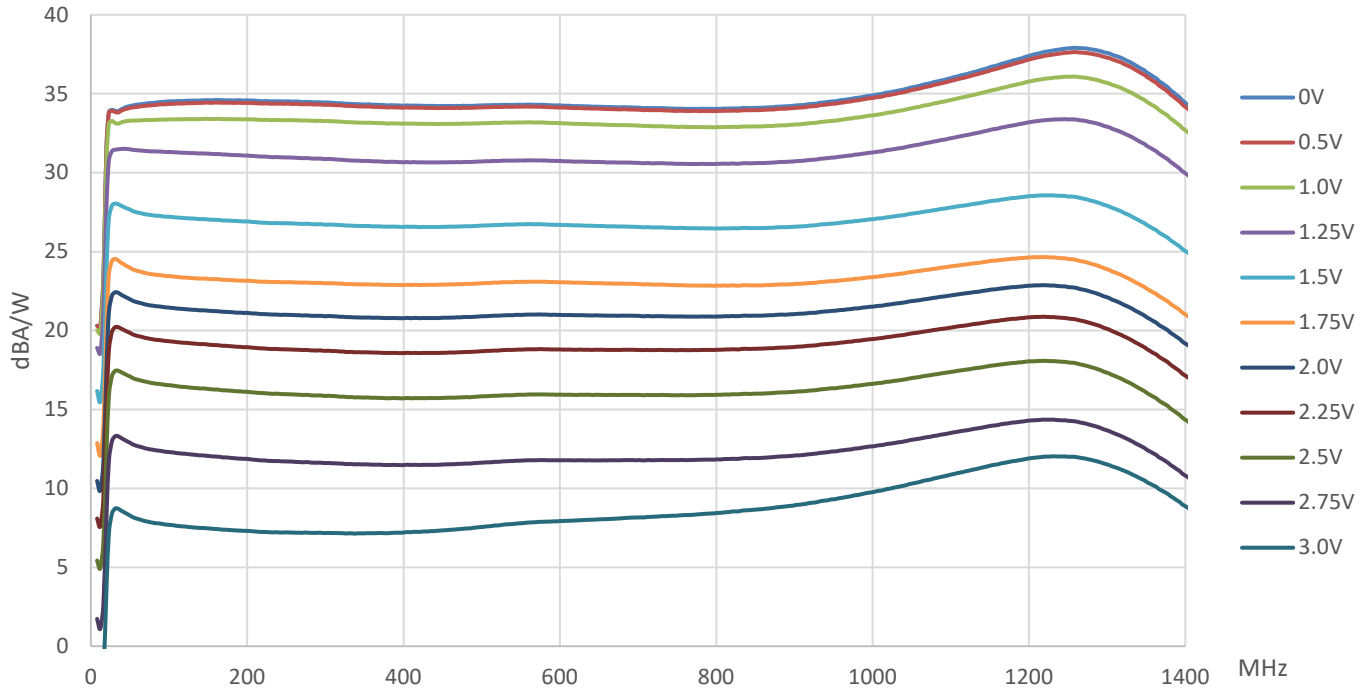
QPB9015 Gain vs. ATT, typ. values



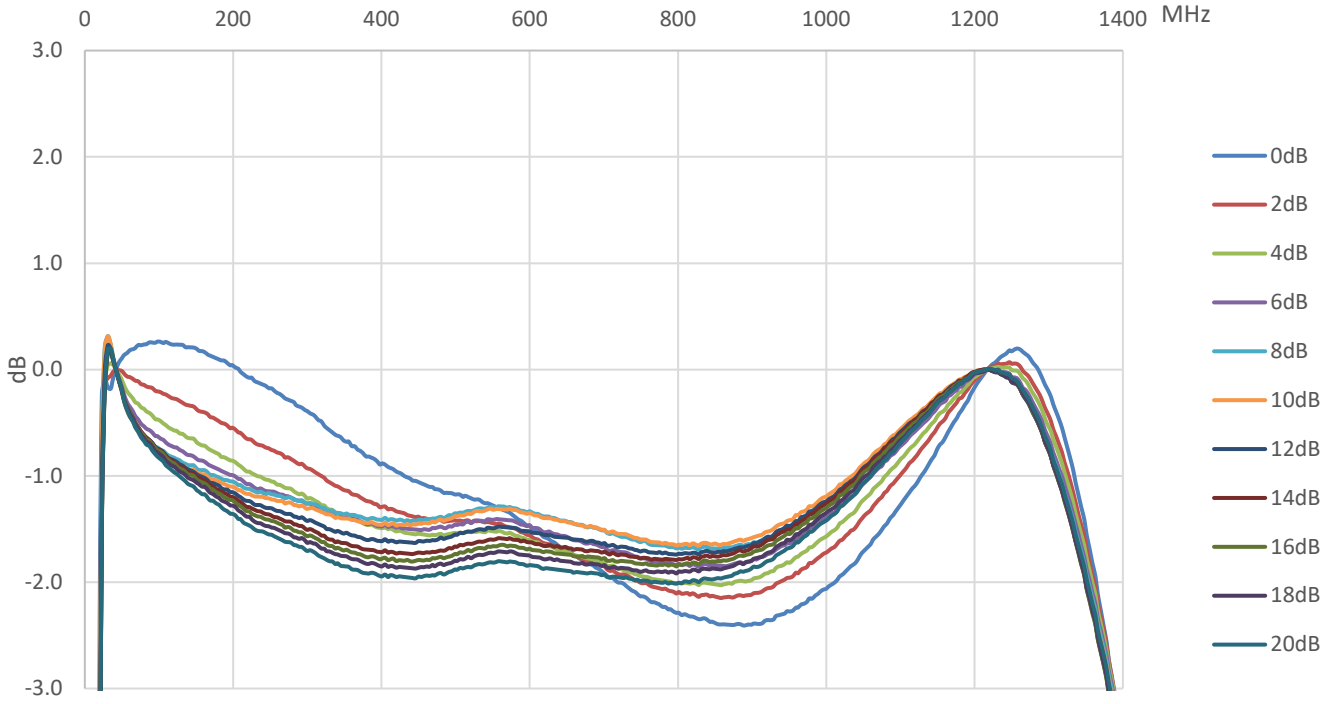
QPB9015 Gain change vs. ATT, reference 45 MHz, 6 dB ATT, typ. values



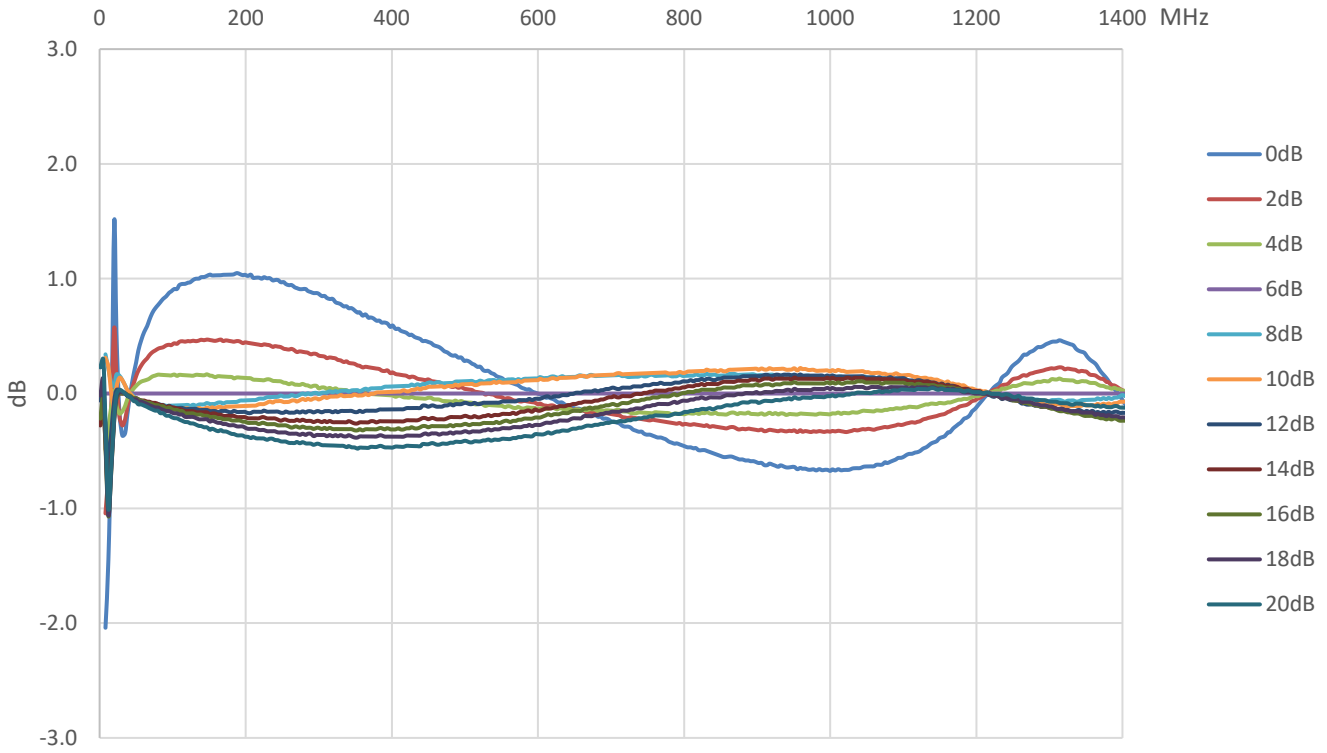
QPB9015 Gain vs. Vc



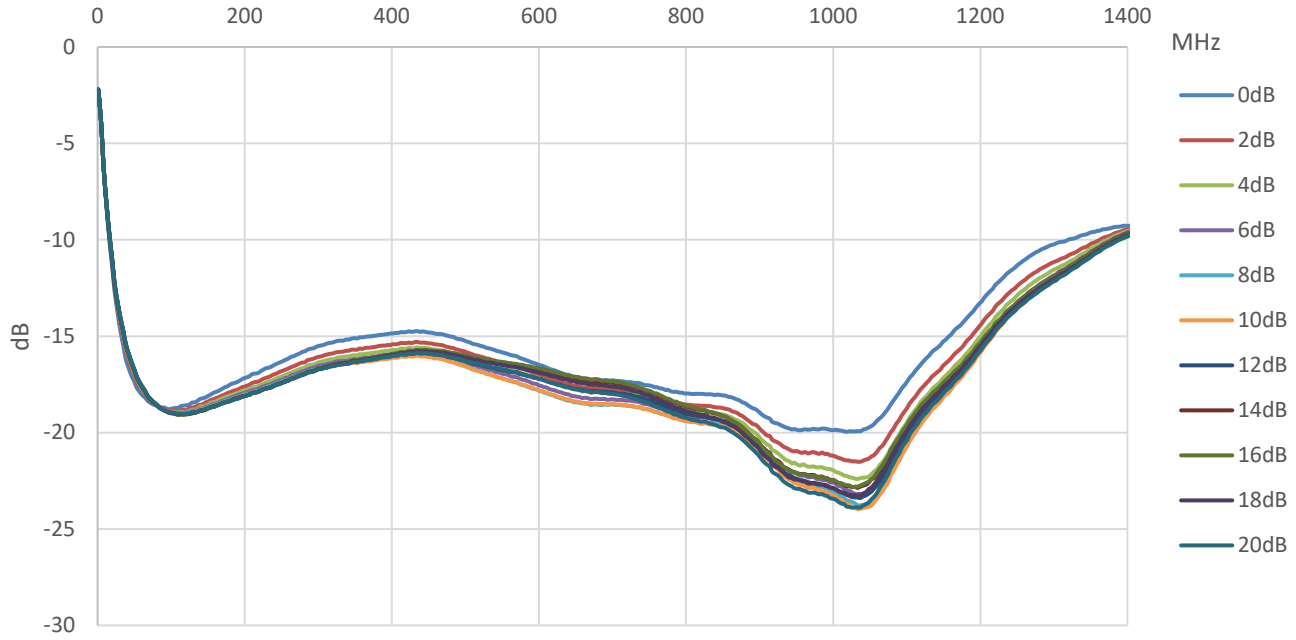
QPB9015 Flatness vs. ATT (45-1218 MHz), typ. values



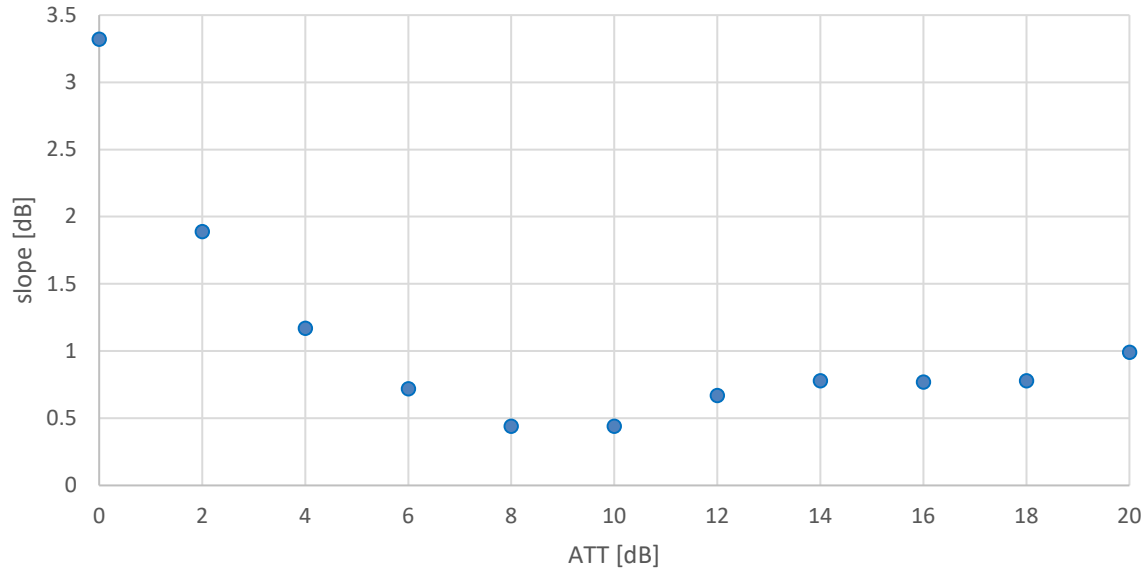
QPB9015 Flatness change vs. ATT, reference 6 dB ATT, typ. values



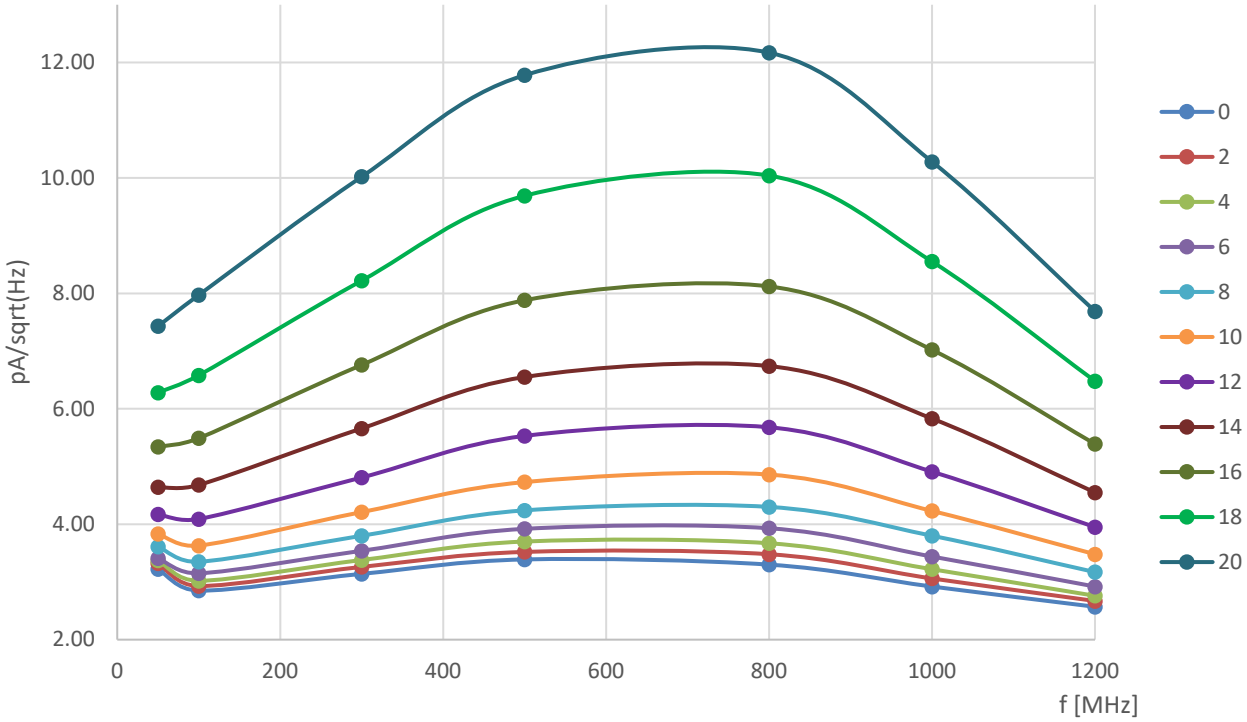
QPB9015 S22 vs. ATT, typical values



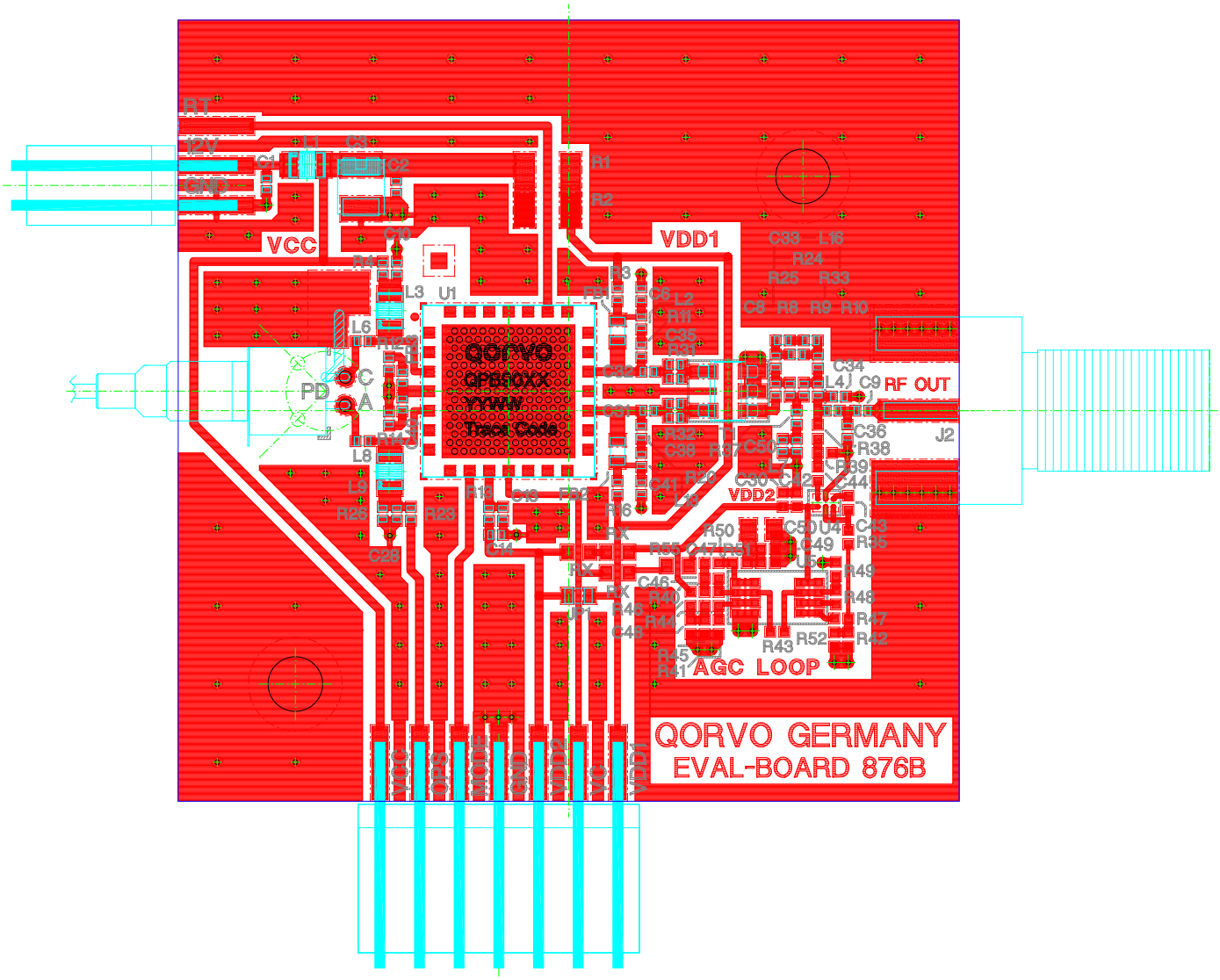
QPB9015 Gain slope vs. ATT, typical values



QPB9015 EINC vs. ATT, typical values, T_{MB}=30°C

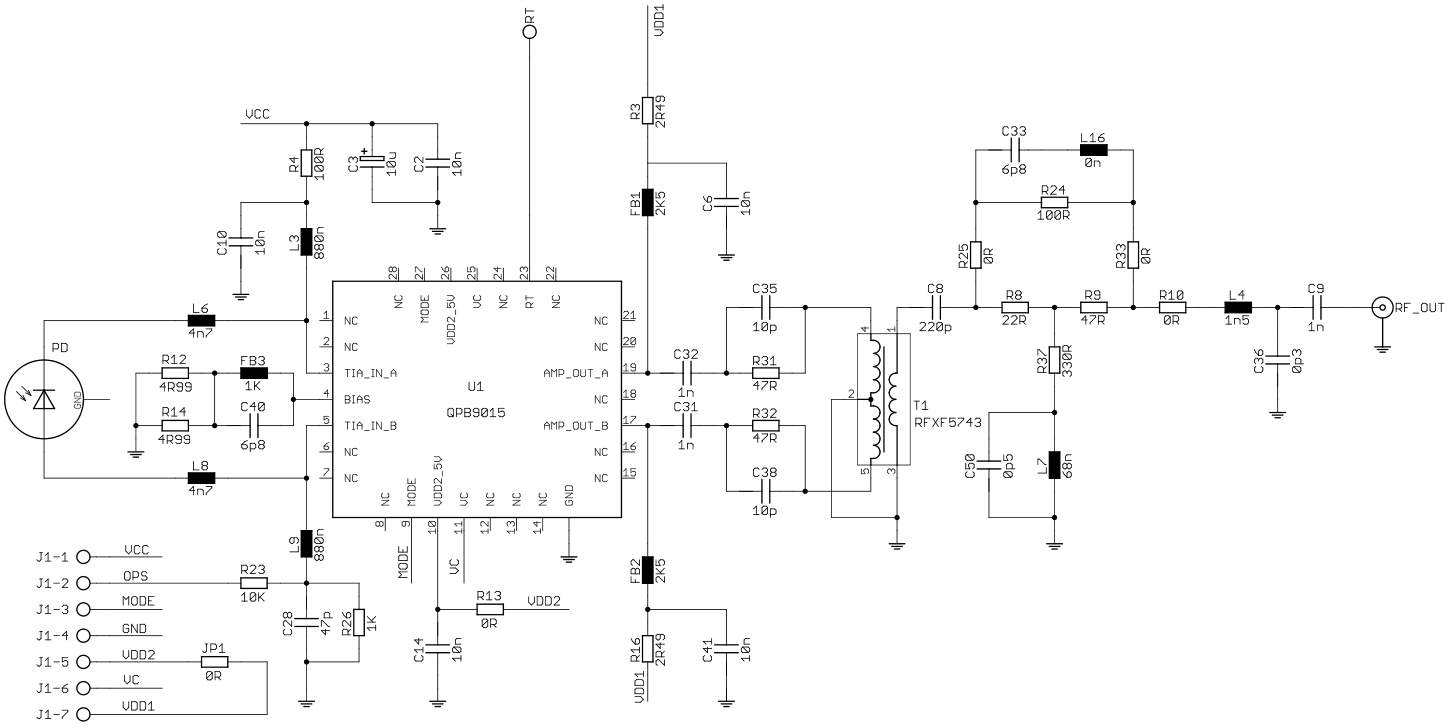


Evaluation Board Assembly Drawing



Note:
The ground plane of the QPB9015 module should be soldered onto a board equipped with as many thermal vias as possible. Underneath this thermal via array a heat sink with thermal grease needs to be placed which is able to dissipate the complete module DC power. In any case the module backside temperature should not exceed 85°C

Evaluation Board Schematic

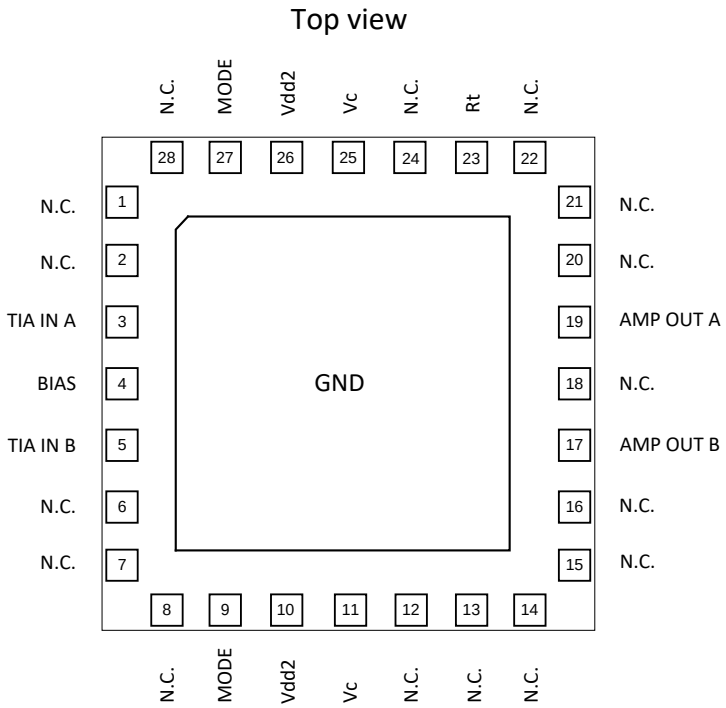


Evaluation Board Bill of Materials (BOM)

Ref. Designator	Value, package	Description	Manufacturer	Part Number
FB1, FB2	2k5, 0603	Impedance bead	Taiyo Yuden	BK 1608 LM 252
FB3	1k, 0402	Impedance bead	Taiyo Yuden	BK 1005 HM 102
T1		Transformer	MiniRF	RFXF5743
L3, L9	880nH, 0805	Inductor, wirewound	Gowanda	CC0805-880J
L6, L8	4n7, 0402	Inductor, Thin Film	Murata	LQP15 series
L4	1n5, 0402	Inductor, Multilayer	Taiyo Yuden	HK1005-1N5J-T
L7	68nH, 0402	Inductor, wirewound	Murata	LQW15AN68NJ80D
L16, R10, R25, R33, JP1, R13	0R, 0402	Jumper 0R	various	
R4, R24	100R, 5%, 0402	Resistor	various	
R8	22R, 5%, 0402	Resistor	various	
R9, R31, R32	47R, 5%, 0402	Resistor	various	
R12, R14	4R99, 5%, 0402	Resistor	various	
R26	1k, 1%, 0402	Resistor	various	
R23	10k, 5%, 0402	Resistor	various	
R37	330R, 5%, 0402	Resistor	various	
R3, R16	2R49, 5%, 0402	Resistor	various	
C33, C40	6p8, 5%, C0G, 0402	Capacitor	Murata, Taiyo Yuden	
C50	0p5, +-0.1p, C0G, 0402	Capacitor	Murata, Taiyo Yuden	
C8	220p, 10%, X7R, 0402	Capacitor	Murata, Taiyo Yuden	
C36	0p3, +-0.1p, C0G, 0402	Capacitor	Murata, Taiyo Yuden	
C35, C38	10p, 5%, C0G, 0402	Capacitor	Murata, Taiyo Yuden	
C9, C31, C32	1n, 10%, X7R, 0402	Capacitor	Murata, Taiyo Yuden	
C2, C6, C10, C14, C41	10n, 10%, X7R, 0402	Capacitor	Murata, Taiyo Yuden	
C28	47p, 10%, C0G, 0402	Capacitor	Murata, Taiyo Yuden	
C3	10uF, 16V, 10%, size B	Tantalum capacitor	AVX, Kemet	
J2		Connector F-type	Amphenol	222181
P2		Connector 2.54mm pin spacing	various	
PD		InGaAs PIN Photodetector Diode	Beijing SWT Science & Technology	PDS133-CSA-C0104
U1		Video Receiver	Qorvo	QPB9015
all others	DNI			

Notes: L6, L8 can be optimized in application circuit for gain slope/flatness
C36, L4 can be optimized in application circuit for output matching
Evaluation pcb material: FR4, 1.5mm thickness

Pin Configuration



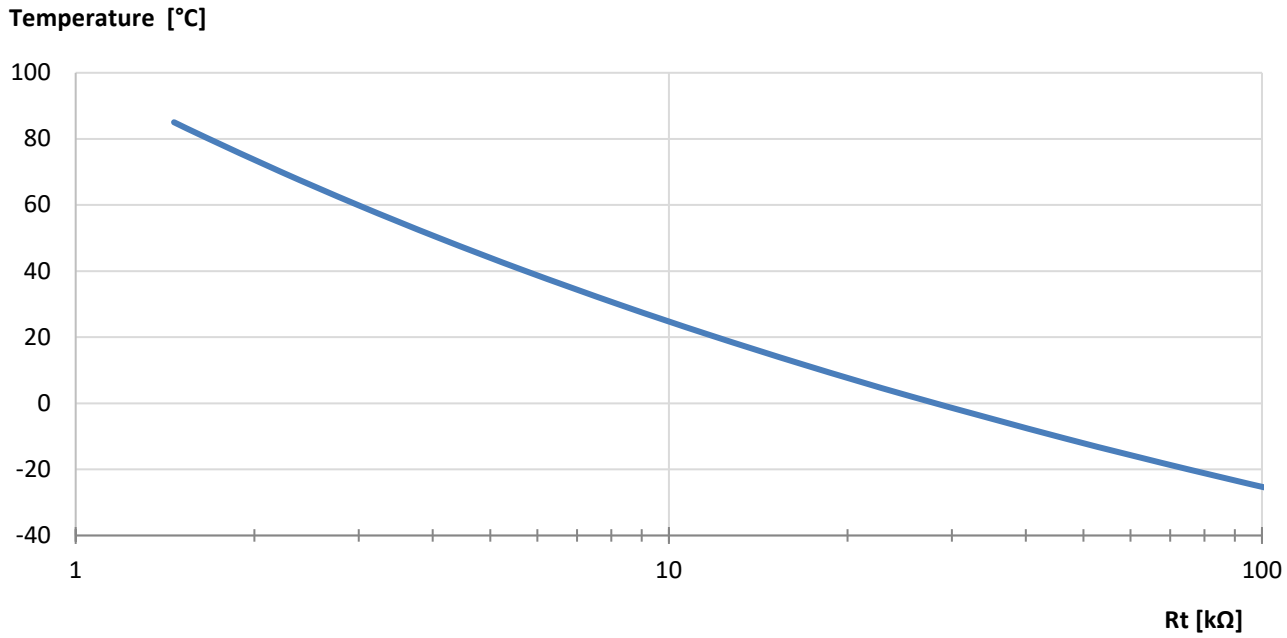
Pin Description

Pin No.	Label	Description
3	TIA IN A	Input to the TIA stage of the receiver
4	BIAS	Biasing for the first stage. The current flowing through this pin is used to control the biasing for the first stage amplifier
5	TIA IN B	Input to the TIA stage of the receiver
9,27	MODE	Attenuator slope control (0V: negative slope or 5V: positive slope)
10,26	Vdd2	+5V supply voltage for attenuator and output stage
11,25	Vc	Attenuator control input, 0V to 5V
17	AMP out B	RF output B and +5V supply voltage for TIA
19	AMP out A	RF output A and +5V supply voltage for TIA
23	Rt	10k NTC close to output stage die, monitoring of output die temperature
GND	GND	Backside GND connection
1,2,6-8, 12-16,18,20-22,24,28	N.C.	

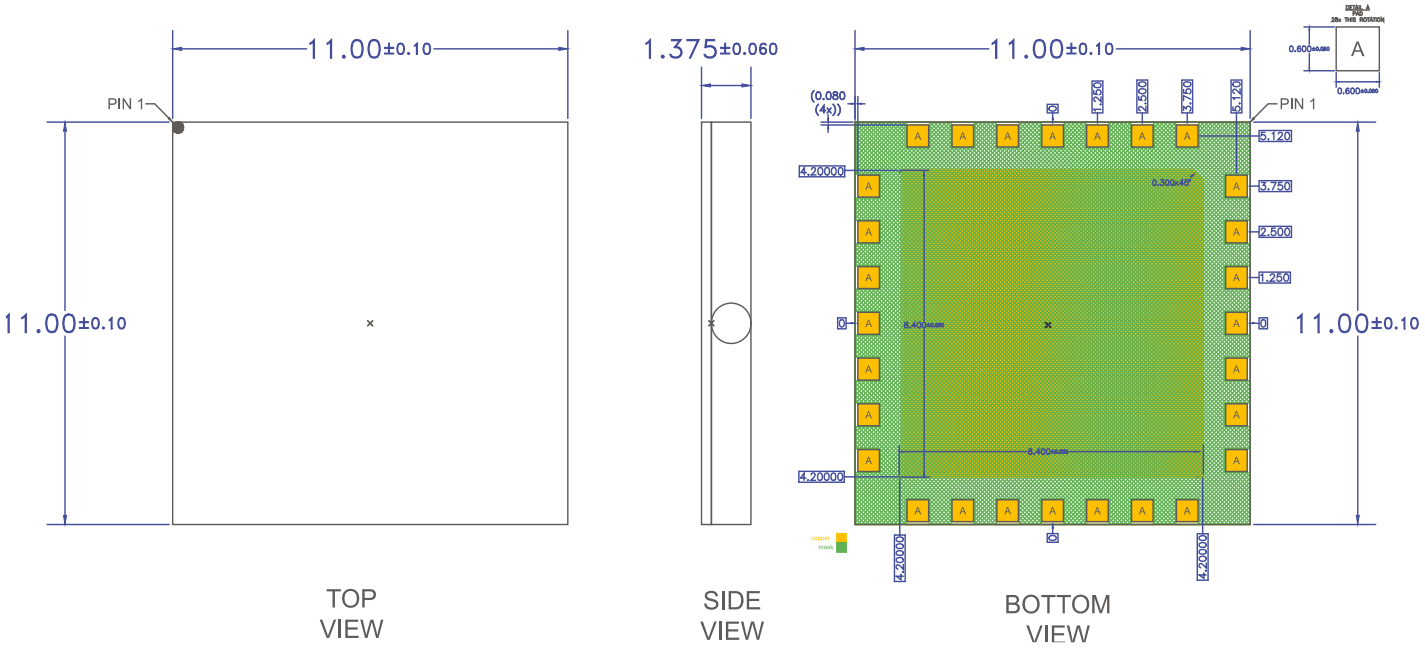
Notes: Pin 9 and 27 (MODE) are connected internally inside QPB9015
Pin 10 and 26 (Vdd2) are connected internally inside QPB9015
Pin 11 and 25 (Vc) are connected internally inside QPB9015

QPB9015 Temperature Sensing Feature

The QPB9015 provides an internal 10k NTC resistor connected to GND for temperature sensing. This resistor is located close to the amplifier stage. The resistor value can be correlated to the module backside temperature. If it is used as part of a voltage divider, current through the NTC should be limited to 1mA or less to minimize heating up of the NTC.

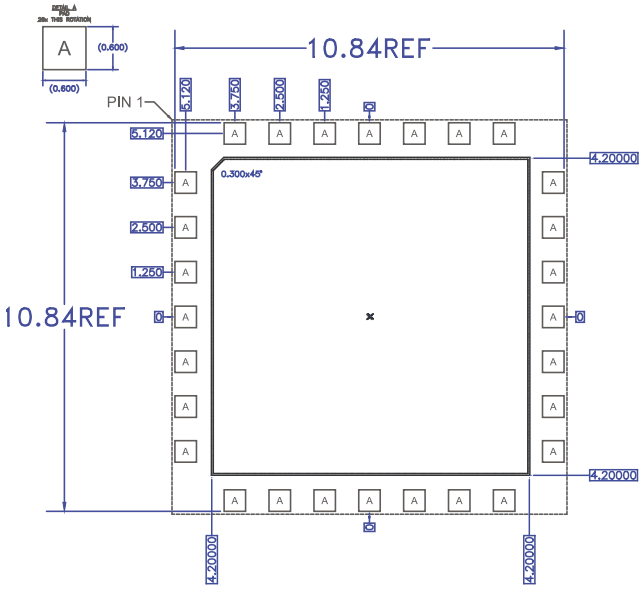


Package Outline Drawing (Dimensions in millimeters)

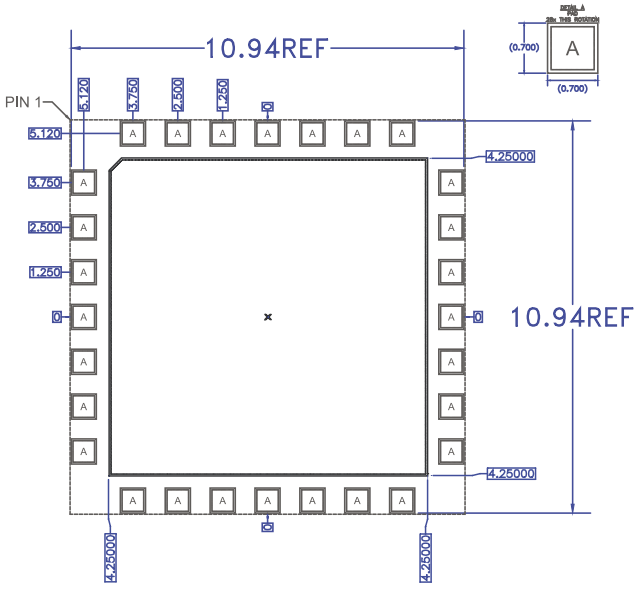


Notes:
1. Dimension and tolerance formats conform to ASME Y14.5M-1994.
2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
3. Co-planarity applies to the exposed ground/thermal pad as well as the contact pins.
4. Package body length/width does not include plastic flash protrusion across mold parting line.

PCB Metal Land Pattern (Dimensions in millimeters)



RECOMMENDED
LAND PATTERN



RECOMMENDED
LAND PATTERN MASK

Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 2 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25mm (0.10").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.
5. Do not apply solder mask to the back side of the PC board in the heat sink contact region.
6. Ensure that the backside via region makes good physical contact with the heat sink.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1A	ANSI/ESD/JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	C1	JEDEC JS-002
MSL – Moisture Sensitivity Level	3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Email: customer.support@qorvo.com

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