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#### ON Semiconductor®



#### FDMS4D4N08C

# N-Channel Shielded Gate PowerTrench® MOSFET 80 V, 123 A, 4.3 m $\Omega$

#### **Features**

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 4.3 m $\Omega$  at  $V_{GS}$  = 10 V,  $I_D$  = 44 A
- Max  $r_{DS(on)}$  = 10.4 m $\Omega$  at  $V_{GS}$  = 6 V,  $I_D$  = 22 A
- 50% Lower Qrr than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant

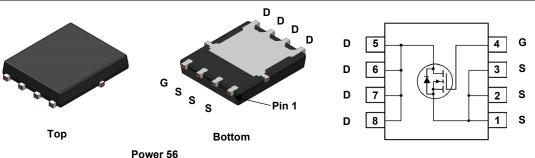
#### **General Description**

This N-Channel MV MOSFET is produced using ON Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized to minimise on-state resistance and yet maintain superior switching performance with best in class soft body diode.

#### **Applications**

- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- Solar





### **MOSFET Maximum Ratings** $T_A = 25$ °C unless otherwise noted.

Symbol	Param	eter		Ratings	Units
$V_{DS}$	Drain to Source Voltage			80	V
$V_{GS}$	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T <sub>C</sub> = 25 °C	(Note 5)	123	
	-Continuous	T <sub>C</sub> = 100 °C	(Note 5)	78	
ID	-Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	17	Α
	-Pulsed		(Note 4)	498	
E <sub>AS</sub>	Single Pulse Avalanche Energy		(Note 3)	486	mJ
D	Power Dissipation	T <sub>C</sub> = 25 °C		125	W
$P_{D}$	Power Dissipation	T <sub>A</sub> = 25 °C	(Note 1a)	2.5	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Tempera	ature Range		-55 to +150	°C

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	0/44

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS4D4N08C	FDMS4D4N08C	Power 56	13 "	12 mm	3000 units

#### **Electrical Characteristics** $T_J = 25$ °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Chara	cteristics					
$BV_{DSS}$	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 μA, referenced to 25 °C		63		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 64 V, V <sub>GS</sub> = 0 V			1	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA

#### On Characteristics

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2.0	3.0	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = 250 μA, referenced to 25 °C		-8.2		mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 44 A		3.7	4.3	
		V <sub>GS</sub> = 6 V, I <sub>D</sub> = 22 A		5.7	10.4	mΩ
, ,		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 44 A, T <sub>J</sub> = 125 °C		5.9	7.2	
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 44 A		98		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, f = 1 MHz		2920	4090	pF
C <sub>oss</sub>	Output Capacitance			1045	1465	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			35	50	pF
$R_g$	Gate Resistance		0.1	1.3	2.5	Ω

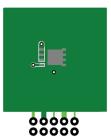
#### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		17	31	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 40 V, I <sub>D</sub> = 44 A,	7	15	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS}$ = 10 V, $R_{GEN}$ = 6 $\Omega$	25	40	ns
t <sub>f</sub>	Fall Time		5	10	ns
$Q_g$	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V	40	56	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0 \text{ V to 6 V}$ $V_{DD} = 40 \text{ V},$	25	35	nC
Q <sub>gs</sub>	Gate to Source Charge	I <sub>D</sub> = 44 A	13		nC
$Q_{gd}$	Gate to Drain "Miller" Charge		8		nC
Q <sub>oss</sub>	Output Charge	V <sub>DD</sub> = 40 V, V <sub>GS</sub> = 0 V	60		nC
Q <sub>sync</sub>	Total Gate Charge Sync.	V <sub>DS</sub> = 0 V, I <sub>D</sub> = 44 A	35		nC

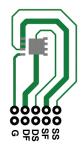
#### **Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2.1 \text{ A}$ (Note 2	)	0.7	1.2	V
	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 44 A (Note 2	)	0.8	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	L = 22 A di/dt = 200 A/		26	42	ns
Q <sub>rr</sub>	Reverse Recovery Charge	-I <sub>F</sub> = 22 A, di/dt = 300 A/μs		44	71	nC
t <sub>rr</sub>	Reverse Recovery Time	L = 22 A di/dt = 4000 A/ a		20	32	ns
Q <sub>rr</sub>	Reverse Recovery Charge	-I <sub>F</sub> = 22 A, di/dt = 1000 A/μs		106	169	nC

Notes: 1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



50 °C/W when mounted on a 1 in  $^2$  pad of 2 oz copper



125 °C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test: Pulse Width < 300 µs, Duty cycle < 2.0%.
  3. E<sub>AS</sub> of 486 mJ is based on starting T<sub>J</sub> = 25 °C; N-ch: L = 3 mH, I<sub>AS</sub> = 18 A, V<sub>DD</sub> = 80 V, V<sub>GS</sub> =10 V. 100% test at L = 0.1 mH, I<sub>AS</sub> = 51 A.
  4. Pulsed ld please refer to Fig 11 SOA graph for more details.
  5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

#### Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted.

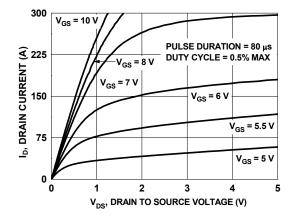


Figure 1. On Region Characteristics

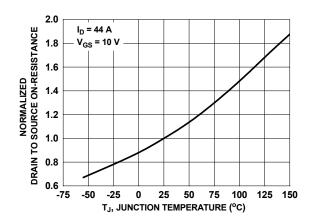


Figure 3. Normalized On Resistance vs. Junction Temperature

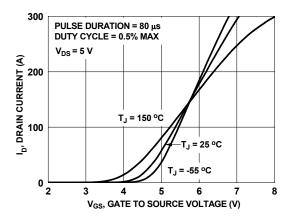


Figure 5. Transfer Characteristics

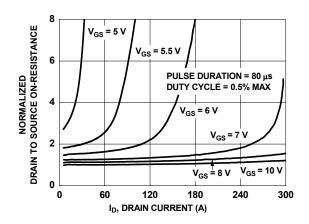


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

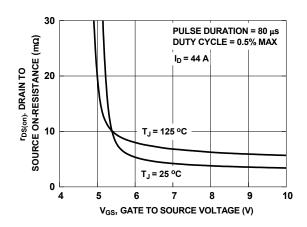


Figure 4. On-Resistance vs. Gate to Source Voltage

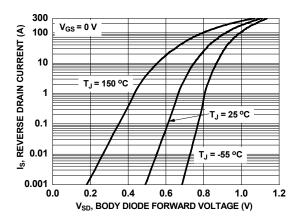


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

#### **Typical Characteristics** $T_J = 25$ °C unless otherwise noted.

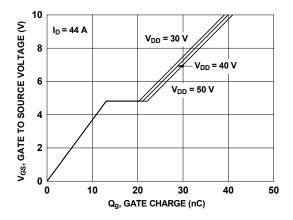


Figure 7. Gate Charge Characteristics

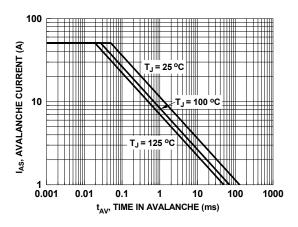


Figure 9. Unclamped Inductive Switching Capability

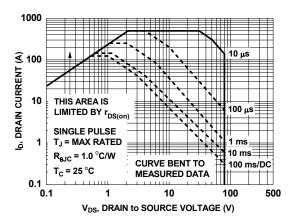


Figure 11. Forward Bias Safe Operating Area

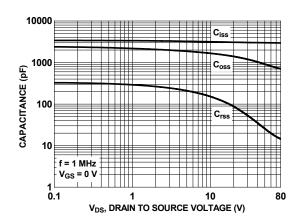


Figure 8. Capacitance vs. Drain to Source Voltage

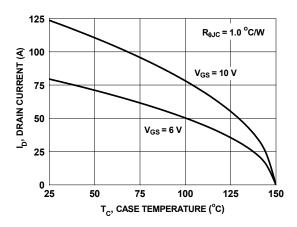


Figure 10. Maximum Continuous Drain Current vs Case Temperature

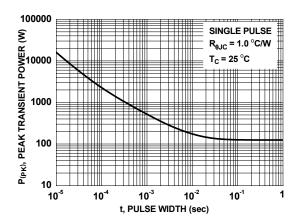


Figure 12. Single Pulse Maximum Power Dissipation



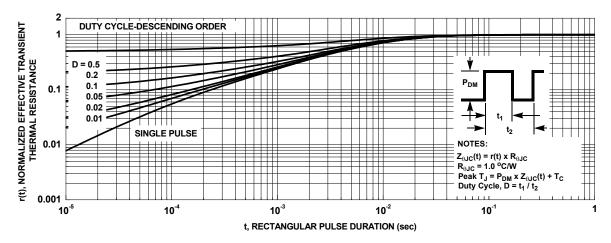
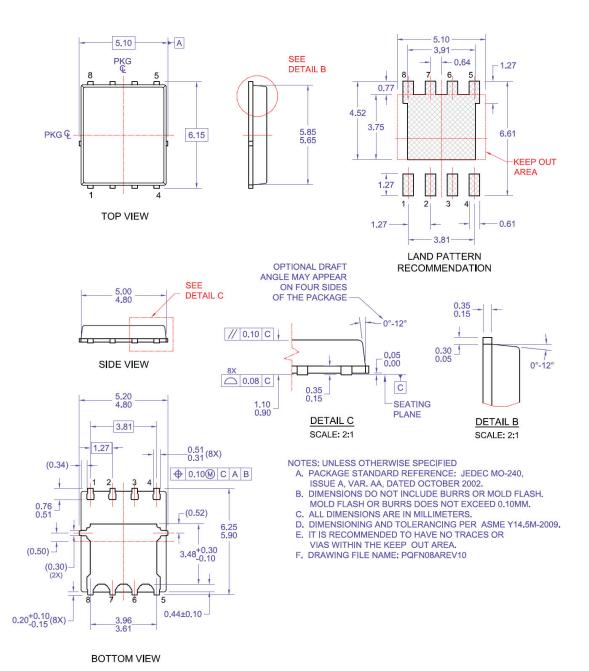


Figure 13. Junction-to-Case Transient Thermal Response Curve

#### **Dimensional Outline and Pad Layout**



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105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

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