

# FDP060AN08A0 / FDB060AN08A0

## N-Channel PowerTrench® MOSFET

75 V, 80 A, 6 mΩ

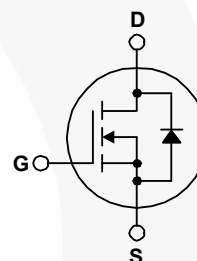
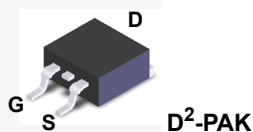
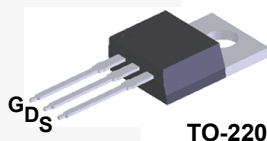
### Features

- $R_{DS(on)} = 4.8 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 80 \text{ A}$
- $Q_{G(tot)} = 73 \text{ nC}$  (Typ.) @  $V_{GS} = 10 \text{ V}$
- Low Miller Charge
- Low  $Q_{rr}$  Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)

### Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor drives and Uninterruptible Power Supplies

Formerly developmental type 82680



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDP060AN08A0 FDB060AN08A0	Unit
$V_{DSS}$	Drain to Source Voltage	75	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current		
	Continuous ( $T_C < 127^\circ\text{C}$ , $V_{GS} = 10\text{V}$ )	80	A
	Continuous ( $T_{amb} = 25^\circ\text{C}$ , $V_{GS} = 10\text{V}$ , with $R_{\theta JA} = 43^\circ\text{C/W}$ )	16	A
	Pulsed	Figure 4	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 1)	350	mJ
$P_D$	Power dissipation	255	W
	Derate above $25^\circ\text{C}$	1.7	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case, Max. TO-220, D²-PAK	0.58	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, Max. TO-220, D²-PAK (Note 2)	62	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, Max. D²-PAK, 1in² copper pad area	43	$^\circ\text{C/W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB060AN08A0	FDB060AN08A0	D <sup>2</sup> -PAK	330 mm	24 mm	800 units
FDP060AN08A0	FDP060AN08A0	TO-220	Tube	N/A	50 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
--------	-----------	-----------------	-----	-----	-----	------

### Off Characteristics

$B_{VDSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	75	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{V}$ $V_{GS} = 0\text{V}$ $T_C = 150^\circ\text{C}$	-	-	1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 80\text{A}, V_{GS} = 10\text{V}$	-	0.0048	0.006	$\Omega$
		$I_D = 40\text{A}, V_{GS} = 6\text{V}$	-	0.0066	0.010	
		$I_D = 80\text{A}, V_{GS} = 10\text{V},$ $T_J = 175^\circ\text{C}$	-	0.010	0.013	

### Dynamic Characteristics

$C_{ISS}$	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$	-	5150	-	pF	
$C_{OSS}$	Output Capacitance		-	800	-	pF	
$C_{RSS}$	Reverse Transfer Capacitance		-	230	-	pF	
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V to } 10\text{V}$	$V_{DD} = 40\text{V}$ $I_D = 80\text{A}$ $I_g = 1.0\text{mA}$	73	95	nC	
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V to } 2\text{V}$		-	10	13	nC
$Q_{gs}$	Gate to Source Gate Charge			-	29	-	nC
$Q_{gs2}$	Gate Charge Threshold to Plateau			-	19	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge			-	16	-	nC

### Switching Characteristics ( $V_{GS} = 10\text{V}$ )

$t_{ON}$	Turn-On Time	$V_{DD} = 40\text{V}, I_D = 80\text{A}$ $V_{GS} = 10\text{V}, R_{GS} = 3.9\Omega$	-	-	147	ns
$t_{d(ON)}$	Turn-On Delay Time		-	19	-	ns
$t_r$	Rise Time		-	79	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	37	-	ns
$t_f$	Fall Time		-	38	-	ns
$t_{OFF}$	Turn-Off Time		-	-	113	ns

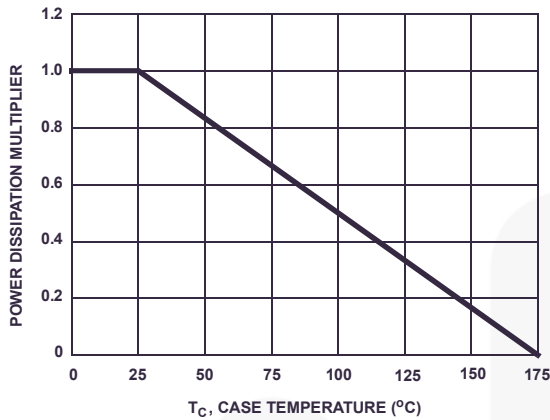
### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 80\text{A}$	-	-	1.25	V
		$I_{SD} = 40\text{A}$	-	-	1.0	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 75\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	37	ns
$Q_{RR}$	Reverse Recovered Charge	$I_{SD} = 75\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	38	nC

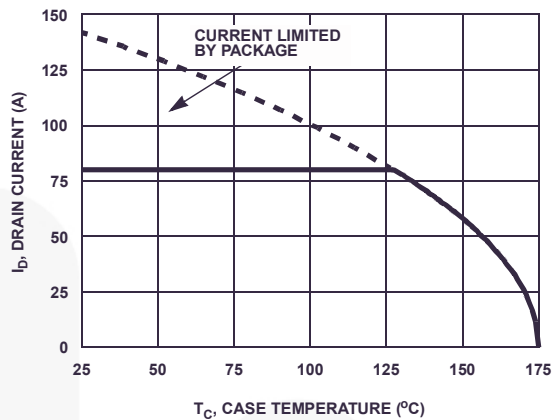
#### Notes:

- Starting  $T_J = 25^\circ\text{C}$ ,  $L = 109\mu\text{H}$ ,  $I_{AS} = 80\text{A}$ .
- Pulse width = 100s

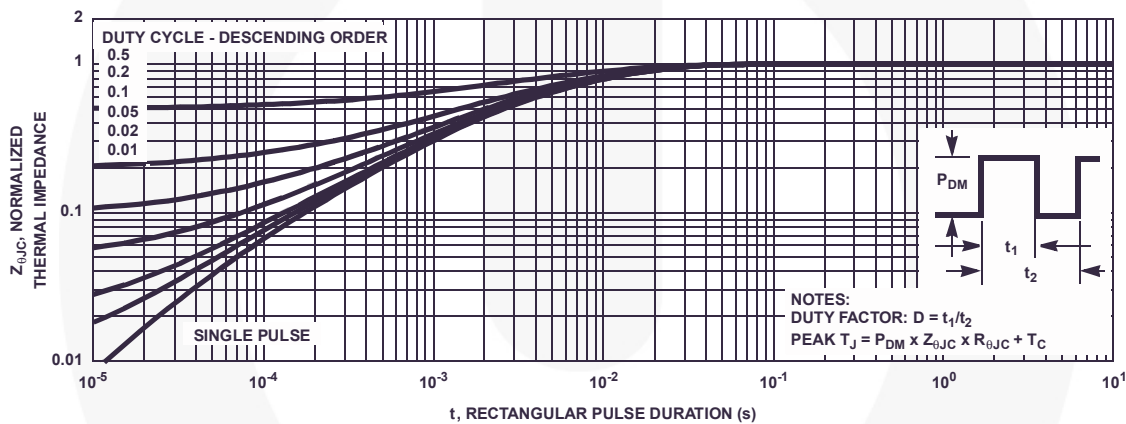
**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted



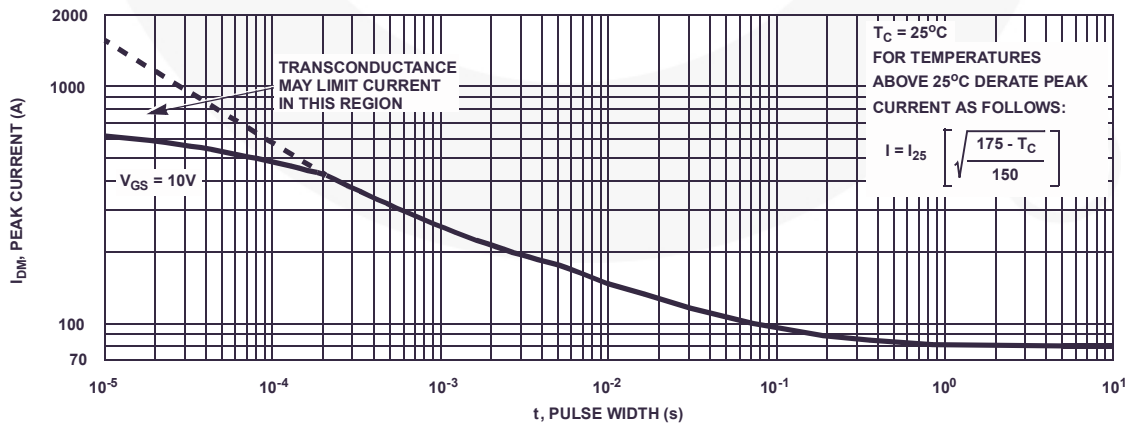
**Figure 1. Normalized Power Dissipation vs Ambient Temperature**



**Figure 2. Maximum Continuous Drain Current vs Case Temperature**

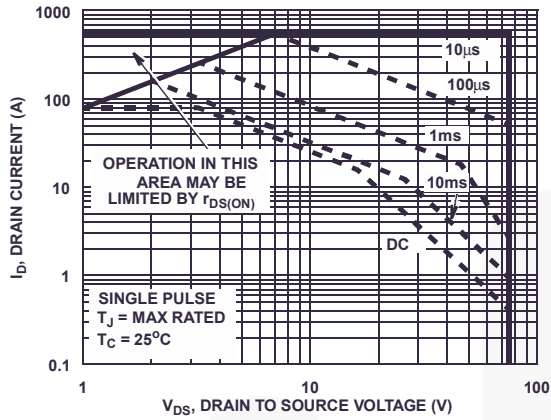


**Figure 3. Normalized Maximum Transient Thermal Impedance**

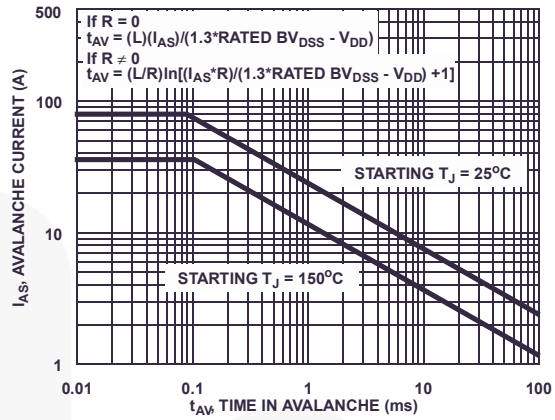


**Figure 4. Peak Current Capability**

**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted

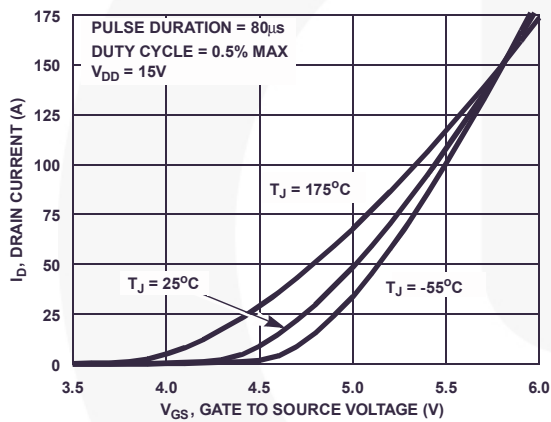


**Figure 5. Forward Bias Safe Operating Area**

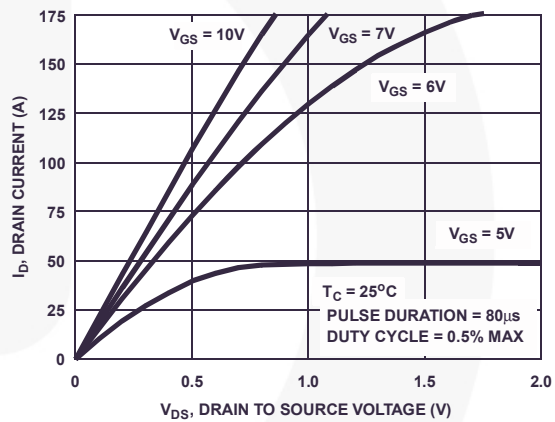


NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

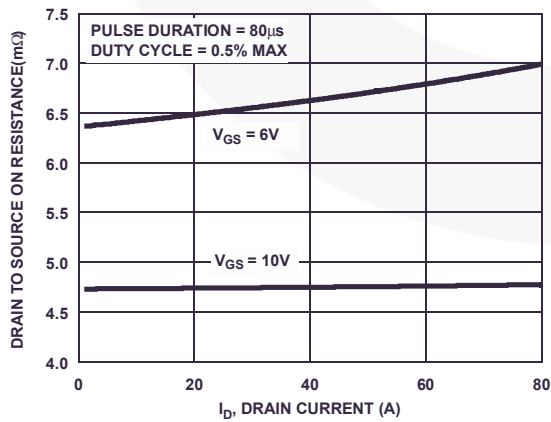
**Figure 6. Unclamped Inductive Switching Capability**



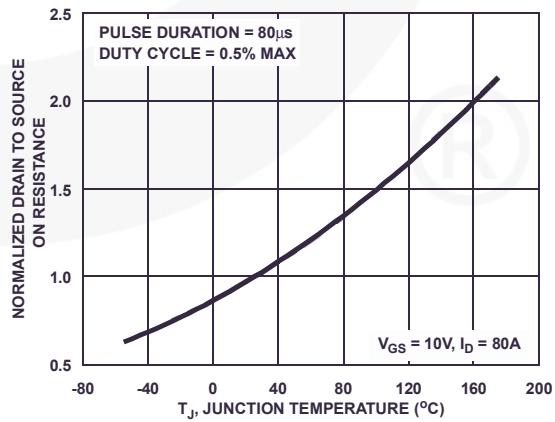
**Figure 7. Transfer Characteristics**



**Figure 8. Saturation Characteristics**

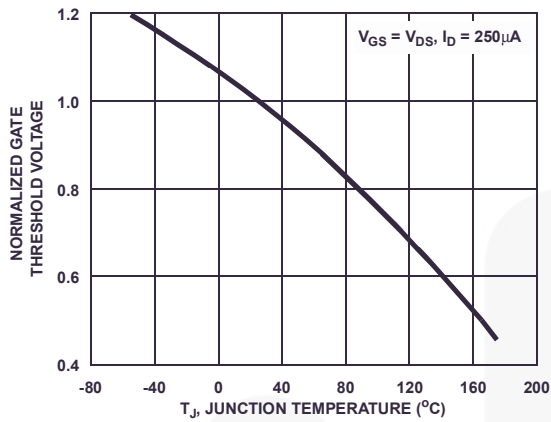


**Figure 9. Drain to Source On Resistance vs Drain Current**

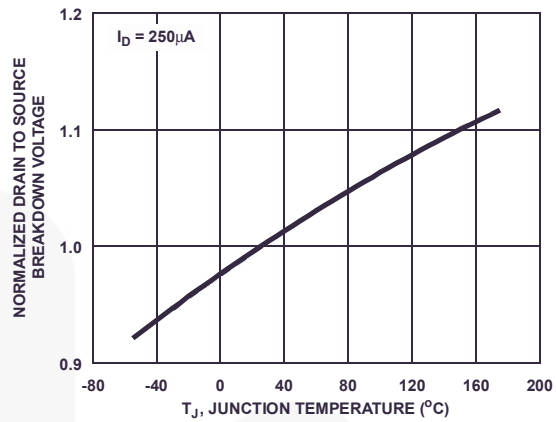


**Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature**

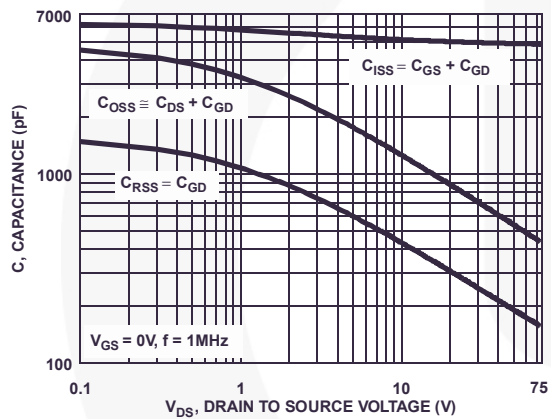
**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted



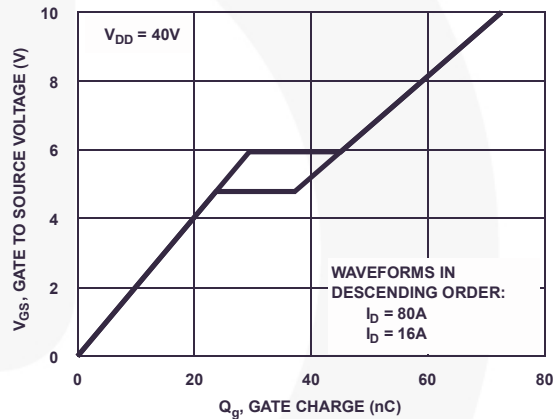
**Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature**



**Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**



**Figure 13. Capacitance vs Drain to Source Voltage**



**Figure 14. Gate Charge Waveforms for Constant Gate Current**

### Test Circuits and Waveforms

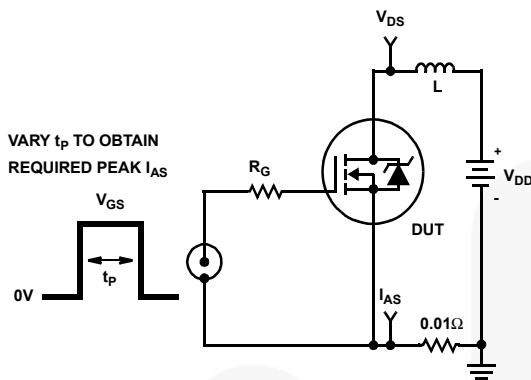


Figure 15. Unclamped Energy Test Circuit

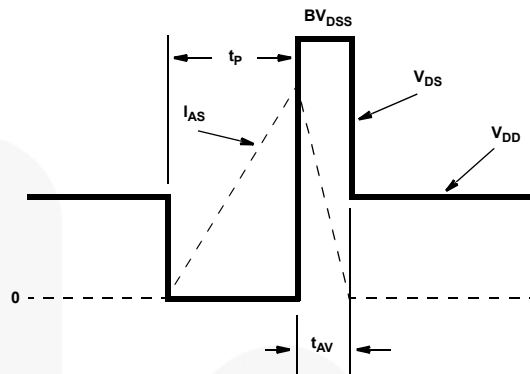


Figure 16. Unclamped Energy Waveforms

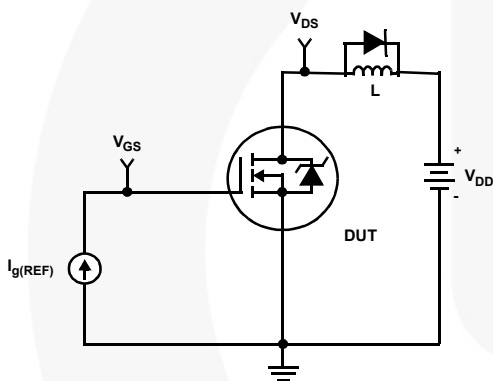


Figure 17. Gate Charge Test Circuit

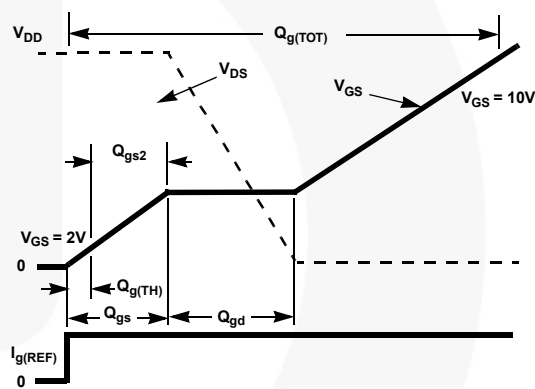


Figure 18. Gate Charge Waveforms

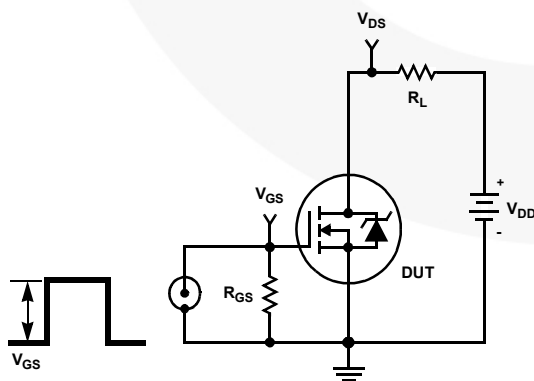


Figure 19. Switching Time Test Circuit

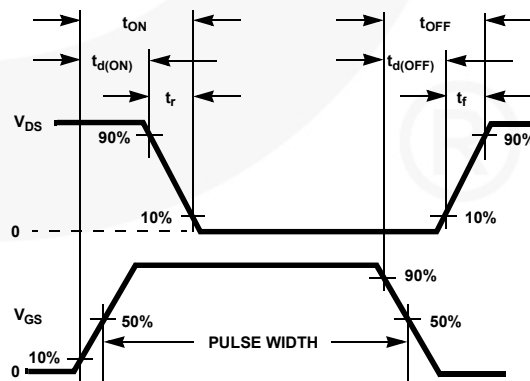


Figure 20. Switching Time Waveforms

### Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature,  $T_{JM}$ , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation,  $P_{DM}$ , in an application. Therefore the application's ambient temperature,  $T_A$  ( $^{\circ}C$ ), and thermal resistance  $R_{\theta JA}$  ( $^{\circ}C/W$ ) must be reviewed to ensure that  $T_{JM}$  is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad (\text{EQ. 1})$$

In using surface mount devices such as the TO-263 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of  $P_{DM}$  is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the  $R_{\theta JA}$  for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 26.51 + \frac{19.84}{(0.262 + Area)} \quad (\text{EQ. 2})$$

Area in Inches Squared

$$R_{\theta JA} = 26.51 + \frac{128}{(1.69 + Area)} \quad (\text{EQ. 3})$$

Area in Centimeters Squared

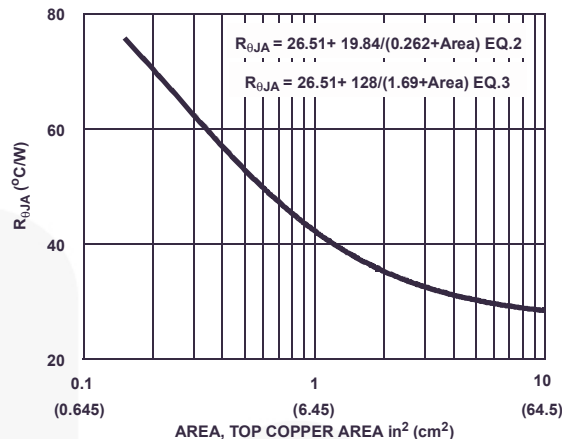


Figure 21. Thermal Resistance vs Mounting Pad Area

### PSPICE Electrical Model

.SUBCKT FDP060AN08A0 2 1 3 ; rev October 2002

Ca 12 8 2.5e-9  
Cb 15 14 2.1e-9  
Cin 6 8 4.7e-9

Dbody 7 5 DbodyMOD  
Dbreak 5 11 DbreakMOD  
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 82.1  
Eds 14 8 5 8 1  
Egs 13 8 6 8 1  
Esg 6 10 6 8 1  
Evthres 6 21 19 8 1  
Evttemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 5.3e-9  
Ldrain 2 5 1.0e-9  
Lsource 3 7 5e-9

RLgate 1 9 53  
RLdrain 2 5 10  
RLsource 3 7 50

Mmed 16 6 8 8 MmedMOD  
Mstro 16 6 8 8 MstroMOD  
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1  
Rdrain 50 16 RdrainMOD 9e-4  
Rgate 9 20 1.4  
RSLC1 5 51 RSLCMOD 1e-6  
RSLC2 5 50 1e3  
Rsource 8 7 RsourceMOD 3e-3  
Rvthres 22 8 RvthresMOD 1  
Rvtemp 18 19 RvtempMOD 1  
S1a 6 12 13 8 S1AMOD  
S1b 13 12 13 8 S1BMOD  
S2a 6 15 14 13 S2AMOD  
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1  
ESLC 51 50 VALUE={{(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51)/(1e-6\*350),5))}}

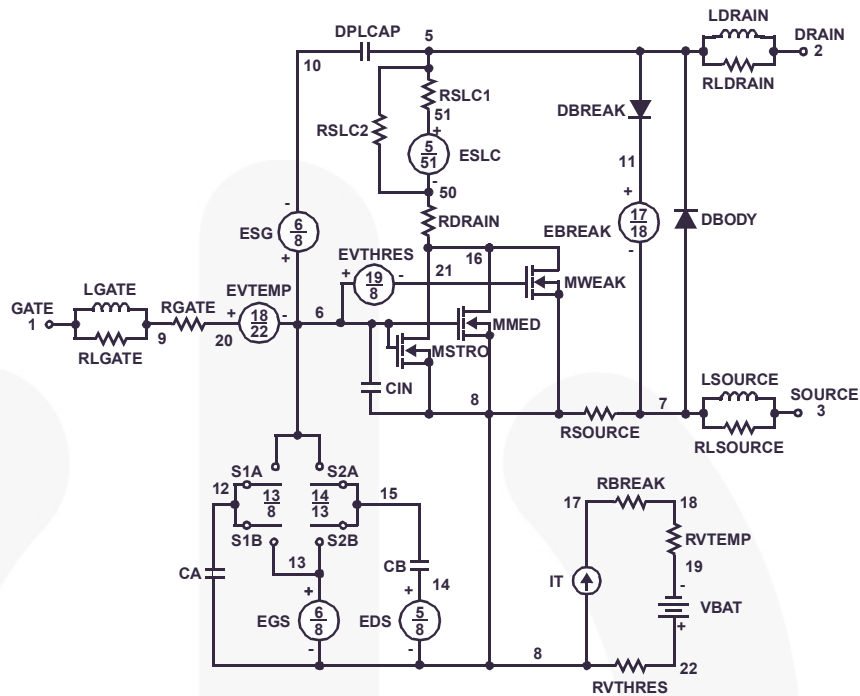
.MODEL DbodyMOD D (IS=2E-11 N=1.04 RS=1.76e-3 TRS1=2.7e-3 TRS2=1e-6  
+ CJO=3.2e-9 M=5.6e-1 TT=3e-10 XTI=3.9)  
.MODEL DbreakMOD D (RS=3e-1 TRS1=1e-3 TRS2=-8.9e-6)  
.MODEL DplcapMOD D (CJO=1.56e-9 IS=1e-30 N=10 M=0.53)

.MODEL MmedMOD NMOS (VTO=3.6 KP=6 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=1.4)  
.MODEL MstroMOD NMOS (VTO=4.22 KP=220 IS=1e-30 N=10 TOX=1 L=1u W=1u)  
.MODEL MweakMOD NMOS (VTO=3 KP=0.03 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=14 RS=0.1)

.MODEL RbreakMOD RES (TC1=9.4e-4 TC2=-9e-7)  
.MODEL RdrainMOD RES (TC1=2.2e-2 TC2=6e-5)  
.MODEL RSLCMOD RES (TC1=2e-3 TC2=1e-5)  
.MODEL RsourceMOD RES (TC1=1e-3 TC2=1e-6)  
.MODEL RvthresMOD RES (TC1=-6e-3 TC2=-1.6e-5)  
.MODEL RvtempMOD RES (TC1=-2.4e-3 TC2=1e-6)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-8 VOFF=-5)  
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-5 VOFF=-8)  
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4 VOFF=-3.5)  
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.5 VOFF=-4)  
.ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.





## SABER Electrical Model

rev October 2002

template FDP060AN08A0 n2,n1,n3

electrical n2,n1,n3

{

var i iscl

dp..model dbodymod = (isl=2e-11,nl=1.04,rs=1.76e-3,trs1=2.7e-3,trs2=1e-6,cjo=3.2e-9,m=5.6e-1,tt=3e-10,xti=3.9)

dp..model dbreakmod = (rs=3e-1,trs1=1e-3,trs2=-8.9e-6)

dp..model dplcapmod = (cjo=1.56e-9,isl=10e-30,nl=10,m=0.53)

m..model mmedmod = (type=\_n,vto=3.6,kp=6, is=1e-30, tox=1)

m..model mstrongmod = (type=\_n,vto=4.22,kp=220, is=1e-30, tox=1)

m..model mweakmod = (type=\_n,vto=3,kp=0.03, is=1e-30, tox=1,rs=0.1)

sw\_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-8,voff=-5)

sw\_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-5,voff=-8)

sw\_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-4,voff=-3.5)

sw\_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=-3.5,voff=-4)

c.ca n12 n8 = 2.5e-9

c.cb n15 n14 = 2.1e-9

c.cin n6 n8 = 4.7e-9

dp.dbody n7 n5 = model=dbodymod

dp.dbreak n5 n11 = model=dbreakmod

dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 82.1

spe.eds n14 n8 n5 n8 = 1

spe.egs n13 n8 n6 n8 = 1

spe.esg n6 n10 n6 n8 = 1

spe.evthres n6 n21 n19 n8 = 1

spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 5.3e-9

l.ldrain n2 n5 = 1.0e-9

l.lsource n3 n7 = 5e-9

res.rlgate n1 n9 = 53

res.rldrain n2 n5 = 10

res.rlsource n3 n7 = 50

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u

m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u

m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1=9.4e-4,tc2=-9e-7

res.rdrain n50 n16 = 9e-4, tc1=2.2e-2,tc2=6e-5

res.rgate n9 n20 = 1.4

res.rslc1 n5 n51 = 1e-6, tc1=2e-3,tc2=1e-5

res.rslc2 n5 n50 = 1e3

res.rsource n8 n7 = 3e-3, tc1=1e-3,tc2=1e-6

res.rvthres n22 n8 = 1, tc1=-6e-3,tc2=-1.6e-5

res.rvtemp n18 n19 = 1, tc1=-2.4e-3,tc2=1e-6

sw\_vcsp.s1a n6 n12 n13 n8 = model=s1amod

sw\_vcsp.s1b n13 n12 n13 n8 = model=s1bmod

sw\_vcsp.s2a n6 n15 n14 n13 = model=s2amod

sw\_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

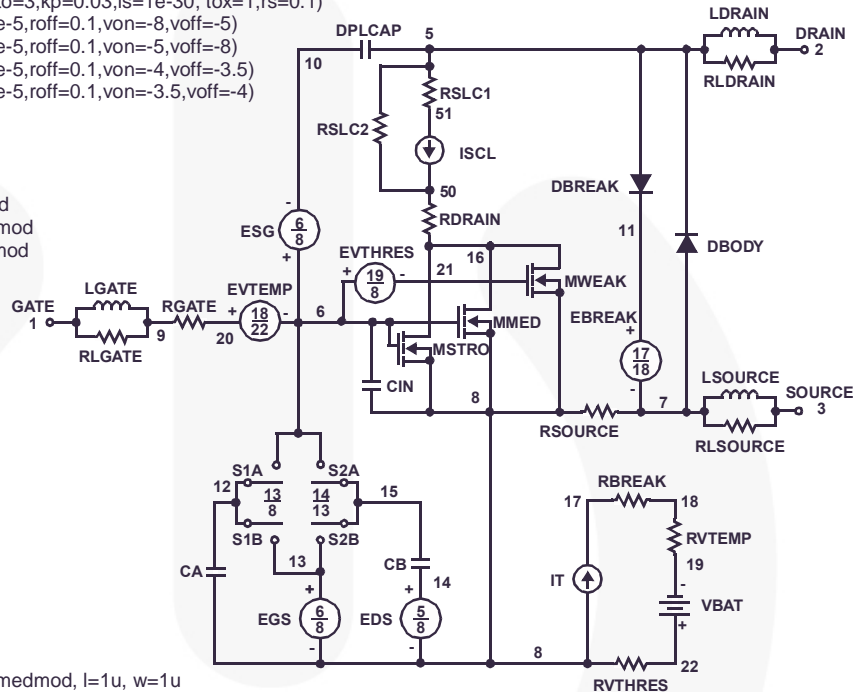
equations {

i (n51->n50) +=iscl

iscl: v(n51,n50) = (((v(n5,n51))/(1e-9+abs(v(n5,n51))))\*((abs(v(n5,n51))\*1e6/350)\*\* 5))

}

}



### SPICE Thermal Model

REV 23 October 2002

FDP060AN08A0T

CTHERM1 TH 6 9.6e-3  
 CHERM2 6 5 9.7e-3  
 CHERM3 5 4 9.8e-3  
 CHERM4 4 3 1e-2  
 CHERM5 3 2 3e-2  
 CHERM6 2 TL 9e-2

R THERM1 TH 6 3.2e-3  
 R THERM2 6 5 8.1e-3  
 R THERM3 5 4 2.3e-2  
 R THERM4 4 3 1.2e-1  
 R THERM5 3 2 1.5e-1  
 R THERM6 2 TL 1.6e-1

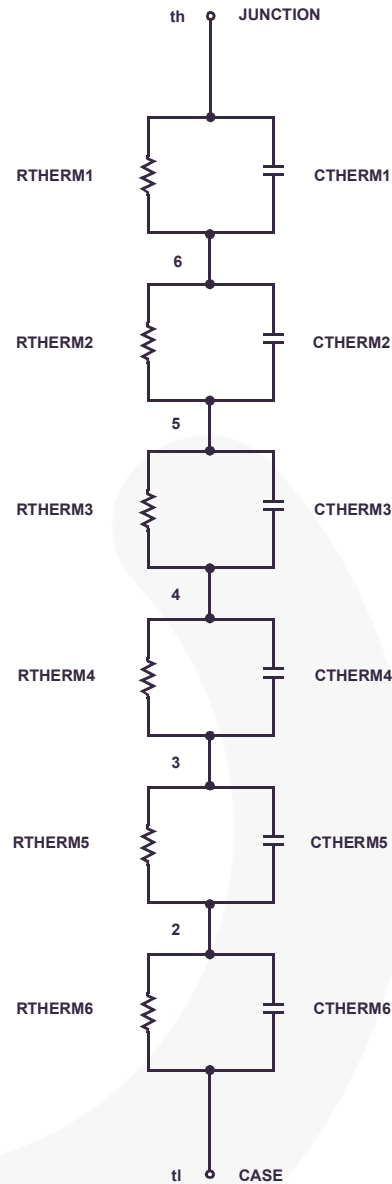
### SABER Thermal Model

SABER thermal model FDP060AN08A0T

template thermal\_model th tl  
 thermal\_c th, tl

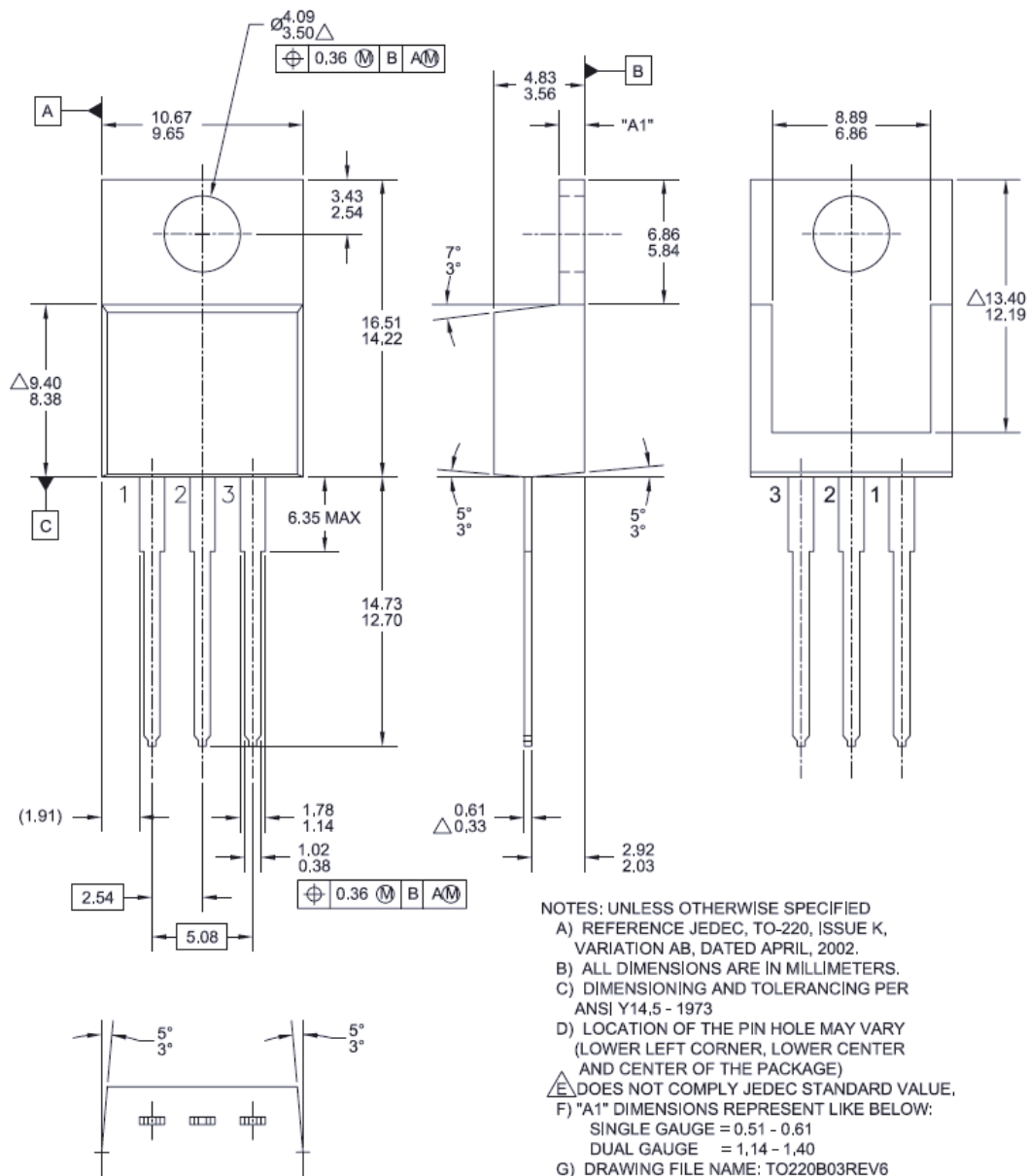
```
{
    ctherm.therm1 th 6 =9.6e-3
    ctherm.therm2 6 5 =9.7e-3
    ctherm.therm3 5 4 =9.8e-3
    ctherm.therm4 4 3 =1e-2
    ctherm.therm5 3 2 =3e-2
    ctherm.therm6 2 tl =9e-2
```

```
rtherm.rtherm1 th 6 =3.2e-3
rtherm.rtherm2 6 5 =8.1e-3
rtherm.rtherm3 5 4 =2.3e-2
rtherm.rtherm4 4 3 =1.2e-1
rtherm.rtherm5 3 2 =1.5e-1
rtherm.rtherm6 2 tl =1.6e-1
}
```



## Mechanical Dimensions

### TO-220 3L



**Figure 22. TO-220, Molded, 3Lead, Jedec Variation AB**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

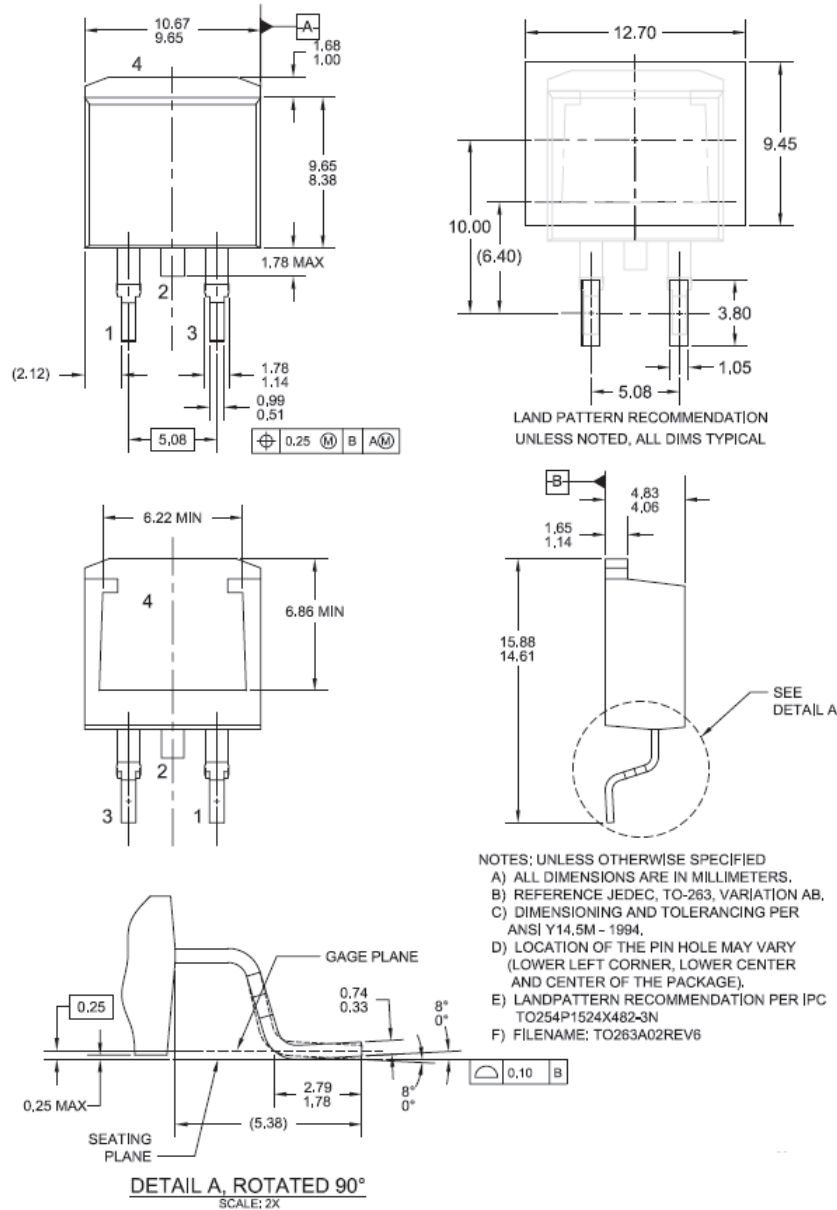
Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

[http://www.fairchildsemi.com/package/packageDetails.html?id=PN\\_TT220-003](http://www.fairchildsemi.com/package/packageDetails.html?id=PN_TT220-003)

Dimension in Millimeters

**Mechanical Dimensions**

**TO-263 2L (D<sup>2</sup>PAK)**



**Figure 23. 2LD, TO263, Surface Mount**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:






[http://www.fairchildsemi.com/package/packageDetails.html?id=PN\\_TT263-002](http://www.fairchildsemi.com/package/packageDetails.html?id=PN_TT263-002)

Dimension in Millimeters



**TRADEMARKS**

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- |  |   |  |
|--|---|--|
| AccuPower™   | F-PFS™  | Sync-Lock™   |
| AX-CAP®*   | FRFET®  |  SYSTEM GENERAL®* |
| BitSiC™  | Global Power ResourceSM   | TinyBoost®   |
| Build it Now™  | GreenBridge™  | TinyBuck®  |
| CorePLUS™  | Green FPS™  | TinyCalc™  |
| CorePOWER™   | Green FPS™ e-Series™  | TinyLogic®   |
| CROSSVOLT™   | Gmax™   | TINYOPTO™  |
| CTL™   | GTO™  | TinyPower™   |
| Current Transfer Logic™  | IntelliMAX™   | TinyPWM™   |
| DEUXPEED®  | ISOPLANAR™  | TinyWire™  |
| Dual Cool™   | Marking Small Speakers Sound Louder and Better™   | TranSiC™   |
| EcoSPARK®  | MegaBuck™   | TriFault Detect™   |
| EfficientMax™  | MICROCOUPLER™   | TRUECURRENT®*  |
| ESBC™  | MicroFET™   | µSerDes™   |
|  Fairchild® | MicroPak™   |  SerDes®          |
| Fairchild Semiconductor®   | MicroPak2™  | UHC®   |
| FACT Quiet Series™   | MillerDrive™  | Ultra FRFET™   |
| FACT®  | MotionMax™  | UniFET™  |
| FAST®  | mWSaver®  | VCX™   |
| FastvCore™   | OptoHiT™  | VisualMax™   |
| FETBench™  | OPTOLOGIC®  | VoltagePlus™   |
| FPS™   | OPTOPLANAR®   | XS™  |
|  |   |  |
|  |  PowerTrench®                          |  |
|  | PowerXS™  |  |
|  | Programmable Active Droop™  |  |
|  | QFET®   |  |
|  | QS™   |  |
|  | Quiet Series™   |  |
|  | RapidConfigure™   |  |
|  |  Saving our world, 1mW/W/kW at a time™ |  |
|  | SignalWise™   |  |
|  | SmartMax™   |  |
|  | SMART START™  |  |
|  | Solutions for Your Success™   |  |
|  | SPM®  |  |
|  | STEALTH™  |  |
|  | SuperFET®   |  |
|  | SuperSOT™-3   |  |
|  | SuperSOT™-6   |  |
|  | SuperSOT™-8   |  |
|  | SupreMOS®   |  |
|  | SyncFET™  |  |

\*Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used here in:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**ANTI-COUNTERFEITING POLICY**

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, [www.Fairchildsemi.com](http://www.Fairchildsemi.com), under Sales Support. Counterfeiting of semiconductor parts is a growing problem in the industry. All manufactures of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed application, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address and warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I66

## Данный компонент на территории Российской Федерации

### Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

### Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

Skype отдела продаж:

moschip.ru

moschip.ru\_4

moschip.ru\_6

moschip.ru\_9