Features

- **E^2 Programmable 524,288 x 1 and 1,048,576 x 1 bit Serial Memories Designed To Store Configuration Programs For Field Programmable Gate Arrays (FPGA)**
- **Simple Interface to SRAM FPGAs**
- **Compatible With Atmel AT6000, AT40K FPGAs, Altera EPF8K, EPF10K, EPF6K FPGAs, ORCA FPGAs, Xilinx XC3000, XC4000, XC5200 FPGAs, Motorola MPA1000 FPGAs**
- **Cascadable To Support Additional Configurations or Future Higher-density Arrays**
- **Low-power CMOS EEPROM Process**
- **Programmable Reset Polarity**
- **Available In PLCC Package (Pin Compatable across Product Family)**
- **In-System Programmable Via 2-Wire Bus**
- **Emulation of 24CXX Serial EPROMs**
- **Available in 3.3V ± 10% LV and 5V Versions**
- **System Friendly READY Pin**

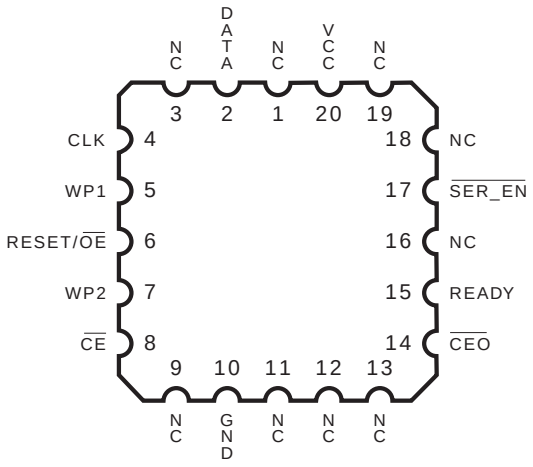
Description

The AT17C512/010 and AT17LV512/010 (high-density AT17 Series) FPGA Configuration EEPROMs (Configurators) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. The high-density AT17 Series is packaged in the popular 20-pin PLCC. The high-density AT17 Series family uses a simple serial-access procedure to configure one or more FPGA devices. The high-density AT17 Series organization supplies enough memory to configure one or multiple smaller FPGAs. The user can select the polarity of the reset function by programming one EEPROM byte. The devices also support a write protection mode and a system friendly READY pin, which signifies a “good” power level to the device and can be used to ensure reliable system power-up.

The high-density AT17 Series can be programmed with industry-standard programmers, and the Atmel ATDH2200 Programming board.

Pin Configurations

20-Pin PLCC



FPGA Configuration E^2PROM Memory

512K and 1M

AT17C512
AT17LV512
AT17C010
AT17LV010

Rev. 0944A-A–12/97

Controlling The High-Density AT17 Series Serial EEPROMs

Most connections between the FPGA device and the Serial EEPROM are simple and self-explanatory:

- The DATA output of the high-density AT17 Series drives DIN of the FPGA devices.
- The master FPGA CCLK output drives the CLK input of the high-density AT17 Series.
- The $\overline{CEO}$ output of any AT17C/LV512/010 drives the $\overline{CE}$ input of the next AT17C/LV512/010 in a cascade chain of PROMs.
- $\overline{SER_EN}$ must be connected to V_{CC}, (except during ISP).

READY is available as an open-collector indicator of the device's RESET status; it is driven Low while the device is in its POWER-ON RESET cycle and released (tri-stated) when the cycle is complete.

There are two different ways to use the inputs $\overline{CE}$ and $\overline{OE}$, as shown in the AC Characteristics waveforms.

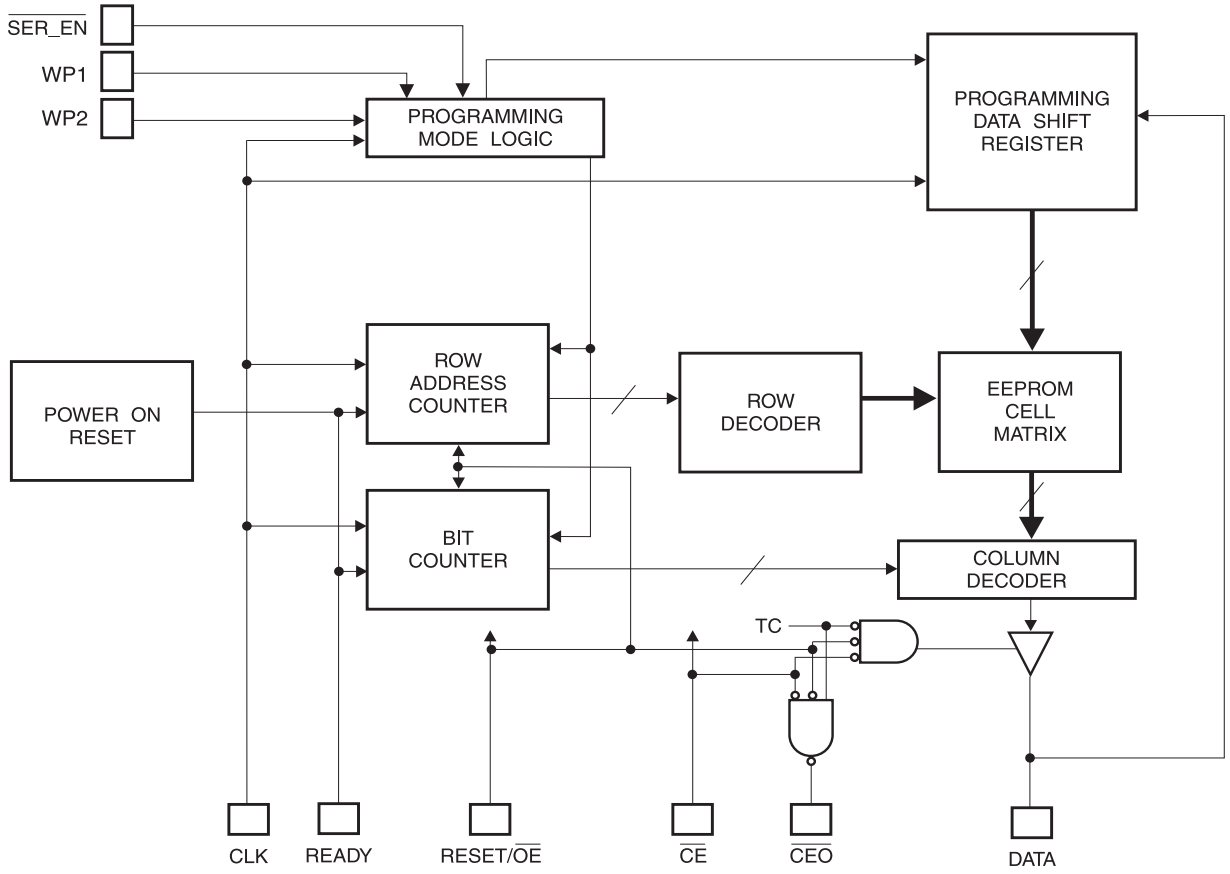
Condition 1

The simplest connection is to have the FPGA D/$\overline{P}$ output drive both $\overline{CE}$ and RESET/$\overline{OE}$ in parallel (Figure 1). Due to its simplicity, however, this method will fail if the FPGA receives an external reset condition during the configuration cycle. If a system reset is applied to the FPGA, it will abort the original configuration and then reset itself for a new configuration, as intended. Of course, the high-density AT17 Series does not see the external reset signal and will not reset its internal address counters and, consequently, will remain out of sync with the FPGA for the remainder of the configuration cycle.

Condition 2

The FPGA D/$\overline{P}$ output drives only the $\overline{CE}$ input of the high-density AT17 Series, while its $\overline{OE}$ input is driven by the inversion of the input to the FPGA $\overline{RESET}$ input pin. This connection works under all normal circumstances, even when the user aborts a configuration before D/$\overline{P}$ has gone High. A High level on the RESET/$\overline{OE}$ input to the AT17C/LVxxx – during FPGA reset – clears the Configurator's internal address pointer, so that the reconfiguration starts at the beginning. The high-density AT17 Series does not require an inverter since the RESET polarity is programmable.

Block Diagram



Pin Configurations

20 PLCC	Name	I/O	Description
2	DATA	I/O	Three-state DATA output for reading. Input/Output pin for programming.
4	CLK	I	Clock input. Used to increment the internal address and bit counter for reading and programming.
5	WP1	I	WRITE PROTECT (1). Used to protect portions of memory during programming. See programming guide for details.
6	RESET/$\overline{OE}$	I	RESET/Output Enable input (when $\overline{SER_EN}$ is High). A Low level on both the $\overline{CE}$ and RESET/$\overline{OE}$ inputs enables the data output driver. A High level on RESET/$\overline{OE}$ resets both the address and bit counters. The logic polarity of this input is programmable as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE. This document describes the pin as RESET/$\overline{OE}$.
7	WP2	I	WRITE PROTECT (2). Used to protect portions of memory during programming. See programming guide for details.
8	$\overline{CE}$	I	Chip Enable input. Used for device selection. A Low level on both $\overline{CE}$ and $\overline{OE}$ enables the data output driver. A High level on $\overline{CE}$ disables both the address and bit counters and forces the device into a low power mode. Note this pin will not enable/disable the device in 2-wire Serial Programming mode (i.e., when $\overline{SER_EN}$ is Low).
10	GND		Ground pin.
14	$\overline{CEO}$	O	Chip Enable Out output. This signal is asserted Low on the clock cycle following the last bit read from the memory. It will stay Low as long as CE and $\overline{OE}$ are both Low. It will then follow $\overline{CE}$ until $\overline{OE}$ goes High. Thereafter, $\overline{CEO}$ will stay High until the entire PROM is read again and senses the status of RESET polarity.
	A2	I	Device selection input, A2. This is used to enable (or select) the device during programming, when $\overline{SER_EN}$ is Low (see Programming Guide for more details)
15	READY	O	Open collector reset state indicator. Driven Low during power-up reset, released when power-up is complete. (Recommend a 4.7KΩ Pull-up on this pin if used).
17	$\overline{SER_EN}$	I	Serial enable is normally high during FPGA loading operations. Bringing SER_EN Low, enables the two wire serial interface mode for programming.
20	V_{CC}		+3.3V/+5V power supply pin.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to V_{CC} + 0.5V
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10 s @ 1/16 in.)	260°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

FPGA Master Serial Mode Summary

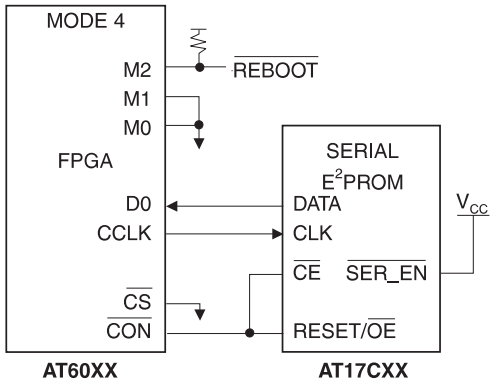
The I/O and logic functions of the FPGA and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Mode, the FPGA automatically loads the configuration program from an external memory. The Serial Configuration EEPROM has been designed for compatibility with the Master Serial Mode.

Cascading Serial Configuration EEPROMs

For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded Configurators provide additional memory.

As the last bit from the first Configurator is read, the clock signal to the Configurator asserts its $\overline{CEO}$ output Low and disables its DATA line. The second Configurator recognizes the Low level on its $\overline{CE}$ input and enables its DATA output.

Figure 1. Condition 1 Connection



After configuration is complete, the address counters of all cascaded Configurators are reset if the reset signal drives the RESET/$\overline{OE}$ on each Configurator to its active (High) level.

If the address counters are not to be reset upon completion, then the RESET/$\overline{OE}$ inputs can be tied to ground. For more details, please reference the AT17C Series Programming Guide.

Programming Mode

The programming mode is entered by bringing $\overline{SER_EN}$ Low. In this mode the chip can be programmed by the 2-wire interface. The programming is done at V_{CC} supply only. Programming super voltages are generated inside the chip. See the Programming Specification for Atmel's Configuration Memories Application Note for further information. The AT17C Series parts are read/write at 5V nominal. The AT17LV parts are read/write at 3.3V nominal.

AT17C/LVXXX Reset Polarity

The AT17C/LVXXX lets the user choose the reset polarity as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE.

Standby Mode

The AT17C/LVXXX enters a low-power standby mode whenever $\overline{CE}$ is asserted High. In this mode, the Configurator consumes less than 0.5mA at 5.0 volts. The output remains in a high impedance state regardless of the state of the $\overline{OE}$ input.

Operating Conditions

Symbol	Description		AT17CXXX Min/Max	AT17LVXXX Min/Max	Units
V_{CC}	Commercial	Supply voltage relative to GND -0°C to +70°C	4.75 / 5.25	3.0 / 3.6	V
	Industrial	Supply voltage relative to GND -40°C to +85°C	4.5 / 5.5	3.0 / 3.6	V
	Military	Supply voltage relative to GND -55°C to +125°C	4.5 / 5.5	3.0 / 3.6	V

DC Characteristics

V_{CC} = 5V ± 5% Commercial / 5V ± 10% Ind./Mil.

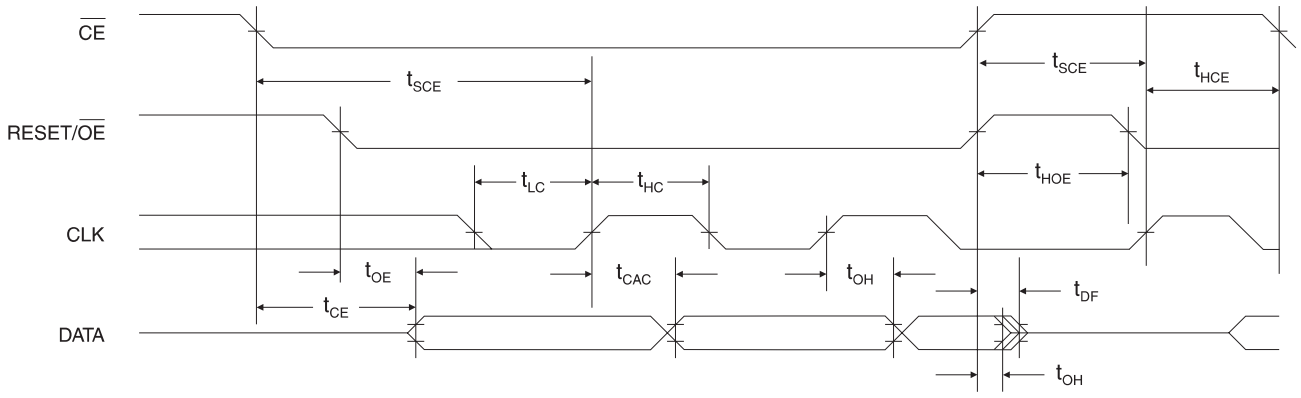
Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Commercial	3.86		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.32	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Industrial	3.76		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.37	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Military	3.7		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.4	V
I_{CCA}	Supply current, active mode (at FMAX)			10	mA
I_L	Input or output leakage current (V_{IN} = V_{CC} or GND)		-10	10	µA
I_{CCS}	Supply current, standby mode	Commercial		0.5	mA
		Industrial/Military		0.5	mA

DC Characteristics

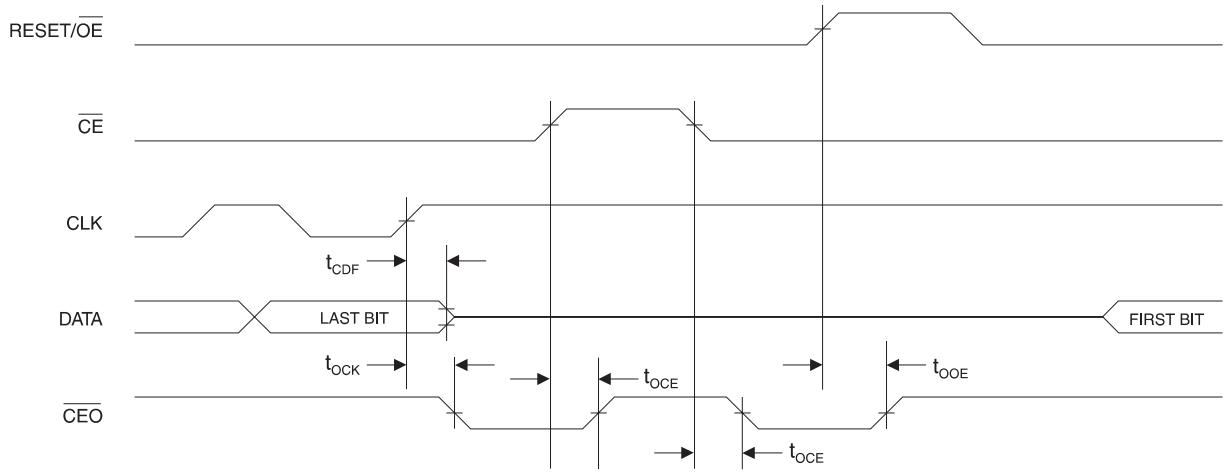
V_{CC} = 3.3V ± 10%

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -2.5 mA)	Commercial	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)			0.4	V
V_{OH}	High-level output voltage (I_{OH} = -2 mA)	Industrial	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)			0.4	V
V_{OH}	High-level output voltage (I_{OH} = -2 mA)	Military	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +2.5 mA)			0.4	V
I_{CCA}	Supply current, active mode			5	mA
I_L	Input or output leakage current (V_{IN} = V_{CC} or GND)		-10	10	µA
I_{CCS}	Supply current, standby mode	Commercial		100	µA
		Industrial/Military		100	µA

AC Characteristics



AC Characteristics When Cascading



.

AC Characteristics for AT17C512/010

V_{CC} = 5V ± 5% Commercial / V_{CC} = 5V ± 10% Ind./Mil

Symbol	Description	Commercial/Industrial		Military		Units
		Min	Max	Min	Max	
T_{OE} (2)	$\overline{OE}$ to Data Delay		30		35	ns
T_{CE} (2)	$\overline{CE}$ to Data Delay		45		45	ns
T_{CAC} (2)	CLK to Data Delay		50		50	ns
T_{OH} (2)	Data Hold From $\overline{CE}$, $\overline{OE}$, or CLK	0		0		ns
T_{DF} (3)	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay		50		50	ns
T_{LC}	CLK Low Time	20		20		ns
T_{HC}	CLK High Time	20		20		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	20		25		ns
T_{HCE}	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)	0		0		ns
T_{HOE}	$\overline{OE}$ High Time (Guarantees Counter Is Reset)	20		20		ns
F_{MAX}	MAX Input Clock Frequency	15		15		MHz
V_{RDY}	Ready Pin Open Collector Voltage	1.2	2.2	1.2	2.2	V

AC Characteristics for AT17C512/010 When Cascading

V_{CC} = 5V± 5% Commercial / V_{CC} = 5V ± 10% Ind./Mil.

Symbol	Description	Commercial/Industrial		Military		Units
		Min	Max	Min	Max	
T_{CDF} (3)	CLK to Data Float Delay		50		50	ns
T_{OCK} (2)	CLK to $\overline{CEO}$ Delay		35		40	ns
T_{OCE} (2)	CE to $\overline{CEO}$ Delay		35		35	ns
T_{OOE} (2)	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		30		30	ns

Notes: 1. Preliminary specifications for military operating range only.

2. AC test load = 50 pF.

3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady state active levels.

AC Characteristics for AT17LV512/010

V_{CC} = 3.3V ± 10%

Symbol	Description	Commercial/Industrial		Military		Units
		Min	Max	Min	Max	
T_{OE}[2]	$\overline{OE}$ to Data Delay		50		55	ns
T_{CE}[2]	$\overline{CE}$ to Data Delay		55		60	ns
T_{CAC}[2]	CLK to Data Delay		55		60	ns
T_{OH}	Data Hold From $\overline{CE}$, $\overline{OE}$, or CLK	0		0		ns
T_{DF}[3]	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay		50		50	ns
T_{LC}	CLK Low Time	25		25		ns
T_{HC}	CLK High Time	25		25		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	30		35		ns
T_{HCE}	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)	0		0		ns
T_{HOE}	$\overline{OE}$ High Time (Guarantees Counter Is Reset)	25		25		ns
F_{MAX}[4]	MAX Input Clock Frequency	15		10		MHz
V_{RDY}	Ready Pin Open Collector Voltage	1.2	2.2	1.2	2.2	V

Notes: 1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady state active levels.
4. During cascade F_{MAX} = 12.5 MHz.

AC Characteristics for AT17LV512/010 When Cascading

V_{CC} = 3.3V ± 10%

Symbol	Description	Commercial/Industrial		Military		Units
		Min	Max	Min	Max	
T_{CDF}[3]	CLK to Data Float Delay		50		50	ns
T_{OCK}[2]	CLK to $\overline{CEO}$ Delay		50		55	ns
T_{OCE}[2]	CE to $\overline{CEO}$ Delay		35		40	ns
T_{OOE}[2]	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		35		35	ns

Ordering Information - 5V Devices

Memory Size	Ordering Code	Package	Operation Range
512K	AT17C512-10JC	20J	Commercial (0°C to 70°C)
	AT17C512-10JI	20J	Industrial (-40°C to 85°C)
1M	AT17C010-10JC	20J	Commercial (0°C to 70°C)
	AT17C010-10JI	20J	Industrial (-40°C to 85°C)

Ordering Information - 3.3V Devices

Memory Size	Ordering Code	Package	Operation Range
512K	AT17LV512-10JC	20J	Commercial (0°C to 70°C)
	AT17LV512-10JI	20J	Industrial (-40°C to 85°C)
1M	AT17LV010-10JC	20J	Commercial (0°C to 70°C)
	AT17LV010-10JI	20J	Industrial (-40°C to 85°C)

Package Type	
20J	20 Lead, Plastic J-Leaded Chip Carrier (PLCC)

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