Polyphase Energy Metering IC with Pulse Output

ADE7752/ADE7752A

FEATURES

High accuracy, supports 50 Hz/60 Hz IEC62053-2x
Less than 0.1% error over a dynamic range of 500 to 1
Compatible with 3-phase/3-wire delta and 3-phase/4-wire Wye configurations
The ADE7752 supplies average real power on frequency outputs F1 and F2
High frequency output CF is intended for calibration and supplies instantaneous real power
Logic output REVP indicates a potential miswiring or negative power for each phase
Direct drive for electromechanical counters and 2-phase stepper motors (F1 and F2)
Proprietary ADCs and DSP provide high accuracy over large variations in environmental conditions and time
On-chip power supply monitoring
On-chip creep protection (no load threshold)
On-chip reference 2.4 V ±8% (20 ppm/°C typical) with external overdrive capability
Single 5 V supply, low power
60 mW typical: ADE7752
30 mW typical: ADE7752A
Low cost CMOS process

GENERAL DESCRIPTION

The ADE7752 is a high accuracy polyphase electrical energy measurement IC. The ADE7752A is a pin-to-pin compatible low power version of ADE7752. The functions of ADE7752 and ADE7752A are the same. Both products are referred to in the text of this data sheet as ADE7752.

The part specifications surpass the accuracy requirements as quoted in the IEC62053-2x standard. The only analog circuitry used in the ADE7752 is in the analog-to-digital converters (ADCs) and reference circuit. All other signal processing (such as multiplication, filtering, and summation) is carried out in the digital domain. This approach provides superior stability and accuracy over extremes in environmental conditions and over time.

The ADE7752 supplies average real power information on the low frequency outputs, F1 and F2. These logic outputs may be used to directly drive an electromechanical counter or to interface with an MCU. The CF logic output gives instantaneous real power information. This output is intended to be used for calibration purposes.

The ADE7752 includes a power supply monitoring circuit on the V_{DD} pin. The ADE7752 remains inactive until the supply voltage on V_{DD} reaches 4 V. If the supply falls below 4 V, no pulses are issued on F1, F2, and CF. Internal phase matching circuitry ensures that the voltage and current channels are phase matched. An internal no load threshold ensures the part does not exhibit any creep when there is no load. The ADE7752 is available in a 24-lead SOIC package.

FUNCTIONAL BLOCK DIAGRAM

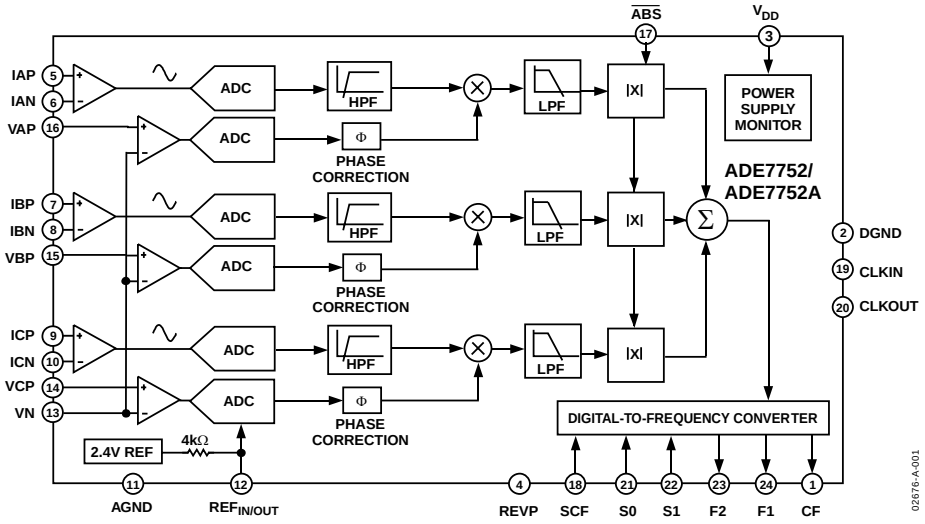


Figure 1. 24-Lead Standard Small Outline Package [SOIC]

Rev. C

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TABLE OF CONTENTS

Specifications ... 3
Timing Characteristics ... 4
Absolute Maximum Ratings ... 5
ESD Caution ... 5
Pin Configuration and Function Descriptions ... 6
Typical Performance Characteristics ... 8
Test Circuit ... 10
Terminology ... 11
Theory of Operation ... 12
Power Factor Considerations ... 12
Nonsinusoidal Voltage and Current ... 13
Analog Inputs ... 14
Current Channels ... 14
Voltage Channels ... 14
Typical Connection Diagrams ... 15
Current Channel Connection ... 15
Voltage Channels Connection ... 15
Meter Connections ... 15
Power Supply Monitor ... 17
HPF and Offset Effects ... 17
Digital-to-Frequency Conversion ... 18
Mode Selection of the Sum of the Three Active Energies ... 19
Power Measurement Considerations ... 19
Transfer Function ... 20
Frequency Outputs F1 and F2 ... 20
Frequency Output CF ... 21
Selecting a Frequency for an Energy Meter Application ... 22
Frequency Outputs ... 22
No Load Threshold ... 22
Negative Power Information ... 23
Outline Dimensions ... 24
Ordering Guide ... 24

REVISION HISTORY

7/05—Rev. B to Rev. C

Added ADE7752A ... Universal
Changed NEGP Pin Name to REVP ... Universal
Changes to Table 1 ... 3
Changes to Table 6, Table 7 ... 21
Changes to Table 8, Table 9, Table 10 ... 22
Updated Outline Dimensions ... 24
Changes to Ordering Guide ... 24

9/03—Rev. A to Rev. B

Updated Format ... Universal
Change to Figure 19 ... 15

5/03—Rev. 0 to Rev. A

Changed F_{1-5} to F_{1-7} ... Universal
Change to Figure 6 ... 10
Changes to Frequency Outputs F1 and F2 section ... 13
Replaced Table II ... 13
Changes to Examples 1, 2, and 3 ... 14
Replaced Table III ... 14
Replaced Tables IV, V, and VI ... 15
Changes to SELECTING A FREQUENCY FOR AN ENERGY METER APPLICATION section ... 15
Changes to NO LOAD THRESHOLD section ... 16
Replaced Table VII ... 16

SPECIFICATIONS

V_{DD} = 5 V ± 5%, AGND = DGND = 0 V, on-chip reference, CLKIN = 10 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	ADE7752 Min	ADE7752 Typ	ADE7752 Max	ADE7752A Min	ADE7752A Typ	ADE7752A Max	Unit	Conditions
ACCURACY[1, 2]								
Measurement Error on Current Channel		0.1			0.1		% Reading	Voltage channel with full-scale signal (±500 mV), 25°C, over a dynamic range of 500 to 1
Phase Error Between Channels								
PF = 0.8 Capacitive			±0.1			±0.1	Degrees	
PF = 0.5 Inductive			±0.1			±0.1	Degrees	
AC Power Supply Rejection								SCF = 0; S0 = S1 = 1
Output Frequency Variation (CF)		0.01			0.01		% Reading	IA = IB = IC = 100 mV rms, VA = VB = VC = 100 mV rms, @ 50 Hz, ripple on V_{DD} of 175 mV rms @ 100 Hz
DC Power Supply Rejection								S1 = 1; S0 = SCF = 0
Output Frequency Variation (CF)		0.1			0.1		% Reading	IA = IB = IC = 100 mV rms, VA = VB = VC = 100 mV rms, V_{DD} = 5 V ±250 mV
ANALOG INPUTS								See the Analog Inputs section.
Maximum Signal Levels			±0.5			±0.5	Vpeak differential	V_{AP} to V_N, V_{BP} to V_N, V_{CP} to V_N, I_{AP} to I_{AN}, I_{BP} to I_{BN}, I_{CP} to I_{CN}
Input Impedance (DC)	370	410		370	450		kΩ	CLKIN = 10 MHz
Bandwidth (−3 dB)		14			14		kHz	CLKIN/256, CLKIN = 10 MHz
ADC Offset Error[1, 2]			±25			±25	mV	
Gain Error		±9			±9		% Ideal	External 2.5 V reference, IA = IB = IC = 500 mV dc
REFERENCE INPUT								
$REF_{IN/OUT}$ Input Voltage Range			2.6			2.6	V	2.4 V + 8%
	2.2			2.2			V	2.4 V − 8%
Input Impedance	3.3			3.3			kΩ	
Input Capacitance			10			10	pF	
ON-CHIP REFERENCE								Nominal 2.4 V
Reference Error			±200			±200	mV	
Temperature Coefficient		25			25		ppm/°C	
CLKIN								All specifications for CLKIN of 10 MHz
Input Clock Frequency		10			10		MHz	
LOGIC INPUTS[3]								
ACF, S0, S1, and $\overline{ABS}$								
Input High Voltage, V_{INH}	2.4			2.4			V	V_{DD} = 5 V ±5%
Input Low Voltage, V_{INL}			0.8			0.8	V	V_{DD} = 5 V ±5%
Input Current, I_{IN}			±3			±3	μA	Typically 10 nA, V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}			10			10	pF	
LOGIC OUTPUTS[3]								
F1 and F2								
Output High Voltage, V_{OH}	4.5			4.5			V	I_{SOURCE} = 10 mA, V_{DD} = 5 V
Output Low Voltage, V_{OL}			0.5			0.5	V	I_{SINK} = 10 mA, V_{DD} = 5 V
CF and REVP								
Output High Voltage, V_{OH}	4				4		V	V_{DD} = 5 V, I_{SOURCE} = 5 mA
Output Low Voltage, V_{OL}			0.5			0.5	V	V_{DD} = 5 V, I_{SINK} = 5 mA
POWER SUPPLY								For specified performance
V_{DD}	4.75		5.25	4.75		5.25	V	5 V ±5%
I_{DD}		12	16		6	9	mA	

[1] See the Terminology section for explanation of specifications.
[2] See the plots in the Typical Performance Characteristics section.
[3] Sample tested during initial release and after any redesign or process change that may affect this parameter.

TIMING CHARACTERISTICS

V_{DD} = 5 V ± 5%, AGND = DGND = 0 V, on-chip reference, CLKIN = 10 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted[1, 2].

Table 2.

Parameter	Conditions	Spec	Unit
t_1 [3]	F1 and F2 Pulse Width (Logic High).	275	ms
t_2	Output Pulse Period. See the Transfer Function section.	See Table 6.	sec
t_3	Time between F1 Falling Edge and F2 Falling Edge.	1/2 t_2	sec
t_4 [3, 4]	CF Pulse Width (Logic High).	96	ms
t_5 [5]	CF Pulse Period. See the Transfer Function and the Frequency Outputs sections.	See Table 7.	sec
t_6	Minimum Time Between the F1 and F2 Pulse.	CLKIN/4	sec

[1] Sample tested during initial release and after any redesign or process change that may affect this parameter.
[2] See Figure 2.
[3] The pulse widths of F1, F2, and CF are not fixed for higher output frequencies. See the Frequency Outputs section.
[4] CF is not synchronous to F1 or F2 frequency outputs.
[5] The CF pulse is always 1 µs in the high frequency mode.

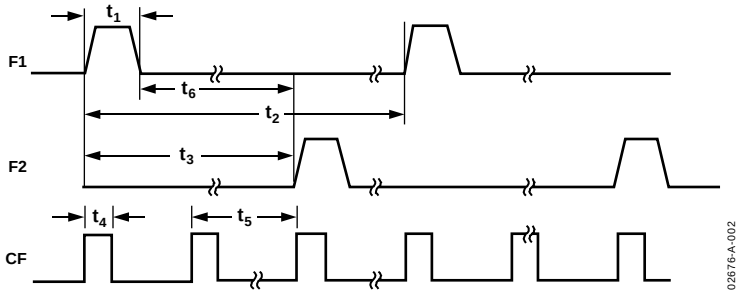


Figure 2. Timing Diagram for Frequency Outputs

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +7 V
V_{DD} to DGND	−0.3 V to +7 V
Analog Input Voltage to AGND	
VAP, VBP, VCP, VN, IAP, IAN, IBP, IBN, ICP, and ICN	−6 V to +6 V
Reference Input Voltage to AGND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
24-Lead SOIC, Power Dissipation	88 mW
θ_{JA} Thermal Impedance	250°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

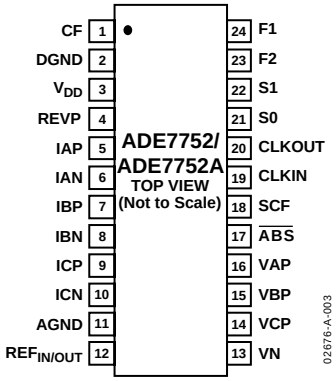


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CF	Calibration Frequency Logic Output. The CF logic output gives instantaneous real power information. This output is intended to be used for calibration purposes. See the SCF pin description.
2	DGND	This provides the ground reference for the digital circuitry in the ADE7752: the multiplier, filters, and digital-to-frequency converter. Because the digital return currents in the ADE7752 are small, it is acceptable to connect this pin to the analog ground plane of the whole system.
3	V_{DD}	Power Supply. This pin provides the supply voltage for the digital circuitry in the ADE7752. The supply voltage should be maintained at 5 V ± 5% for specified operation. This pin should be decoupled to DGND with a 10 µF capacitor in parallel with a 100 nF ceramic capacitor.
4	REVP	This logic output goes logic high when negative power is detected on any of the three phase inputs, that is, when the phase angle between the voltage and the current signals is greater than 90°. This output is not latched and is reset when positive power is once again detected. See the Negative Power Information section.
5, 6; 7, 8; 9, 10	IAP, IAN; IBP, IBN; ICP, ICN	Analog Inputs for Current Channel. This channel is intended for use with the current transducer and is referenced in this document as the current channel. These inputs are fully differential voltage inputs with maximum differential input signal levels of ±0.5 V. See the Analog Inputs section. Both inputs have internal ESD protection circuitry. In addition, an overvoltage of ±6 V can be sustained on these inputs without risk of permanent damage.
11	AGND	This pin provides the ground reference for the analog circuitry in the ADE7752: the ADCs, temperature sensor, and reference. This pin should be tied to the analog ground plane or the quietest ground reference in the system. This quiet ground reference should be used for all analog circuitry, such as antialiasing filters, current and voltage transducers, and so on. To keep ground noise around the ADE7752 to a minimum, the quiet ground plane should connect to the digital ground plane at only one point. It is acceptable to place the entire device on the analog ground plane.
12	$REF_{IN/OUT}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 2.4 V ± 8% and a typical temperature coefficient of 20 ppm/°C. An external reference source may also be connected at this pin. In either case, this pin should be decoupled to AGND with a 1 µF ceramic capacitor.
13–16	VN, VCP, VBP, VAP	Analog Inputs for the Voltage Channel. This channel is intended for use with the voltage transducer and is referenced in this document as the voltage channel. These inputs are single-ended voltage inputs with a maximum signal level of ±0.5 V with respect to VN for specified operation. All inputs have internal ESD protection circuitry. In addition, an overvoltage of ± 6 V can be sustained on these inputs without risk of permanent damage.
17	$\overline{ABS}$	This logic input is used to select the way the three active energies from the three phases are summed. This offers the designer the capability to do the arithmetical sum of the three energies ($\overline{ABS}$ logic high) or the sum of the absolute values ($\overline{ABS}$ logic low). See the Mode Selection of the Sum of the Three Active Energies section.
18	SCF	Select Calibration Frequency. This logic input is used to select the frequency on the calibration output CF. Table 7 shows how the calibration frequencies are selected.

Pin No.	Mnemonic	Description
19	CLKIN	Master Clock for ADCs and Digital Signal Processing. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7752. The clock frequency for specified operation is 10 MHz. Ceramic load capacitors between 22 pF and 33 pF should be used with the gate oscillator circuit. Refer to the crystal manufacturer's data sheet for load capacitance requirements.
20	CLKOUT	A crystal can be connected across this pin and CLKIN as described previously to provide a clock source for the ADE7752. The CLKOUT pin can drive one CMOS load when an external clock is supplied at CLKIN or when a crystal is being used.
21, 22	S0, S1	These logic inputs are used to select one of four possible frequencies for the digital-to-frequency conversion. This offers the designer greater flexibility when designing the energy meter. See the Selecting a Frequency for an Energy Meter Application section.
24, 23	F1, F2	Low Frequency Logic Outputs. F1 and F2 supply average real power information. The logic outputs can be used to drive electromechanical counters and two-phase stepper motors directly. See the Transfer Function section.

TYPICAL PERFORMANCE CHARACTERISTICS

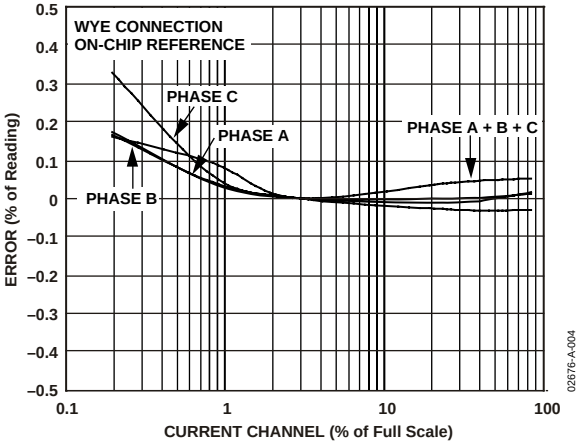


Figure 4. Error as a Percent of Reading with Internal Reference (Wye Connection)

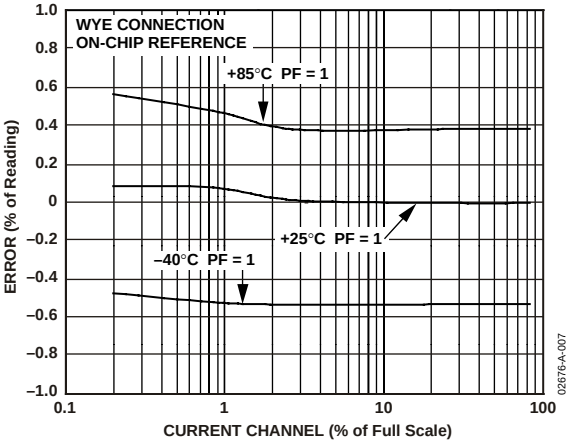


Figure 7. Error as a Percent of Reading over Temperature with Internal Reference (Wye Connection)

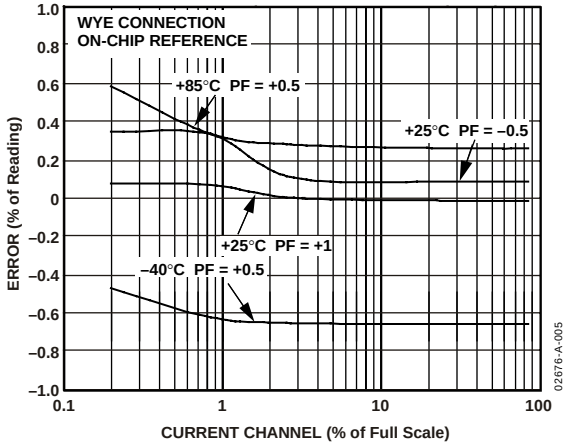


Figure 5. Error as a Percent of Reading over Power Factor with Internal Reference (Wye Connection)

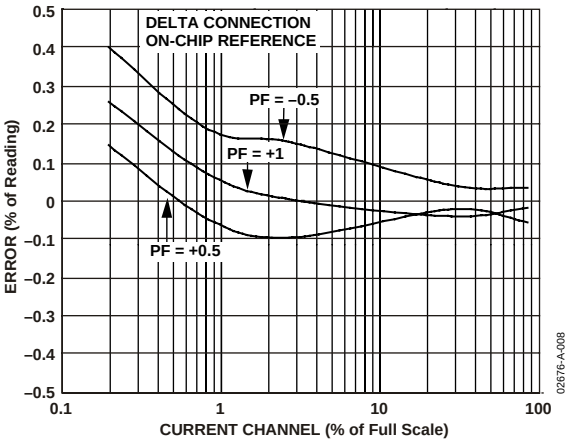


Figure 8. Error as a Percent of Reading over Power Factor with Internal Reference (Delta Connection)

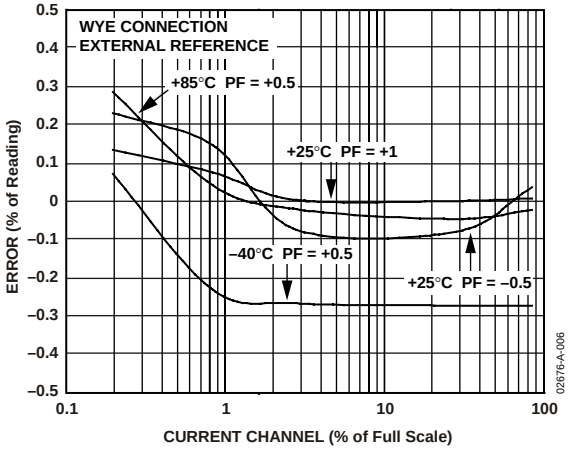


Figure 6. Error as a Percent of Reading over Power Factor with External Reference (Wye Connection)

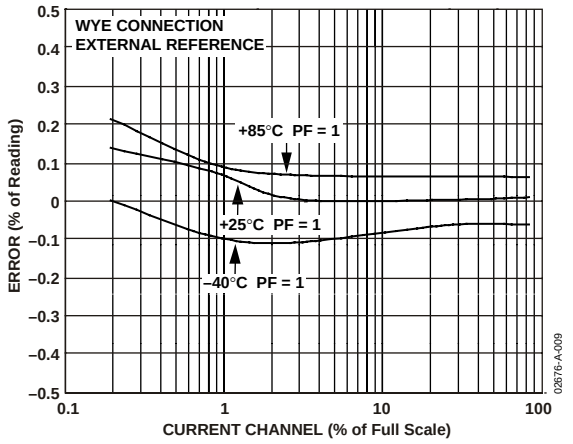


Figure 9. Error as a Percent of Reading over Temperature with External Reference (Wye Connection)

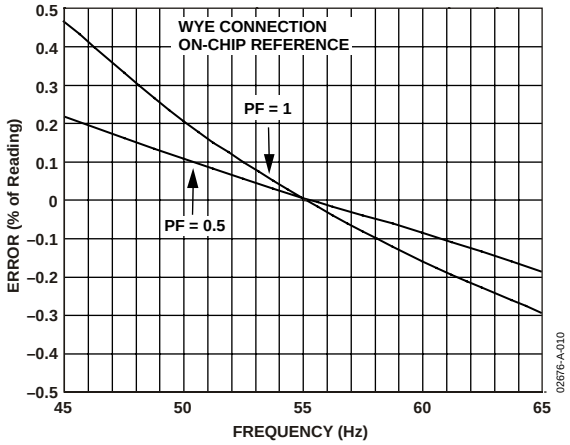


Figure 10. Error as a Percent of Reading over Frequency with an Internal Reference (Wye Connection)

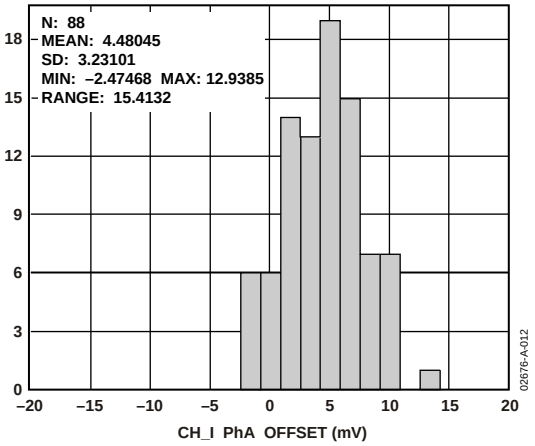


Figure 12. Channel 1 Offset Distribution

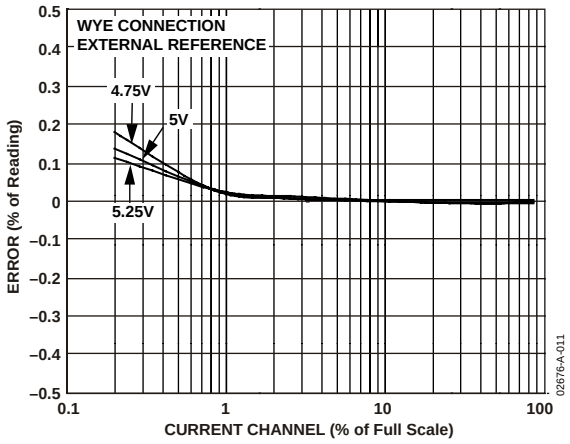


Figure 11. Error as a Percent of Reading over Power Supply with External Reference (Wye Connection)

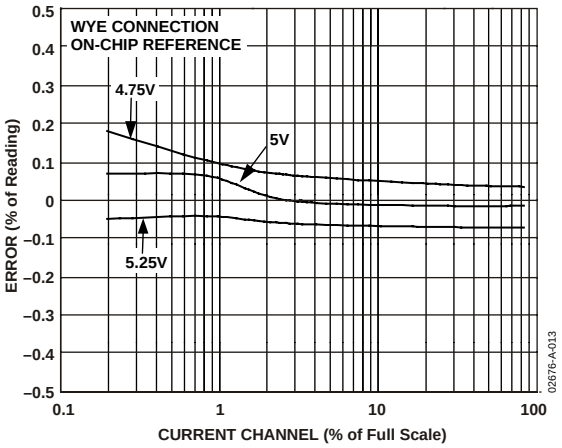


Figure 13. Error as a Percent of Reading over Power Supply with Internal Reference (Wye Connection)

TEST CIRCUIT

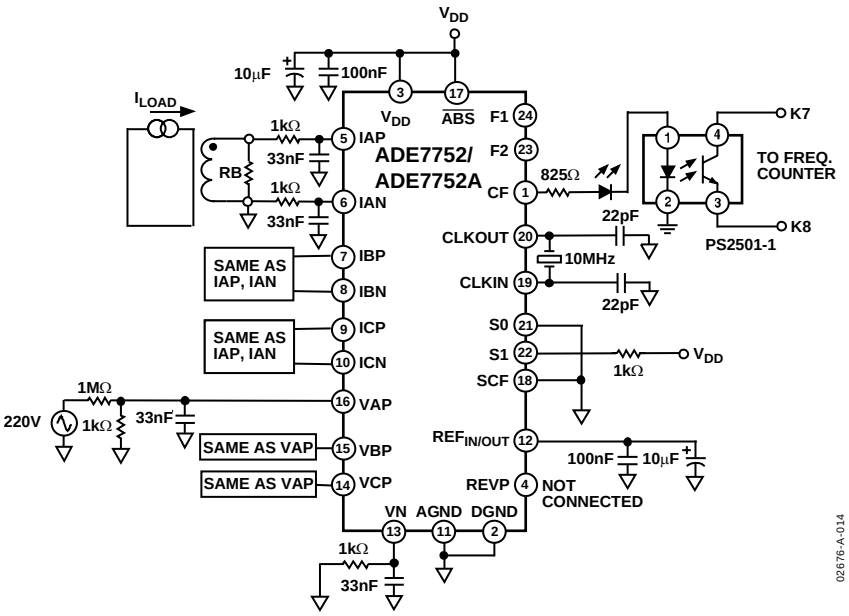


Figure 14. Test Circuit for Performance Curves

TERMINOLOGY

Measurement Error
The error associated with the energy measurement made by the ADE7752 is defined by the following formula:

$$Percentage\ Error = \left\{ \frac{Energy\ Registered\ by\ ADE7752 - True\ Energy}{True\ Energy} \right\} \times 100\%$$

Error Between Channels
The high-pass filter (HPF) in the current channel has a phase lead response. To offset this phase response and equalize the phase response between channels, a phase correction network is also placed in the current channel. The phase correction network ensures a phase match between the current channels and voltage channels to within ±0.1° over a range of 45 Hz to 65 Hz and ±0.2° over a range of 40 Hz to 1 kHz. See Figure 24 and Figure 26.

Power Supply Rejection (PSR)
This quantifies the ADE7752 measurement error as a percentage of reading when the power supplies are varied.

For the ac PSR measurement, a reading at a nominal supply (5 V) is taken. A 200 mV rms/100 Hz signal is then introduced onto the supply and a second reading is obtained under the same input signal levels. Any error introduced is expressed as a percentage of reading. See definition for Measurement Error.

For the dc PSR measurement, a reading at nominal supplies (5 V) is taken. The supply is then varied ±5% and a second reading is obtained with the same input signal levels. Any error introduced is again expressed as a percentage of reading.

ADC Offset Error
This refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND, the ADCs still see an analog input signal offset. However, because the HPF is always present, the offset is removed from the current channel, and the power calculation is not affected by this offset.

Gain Error
The gain error of the ADE7752 is defined as the difference between the measured output frequency (minus the offset) and the ideal output frequency. The difference is expressed as a percentage of the ideal frequency. The ideal frequency is obtained from the ADE7752 transfer function. See the Transfer Function section.

THEORY OF OPERATION

The six voltage signals from the current and voltage transducers are digitized with ADCs. These ADCs are 16-bit second-order Σ-Δ with an oversampling rate of 833 kHz. This analog input structure greatly simplifies transducer interface by providing a wide dynamic range for direct connection to the transducer and also by simplifying the antialiasing filter design. A high-pass filter in the current channel removes the dc component from the current signal. This eliminates any inaccuracies in the real power calculation due to offsets in the voltage or current signals. See the HPF and Offset Effects section.

The real power calculation is derived from the instantaneous power signal. The instantaneous power signal is generated by a direct multiplication of the current and voltage signals of each phase. In order to extract the real power component (the dc component), the instantaneous power signal is low-pass filtered on each phase. Figure 15 illustrates the instantaneous real power signal and shows how the real power information can be extracted by low-pass filtering the instantaneous power signal. This method is used to extract the real power information on each phase of the polyphase system. The total real power information is then obtained by adding the individual phase real power. This scheme correctly calculates real power for nonsinusoidal current and voltage waveforms at all power factors. All signal processing is carried out in the digital domain for superior stability over temperature and time.

The low frequency output of the ADE7752 is generated by accumulating the total real power information. This low frequency inherently means a long accumulation time between output pulses. The output frequency is therefore proportional to the average real power. This average real power information can, in turn, be accumulated (by a counter, for example) to generate real energy information. Because of its high output frequency and therefore shorter integration time, the CF output is proportional to the instantaneous real power. This pulse is useful for system calibration purposes that would take place under steady load conditions.

POWER FACTOR CONSIDERATIONS

Low-pass filtering, the method used to extract the real power information from the individual instantaneous power signal, is still valid when the voltage and current signals of each phase are not in phase. Figure 16 displays the unity power factor condition and a DPF (displacement power factor) = 0.5, or current signal lagging the voltage by 60°, for one phase of the polyphase. Assuming that the voltage and current waveforms are sinusoidal, the real power component of the instantaneous power signal, or the dc term, is given by

$$\left(\frac{V \times 1}{2}\right) \times \cos(60°)$$

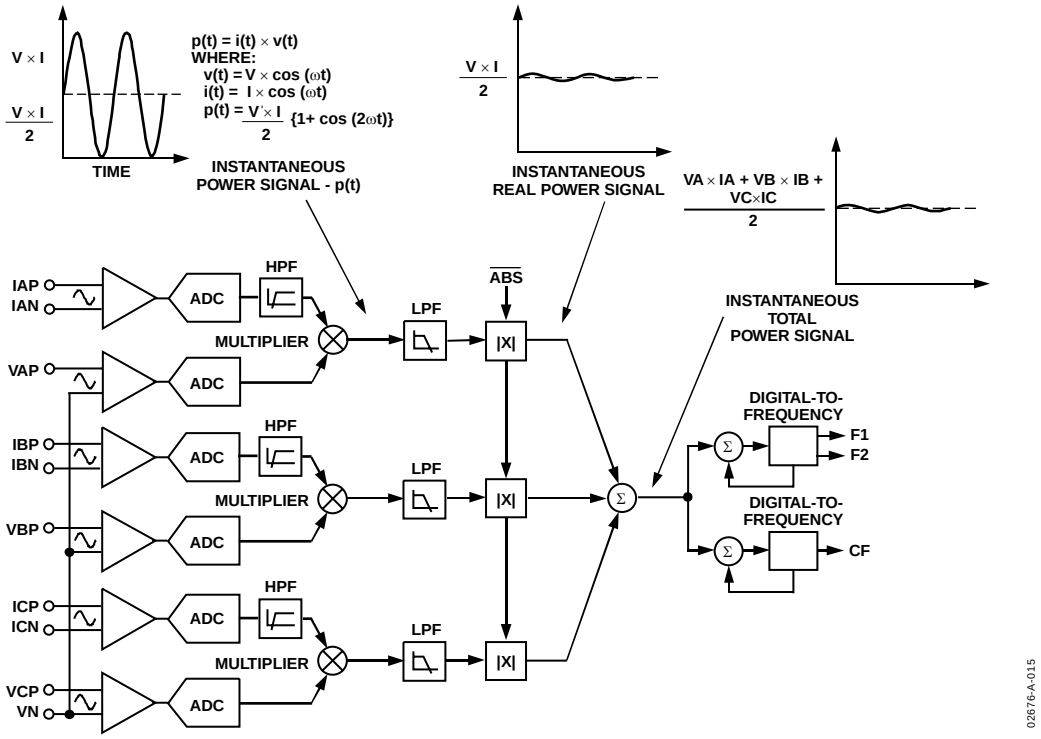


Figure 15. Signal Processing Block Diagram

This is the correct real power calculation.

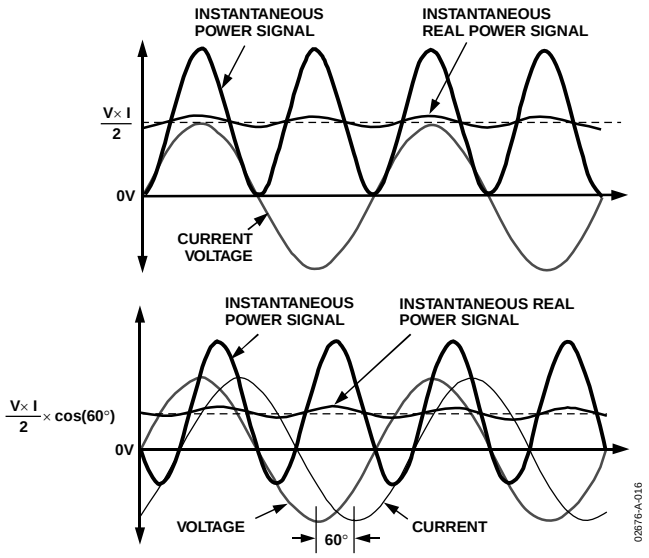


Figure 16. DC Component of Instantaneous Power Signal Conveys Real Power Information PF < 1

NONSINUSOIDAL VOLTAGE AND CURRENT

The real power calculation method also holds true for nonsinusoidal current and voltage waveforms. All voltage and current waveforms in practical applications have some harmonic content. Using the Fourier Transform, instantaneous voltage and current waveforms can be expressed in terms of their harmonic content:

$$v(t) = V_o + \sqrt{2} \times \sum_{n=0}^{\infty} V_n \times \sin\left(n\omega t + \alpha_n\right) \quad (1)$$

where:

$v(t)$ is the instantaneous voltage.
V_O is the average value.
V_n is the rms value of voltage harmonic n.
α_n is the phase angle of the voltage harmonic.

$$i(t) = I_O + \sqrt{2} \times \sum_{n=0}^{\infty} V_n I \times \sin\left(n\omega t\ \beta_n\right) \quad (2)$$

where:

$i(t)$ is the instantaneous current.
I_O is the dc component.
I_n is the rms value of current harmonic n.
β_n is the phase angle of the current harmonic.

Using Equations 1 and 2, the real power, P, can be expressed in terms of its fundamental real power (P_1) and harmonic real power (P_H).

$$P = P_1 + P_H$$

where:

$$P_1 = V_1 \times I_1 \cos\varphi_1$$
$$\varphi_1 = \alpha_1 - \beta_1 \quad (3)$$

$$P_H = \sum_{n=1}^{\infty} V_n \times I_n \cos\varphi_n$$
$$\varphi n = \alpha_n - \beta_n \quad (4)$$

As can be seen from Equation 4, a harmonic real power component is generated for every harmonic, provided that harmonic is present in both the voltage and current waveforms. The power factor calculation has been shown to be accurate in the case of a pure sinusoid. Therefore, the harmonic real power must also correctly account for power factor since it is made up of a series of pure sinusoids.

Note that the input bandwidth of the analog inputs is 14 kHz with a master clock frequency of 10 MHz.

ANALOG INPUTS

CURRENT CHANNELS

The voltage outputs from the current transducers are connected to the ADE7752 current channels, which are fully differential voltage inputs. IAP, IBP, and ICP are the positive inputs for IAN, IBN, and ICN, respectively.

The maximum peak differential signal on the current channel should be less than ±500 mV (353 mV rms for a pure sinusoidal signal) for the specified operation.

Figure 17 illustrates the maximum signal levels on IAP and IAN. The maximum differential voltage between IAP and IAN is ±500 mV. The differential voltage signal on the inputs must be referenced to a common mode, such as AGND. The maximum common-mode signal shown in Figure 17 is ±25 mV.

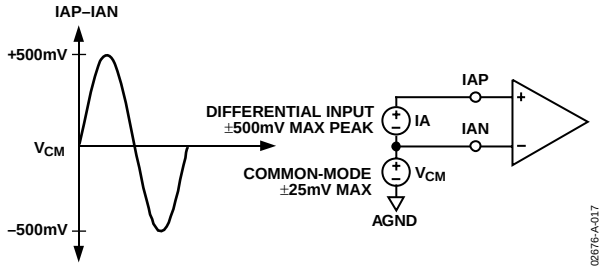


Figure 17. Maximum Signal Levels, Current Channel

VOLTAGE CHANNELS

The output of the line voltage transducer is connected to the ADE7752 at this analog input. Voltage channels are a pseudo-differential voltage input. VAP, VBP, and VCP are the positive inputs with respect to VN.

The maximum peak differential signal on the voltage channel is ±500 mV (353 mV rms for a pure sinusoidal signal) for specified operation.

Figure 18 illustrates the maximum signal levels that can be connected to the voltage channels of the ADE7752.

Voltage channels must be driven from a common-mode voltage. In other words, the differential voltage signal on the input must be referenced to a common mode (usually AGND). The analog inputs of the ADE7752 can be driven with common-mode voltages of up to 25 mV with respect to AGND. However, best results are achieved using a common mode equal to AGND.

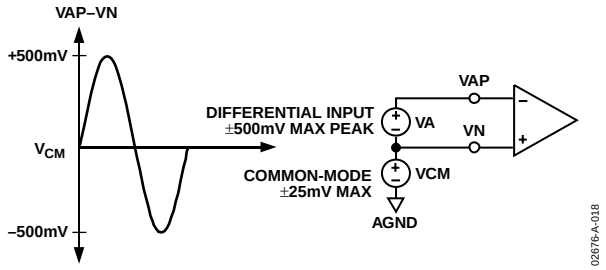


Figure 18. Maximum Signal Levels, Voltage Channel

TYPICAL CONNECTION DIAGRAMS

CURRENT CHANNEL CONNECTION

Figure 19 shows a typical connection diagram for the current channel (IA). A current transformer (CT) is the current transducer selected for this example. Notice the common-mode voltage for the current channel is AGND and is derived by center tapping the burden resistor to AGND. This provides the complementary analog input signals for IAP and IAN. The CT turns ratio and burden resistor Rb are selected to give a peak differential voltage of ±500 mV at maximum load.

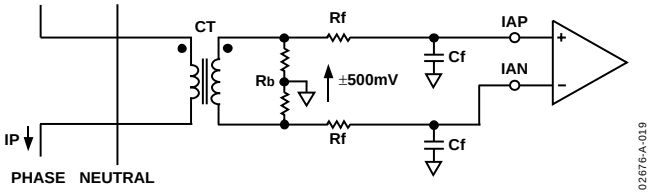


Figure 19. Typical Connection for Current Channels

VOLTAGE CHANNELS CONNECTION

Figure 20 shows two typical connections for the voltage channel. The first option uses a potential transformer (PT) to provide complete isolation from the main voltage. In the second option, the ADE7752 is biased around the neutral wire, and a resistor divider is used to provide a voltage signal proportional to the line voltage. Adjusting the ratio of Ra, Rb, and VR is also a convenient way of carrying out a gain calibration on the meter.

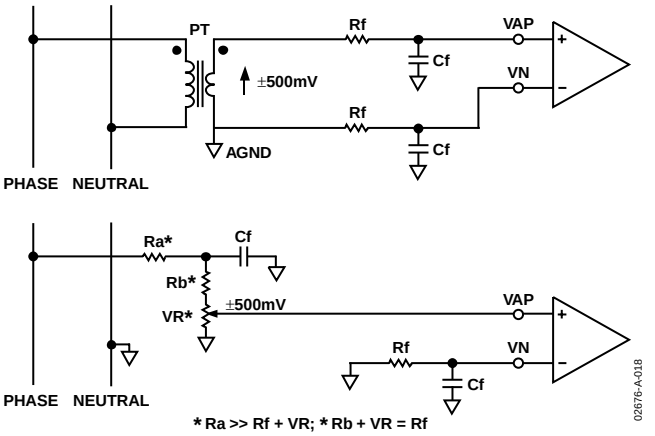


Figure 20. Typical Connections for Voltage Channels

METER CONNECTIONS

In 3-phase service, two main power distribution services exist: 3-phase 4-wire or 3-phase 3-wire. The additional wire in the 3-phase 4-wire arrangement is the neutral wire. The voltage lines have a phase difference of ±120° (±2π/3 radians) between each other. See Equation 5.

$$V_A(t) = \sqrt{2} \times V_A \times \cos(\omega_l t)$$
$$V_B(t) = \sqrt{2} \times V_B \times \cos\left(\omega_l t + \frac{2\pi}{3}\right) \quad (5)$$
$$V_C(t) = \sqrt{2} \times V_C \times \cos\left(\omega_l t + \frac{4\pi}{3}\right)$$

where V_A, V_B, and V_C represent the voltage rms values of the different phases.

The current inputs are represented by Equation 6.

$$I_A(t) = \sqrt{2}\ I_A \times \cos\left(\omega_l t + \varphi_A\right)$$
$$I_B(t) = \sqrt{2}\ I_B \times \cos\left\{\omega_l t + \frac{2\pi}{3} + \varphi_B\right\} \quad (6)$$
$$I_C(t) = \sqrt{2}\ I_C \times \cos\left\{\omega_l t + \frac{4\pi}{3} + \varphi_C\right\}$$

where I_A, I_B, and I_C represent the rms value of the current of each phase and ϕ_A, ϕ_B, and ϕ_C represent the phase difference of the current and voltage channel of each phase.

The instantaneous powers can then be calculated as follows:

$$P_A(t) = V_A(t) \times I_A(t)$$
$$P_B(t) = V_B(t) \times I_B(t)$$
$$P_C(t) = V_C(t) \times I_C(t)$$

Then:

$$P_A(t) = V_A \times I_A \times \cos(\varphi_A) - V_A \times I_A \times \cos\left(2\omega_l t + \varphi_A\right)$$
$$P_B(t) = V_B \times I_B \times \cos(\varphi_B) - V_B \times I_B \times \cos\left(2\omega_l t + \frac{4\pi}{3} + \varphi_B\right) \quad (7)$$
$$P_C(t) = V_C \times I_C \times \cos(\varphi_C) - V_C \times I_C \times \cos\left(2\omega_l t + \frac{8\pi}{3} + \varphi_C\right)$$

As shown in Equation 7, in the ADE7752, the real power calculation per phase is made when current and voltage inputs of one phase are connected to the same channel (A, B, or C). Then the summation of each individual real power calculation gives the total real power information, $P(t) = P_A(t) + P_B(t) + P_C(t)$.

Figure 21 shows the connections of the analog inputs of the ADE7752 with the power lines in a 3-phase 3-wire delta service. Note that only two current inputs and two voltage inputs of the ADE7752 are used in this case. The real power calculated by the ADE7752 does not depend on the selected channels.

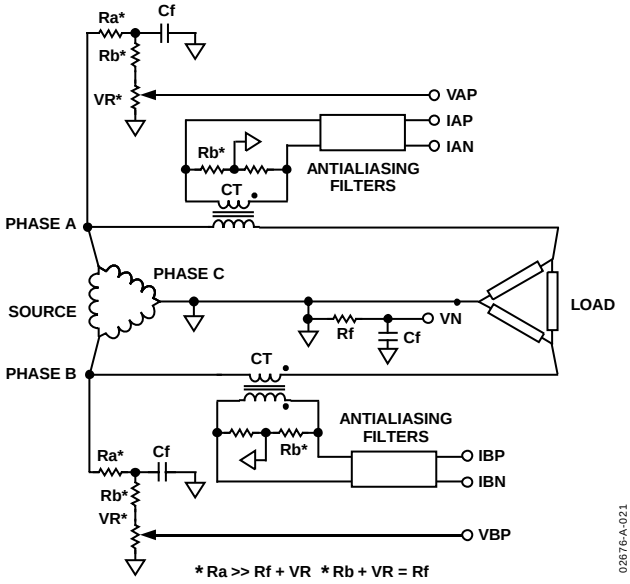


Figure 21. 3-Phase 3-Wire Meter Connection with ADE7752

Figure 22 shows the connections of the analog inputs of the ADE7752 with the power lines in a 3-phase 4-wire Wye service.

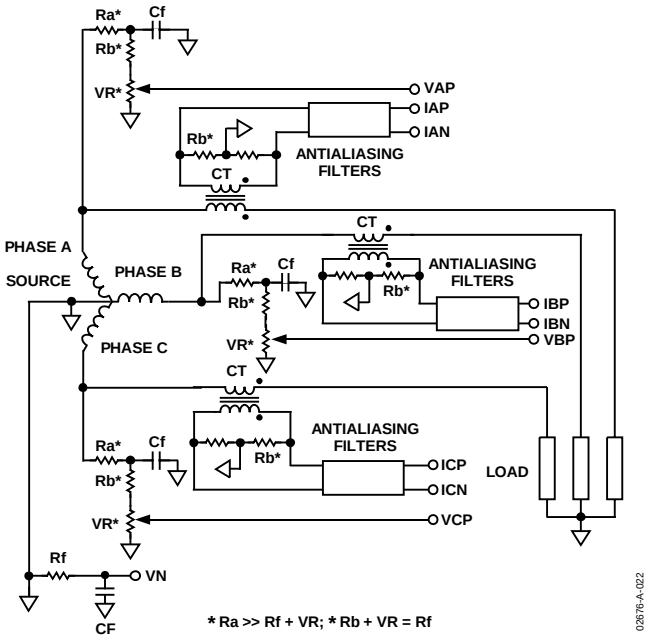


Figure 22. 3-Phase 4-Wire Meter Connection with ADE7752

POWER SUPPLY MONITOR

The ADE7752 contains an on-chip power supply monitor. The power supply (V_{DD}) is continuously monitored by the ADE7752. If the supply is less than 4 V ± 5%, the outputs of the ADE7752 are inactive. This is useful to ensure correct device startup at power-up and power-down. The power supply monitor has built-in hysteresis and filtering. This gives a high degree of immunity to false triggering due to noisy supplies.

As can be seen from Figure 23, the trigger level is nominally set at 4 V. The tolerance on this trigger level is about ±5%. The power supply and decoupling for the part should be such that the ripple at V_{DD} does not exceed 5 V ± 5% as specified for normal operation.

HPF AND OFFSET EFFECTS

Figure 25 shows the effect of offsets on the real power calculation. As can be seen, an offset on the current channel and voltage channel contribute a dc component after multiplication. Since this dc component is extracted by the LPF and is used to generate the real power information for each phase, the offsets contribute a constant error to the total real power calculation.

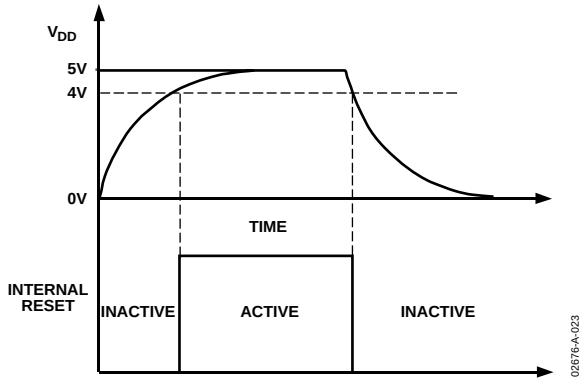


Figure 23. On-Chip Power Supply Monitor

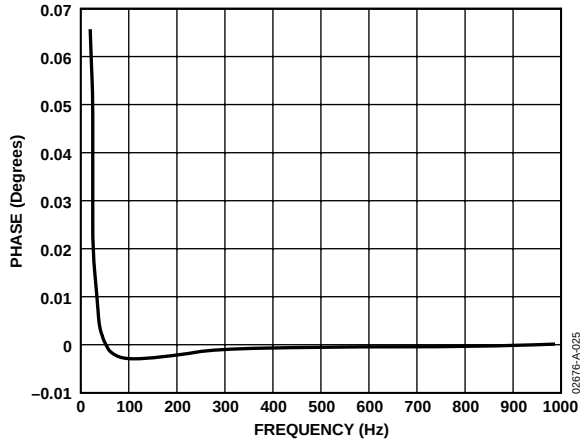


Figure 24. Phase Error Between Channels (0 Hz to 1 kHz)

This problem is easily avoided by the HPF in the current channels. By removing the offset from at least one channel, no error component can be generated at dc by the multiplication. Error terms at cos(ωt) are removed by the LPF and the digital-to-frequency conversion. See the Digital-to-Frequency Conversion section.

$$\{V\cos(\omega t)+V_{OS}\}\times\{I\cos(\omega t)+I_{OS}\}=$$
$$\frac{V\times I}{2}+V_{OS}\times I_{OS}+V_{OS}\times I\cos(\omega t)+I_{OS}\times V\cos(\omega t)$$
$$+\frac{V\times I}{2}\times\cos(2\omega t)$$

The HPFs in the current channels have an associated phase response that is compensated for on-chip. Figure 24 and Figure 26 show the phase error between channels with the compensation network. The ADE7752 is phase compensated up to 1 kHz as shown. This ensures correct active harmonic power calculation even at low power factors.

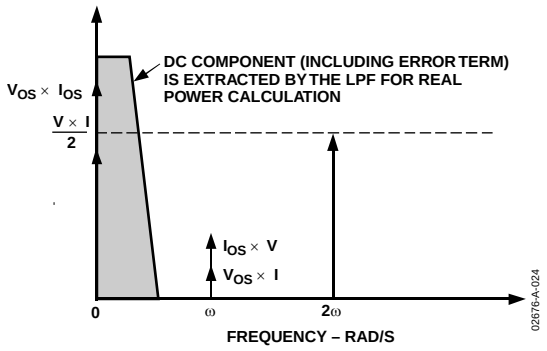


Figure 25. Effect of Channel Offset on the Real Power Calculation

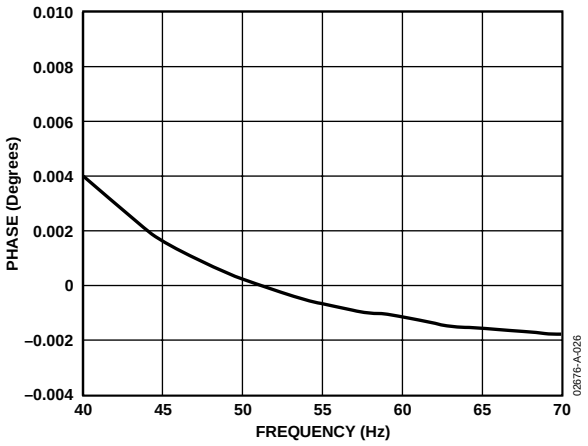


Figure 26. Phase Error Between Channels (40 Hz to 70 Hz)

DIGITAL-TO-FREQUENCY CONVERSION

After multiplication, the digital output of the low-pass filter contains the real power information of each phase. Because this LPF is not an ideal brick wall filter implementation, however, the output signal also contains attenuated components at the line frequency and its harmonics (cos(hωt), where h = 1, 2, 3, and so on).

The magnitude response of the filter is given by

$$|H(f)| = \frac{1}{\sqrt{1+\left\{\frac{f}{8}\right\}^2}} \quad (8)$$

where the −3 dB cutoff frequency of the low-pass filter is 8 Hz. For a line frequency of 50 Hz, this would give an attenuation of the 2ω(100 Hz) component of approximately −22 dB. The dominating harmonic is twice the line frequency, cos(2ωt), due to the instantaneous power signal. Figure 27 shows the instantaneous real power signal at the output of the CF, which still contains a significant amount of instantaneous power information, cos (2ωt).

This signal is then passed to the digital-to-frequency converter where it is integrated (accumulated) over time to produce an output frequency. This accumulation of the signal suppresses or averages out any non-dc component in the instantaneous real power signal. The average value of a sinusoidal signal is zero. Thus, the frequency generated by the ADE7752 is proportional to the average real power. Figure 27 shows the digital-to-frequency conversion for steady load conditions, constant voltage, and current.

As can be seen in Figure 27, the frequency output CF varies over time, even under steady load conditions. This frequency variation is primarily due to the cos(2ωt) components in the instantaneous real power signal. The output frequency on CF can be up to 160 times higher than the frequency on F1 and F2. The higher output frequency is generated by accumulating the instantaneous real power signal over a much shorter time, while converting it to a frequency. This shorter accumulation period means less averaging of the cos(2ωt) component. As a consequence, some of this instantaneous power signal passes through the digital-to-frequency conversion. This is not a problem in the application. Where CF is used for calibration purposes, the frequency should be averaged by the frequency counter. This removes any ripple. If CF is being used to measure energy, such as in a microprocessor-based application, the CF output should also be averaged to calculate power. Because the outputs F1 and F2 operate at a much lower frequency, much more averaging of the instantaneous real power signal is carried out. The result is a greatly attenuated sinusoidal content and a virtually ripple-free frequency output.

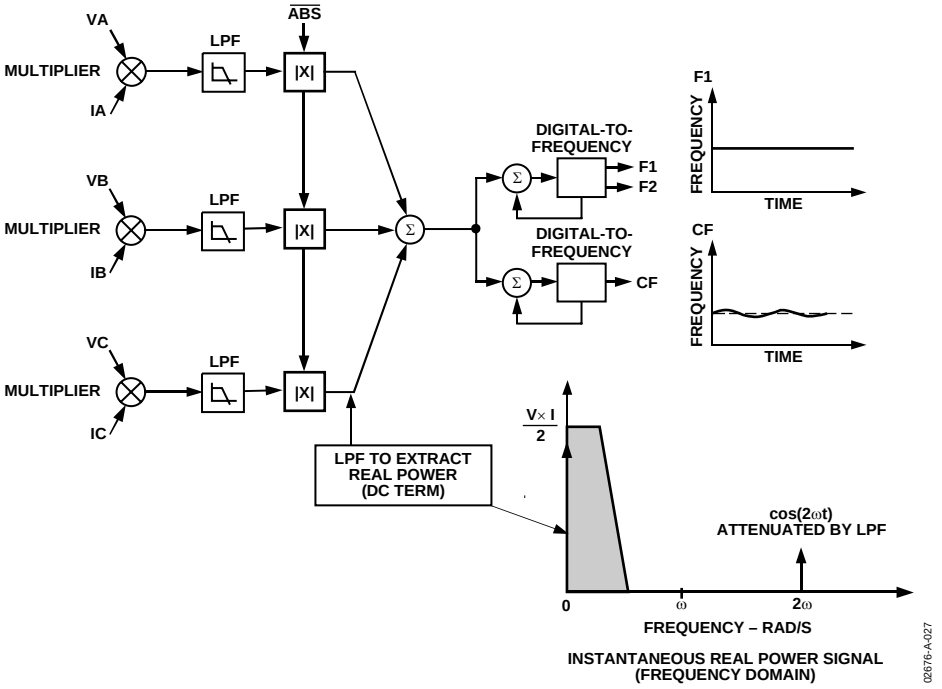


Figure 27. Real Power-to-Frequency Conversion

MODE SELECTION OF THE SUM OF THE THREE ACTIVE ENERGIES

The ADE7752 can be configured to execute the arithmetic sum of the three active energies, $Wh = Wh_{\phi A} + Wh_{\phi B} + Wh_{\phi C}$, or the sum of the absolute value of these energies, $Wh = |Wh_{\phi A}| + |Wh_{\phi B}| + |Wh_{\phi C}|$. The selection between the two modes can be made by setting the $\overline{\text{ABS}}$ pin. Logic high and logic low applied on the $\overline{\text{ABS}}$ pin correspond to the arithmetic sum and the sum of absolute values, respectively.

When the sum of the absolute values is selected, the active energy from each phase is always counted positive in the total active energy. It is particularly useful in 3-phase 4-wire installation where the sign of the active power should always be the same. If the meter is misconnected to the power lines, (for instance, if CT is connected in the wrong direction), the total active energy recorded without this solution can be reduced by two-thirds.

The sum of the absolute values assures that the active energy recorded represents the actual active energy delivered. In this mode, the reverse power pin still detects when negative power is present on any of the three phase inputs.

POWER MEASUREMENT CONSIDERATIONS

Calculating and displaying power information always has some associated ripple that depends on the integration period used in the MCU to determine average power as well as the load. For example, at light loads, the output frequency may be 10 Hz. With an integration period of 2 seconds, only about 20 pulses are counted. The possibility of missing one pulse always exists since the ADE7752 output frequency is running asynchronously to the MCU timer. This would result in a 1-in-20 or 5% error in the power measurement.

TRANSFER FUNCTION

FREQUENCY OUTPUTS F1 AND F2

The ADE7752 calculates the product of six voltage signals (on current channel and voltage channel) and then low-pass filters this product to extract real power information. This real power information is then converted to a frequency. The frequency information is output on F1 and F2 in the form of active high pulses. The pulse rate at these outputs is relatively low, such as 29.32 Hz maximum for ac signals with SCF = 1; S0 = S1 = 1 (see Table 6). This means that the frequency at these outputs is generated from real power information accumulated over a relatively long period of time. The result is an output frequency that is proportional to the average real power. The averaging of the real power signal is implicit to the digital-to-frequency conversion. The output frequency or pulse rate is related to the input voltage signals by the following equation:

$$Freq = \frac{6.181 \times \left(V_{AN} \times I_A + V_{BN} \times I_B + V_{CN} \times I_C\right) \times F_{1-7}}{{V_{REF}}^2}$$

where:

Freq = the output frequency on F1 and F2 (Hz).
V_{AN}, V_{BN}, and V_{CN} = the differential rms voltage signal on voltage channels (V).
I_A, I_B, and I_C = the differential rms voltage signal on current channels (V).
V_{REF} = the reference voltage (2.4 V ± 8%) (V).
F_{1-7} = one of seven possible frequencies selected by using the logic inputs SCF, S0, and S1 (see Table 5).

Table 5. F_{1-7} Frequency Selection[1]

SCF	S1	S0	F_{1-7} (Hz)
0	0	0	1.27
1	0	0	1.19
0	0	1	5.09
1	0	1	4.77
0	1	0	19.07
1	1	0	19.07
0	1	1	76.29
1	1	1	0.60

[1] F_{1-7} is a fraction of the master clock and therefore varies if the specified CLKIN frequency is altered.

Example 1

Thus, if full-scale differential dc voltages of +500 mV are applied to VA, VB, VC, IA, IB, and IC, respectively (500 mV is the maximum differential voltage that can be connected to current and voltage channels), the expected output frequency is calculated as follows:

F_{1-7} = 0.60 Hz, *SCF* = *S*0 = *S*1 = 1
$V_{AN} = V_{BN} = V_{CN} = IA = IB = IC$ = 500 mV *dc* = 0.5 V(*rms of dc = dc*)
V_{REF} = 2.4 V (*nominal reference value*)

Note that if the on-chip reference is used, actual output frequencies may vary from device to device due to reference tolerance of ±8%.

$$Freq = 3 \times \frac{6.181 \times 0.5 \times 0.5 \times 0.60}{2.4^2} = 0.483 \text{ Hz}$$

Example 2

In this example, with ac voltages of ±500 mV peak applied to the voltage channels and current channels, the expected output frequency is calculated as follows:

$$F_{1-7} = 0.60 \text{ Hz}, SCF = S0 = S1 = 1$$
$$V_{AN} = V_{BN} = V_{CN} = IA = IB = IC$$
$$= 500 \text{ mV peak } AC = \frac{0.5}{\sqrt{2}} \text{ Vrms}$$
$$V_{REF} = 2.4 \text{ V} \left(\textit{nominal reference value}\right)$$

Note that if the on-chip reference is used, actual output frequencies may vary from device to device due to reference tolerance of ±8%.

$$Freq = 3 \times \frac{6.181 \times 0.5 \times 0.5 \times 0.6}{\sqrt{2} \times \sqrt{2} \times 2.4^2} = 0.24 \text{ Hz}$$

As can be seen from these two example calculations, the maximum output frequency for ac inputs is always half of that for dc input signals. The maximum frequency also depends on the number of phases connected to the ADE7752. In a 3-phase 3-wire delta service, the maximum output frequency is different from the maximum output frequency in a 3-phase 4-wire Wye service. The reason is that there are only two phases connected to the analog inputs, but also that in a delta service, the current channel input and voltage channel input of the same phase are not in phase in normal operation.

Example 3

In this example, the ADE7752 is connected to a 3-phase 3-wire delta service as shown in Figure 21. The total real energy calculation processed in the ADE7752 can be expressed as

$$\textit{Total Real Power} = (V_A - V_C) \times I_A + (V_B - V_C) \times I_B$$

where V_A, V_B, and V_C represent the voltage on Phase A, B, and C, respectively. I_A and I_B represent the current on Phase A and B, respectively.

As the voltage and current inputs respect Equations 5 and 6, the total real power (P) is

$$P = (V_A - V_C)\quad (I_{AP} - I_{AN}) + (V_B - V_C) \times (I_{BP} - I_{BN})$$
$$P = \left(\sqrt{2} \times V_A \times \cos(\omega_l t) - \sqrt{2} \times V_C \times \cos\left(\omega_l t + \frac{4\pi}{3}\right)\right) \times \sqrt{2} \times I_A \times \cos(\omega_l t) + \left(\sqrt{2} \times V_B \times \cos\left(\omega_l t + \frac{2\pi}{3}\right) - v\sqrt{2} \times V_C \times \cos\left(\omega_l t + \frac{4\pi}{3}\right)\right) \times \sqrt{2} \times I_B \times \cos\left(\omega_l t + \frac{2\pi}{3}\right)$$

For simplification, assume that $\phi_A = \phi_B = \phi_C = 0$ and $V_A = V_B = V_C = V$. The preceding equation becomes:

$$P = 2 \times V \times I_A \times \sin\left(\frac{2\pi}{3}\right) \times \sin\left(\omega_l t + \frac{2\pi}{3}\right) \times \cos(\omega_l t) + 2 \times V \times I_B \times \sin\left(\frac{\pi}{3}\right) \times \sin(\omega_l t + \pi) \times \cos\left(\omega_l t + \frac{2\pi}{3}\right) \quad (9)$$

P then becomes:

$$P = V_{AN} \times I_A \times \left(\sin\left(\frac{2\pi}{3}\right) + \sin\left(2\omega_l t + \frac{2\pi}{3}\right)\right) + V_{BN} \times I_B \times \left(\sin\left(\frac{\pi}{3}\right) + \sin\left(2\omega_l t + \frac{\pi}{3}\right)\right) \quad (10)$$

where $V_{AN} = V \times \sin(2\pi/3)$ and $V_{BN} = V \times \sin(\pi/3)$.

As the LPF on each channel eliminates the $2\omega l$ component of the equation, the real power measured by the ADE7752 is

$$P = V_{AN} \times I_A \times \frac{\sqrt{3}}{2} + V_{BN} \times I_B \times \frac{\sqrt{3}}{2}$$

If full-scale ac voltage of ±500 mV peak is applied to the voltage channels and current channels, the expected output frequency is calculated as follows:

$F_{1-7} = 0.60$ Hz, $SCF = S0 = S1 = 1$

$V_{AN} = V_{BN} = I_A = I_B = I_C = 500$ mV *peak ac* $= \frac{0.5}{\sqrt{2}}$ V *rms*

$V_{CN} = I_C = 0$

$V_{REF} = 2.4$ V *nominal reference value*

Note that if the on-chip reference is used, actual output frequencies may vary from device to device due to reference tolerance of ±8%.

$$Freq = 2 \times \frac{6.181 \times 0.5 \times 0.5 \times 0.60}{\sqrt{2} \times \sqrt{2} \times 2.4^2} \times \frac{\sqrt{3}}{2} = 0.139 \text{ Hz}$$

Table 6 shows a complete listing of all maximum output frequencies when using all three channel inputs.

Table 6. Maximum Output Frequency on F1 and F2

SCF	S1	S0	Max Frequency for AC Inputs (Hz)	Max Frequency for DC Inputs (Hz)
0	0	0	0.51	1.02
1	0	0	0.48	0.96
0	0	1	2.04	4.09
1	0	1	1.91	3.84
0	1	0	7.67	15.35
1	1	0	7.67	15.35
0	1	1	30.70	61.4
1	1	1	0.24	0.48

FREQUENCY OUTPUT CF

The pulse output calibration frequency (CF) is intended for use during calibration. The output pulse rate on CF can be up to 160 times the pulse rate on F1 and F2. The lower the F_{1-7} frequency selected, the higher the CF scaling. Table 7 shows how the two frequencies are related, depending on the states of the logic inputs S0, S1, and SCF. Because of its relatively high pulse rate, the frequency at this logic output is proportional to the instantaneous real power. As with F1 and F2, the frequency is derived from the output of the low-pass filter after multiplication. However, because the output frequency is high, this real power information is accumulated over a much shorter time. Thus, less averaging is carried out in the digital-to-frequency conversion. With much less averaging of the real power signal, the CF output is much more responsive to power fluctuations. See Figure 15.

Table 7. Maximum Output Frequency on CF

SCF	S1	S0	F_{1-7} (Hz)	CF Max for AC Signals (Hz)
0	0	0	1.27	160 × F1, F2 = 81.87
1	0	0	1.19	8 × F1, F2 = 3.83
0	0	1	5.09	160 × F1, F2 = 327.46
1	0	1	4.77	16 × F1, F2 = 30.70
0	1	0	19.07	16 × F1, F2 = 122.81
1	1	0	19.07	8 × F1, F2 = 61.40
0	1	1	76.29	8 × F1, F2 = 245.61
1	1	1	0.60	16 × F1, F2 = 3.84

SELECTING A FREQUENCY FOR AN ENERGY METER APPLICATION

As shown in Table 5, the user can select one of seven frequencies. This frequency selection determines the maximum frequency on F1 and F2. These outputs are intended to be used to drive the energy register (electromechanical or other). Since only seven different output frequencies can be selected, the available frequency selection has been optimized for a 3-phase 4-wire service with a meter constant of 100 imp/kWhr and a maximum current between 10 A and 100 A. Table 8 shows the output frequency for several maximum currents (I_{MAX}) with a line voltage of 220 V (phase neutral). In all cases, the meter constant is 100 imp/kWhr.

Table 8. V. F1 and F2 Frequency at 100 imp/kWhr

I_{MAX} (A)	F1 and F2 (Hz)
10	0.18
25	0.46
40	0.73
60	1.10
80	1.47
100	1.83

The F_{1-7} frequencies allow complete coverage of this range of output frequencies on F1 and F2. When designing an energy meter, the nominal design voltage on the voltage channels should be set to half scale to allow for calibration of the meter constant. The current channel should also be no more than half scale when the meter sees maximum load. This allows overcurrent signals and signals with high crest factors to be accommodated. Table 9 shows the output frequency on F1 and F2 when all six analog inputs are half scale.

Table 9. F1 and F2 Frequency with Half-Scale AC Inputs

SCF	S1	S0	F_{1-7}	Frequency on F1 and F2 (Half-Scale AC Inputs)
0	0	0	1.27	0.26
1	0	0	1.19	0.24
0	0	1	5.09	1.02
1	0	1	4.77	0.96
0	1	0	19.07	3.84
1	1	0	19.07	3.84
0	1	1	76.29	15.35
1	1	1	0.60	0.12

When selecting a suitable F_{1-7} frequency for a meter design, the frequency output at I_{MAX} (maximum load) with a 100 imp/kWhr meter constant should be compared with column 5 of Table 9. The frequency closest to that listed in Table 9 is the best choice of frequency (F_{1-7}). For example, if a 3-phase 4-wire Wye meter with a 25 A maximum current is being designed, the output frequency on F1 and F2 with a 100 imp/kWhr meter constant is 0.15 Hz at 25 A and 220 V (from Table 8). Looking at Table 9, the closest frequency to 0.15 Hz in column 5 is 0.12 Hz. Therefore, F_{1-7} = 0.6 Hz is selected for this design.

FREQUENCY OUTPUTS

Figure 2 shows a timing diagram for the various frequency outputs. The outputs F1 and F2 are the low frequency outputs that can be used to directly drive a stepper motor or electromechanical impulse counter. The F1 and F2 outputs provide two alternating high going pulses. The pulse width (t_1) is set at 275 ms, and the time between the rising edges of F1 and F2 (t_3) is approximately half the period of F1 (t_2). If, however, the period of F1 and F2 falls below 550 ms (1.81 Hz), the pulse width of F1 and F2 is set to half of their period. The maximum output frequencies for F1 and F2 are shown in Table 6.

The high frequency CF output is intended to be used for communications and calibration purposes. CF produces a 96 ms-wide active high pulse (t_4) at a frequency proportional to active power. The CF output frequencies are given in Table 7. As in the case of F1 and F2, if the period of CF (t_5) falls below 192 ms, the CF pulse width is set to half the period. For example, if the CF frequency is 20 Hz, the CF pulse width is 25 ms. One exception to this is when the mode is S0 = 1, SCF = S1 = 0. In this case, the CF pulse width is 66% of the period.

NO LOAD THRESHOLD

The ADE7752 also includes no load threshold and start-up current features that eliminate any creep effects in the meter. The ADE7752 is designed to issue a minimum output frequency. Any load generating a frequency lower than this minimum frequency does not cause a pulse to be issued on F1, F2, or CF. The minimum output frequency is given as 0.005% of the full-scale output frequency for each of the F_{1-7} frequency selections or approximately 0.00204% of the F_{1-7} frequency (see Table 10). For example, for an energy meter with a 100 imp/kWhr meter constant using F_{1-7} (4.77 Hz), the minimum output frequency at F1 or F2 would be 9.59×10^{-5} Hz. This would be 1.54×10^{-3} Hz at CF (16 × F1 Hz). In this example, the no load threshold would be equivalent to 3.45 W of load or a start-up current of 15.70 mA at 240 V.

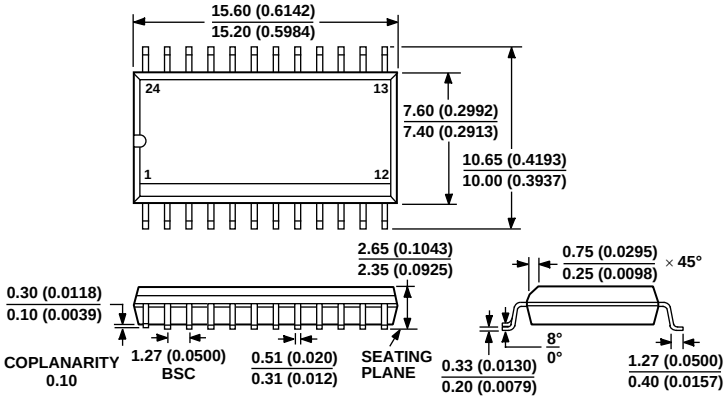
Table 10. CF, F1, and F2 Minimum Frequency at No Load Threshold

SCF	S1	S0	F1, F2 Min (Hz)	CF Min (Hz)
0	0	0	2.56×10^{-05}	4.09×10^{-03}
1	0	0	2.40×10^{-05}	1.92×10^{-04}
0	0	1	1.02×10^{-04}	1.64×10^{-02}
1	0	1	9.59×10^{-05}	1.54×10^{-03}
0	1	0	3.84×10^{-04}	6.14×10^{-03}
1	1	0	3.84×10^{-04}	3.07×10^{-03}
0	1	1	1.54×10^{-03}	1.23×10^{-02}
1	1	1	1.20×10^{-05}	1.92×10^{-04}

NEGATIVE POWER INFORMATION

The ADE7752 detects when the current and voltage channels of any of the three phase inputs have a phase difference greater than 90°: ϕ_A or ϕ_B or ϕ_C > 90°. This mechanism can detect wrong connection of the meter or generation of active energy. The REVP pin output goes active high when negative power is detected on any of the three phase inputs. If positive active energy is detected on all the three phases, REVP pin output is low. The REVP pin output changes state at the same time a pulse is issued on CF. If several phases measure negative power, the REVP pin output stays high until all the phases measure positive power. If a phase has gone below the no load threshold, REVP detection on this phase is disabled. REVP detection on this phase resumes when the power returns out of no load condition. See the No Load Threshold section.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AD
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Figure 28. 24-Lead Standard Small Outline Package [SOIC]
Wide Body (RW-24)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADE7752AR	-40°C to + 85°C	24- Lead SOIC Package	RW-24 in Tubes
ADE7752ARRL	-40°C to + 85°C	24- Lead SOIC Package	RW-24 on 13" Reels
ADE7752ARZ[1]	-40°C to + 85°C	24- Lead SOIC Package	RW-24 in Tubes
ADE7752ARZ-RL[1]	-40°C to + 85°C	24- Lead SOIC Package	RW-24 on 13" Reels
ADE7752AAR	-40°C to + 85°C	24- Lead SOIC Package	RW-24 in Tubes
ADE7752AAR-RL	-40°C to + 85°C	24- Lead SOIC Package	RW-24 on 13" Reels
ADE7752AARZ[1]	-40°C to + 85°C	24- Lead SOIC Package	RW-24 in Tubes
ADE7752AARZ-RL[1]	-40°C to + 85°C	24- Lead SOIC Package	RW-24 on 13" Reels
EVAL-ADE7752EB		Evaluation Board	
EVAL-ADE7752AEB		Evaluation Board	

[1] Z = Pb-free part.

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C02676-0-7/05(C)

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