## Features

- **Serial EEPROM Family for Configuring Altera FLEX® Devices**
- **Simple Interface to SRAM FPGAs**
- **EE Programmable 2M-bit Serial Memories Designed to Store Configuration Programs for Field Programmable Gate Arrays (FPGAs)**
- **Cascadable Read Back to Support Additional Configurations or Future Higher-density Arrays**
- **Low-power CMOS EEPROM Process**
- **Programmable Reset Polarity**
- **Available in the Space-efficient Surface-mount PLCC Package**
- **In-System Programmable Via 2-wire Bus**
- **Emulation of Atmel's AT24CXXX Serial EEPROMs**
- **Available in 3.3V ± 5% LV and 5V ± 5% C Versions**
- **System-friendly READY Pin**

## Description

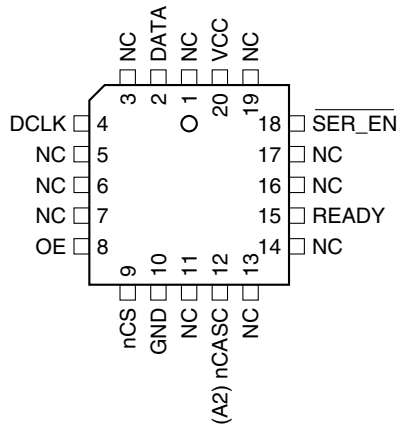
The AT17C020A and AT17LV020A (high-density AT17A Series) FPGA Configuration EEPROMs (Configurators) provide an easy-to-use, cost-effective configuration memory for programming Altera FLEX® devices. The AT17A Series is packaged in the popular 20-lead PLCC. The AT17A Series family uses a simple serial-access procedure to configure one or more FPGA devices. The AT17A Series organization supplies enough memory to configure one or multiple smaller FPGAs. Using a feature of the AT17A Series, the user can select the polarity of the reset function by programming internal EEPROM bytes. The AT17A parts generate their own internal clock and can be used as a system "master" for loading the FPGA devices.

The Atmel devices also support a system-friendly READY pin. The READY pin is used to simplify system power-up considerations.

The AT17A Series Configurators can be programmed with industry-standard programmers, or Atmel's ATDH2200E Programming Kit.

## Pin Configurations

**PLCC**




# FPGA Configuration EEPROM Memory

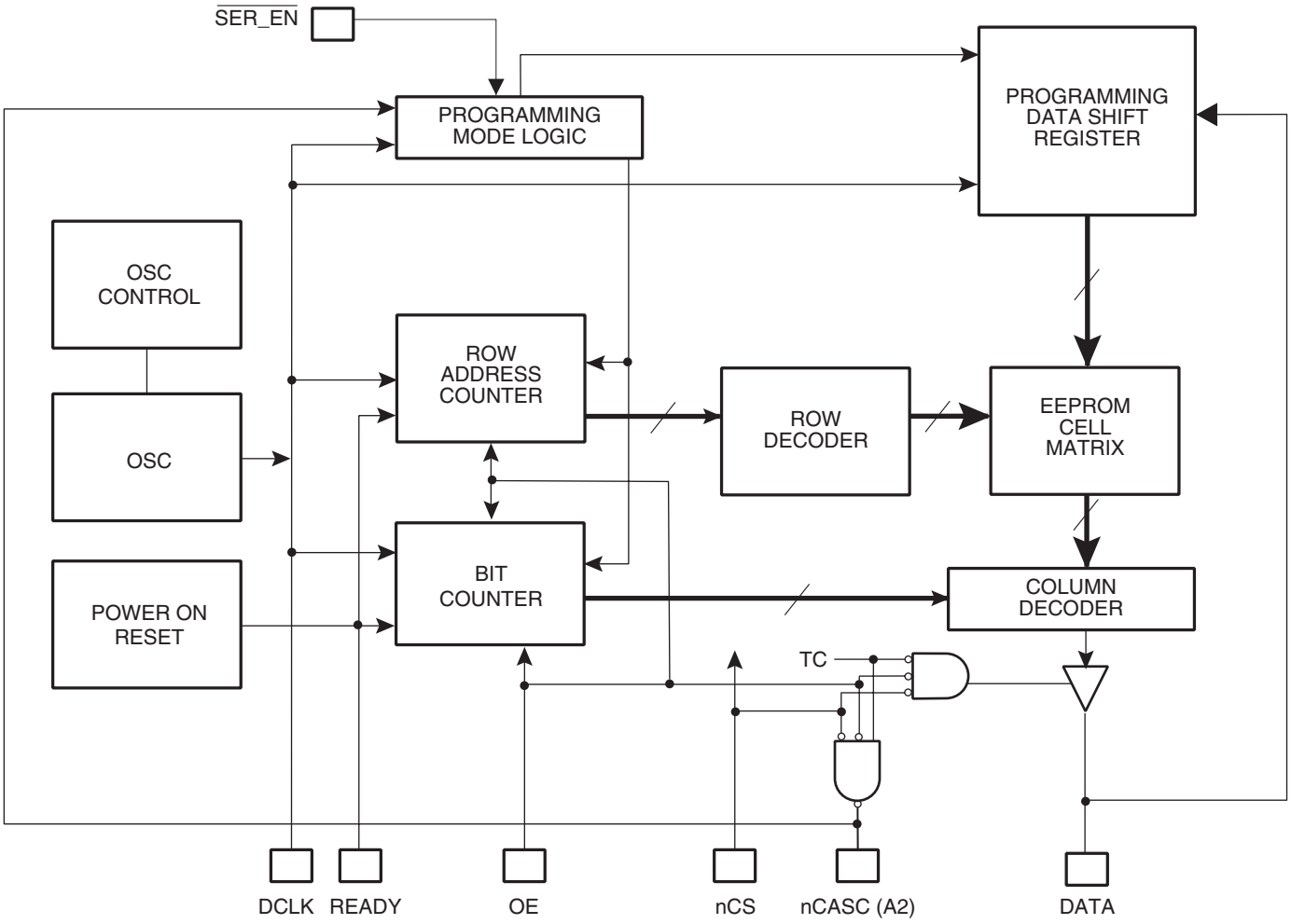
**2-Mbit**

**Altera Pinout**

# AT17C020A
# AT17LV020A

Rev. 1270A–05/00

## Block Diagram




## Device Configuration

The control signals for the configuration EEPROM-nCS, OE, and DCLK-interface directly with the FPGA device control signals. All FPGA devices can control the entire configuration process and retrieve data from the configuration EEPROM without requiring an external intelligent controller.

The configuration EEPROM's OE and nCS pins control the tri-state buffer on the DATA output pin and enable the address counter and the oscillator. When OE is driven Low, the configuration EEPROM resets its address counter and tri-states its DATA pin. The nCS pin also controls the output of the AT17A Series Configurator. If nCS is held High after the OE reset pulse, the counter is disabled and the DATA output pin is tri-stated. When nCS is driven Low, the counter and the DATA output pin are enabled. When OE is driven Low again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of the nCS.

When the Configurator has driven out all of its data and nCASC is driven Low, the device tri-states the DATA pin to avoid contention with other Configurators. Upon power-up, the address counter is automatically reset.

The READY pin is available as an open-collector indicator of the device's reset status; it is driven Low while the device is in its power-on reset cycle and released (tri-stated) when the cycle is complete.

This document discusses the EPF10K device interface. For more details or information on other Altera applications, please reference the "AT17A Series Conversions from Altera FPGA Serial Configuration Memories" application note.

## FPGA Device Configuration

FPGA devices can be configured with an AT17A Series EEPROM as shown in Figure 1. The AT17A Series device stores configuration data in its EEPROM array and clocks the data out serially with its internal oscillator. The OE, nCS, and DCLK pins supply the control signals for the address counter and the output tri-state buffer. The AT17A Series device sends a serial bitstream of configuration data to its DATA pin, which is connected to the DATA0 input pin on the FPGA device.

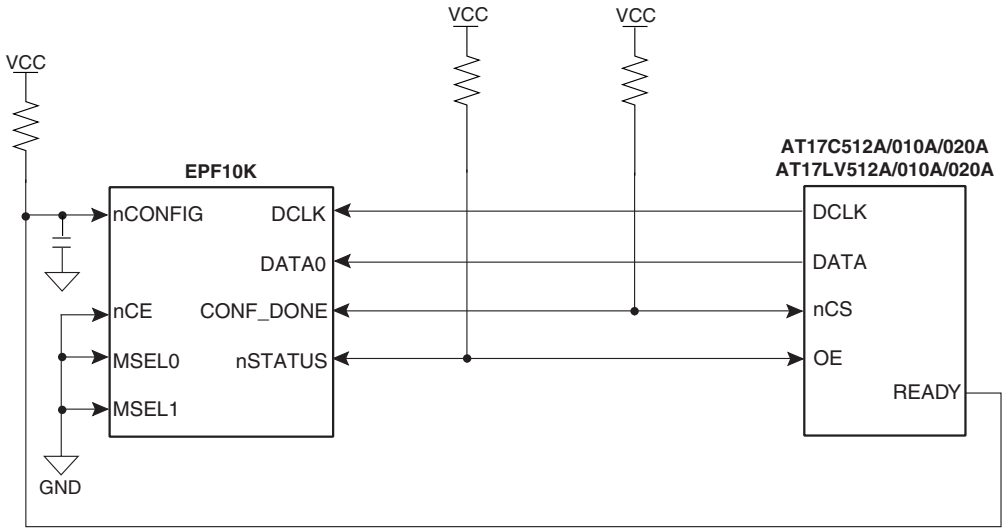
When configuration data for an FPGA device exceeds the capacity of a single AT17A Series device, multiple AT17A Series devices can be serially linked together (Figure 2). When multiple AT17A Series devices are required, the nCASC and nCS pins provide handshaking between the cascaded EEPROMs.

The position of an AT17A Series device in a chain determines its operation. The first AT17A Series device in a Configurator chain is powered up or reset with nCS Low and is configured for the FPGA device's protocol. This AT17A Series device supplies all clock pulses to one or more FPGA devices and to any downstream AT17A Series Configurator during configuration. The first AT17A Series Configurator also provides the first stream of data to the FPGA devices during multi-device configuration. Once the first AT17A Series device finishes sending configuration data, it drives its nCASC pin Low, which drives the nCS pin of the second AT17A Series device Low. This activates the second AT17A Series device to send configuration data to the FPGA device.

The first AT17A Series device clocks all subsequent AT17A Series devices until configuration is complete. Once all configuration data is transferred and nCS on the first AT17A Series device is driven High by CONF_DONE on the FPGA devices, the first AT17A Series device clocks 16 additional cycles to initialize the FPGA device before going into zero-power (idle) state. If nCS on the first AT17A Series device is driven High before all configuration data is transferred – or if the nCS is not driven High after all configuration data is transferred – nSTATUS is driven Low, indicating a configuration error.

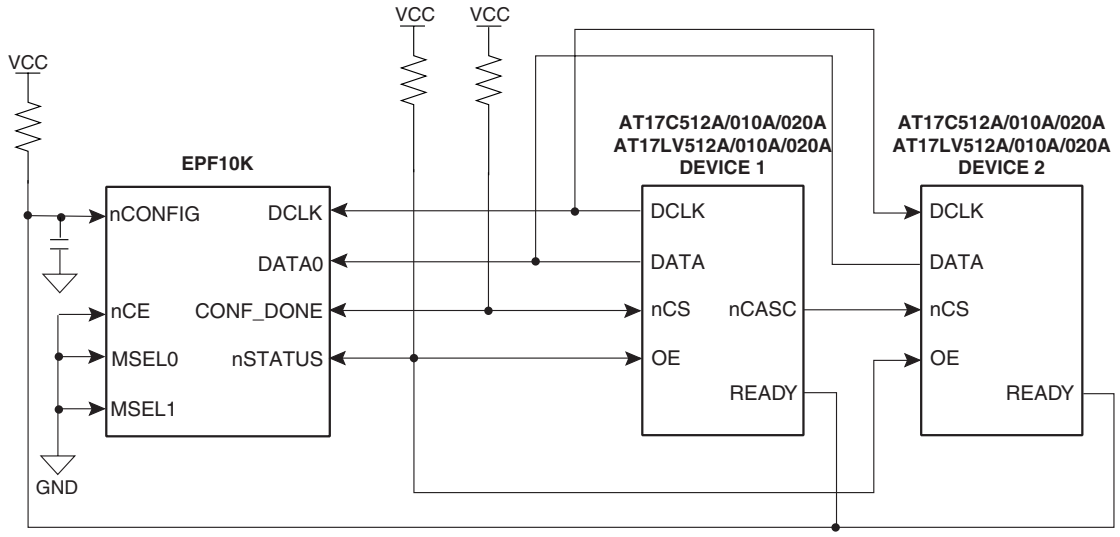
The READY pin is available as an open-collector indicator of the device's reset status; it is driven Low while the device is in its power-on reset cycle and released (tri-stated) when the cycle is complete. It can be used to hold the FPGA device in reset while it is completing its power-on reset but it cannot be used to effectively delay configuration (i.e., the output is released well before the system $V_{CC}$ has stabilized).

**Figure 1.** Configuration with a Single AT17A Series Configurator




Notes:
1. 1.0 kΩ resistors used unless otherwise specified.
2. Applicable to EPF6K.
3. Use of the READY pin is optional.
4. Introducing a RC delay to the input of nCONFIG is recommended to ensure that $V_{CC}$ (5V/3.3V) is reached before configuration begins. (nCONFIG can instead be connected to an active Low system reset signal.)
5. Reset polarity of EEPROM must be set active Low (OE active High).

**Figure 2.** Configuration with Multiple AT17A Series Configurators




Notes:
1. 1.0 kΩ resistors used unless otherwise specified.
2. Use of the READY pin is optional.
3. Introducing a RC delay to the input of nCONFIG is recommended to ensure that $V_{CC}$ (5V/3.3V) is reached before configuration begins. (nCONFIG can instead be connected to an active Low system reset signal.)
4. Reset polarity of EEPROM must be set active Low (OE active High).

## AT17A Series Reset Polarity

The AT17A Series Configurator allows the user to program the polarity of the OE pin as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE. For more details, please reference the "Programming Specification for Atmel's FPGA Configuration EEPROMs" application note.

## Programming Mode

The programming mode is entered by bringing $\overline{SER\_EN}$ Low. In this mode the chip can be programmed by the 2-wire serial interface. The programming is done at $V_{CC}$ supply only. Programming super voltages are generated inside the chip. See the "Programming Specification for Atmel's Configuration EEPROMs" application note for further information. The AT17 A-series parts are read/write at 5V nominal. The AT17LV A-series parts are read/write at 3.3V nominal.

## Standby Mode

The AT17A Series Configurator enters a low-power standby mode whenever nCS is asserted High. In this mode, the configuration consumes less than 0.5 mA of current at 5V. The output remains in a high-impedance state regardless of the state of the OE input.

## Pin Configurations

| 20 PLCC Pin | Name | I/O | Description |
|---|---|---|---|
| 2 | DATA | I/O | Three-state data output for configuration. Open-collector bi-directional pin for programming. |
| 4 | DCLK | I/O | Clock output or clock input. Rising edges on DCLK increment the internal address counter and present the next bit of data to the DATA pin. The counter is incremented only if the OE input is held High, the nCS input is held Low, and all configuration data has not been transferred to the target device (otherwise, as the master device, the DCLK pin drives Low). |
| 8 | OE | I | Output enable (active High) and reset (active Low) when $\overline{\text{SER\_EN}}$ is High. A Low logic level resets the address counter. A High logic level (with nCS Low) enables DATA and permits the address counter to count. In the mode, if this pin is Low (reset), the internal oscillator becomes inactive and DCLK drives Low. The logic polarity of this input is programmable and must be programmed active High (RESET active Low) by the user during programming for Altera applications. |
| 9 | nCS | I | Chip select input (active Low). A Low input (with OE High) allows DCLK to increment the address counter and enables DATA to drive out. If the AT17A Series is reset with nCS Low, the device initializes as the first (and master) device in a daisy-chain. If the AT17A Series is reset with nCS High, the device initializes as a subsequent AT17A Series device in the chain. |
| 10 | GND | | Ground pin. A 0.2 µF decoupling capacitor should be placed between the VCC and GND pins. |
| 12 | nCASC | O | Cascade select output (active Low). This output goes Low when the address counter has reached its maximum value. In a daisy-chain of AT17A Series devices, the nCASC pin of one device is usually connected to the nCS input pin of the next device in the chain, which permits DCLK from the master Configurator to clock data from a subsequent AT17A Series device in the chain. |
| | A2 | I | Device selection input, A2. This is used to enable (or select) the device during programming, (i.e., when $\overline{\text{SER\_EN}}$ is Low; please refer to the “Programming Specification” application note for more details). |
| 15 | READY | O | Open collector reset state indicator. Driven Low during power-up reset, released (tri-stated) when power-up is complete. (Recommend a 4.7 kΩ pull-up on this pin if used). |
| 18 | $\overline{\text{SER\_EN}}$ | I | Serial enable must be held High during FPGA loading operations. Bringing $\overline{\text{SER\_EN}}$ Low, enables the 2-wire serial programming mode. |
| 20 | VCC | | +3.3V/+5V power supply pin |

## Absolute Maximum Ratings*

| | |
|---|---|
| Operating Temperature | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | -0.1V to $V_{CC}$ +0.5V |
| Supply Voltage ($V_{CC}$) | -0.5V to +7.0V |
| Maximum Soldering Temp. (10 sec @ 1/16 in.) | 260°C |
| ESD ($R_{ZAP}$ = 1.5K, $C_{ZAP}$ = 100 pF) | 2000V |

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

## Operating Conditions

| Symbol | Description | | AT17C020A Min/Max | AT17LV020A Min/Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Commercial | Supply voltage relative to GND<br>-0°C to +70°C | 4.75/5.25 | 3.15/3.45 | V |
| | Industrial | Supply voltage relative to GND<br>-40°C to +85°C | 4.5/5.5 | 3.15/3.45 | V |
| | Military | Supply voltage relative to GND<br>-55°C to +125°C | 4.5/5.5 | 3.15/3.45 | V |

## DC Characteristics

$V_{CC}$ = 5V ± 5% Commercial / 5V ± 10% Ind./Mil.

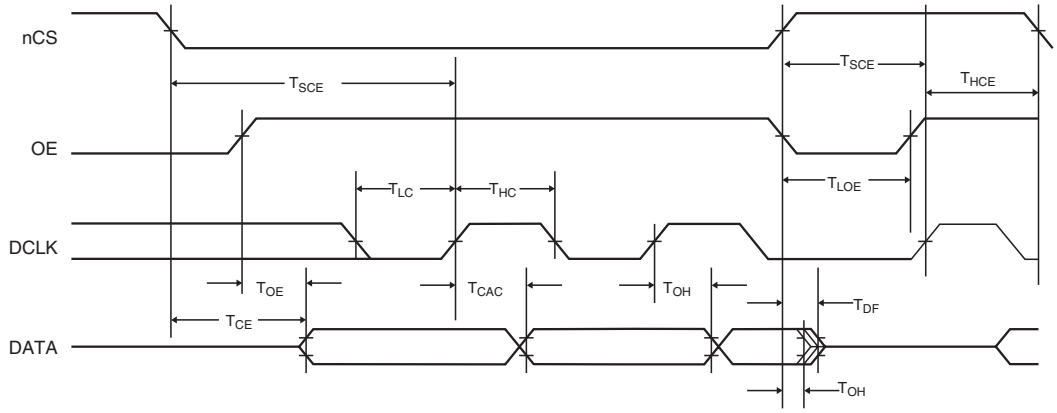
| Symbol | Description | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2.0 | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage | | 0 | 0.8 | V |
| $V_{OH}$ | High-level output voltage ($I_{OH}$ = -4 mA) | Commercial | 3.86 | | V |
| $V_{OL}$ | Low-level output voltage ($I_{OL}$ = +4 mA) | | | 0.32 | V |
| $V_{OH}$ | High-level output voltage ($I_{OH}$ = -4 mA) | Industrial | 3.76 | | V |
| $V_{OL}$ | Low-level output voltage ($I_{OL}$ = +4 mA) | | | 0.37 | V |
| $V_{OH}$ | High-level output voltage ($I_{OH}$ = -4 mA) | Military | 3.7 | | V |
| $V_{OL}$ | Low-level output voltage ($I_{OL}$ = +4 mA) | | | 0.4 | V |
| $I_{CCA}$ | Supply current, active mode (at FMAX) | | | 10 | mA |
| $I_L$ | Input or output leakage current ($V_{IN}$ = $V_{CC}$ or GND) | | -20 | 20 | µA |
| $I_{CCS}$ | Supply current, standby mode AT17C020A | Commercial | | 0.5 | mA |
| | | Industrial/Military | | 0.75 | mA |

## DC Characteristics

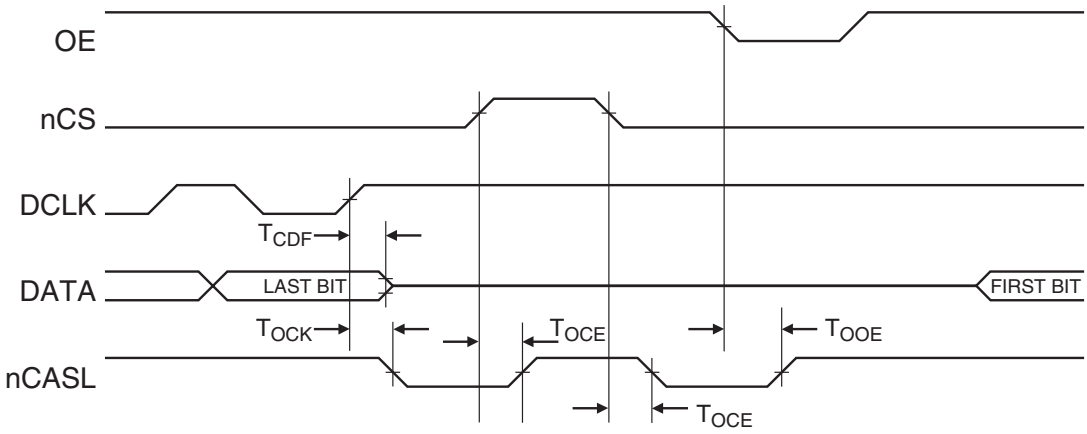
$V_{CC}$ = 3.3V ± 5%

| Symbol | Description | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2.0 | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage | | 0 | 0.8 | V |
| $V_{OH}$ | High-level output voltage ($I_{OH}$ = -2.5 mA) | Commercial | 2.4 | | V |
| $V_{OL}$ | Low-level output voltage ($I_{OL}$ = +3 mA) | | | 0.4 | V |
| $V_{OH}$ | High-level output voltage ($I_{OH}$ = -2 mA) | Industrial | 2.4 | | V |
| $V_{OL}$ | Low-level output voltage ($I_{OL}$ = +3 mA) | | | 0.4 | V |
| $V_{OH}$ | High-level output voltage ($I_{OH}$ = -2 mA) | Military | 2.4 | | V |
| $V_{OL}$ | Low-level output voltage ($I_{OL}$ = +2.5 mA) | | | 0.4 | V |
| $I_{CCA}$ | Supply current, active mode (at FMAX) | | | 5 | mA |
| $I_L$ | Input or output leakage current ($V_{IN}$ = $V_{CC}$ or GND) | | -20 | 20 | µA |
| $I_{CCS}$ | Supply current, standby mode | Commercial | | 200 | µA |
| | | Industrial/Military | | 200 | µA |

## AC Characteristics




## AC Characteristics When Cascading



## AC Characteristics for AT17C020A

$V_{CC}$ = 5V ± 5% Commercial / $V_{CC}$ = 5V ± 10% Ind./Mil

| Symbol | Description | Commercial | | Industrial/Military[1] | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $T_{OE}$[2] | OE to Data Delay | | 30 | | 35 | ns |
| $T_{CE}$[2] | nCS to Data Delay | | 45 | | 45 | ns |
| $T_{CAC}$[2] | DCLK to Data Delay | | 50 | | 55 | ns |
| $T_{OH}$ | Data Hold From nCS, OE, or DCLK | 0 | | 0 | | ns |
| $T_{DF}$[3] | nCS or OE to Data Float Delay | | 50 | | 50 | ns |
| $T_{LC}$ | DCLK Low Time Slave Mode | 20 | | 20 | | ns |
| $T_{HC}$ | DCLK High Time Slave Mode | 20 | | 20 | | ns |
| $T_{SCE}$ | nCS Setup Time to DCLK (to guarantee proper counting) | 20 | | 25 | | ns |
| $T_{HCE}$ | nCS Hold Time from DCLK (to guarantee proper counting) | 0 | | 0 | | ns |
| $T_{LOE}$ | OE Low Time (guarantees counter is reset) | 20 | | 20 | | ns |
| $F_{MAX}$ | MAX Input Clock Frequency Slave Mode | 12.5 | | 12.5 | | MHz |
| $T_{LC}$ | DCLK Low Time Master Mode | 30 | 250 | 30 | 250 | ns |
| $T_{HC}$ | DCLK High Time Master Mode | 30 | 250 | 30 | 250 | ns |

## AC Characteristics for AT17C020A When Cascading

$V_{CC}$ = 5V ± 5% Commercial / $V_{CC}$ = 5V ± 10% Ind./Mil.

| Symbol | Description | Commercial | | Industrial/Military[1] | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $T_{CDF}$ [3] | DCLK to Data Float Delay | | 50 | | 50 | ns |
| $T_{OCK}$[2] | DCLK to nCASC Delay | | 35 | | 40 | ns |
| $T_{OCE}$[2] | nCS to nCASC Delay | | 35 | | 35 | ns |
| $T_{OOE}$[2] | OE to nCASC Delay | | 30 | | 30 | ns |
| $F_{MAX}$ | MAX Input Clock Frequency | 12.5 | | 12.5 | | MHz |

Notes: 1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ±200 mV from steady state active levels.

## AC Characteristics for AT17LV020A

$V_{CC}$ = 3.3V ± 5% Commercial / $V_{CC}$ = 3.3V ± 5% Ind./Mil.

| Symbol | Description | Commercial | | Industrial/Military[1] | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $T_{OE}$[2] | OE to Data Delay | | 50 | | 55 | ns |
| $T_{CE}$[2] | nCS to Data Delay | | 55 | | 60 | ns |
| $T_{CAC}$[2] | DCLK to Data Delay | | 60 | | 65 | ns |
| $T_{OH}$ | Data Hold From nCS, OE, or DCLK | 0 | | 0 | | ns |
| $T_{DF}$[3] | nCS or OE to Data Float Delay | | 50 | | 50 | ns |
| $T_{LC}$ | DCLK Low Time Slave Mode | 25 | | 25 | | ns |
| $T_{HC}$ | DCLK High Time Slave Mode | 25 | | 25 | | ns |
| $T_{SCE}$ | nCS Setup Time to DCLK (to guarantee proper counting) | 35 | | 40 | | ns |
| $T_{HCE}$ | nCS Hold Time from DCLK (to guarantee proper counting) | 0 | | 0 | | ns |
| $T_{LOE}$ | OE Low Time (guarantees counter is reset) | 20 | | 20 | | ns |
| $F_{MAX}$ | MAX Input Clock Frequency Slave Mode | 12 | | 7.5 | | MHz |
| $T_{LC}$ | DCLK Low Time Master Mode | 30 | 300 | 30 | 300 | ns |
| $T_{HC}$ | DCLK High Time Master Mode | 30 | 300 | 30 | 300 | ns |

## AC Characteristics for AT17LV020A When Cascading

$V_{CC}$ = 3.3V ± 5% Commercial / $V_{CC}$ = 3.3V ± 5% Ind./Mil.

| Symbol | Description | Commercial | | Industrial/Military[1] | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $T_{CDF}$[3] | DCLK to Data Float Delay | | 50 | | 50 | ns |
| $T_{OCK}$[2] | DCLK to nCASC Delay | | 50 | | 55 | ns |
| $T_{OCE}$[2] | nCS to nCASC Delay | | 35 | | 40 | ns |
| $T_{OOE}$[2] | OE to nCASC Delay | | 35 | | 35 | ns |
| $F_{MAX}$ | MAX Input Clock Frequency Slave Mode | 12 | | 7.5 | | MHz |

Notes: 1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ±200 mV from steady state active levels.

## Ordering Information - 5V Devices

| Memory Size | Ordering Code | Package | Operation Range |
|---|---|---|---|
| 2M[1] | AT17C020A-10JC | 20J | Commercial (0°C to 70°C) |
| | AT17C020A-10JI | 20J | Industrial (-40°C to 85°C) |

## Ordering Information - 3.3V Devices

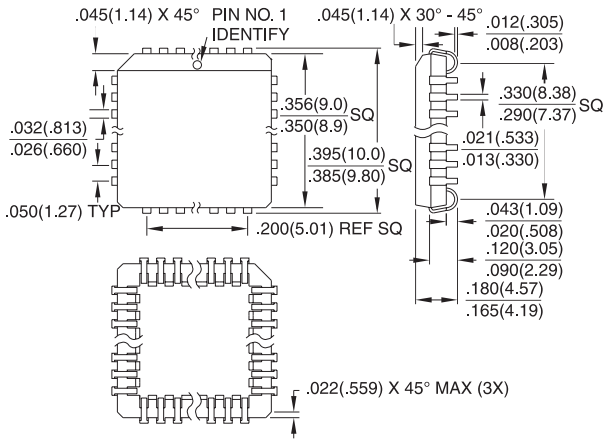
| Memory Size | Ordering Code | Package | Operation Range |
|---|---|---|---|
| 2M[1] | AT17LV020A-10JC | 20J | Commercial (0°C to 70°C) |
| | AT17LV020A-10JI | 20J | Industrial (-40°C to 85°C) |

Note: 1. Use 2M density parts to replace Altera EPC2.

| Package Type | |
|---|---|
| **20J** | 20-lead, Plastic J-leaded Chip Carrier (PLCC) |

## Packaging Information

**20J**, 20-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AA



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1270A–05/00/xM

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