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July 2015



# FCD5N60\_F085

# N-Channel SuperFET® MOSFET

**600 V, 4.6 A, 1.1** Ω

### **Features**

- 600V, 4.6A, typ.  $R_{ds(on)}$ =860m $\Omega$ @ $V_{GS}$ =10V
- Ultra Low Gate Charge (Typ. Q<sub>q</sub> = 16 nC)
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

### **Applications**

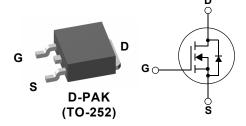
- Automotive On Board Charger
- Automotive DC/DC Converter for HEV



SuperFETTM is Fairchild's proprietary new generation of high voltage MOSFETs utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance.

This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFET is suitable for various automotive DC/DC power conversion.





For current package drawing, please refer to the Fairchild website at http://www.fairchildsemi.com/package-drawings/TO/TO252A03.pdf.

### **MOSFET Maximum Ratings** T<sub>.1</sub> = 25°C unless otherwise noted.

Symbol	Parameter		Ratings	Units
$V_{DSS}$	Drain-to-Source Voltage		600	V
$V_{GS}$	Gate-to-Source Voltage		±30	V
	Drain Current - Continuous (V <sub>GS</sub> =10) (Note 1)	T <sub>C</sub> = 25°C	4.6	^
ID	Pulsed Drain Current	T <sub>C</sub> = 25°C	See Figure 4	A
E <sub>AS</sub>	Single Pulse Avalanche Energy	(Note 1)	29	mJ
D	Power Dissipation		54	W
$P_{D}$	Derate Above 25°C		1.56	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature		-55 to + 150	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case		2.3	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 2)		83	°C/W

#### Notes:

- 1: Starting  $T_J = 25^{\circ}C$ , L = 10mH,  $I_{AS} = 2.4A$ ,  $V_{DD} = 100V$  during inductor charging and  $V_{DD} = 0V$  during time in avalanche.
- 2: R<sub>0,JA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>0,JC</sub> is guaranteed by design, while R<sub>0,JA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2oz copper.

### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCD5N60	FCD5N60_F085	D-PAK(TO-252)	13"	16mm	2500units

Units

nΑ

Max.

±100

# **Electrical Characteristics** $T_J = 25^{\circ}C$ unless otherwise noted.

**Parameter** 

Gate-to-Source Leakage Current

Off Characteristics							
B <sub>VDSS</sub>	Drain-to-Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	600	-	-	V	
1	Drain-to-Source Leakage Current	$V_{DS}$ =600V, $T_J = 25^{\circ}C$	-	-	1	μΑ	
IDSS	Dialii-to-Source Leakage Current	$V_{00} = 0V$ $T_1 = 150^{\circ}C$ (Note 4)	_	_	10	пΔ	

 $V_{GS} = \pm 30V$ 

**Test Conditions** 

Min.

Тур.

### **On Characteristics**

Symbol

 $I_{GSS}$ 

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , I	<sub>D</sub> = 250μA	3.0	-	5.0	V
R <sub>DS(on)</sub> Drain to Source On Resistance	I <sub>D</sub> = 4.6A,	$T_J = 25^{\circ}C$	-	0.86	1.1	Ω	
	V <sub>GS</sub> = 10V	$T_J = 150^{\circ}C \text{ (Note 4)}$	-	2.5	3.2	Ω	

## **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	.,		-	570	-	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = — f = 1MHz	$V_{DS} = 25V, V_{GS} = 0V,$		280	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			-	20	-	pF
$R_g$	Gate Resistance	f = 1MHz		-	1.9	-	Ω
$Q_{g(ToT)}$	Total Gate Charge	$V_{GS} = 0$ to 10V	V <sub>DD</sub> = 480V	-	16	21	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0$ to 2V	I <sub>D</sub> = 4.6A	-	1.0	-	nC
$Q_{gs}$	Gate-to-Source Gate Charge		_	-	3.2	-	nC
$Q_{gd}$	Gate-to-Drain "Miller" Charge			-	7.6	-	nC

## **Switching Characteristics**

t <sub>on</sub>	Turn-On Time		-	-	84	ns
t <sub>d(on)</sub>	Turn-On Delay		-	18	-	ns
t <sub>r</sub>	Rise Time	$V_{DD} = 300V, I_{D} = 4.6A,$	-	19	-	ns
t <sub>d(off)</sub>	Turn-Off Delay	$V_{DD}$ = 300V, $I_{D}$ = 4.6A, $V_{GS}$ = 10V, $R_{GEN}$ = 25 $\Omega$	-	48	-	ns
t <sub>f</sub>	Fall Time		-	13	-	ns
t <sub>off</sub>	Turn-Off Time		-	-	178	ns

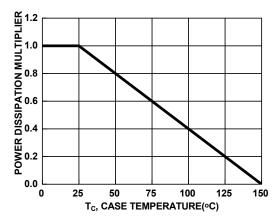
### **Drain-Source Diode Characteristics**

$V_{SD}$	Source-to-Drain Diode Voltage	I <sub>SD</sub> = 4.6A, V <sub>GS</sub> = 0V	-	-	1.25	V
t <sub>rr</sub>	Reverse-Recovery Time	V <sub>DD</sub> = 480V, I <sub>F</sub> = 4.6A,	-	190	250	ns
Q <sub>rr</sub>	Reverse-Recovery Charge	$dI_{SD}/dt = 100A/\mu s$	-	1.7	2.2	μС

#### Note

4: The maximum value is specified by design at  $T_J$  = 150°C. Product is not tested to this condition in production.

# **Typical Characteristics**



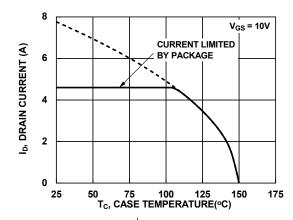


Figure 1. Normalized Power Dissipation vs. Case Temperature

Figure 2. Maximum Continuous Drain Current vs.

Case Temperature

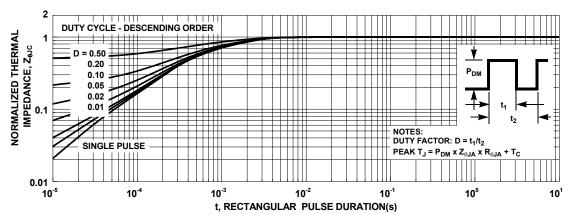


Figure 3. Normalized Maximum Transient Thermal Impedance

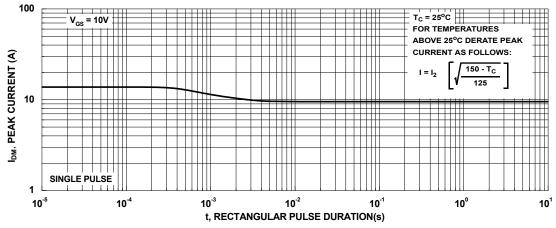
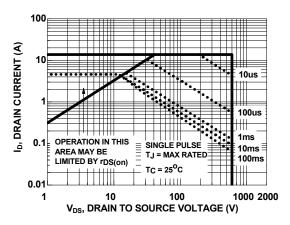


Figure 4. Peak Current Capability

## **Typical Characteristics**



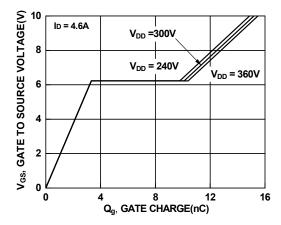
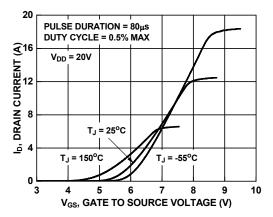


Figure 5. Forward Bias Safe Operating Area

Figure 6. Gate Charge vs. Gate to Source Voltage



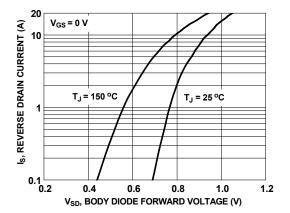
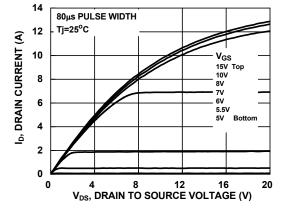


Figure 7. Transfer Characteristics

Figure 8. Forward Diode Characteristics



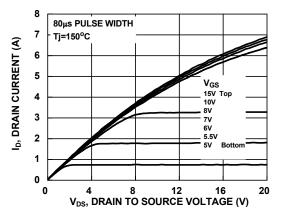


Figure 9. Saturation Characteristics

Figure 10. Saturation Characteristics

# **Typical Characteristics**

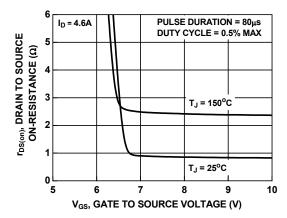


Figure 11. R<sub>DSON</sub> vs. Gate Voltage

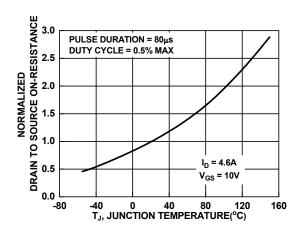


Figure 12. Normalized R<sub>DSON</sub> vs. Junction Temperature

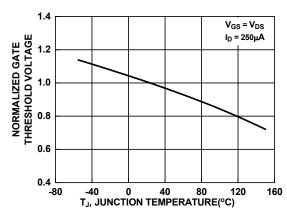


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

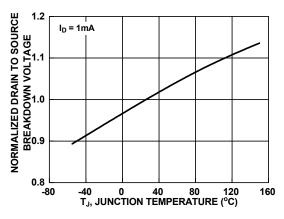


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

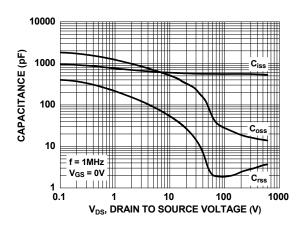


Figure 15. Capacitance vs. Drain to Source Voltage





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