High Stability Isolated Error Amplifier

ADuM3190S

1.0 Scope

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. http://www.analog.com/aeroinfo

This data specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at http://www.analog.com/ADuM3190

2.0 Part Number

The complete part number(s) of this specification follows:

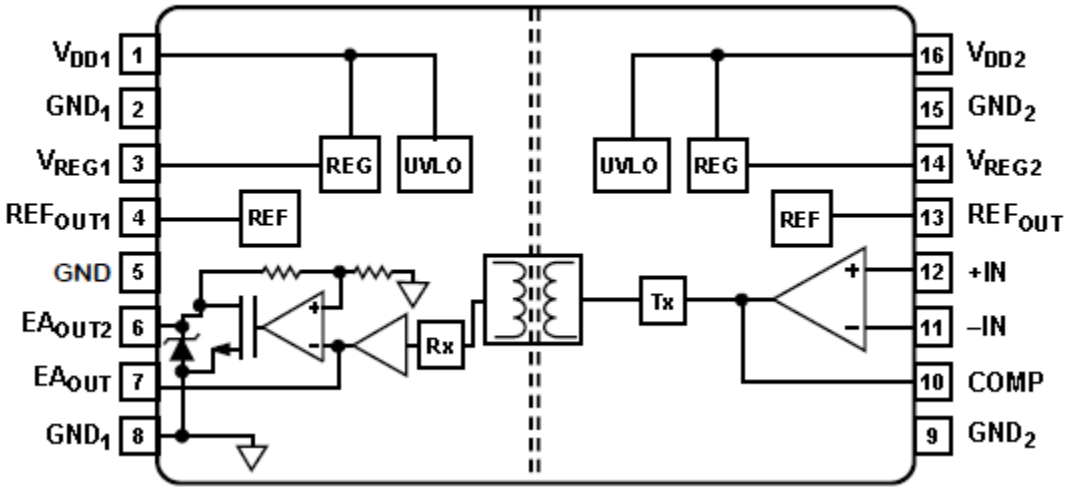
Specific Part Number	Description
ADUM3190P703F	High Stability Isolated Error Amplifier tested to 30krad
ADUM3190L703F	High Stability Isolated Error Amplifier tested to 50krad

3.0 Case Outline

The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline Letter	Descriptive Designator	Terminals	Lead Finish	Package style
X	CDFP4-F16	16 lead	Hot Solder Dip	Bottom Brazed FlatPack

FUNCTIONAL BLOCK DIAGRAM



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Package: X			
Pin Number	Terminal Symbol	Pin Type	Pin Description
1	VDD1	Power	Supply Voltage for Side 1 (3.0 V to 20 V). 1/
2	GND1	Power	Ground Reference for Side 1. 3/, 12/
3	VREG1	Power	Internal Supply Voltage for Side 1. 2/
4	REFOUT1	Analog output	Reference Output Voltage for Side 1. 5/
5	GND	Power	Ground 6/, 12/
6	EAOUT2	Analog output	Isolated Output Voltage 2, Open-Drain Output. 7/
7	EAOUT	Analog output	Isolated Output Voltage.
8	GND1	Power	Ground Reference for Side 1. 3/, 12/
9	GND2	Power	Ground Reference for Side 2. 4/
10	COMP	Analog output	Output of the Op Amp. 8/
11	−IN	Analog input	Inverting Op Amp Input. 9/
12	+IN	Analog input	Noninverting Op Amp Input. 10/
13	REFOUT	Analog output	Reference Output Voltage for Side 2. 11/
14	VREG2	Power	Internal Supply Voltage for Side 2. 2/
15	GND2	Power	Ground Reference for Side 2. 4/
16	VDD2	Power	Supply Voltage for Side 2 (3.0 V to 20) V 1/
Lid		Power	Metal Lid electrically connected to ground (GND1)

Figure 1 – Terminal Connections

1/ Connect a ceramic bypass capacitor of value 1 µF between VDD1 (Pin 1) and GND1 (Pin 2) and between VDD2 (Pin 16) and GND2 (Pin 15)
2/ Connect a 1 µF capacitor between VREG1 (Pin 3) and GND1 (Pin2) and VREG2 (Pin 14)and GND2(Pin 15).
3/ Pin 2 and Pin 8 are internally connected, and connecting both to GND1 is recommended.
4/ Pin 9 and Pin 15 are internally connected, and connecting both to GND2 is recommended.
5/ The maximum capacitance for this pin (CREFOUT1) must not exceed 15 pF.
6/ Connect Pin 5 to GND1; do not leave this pin floating.
7/ Connect a pull-up resistor between EAOUT2 and VDD1 for current up to 1 mA.
8/ A loop compensation network can be connected between the COMP pin and the −IN pin.
9/ Pin 11 is the connection for the power supply setpoint and compensation network.
10/ Pin 12 can be used as a reference input.
11/ The maximum capacitance for this pin (CREFOUT) must not exceed 15 pF.
12/ Internally connected to Metal Lid.

4.0 Specifications

4.1. Absolute Maximum Ratings 1/

Supply voltage (V_{DD1}, V_{DD2})	24 V 2/
Supply voltage (V_{REG1}, V_{REG2})	3.6 V 2/
Input voltage (+IN, -IN)	3.6 V 7/
Output voltages (REF_{OUT}, COMP, REF_{OUT1}, EA_{OUT})	3.6 V
Output voltages (EA_{OUT2})	5.8 V
Output Current per Output Pin	-11 mA to +11 mA 7/
Common-Mode Transients	-100 kV/µs – 100 kV/µs 3/
Storage temperature range	-65°C to +150°C
Junction temperature maximum (T_J)	+150°C
Lead temperature (soldering, 60 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	52 °C/W 4/
Thermal resistance, junction-to-ambient (θ_{JA})	104 °C/W 4/
ESD Sensitivity (HBM)……..	Class 2

4.2. Recommended Operating Conditions

Supply voltage (V_{DD1}, V_{DD2})	3.0 V to 20.0 V
Ambient operating temperature range (T_A)…….	-55°C to +125°C
Max input signal rise and fall times (t_R, t_F)	1 ms

4.3. Nominal Operating Performance Characteristics 5/

Input Capacitance	2 pF
EA_{OUT} Impedance (V_{DD2} or V_{DD1} < UVLO threshold)	High-Z
Input-to-Output Capacitance (C_{I-O})	2.2 pF 6/
Input Capacitance (C_I)	4 pF

4.4. Radiation Features

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s)….50 krads(Si)

1/ Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

2/ All voltages are relative to their respective grounds.

3/ Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage

4/ Measurement taken under absolute worst case condition and represents data taken with thermal camera for highest power density location. See MIL-STD-1835 for average Θ_{JC} number.

5/ All typical specifications are at TA = 25°C and VDD1 = VDD2 = 5 V, unless otherwise noted.

6/ Input capacitance is from any input data pin to ground.

7/ See Figure 2 for maximum rated power for various temperatures.

TABLE IA – ELECTRICAL PERFORMANCE CHARACTERISTICS

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
ACCURACY						
Error 7/	Err	(1.225 V – EA_{OUT})/1.225 V × 100% (1.225 V – EA_{OUT2})/1.225 V × 100%	1,3	-0.5	0.5	%
			2		0.7	
		M,D,P	1	-0.75	0.75	
		M,D,P,L	1	-1	1	
OP AMP						
Offset Error	V_{OS_OPAMP}		1,2,3	-5	5	mV
		M,D,P,L	1	-5	5	
Open –Loop Gain	Avo		1,2,3	66		dB
		M,D,P,L	1	66		
Input Common-Mode Range	IVR		1,2,3	0.35	1.5	V
		M,D,P,L	1	0.35	1.5	
Gain Bandwidth	GBP		4,5,6		10	MHz
Common-Mode Rejection Ratio	CMRR		1,2,3	60		dB
		M,D,P,L	1	60		
Output Voltage Range	VOH_{OPAMP}	COMP pin	1,2,3	2.7		V
		M,D,P,L	1	2.7		
	VOL_{OPAMP}		1,2,3		0.2	
		M,D,P,L	1		0.2	
Input Bias Current	I_B		1,2,3	-0.01	0.01	uA
		M,D,P,L	1	-0.01	0.01	
REFERENCE						
Output Voltage	Vref	0 to 2mA, C_{REFOUT} = 15 pF	1	1.215	1.235	V
			2,3	1.213	1.237	
		M,D,P,L	1	1.215	1.235	
Output Current	I_{VREF}	C_{REFOUT} = 15pF	1,2,3	2.0		mA
		M,D,P,L	1	2.0		
UVLO						
Positive Going Threshold 6/	$UVLO_{LO-HI}$		1,2,3		2.96	V
		M,D,P,L	1		2.96	
Negative Going Threshold	$UVLO_{HI-LO}$		1,2,3	2.4		V
		M,D,P,L	1	2.4		
OUTPUT CHARACTERISTICS						
Output Gain 4/	Gain	From COMP to E_{Aout}, 0.4V to 1.92V, +/-3mA, VDD1 = 3V, 5V	1,2,3	0.83	1.17	V/V
		M,D,P,L	1	0.83	1.17	
		From E_{Aout} to E_{Aout2}, 0.4V to 1.92V, +/-1mA, VDD1 = 10V, 20V	1,2,3	2.5	2.7	
		M,D,P,L	1	2.5	2.7	
Output Offset Voltage	$V_{OS\_COMP\_EAout}$	From COMP to EAout, 0.4V to 1.92V, +/-3mA , VDD1 = 3V, 5V	1,2,3	-0.2	+0.2	V
		M,D,P,L	1	-0.2	+0.2	
	$V_{OS\_EAout\_EAout2}$	From E_{Aout} to E_{Aout2}, 0.4V to 1.92V, +/-1mA, VDD1 = 10V, 20V	1,2,3	-0.1	+0.1	
		M,D,P,L	1	-0.1	+0.1	
Output Linearity 5/	LE	From COMP to EAout, 0.4V to 1.92V, +/-3mA, VDD1 = 3V, 5V	1,2,3	-1	+1	%
		M,D,P,L	1	-1	+1	
		From EAout to EAout2, 0.4V to 1.92V, +/-1mA, VDD1 = 10V, 20V	1,2,3	-1	+1	
		M,D,P,L	1	-1	+1	

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
-3dB Bandwidth 2/, 3/	$-3dB_{EAOUT}$	From COMP to EAOUT, Vin= 0.4 V to 0.95V, VDD1 = 3V, 5V Vin= 0.4 V to 2.1V, VDD1 = 20 V	1,2,3	250		kHz
	$-3dB_{EAOUT2}$	From COMP to EAOUT2 Vin= 0.4 V to 0.95V, VDD1 = 3V, 5V Vin= 0.4 V to 2.1V, VDD1 = 20 V	1,2,3	250		
Output Voltage, EA_{OUT}	VOL_{EAOUT}	+/-3mA output, VDD1 = 3V, 5V	1,2,3		0.4	V
		M,D,P,L	1		0.4	
	VOH_{EAOUT}	+/-3mA output, VDD1 = 3V, 5V	1,2,3	2.4		
		M,D,P,L	1	2.4		
Output Voltage, EA_{OUT2}	VOL_{EAOUT2}	+/-1mA output, VDD1 = 4.5V, 5.5V, 10V, 15V, 20V	1,2,3		0.6	V
		M,D,P,L	1		0.6	
	VOH_{EAOUT2}	+/-1mA output, VDD1 = 4.5V	1,2,3	4.4		
		M,D,P,L	1	4.4		
		+/-1mA output, VDD1 = 5V, 5.5V	1,2,3	4.8		
		M,D,P,L	1	4.8		
		+/-1mA output, VDD1 = 10V, 15V, & 20V	1,2,3	5		
		M,D,P,L	1	5		
Noise, E_{Aout} 2/, 3/	e_n rms	VDD1=VDD2=3V	4,5,6		2	mVrms
		VDD1=VDD2=5V	4,5,6		2.8	
		VDD1=VDD2=20V	4,5,6		3.5	
Noise, E_{Aout2} 2/, 3/	e_n rms	VDD1=VDD2=3V	4,5,6		4.8	
		VDD1=VDD2=5V	4,5,6		7	
		VDD1=VDD2=20V	4,5,6		7.5	
POWER SUPPLY						
Operating range: Both Sides	V_{DD1}, V_{DD2}		1,2,3	3	20	V
		M,D,P,L	1	3	20	
Power Supply Rejection Ratio	PSRR	DC, VDD1 = VDD2 = 3 V to 20 V	1,2,3	60		dB
		M,D,P,L	1	60		
Supply Current	I_{DD1}		1,2,3		2	mA
		M,D,P,L	1		2	
	I_{DD2}		1,2,3		5	
		M,D,P,L	1		5	

TABLE IA NOTES:

1/ T_A nom = 25ºC, T_A max = 125ºC, T_A min = -55ºC and VDD1 = VDD2 = 3V min, VDD1 = VDD2 = 5V nom and VDD1 = VDD2 = 20V max unless otherwise noted.

2/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.

3/ Parameter is not tested post irradiation

4/ Output gain is defined as the slope of the best-fit line of the output voltage vs. the input voltage over the specified input range, with the offset error adjusted out.

5/ Output linearity is defined as the peak-to-peak output deviation from the best-fit line of the output gain, expressed as a percentage of the full-scale output voltage.

6/ For VDD2, if ramping the supply voltage to turn on the outputs, be sure to start ramp where 2.55V $\leq$ VDD2 $\leq$ 2.7V.

7/ Accuracy is measured using circuit configuration in Figure 3 for EAout and Figure 4 for EAout2

TABLE IB – ELECTRICAL PERFORMANCE CHARACTERISTICS- INSULATION AND SAFETY-RELATED SPECIFICATIONS1/, 2/

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage	Iso	700	Vpeak	1-minute duration
Resistance (Input-to-Output) 3/	R_{I-O}	10^{12}	Ω	
Maximum Working Insulation Voltage 4/	CWV	466	Vpeak	1ppm for 30-year minimum lifetime 5/

TABLE IB NOTES:

1/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots T_A = 25ºC.

2/ Parameter is not tested post irradiation

3/ The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together and Pin 9 through Pin 16 are shorted together.

4/ Refers to continuous voltage magnitude imposed across the isolation barrier. Long term operation at this high voltage can lead to shortened isolation life. Continuous working voltage exceeding the rated value may cause permanent damage.

5/ For Bipolar AC Voltage environment which is worst case condition for *i*Coupler products.

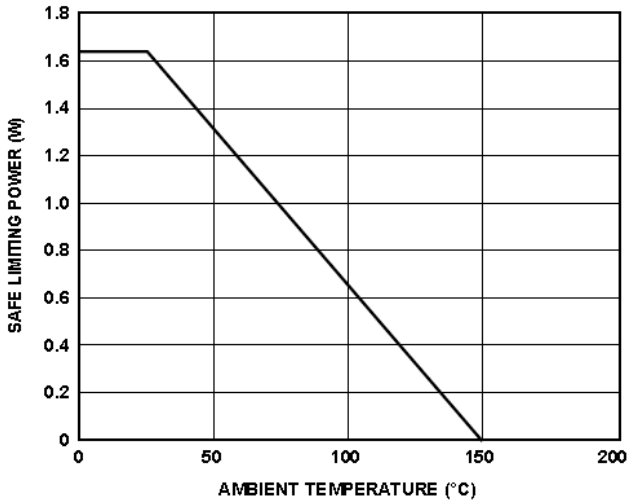

Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DINV VDE V 0884-10
See note 8/ at the end of Section 4.0

TABLE IIA – ELECTRICAL TEST REQUIREMENTS:

Table IIA	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1,2,3,4,5,6 1/ 2/
Group A Test Requirements	1,2,3, 4,5,6
Group C end-point electrical parameters	1,2,3, 4,5,6 2/
Group D end-point electrical parameters	1,2,3, 4,5,6
Group E end-point electrical parameters	1

Table IIA Notes:
1/ PDA applies to Table I subgroup 1 and Table IIB delta parameters.
2/ See Table IIB for delta parameters

TABLE IIB – LIFE TEST/BURN-IN DELTA LIMITS (V_{DD1} = V_{DD2}= 3v to 20V) 1/ 2/

Table IIB			
Parameter	Symbol	Delta	Units
Offset Error VDD1=VDD2 = 3 V	V_{OS_OPAMP}	±0.25	mV
Offset Error VDD1=VDD2 = 5 V	V_{OS_OPAMP}	±0.25	mV
Offset Error VDD1=VDD2 = 20 V	V_{OS_OPAMP}	±0.25	mV
Input Bias Current VDD1=VDD2 = 3 V	I_B	±0.95	nA
Input Bias Current VDD1=VDD2 = 5 V	I_B	±0.95	nA
Input Bias Current VDD1=VDD2 = 20 V	I_B	±0.95	nA
Output Offset Voltage (EAout to EAout2) at VDD1 = VDD2 =10 V, -1 mA	$V_{OS\_EAout\_EAout2}$	16	mV
Output Offset Voltage (EAout to EAout2) at VDD1 = VDD2 =20 V, -1 mA	$V_{OS\_EAout\_EAout2}$	16	mV
Output Offset Voltage (Comp to EAout) at VDD1 = VDD2 =3 V, -3 mA	$V_{OS\_COMP\_EAout}$	10	mV
Output Offset Voltage (Comp to EAout) at VDD1 = VDD2 =5 V, -3 mA	$V_{OS\_COMP\_EAout}$	10	mV
Supply Current IDD1 at Vdd =3 V, Vdd =5 V and Vdd =20 V	I_{DD1}	±0.5	mA
Supply Current, IDD2 at Vdd =3 V, Vdd =5 V and Vdd =20 V	I_{DD2}	±0.5	mA

1/ 240 hour burn in and group C end point electrical parameters.
2/ Deltas are performed at room temperature TA = +25°C.

5.0 Burn-In Life Test, and Radiation

5.1. Burn-In Test Circuit, Life Test Circuit

5.1.1. The test conditions and circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 test condition B of MIL –STD-883.

5.1.2. HTRB is not applicable for this drawing.

5.2. Radiation Exposure Circuit

5.2.1. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A.

6.0 MIL-PRF-38535 QMLV Exceptions

6.1. Wafer Fabrication

Wafer fabrication occurs at MIL-PRF-38535 QML Class Q certified facility.

6.2. Wafer Lot Acceptance (WLA)

WLA per MIL-STD-883 TM 5007 is not available for this product. SEM inspection per MIL-STD-883 TM2018 is not applicable to the ADuM3190S. The wafer fabrication process is manufactured using planarized metallization

6.3. Device contains bi-metallic wire bonds (Gold bond wires on Aluminum die pads).

7.0 Application Notes

TEST CIRCUITS

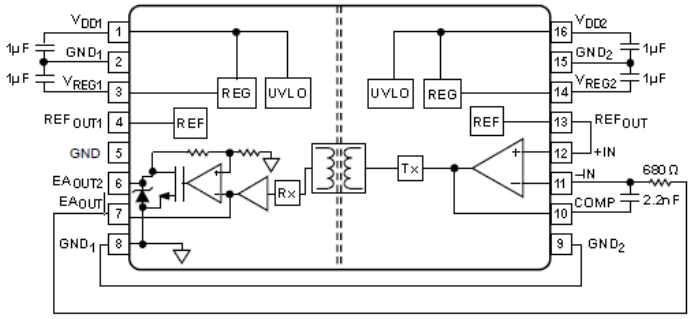

Figure 3. Test Circuit 1: Accuracy Circuit Using EA_{OUT}

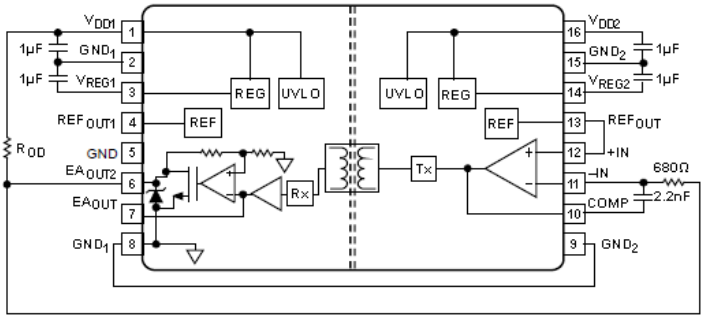

Figure 4. Test Circuit 2: Accuracy Circuit Using EA_{OUT2}

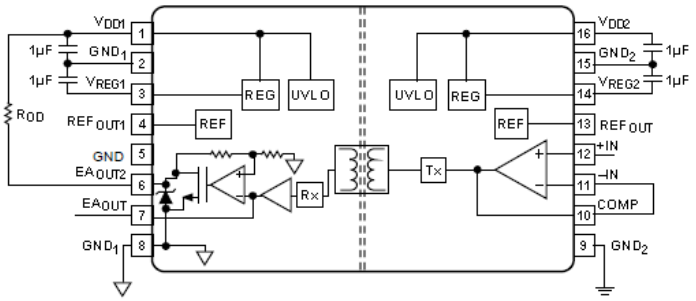

Figure 5. Test Circuit 3: Isolated Amplifier Circuit

THEORY OF OPERATION

In the test circuits of the ADuM3190 (see Figure 3 through Figure 5), external supply voltages from 3 V to 20 V are provided to the VDD1 and VDD2 pins, and internal regulators provide 3.0 V to operate the internal circuits of each side of the ADuM3190. An internal precision 1.225 V reference provides the reference for the ±1% accuracy of the isolated error amplifier. UVLO circuits monitor the VDDx supplies to turn on the internal circuits when the 2.96 V rising threshold is met and to turn off the error amplifier outputs to a high impedance state when VDDx falls below 2.5 V.

The op amp on the right side of the device has a noninverting +IN pin and an inverting −IN pin available for connecting a feedback voltage in an isolated dc-to-dc converter output, usually through a voltage divider. The COMP pin is the op amp output, which can be used to attach resistor and capacitor components in a compensation network. The COMP pin internally drives the Tx transmitter block, which converts the op amp

output voltage into an encoded output that is used to drive the digital isolator transformer.

On the left side of the ADuM3190, the transformer output PWM signal is decoded by the Rx block, which converts the signal into a voltage that drives an amplifier block; the amplifier block produces the error amplifier output available at the EA_{OUT} pin. The EA_{OUT} pin can deliver ±3 mA and has a voltage level between 0.4 V and 2.4 V, which is typically used to drive the input of a PWM controller in a dc-to-dc circuit.

For applications that need more output voltage to drive their controllers, Figure 4 illustrates the use of the EA_{OUT2} pin output, which delivers up to ±1 mA with an output voltage of 0.6 V to 4.8 V for an output that has a pull-up resistor to a 5 V supply. If the EA_{OUT2} pull-up resistor connects to a 10 V to 20 V supply, the output is specified to a minimum of 5.0 V to allow use with a PWM controller requiring a minimum input operation of 5V.

ACCURACY CIRCUIT OPERATION

See Figure 3 and Figure 4 for stability of the accuracy circuits. The op amp on the right side of the ADuM3190, from the −IN pin to the COMP pin, has a unity-gain bandwidth (UGBW) of10 MHz. Figure 6, Bode Plot 1, shows a dashed line for the op amp alone and its 10 MHz pole.

Figure 6 also shows the linear isolator alone (the blocks from the op amp output to the ADuM3190 output, labeled as the linear isolator), which introduces a pole at approximately 400 kHz. This total Bode plot of the op amp and linear isolator shows that the phase shift is approximately −180° from the −IN pin to the EA_{OUT} pin before the crossover frequency. Because a −180° phase shift can make the system unstable, adding an integrator configuration, as shown in the test circuits in Figure 3 and Figure 4, consisting of a 2.2 nF capacitor and a 680 Ω resistor helps to make the system stable. In Figure 7, Bode Plot 2 with an integrator configuration added, the system crosses over 0 dB at approximately 100 kHz, but the circuit is more stable with a phase shift of approximately −120°, which yields a stable 60° phase margin.

This circuit is used for accuracy tests only, not for real-world applications, because it has a 680 Ω resistor across the isolation barrier to close the loop for the error amplifier; this resistor causes leakage current to flow across the isolation barrier. For this test circuit only, GND1 must be connected to GND2 to create a return for the leakage current created by the 680 Ω resistor connection.

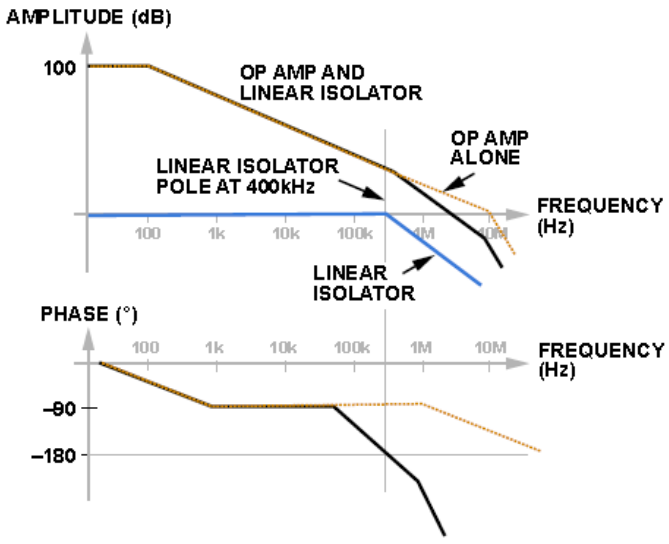

Figure 6. Bode Plot 1

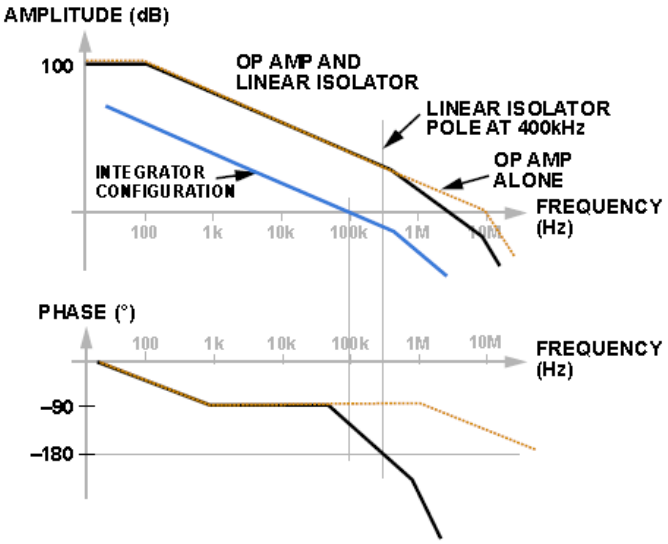

Figure 7. Bode Plot 2

ISOLATED AMPLIFIER CIRCUIT OPERATION

Figure 5 shows an isolated amplifier circuit. In this circuit, the input side amplifier is set as a unity-gain buffer so that the EA_{OUT} output follows the +IN input. The EA_{OUT2} output follows the EA_{OUT} output, but with a voltage gain of 2.6.

This circuit has an open-drain output, which must be pulled up to a supply voltage from 3 V to 20 V using a resistor value set for an output current of up to 1 mA. The EA_{OUT2} output can be used to drive up to 1 mA to the input of a device that requires a minimum input operation of 5 V. The EA_{OUT2} circuit has an internal diode clamp to protect the internal circuits from voltages greater than 5 V.

The gain, offset, and linearity of EA_{OUT} and EA_{OUT2} are specified in Table 1 using this test circuit. When designing applications for voltage monitoring using an isolated amplifier, review these specifications, noting that the 1% accuracy specifications for the isolated error amplifier do not apply. In addition, the EA_{OUT} circuit in Figure 5 is shown with an optional external RC low-pass filter with a corner frequency of 500 kHz, which can reduce the 3 MHz output noise from the internal voltage to the PWM converter.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions of more than 1 µs at the input, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output.

If the decoder receives no internal pulses for more than approximately 3 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default high impedance state by the watchdog timer circuit. In addition, the outputs are in a default high impedance state while the power is increasing before the UVLO threshold is crossed.

The ADuM3190 is immune to external magnetic fields. The limitation on the ADuM3190 magnetic field immunity is set by the condition whereby induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM3190 is examined because it represents the most susceptible mode of operation. The pulses at the transformer output have an amplitude that is greater than 1.0 V. The decoder has a sensing threshold at approximately 0.5 V, therefore establishing a 0.5 V margin within which induced voltages are tolerated. The voltage induced across the receiving coil is given by

$V = (-d\beta/dt) \sum \pi r_n^2, n = 1, 2, \ldots, N$

where:

β is the magnetic flux density (gauss).

r_n is the radius of the nth turn in the receiving coil (cm).

N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM3190 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 8.

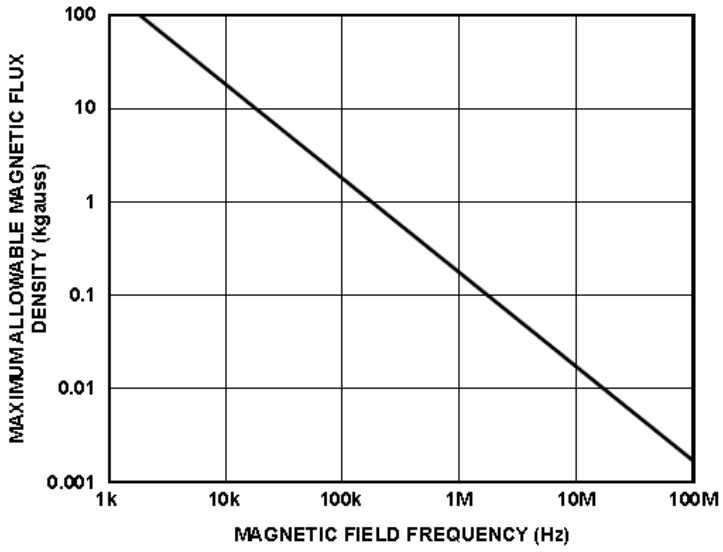

Figure 8. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.02 kgauss induces a voltage of 0.25 V at the receiving coil. This is approximately 50% of the sensing threshold and does not cause a faulty output transition.

Similarly, if such an event were to occur during a transmitted pulse (and had the worst-case polarity), the received pulse is reduced from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM3190 transformers. Figure 9 shows these allowable current magnitudes as a function of

frequency for selected distances. As shown in Figure 9, the ADuM3190 is immune and can be affected only by extremely large currents operating at a high frequency very close to the component. For the 1 MHz example, a 0.7 kA current must be placed 5 mm away from the ADuM3190 to affect the operation of the device.

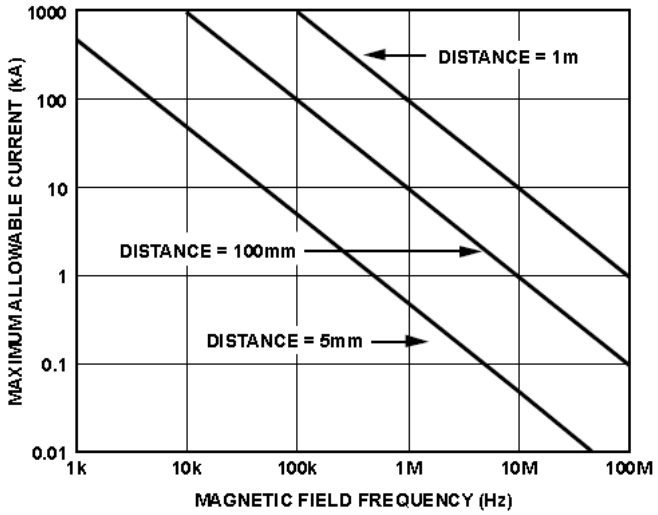

Figure 9. Maximum Allowable Current for Various Current-to-ADuM3190 Spacings

8.0 Package Outline Dimensions

The CDFP4-F16 package and outline dimensions can be found at http://www.analog.com or upon request.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADUM3190P703F	–55°C to +125°C	16 Lead Bottom Brazed Flat Pack	CDFP4-F16
ADUM3190L703F	–55°C to +125°C	16 Lead Bottom Brazed Flat Pack	CDFP4-F16

9.0 Revision History

Revision History		
Rev	Description of Change	Date
A	Initial Release	2/15/2018
B	Remove "Preliminary" from 1st page	2/21/2018
C	Corrected typo on Delta Limits, added bi-metallic bonding note, added functional block diagram, corrected typo for burn in condition section 5.1.1, added ESD sensitivity level	3/19/2018
D	Corrected typo for thermal resistance specifications	8/30/2018
E	Added ADUM3190L703F device model. Widened accuracy limits for ADUM3190P703F. Moved Maximum Working Voltage from Section 4.3 to Table IB. Editorial corrections.	12/06/2019

12/19

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