Low Noise Single-Ended to Differential Converter/ADC Driver

FEATURES

- Rail-to-Rail Input and Outputs
- Fast Settling Time: 240ns, 0.01%, $8V_{P-P}$ Output Step
- $1.9nV/\sqrt{Hz}$ Input-Referred Op Amp Noise
- High Impedance Input
- –3dB Bandwidth: 33MHz
- 2.7V to 12V Supply Operation
- No External Gain Resistors Required
- 4.8mA Supply Current
- Low Power Shutdown
- Low Distortion (HD2/HD3): –102dBc/–97dBc at 100kHz, $V_{OUTDIFF} = 4V_{P-P}$
- Low Offset Voltage: ±400µV Max
- High DC Linearity: <±1LSB, 16-Bit, $8V_{P-P}$
- Low Input Current Noise: $1.1pA/\sqrt{Hz}$
- 3mm × 3mm 8-Pin DFN and 8-Lead MSOP Packages

APPLICATIONS

- 16-Bit and 18-Bit SAR ADC Drivers
- Single-Ended to Differential Conversion
- Differential Line Driver

DESCRIPTION

The LT®6350 is a rail-to-rail input and output low noise single-ended to differential converter/ADC driver featuring fast settling time. It converts a high or low impedance, single-ended input signal to a low impedance, balanced, differential output suitable for driving high performance differential succesive approximation register (SAR) ADCs. The two op amp topology features very low noise op amps, that can support SNR >110dB in a 1MHz bandwidth.

The input op amp is trimmed for constant low input-referred voltage offset over the input range to prevent V_{OS} steps from degrading distortion.

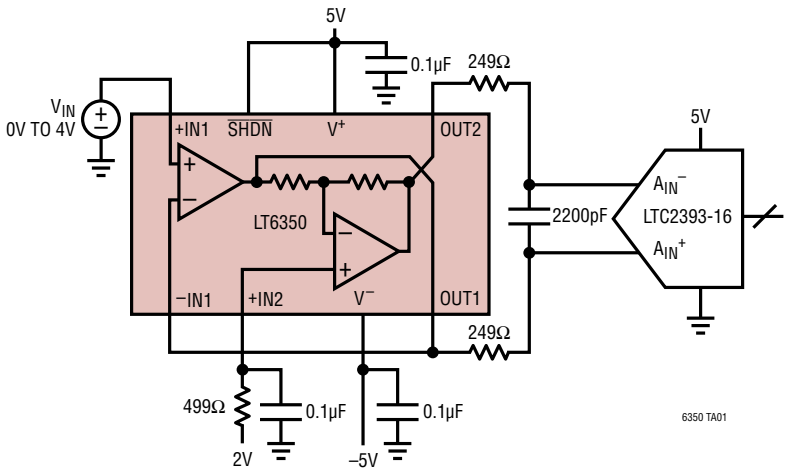
On a single 5V supply, the outputs can swing from 55mV to 4.945V. With the addition of a negative supply, the LT6350 can swing from 0V to 4.945V. Output common mode voltage is set by applying a voltage to the +IN2 pin.

The LT6350 draws 4.8mA from a 5V supply and consumes just 60µA in shutdown mode.

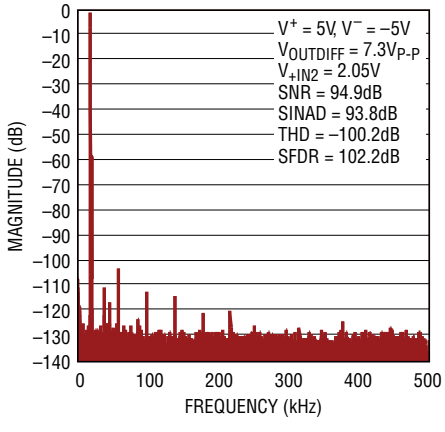
The LT6350 is available in a compact 3mm × 3mm, 8-pin leadless DFN package and also in an 8-pin MSOP package and operates over a –40°C to 125°C temperature range.

TYPICAL APPLICATION

ADC Driver: Single-Ended Input to Differential Output



20kHz Sine Wave, –1dBFS 8192-Point FFT

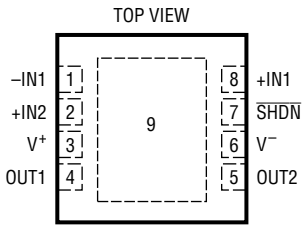


ABSOLUTE MAXIMUM RATINGS (Note 1)

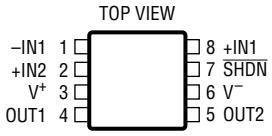
Total Supply Voltage
($V^+ – V^–$).....12.6V
Input Current (Note 2).....±20mA
Output Short-Circuit Current Duration
(Note 3)..... Indefinite
Operating Temperature Range
(Note 4).....–40°C to 125°C

Specified Temperature Range
(Note 5).....–40°C to 125°C
Maximum Junction Temperature..... 150°C
Storage Temperature Range.....–65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSOP Package Only ..... 300°C

PIN CONFIGURATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
UNDERSIDE METAL CONNECTED TO $V^–$



MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 250°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT6350CDD#PBF	LT6350CDD#TRPBF	LFJT	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LT6350IDD#PBF	LT6350IDD#TRPBF	LFJT	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LT6350HDD#PBF	LT6350HDD#TRPBF	LFJT	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT6350CMS8#PBF	LT6350CMS8#TRPBF	LTFJV	8-Lead Plastic MSOP	0°C to 70°C
LT6350IMS8#PBF	LT6350IMS8#TRPBF	LTFJV	8-Lead Plastic MSOP	–40°C to 85°C
LT6350HMS8#PBF	LT6350HMS8#TRPBF	LTFJV	8-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. Unless noted otherwise, V^+ = 5V, V^- = 0V, V_{+IN1} = V2 = Mid-Supply, $V_{\overline{SHDN}} = V^+$, R_L = OPEN, R_F = SHORT, R_G = OPEN. V_S is defined as ($V^+ - V^-$). V_{OUTCM} is defined as ($V_{OUT1} + V_{OUT2}$)/2. $V_{OUTDIFF}$ is defined as ($V_{OUT1} - V_{OUT2}$). See Figure 1.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OSDIFF}	Differential Input-Referred Offset Voltage	V_S = 5V					
		V_{+IN1} = V2 = Mid-Rail		–0.4		0.4	mV
		V_{+IN1} = V2 = V^-+1.5V to V^+ – 0.1V		–0.45	±0.1	0.45	mV
		V_{+IN1} = V2 = V^-+1.5V to V^+ – 0.1V	●	–0.77		1.36	mV
		V_S = 3V					
		V_{+IN1} = V2 = V^-+1.5V to V^+ – 0.1V		–0.45	±0.1	0.45	mV
		V_{+IN1} = V2 = V^-+1.5V to V^+ – 0.1V	●	–0.8		1.36	mV
		V_S = 10V					
		V_{+IN1} = V2 = V^-+1.5V to V^+ – 0.1V		–0.52	±0.1	0.52	mV
		V_{+IN1} = V2 = V^-+1.5V to V^+ – 0.1V	●	–0.78		1.48	mV
V_{OS1}	Input Offset Voltage, Op Amp 1	V_S = 5V					
		V_{+IN1} = V^-+1.5V to V^+	●	–0.35	±0.08	0.68	mV
		V_{+IN1} = V^- to V^+	●	–1.5	±0.28	1.5	mV
		V_S = 3V					
		V_{+IN1} = V^-+1.5V to V^+	●	–0.35	±0.08	0.68	mV
		V_{+IN1} = V^- to V^+	●	–1.5	±0.32	1.5	mV
		V_S = 10V					
		V_{+IN1} = V^-+1.5V to V^+	●	–0.68	±0.07	0.68	mV
		V_{+IN1} = V^- to V^+	●	–1.5	±0.28	1.5	mV
V_{OS2}	Input Offset Voltage, Op Amp 2 (Note 6)	V_S = 3V, 5V, 10V					
		V_{+IN1} = V2 = V^-+1.5V to V^+ – 0.1V	●	–1.0	±0.1	0.66	mV
$\Delta V_{OSDIFF}/\Delta T$	Differential Offset Voltage Drift	V_{+IN1} = V2 = V^- +1.5V	●		5		µV/°C
		V_{+IN1} = V2 = V^+ –0.1V	●		5.5		µV/°C
I_{B1}	Input Bias Current, Op Amp 1 (at +IN1, –IN1)	V_{+IN1} = Mid-Supply	●	–6.8	–1.2		µA
		V_{+IN1} = V^-	●	–8.0	–3.0		µA
		V_{+IN1} = V^+	●		1.4	2.6	µA
I_{OS1}	Input Offset Current, Op Amp 1 (at +IN1, –IN1)	V_{+IN1} = Mid-Supply	●	–1	±0.1	1	µA
		V_{+IN1} = V^-	●	–1	±0.1	1	µA
		V_{+IN1} = V^+	●	–1	±0.1	1	µA
I_{+IN2}	Input Bias Current, Op Amp 2 (at +IN2)	V_{+IN1} = V2 = Mid-Supply	●		2.5	4.4	µA
I_{OS2}	Input Offest Current, Op Amp 2	V2 = Mid-Supply			±0.1		µA
e_{n1}	Input Voltage Noise Density, Op Amp 1	Op Amp Input Referred			1.9		nV/√Hz
i_{n1}	Input Current Noise Density, Op Amp 1				1.1		pA/√Hz
e_{n2}	Input Voltage Noise Density, Op Amp 2	Op Amp Input Referred			2.1		nV/√Hz
i_{n2}	Input Current Noise Density, Op Amp 2				1		pA/√Hz
$e_{n(OUT)}$	Differential Output Noise Voltage Density	Total Output Noise Including Both Op Amps and On-Chip Resistors. Input Shorted. f = 10kHz			8.2		nV/√Hz
	Input Noise Voltage	0.1Hz to 10Hz			300		nV_{P-P}
SNR	Output Signal-to-Noise Ratio	$V_{OUTDIFF}$ = $8V_{P-P}$, 1MHz Noise Bandwidth			110		dB
V_{+IN1}	Input Voltage Range, +IN1	Guaranteed by CMRR1	●	V^-		V^+	V
V_{+IN2}	Input Voltage Range, +IN2	Guaranteed by CMRR2	●	V^- +1.5V		V^+ –0.1V	V
R_{IN}	Input Resistance	Single-Ended Input at +IN1			4		MΩ

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. Unless noted otherwise, V^+ = 5V, V^- = 0V, V_{+IN1} = V2 = Mid-Supply, $V_{\overline{SHDN}} = V^+$, R_L = OPEN, R_F = SHORT, R_G = OPEN. V_S is defined as ($V^+ - V^-$). V_{OUTCM} is defined as ($V_{OUT1} + V_{OUT2}$)/2. $V_{OUTDIFF}$ is defined as ($V_{OUT1} - V_{OUT2}$). See Figure 1.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance	Single-Ended Input at +IN1			1.8		pF
CMRR1	Common Mode Rejection Ratio, Op Amp 1	V_S = 5V, $V_{+IN1} = V_{-IN1} = V^-$ +1.5V to V^+		82	94		dB
		V_S = 5V, $V_{+IN1} = V_{-IN1} = V^-$ +1.5V to V^+	●	77	94		dB
		V_S = 5V, $V_{+IN1} = V_{-IN1} = V^-$ to V^+	●	72	88		dB
		V_S = 3V, $V_{+IN1} = V_{-IN1} = V^-$ to V^+	●	67	82		dB
CMRR2	Common Mode Rejection Ratio, Op Amp 2	V_S = 5V, V_{+IN1} = V2 = V^-+1.5V to V^+ –0.1V	●	93	118		dB
		V_S = 3V, V_{+IN1} = V2 = V^-+1.5V to V^+ –0.1V	●	85	110		dB
		V_S = 10V, V_{+IN1} = V2 = V^-+1.5V to V^+ –0.1V	●	96	118		dB
PSRR	Power Supply Rejection Ratio ($\Delta V_S/\Delta V_{OSDIFF}$)	V_S = 2.7V to 12V	●	80	108		dB
V_S	Supply Voltage (Note 7)		●	2.7		12	V
BAL	Output Balance ($\Delta V_{OUTDIFF}/\Delta V_{OUTCM}$) (Note 8)	$V_{OUTDIFF}$ = 2V	●	50	68		dB
GAIN	Closed-Loop Gain ($\Delta V_{OUTDIFF}/\Delta(V_{+IN1} - V2)$)	$\Delta(V_{+IN1} - V2)$ = 4V	●		2		V/V
$GAIN_{ERR}$	Closed-Loop Gain Error		●	–0.6	±0.08	0.6	%
$\Delta GAIN_{ERR}/\Delta T$	Closed-Loop Gain Error Drift		●		3		ppm/°C
INL	DC Linearity (Note 9)	V^+ = 5V, V^- = 0V			230		µV
		V^+ = 5V, V^- = –2V			125		µV
		V^+ = 5V, V– = –2V, 16-Bit, $8V_{P-P}$			±1		LSB
R_{INT}	Internal Resistors				1000		Ω
V_{OH}	Output Swing to V^+, Either Output (Note 10)	No Load	●		55	170	mV
		Sourcing 12.5mA	●		360	750	mV
V_{OL}	Output Swing to V^-, Either Output (Note 10)	No Load	●		55	170	mV
		Sourcing 12.5mA	●		260	460	mV
I_{SC}	Output Short-Circuit Current	V_{+IN1} = Mid-Rail ±200mV, V_{-IN1} = Mid-Rail					
		V_S = 5V		±27	±45		mA
		V_S = 5V	●	±15	±45		mA
		V_S = 3V	●	±15	±40		mA
V_{IL}	$\overline{SHDN}$ Input Logic Low	V_S = 2.7V to 12V	●			V^- + 0.3	V
V_{IH}	$\overline{SHDN}$ Input Logic High	V_S = 2.7V to 12V	●	V^- + 2.0			V
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$\overline{SHDN} = V^+$	●	–1		1	µA
		$\overline{SHDN} = V^-$	●	–45	–20		µA
I_S	Supply Current	V_S = 3V	●		4.5	8.1	mA
		V_S = 5V				5.8	mA
		V_S = 5V	●		4.8	8.3	mA
		V_S = 10V	●		5.4	10.4	mA
$I_{S(\overline{SHDN})}$	Supply Current in Shutdown	V_S = 3V, $V_{\overline{SHDN}} = V_{IL}$	●		43	220	µA
		V_S = 5V, $V_{\overline{SHDN}} = V_{IL}$	●		60	240	µA
		V_S = 10V, $V_{\overline{SHDN}} = V_{IL}$	●		70	260	µA
GBW	Gain-Bandwidth Product Frequency = 1MHz	Op Amp 1 (Noninverting)			85		MHz
		Op Amp 2 (Inverting)			115		MHz
BW	Differential –3dB Small-Signal Bandwidth	$V_{OUTDIFF}$ = $100mV_{P-P}$		23			MHz
		$V_{OUTDIFF}$ = $100mV_{P-P}$	●	19	33		MHz

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. Unless noted otherwise, V^+ = 5V, V^- = 0V, V_{+IN1} = V2 = Mid-Supply, $V_{\overline{SHDN}} = V^+$, R_L = OPEN, R_F = SHORT, R_G = OPEN. V_S is defined as ($V^+ - V^-$). V_{OUTCM} is defined as ($V_{OUT1} + V_{OUT2}$)/2. $V_{OUTDIFF}$ is defined as ($V_{OUT1} - V_{OUT2}$). See Figure 1.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FPBW	Full-Power Bandwidth (Note 11)	$V_{OUTDIFF}$ = $8V_{P-P}$			1.6		MHz
C_L	Capacitive Load Drive, 20% Overshoot	No Series Output Resistors			56		pF
SR	Differential Slew Rate	OUT1 Rising (OUT2 Falling) OUT1 Falling (OUT2 Rising)			48 41		V/µs V/µs
	10kHz Distortion	V_S = 5V, $V_{OUTDIFF}$ = $4V_{P-P}$, R_L = 2kΩ					
HD2		2nd Harmonic			–115		dBc
HD3		3rd Harmonic			–115		dBc
	100kHz Distortion	V_S = 5V, $V_{OUTDIFF}$ = $4V_{P-P}$, R_L = 2kΩ					
HD2		2nd Harmonic			–102		dBc
HD3		3rd Harmonic			–97		dBc
	1MHz Distortion	V_S = 5V, $V_{OUTDIFF}$ = $4V_{P-P}$, R_L = 2kΩ					
HD2		2nd Harmonic			–86		dBc
HD3		3rd Harmonic			–75		dBc
t_S	Settling Time to a 4V Input Step	0.1% 0.01% 0.0015% (±1LSB, 16-Bit, Falling Edge)			200 240 350		ns ns ns
t_{OVDR}	Overdrive Recovery Time	+IN1 to V^- and V^+			200		ns
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0V to 5V			400		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 5V to 0V			400		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Inputs are protected by diodes to each supply. Additionallly, op amp inputs +IN1, –IN1 and +IN2 are protected by back-to-back diodes across the op amp inputs. If inputs are taken beyond the supplies or if either op amp's differential input voltage exceeds 0.7V, the input current must be limited to less than 20mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LT6350C/LT6350I are guaranteed functional over the temperature range of –40°C to 85°C. The LT6350H is guaranteed functional over the temperature range of –40°C to 125°C.

Note 5: The LT6350C is guaranteed to meet specified performance from 0°C to 70°C. The LT6350C is designed, characterized and expected to meet specified performance from –40°C to 85°C, but is not tested or QA sampled at these temperatures. The LT6350I is guaranteed to meet specified performance from –40°C to 85°C. The LT6350H is guaranteed to meet specified performance from –40°C to 125°C.

Note 6: V_{OS2} is measured as the total output common mode voltage offset (error between output common mode and voltage at V2). V_{OS2} includes the combined effects of op amp 2's voltage offset, I_B, I_{OS} and mismatch between on-chip resistors and the 499Ω external resistor, R1 (See Figure 1).

Note 7: Supply voltage range is guaranteed by the power supply rejection ratio test.

Note 8: Output balance is calculated from gain error and gain as:

$$BAL = \frac{GAIN}{GAIN_{ERR}}$$

Note 9: DC linearity is measured by measuring the differential output for each input in the set V_{+IN1} = 0.5V, 2.5V, 4.5V, and calculating the maximum deviation from the least squares best fit straight line generated from the three data points.

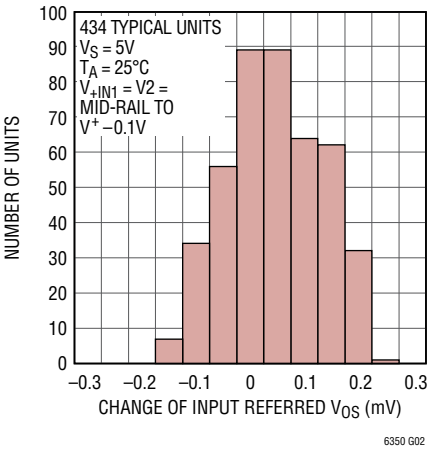
Note 10: Output voltage swings are measured between the output and power supply rails.

Note 11: Full- power bandwidth is calculated from the slew rate. FPBW = $SR/2\pi V_P$.

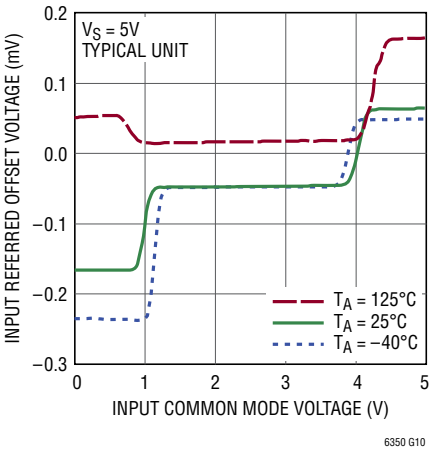
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V^+ = 5V, V^- = 0V, V_{+IN1} = V2 = Mid-Supply, $V_{\overline{SHDN}}$ = V^+, R_F = SHORT, R_G = OPEN, R_L = OPEN. See Figure 1.

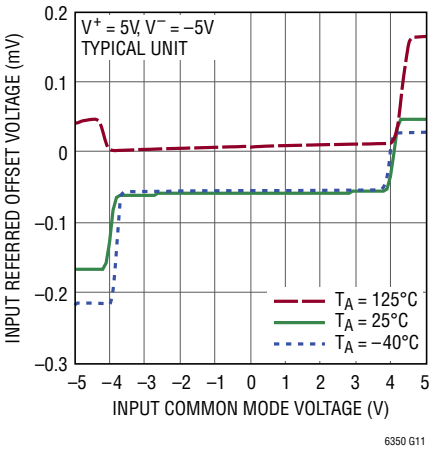
Differential V_{OS} Delta Distribution



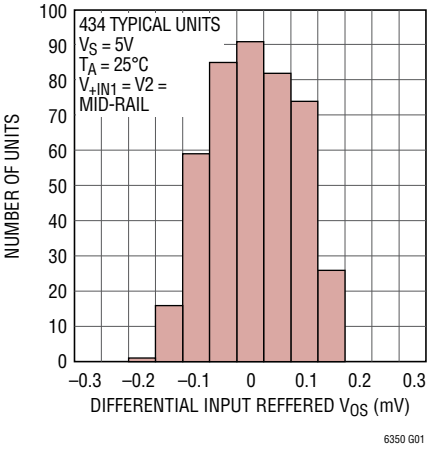
Offset Voltage vs Input Common Mode Voltage, Op Amp 1



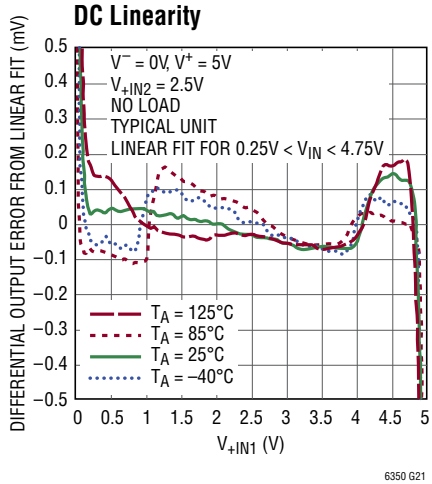
Offset Voltage vs Input Common Mode Voltage, Op Amp 1



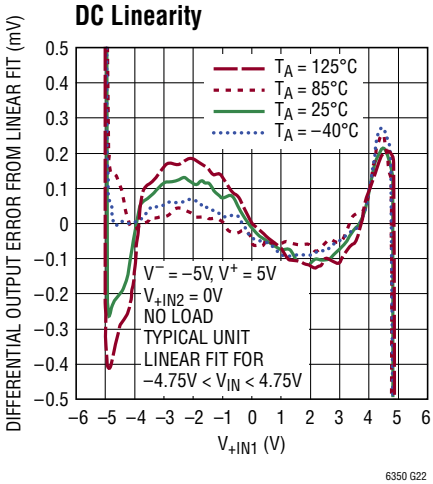
Differential V_{OS} Distribution



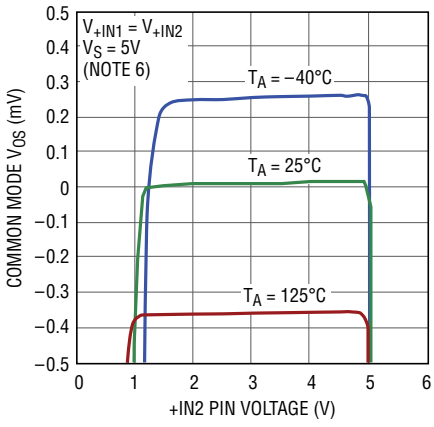
DC Linearity



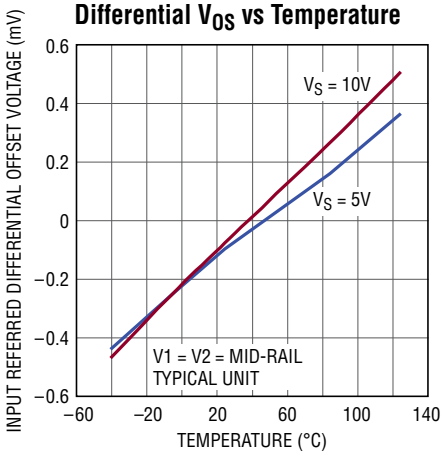
DC Linearity



Common Mode V_{OS} vs Input (+IN2) Voltage



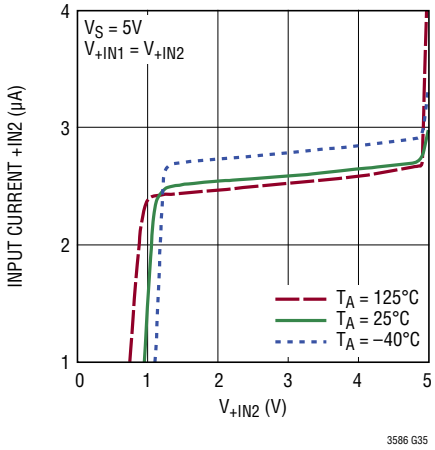
Differential V_{OS} vs Temperature



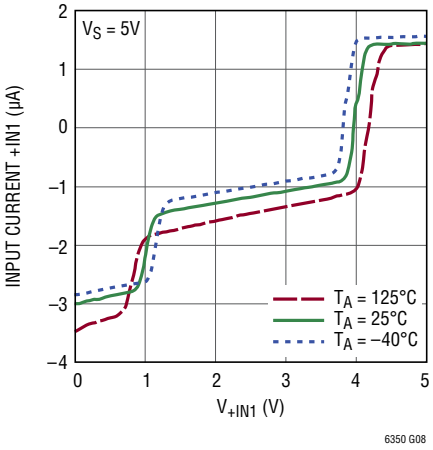
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V^+ = 5V, V^- = 0V, V_{+IN1} = V2 = Mid-Supply, $V_{\overline{SHDN}}$ = V^+, R_F = SHORT, R_G = OPEN, R_L = OPEN. See Figure 1.

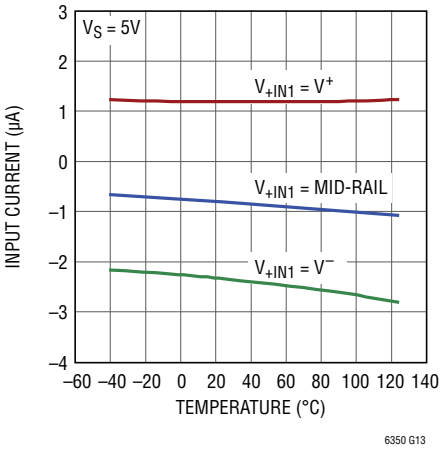
Input Bias Current vs Input Voltage, Op Amp 2



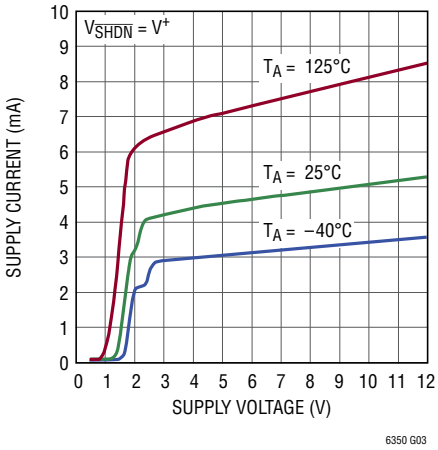
Input Bias Current vs Input Voltage, Op Amp 1



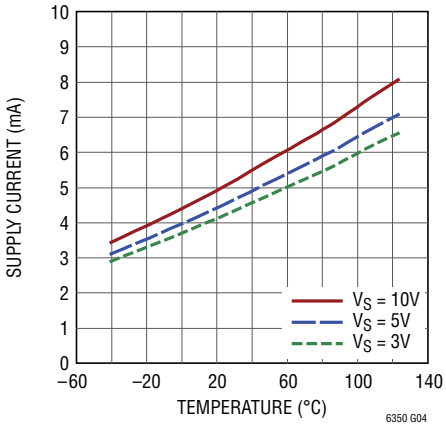
Input Bias Current vs Temperature, Op Amp 1



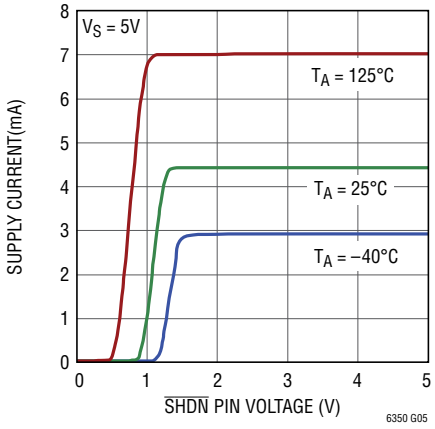
Supply Current vs Supply Voltage



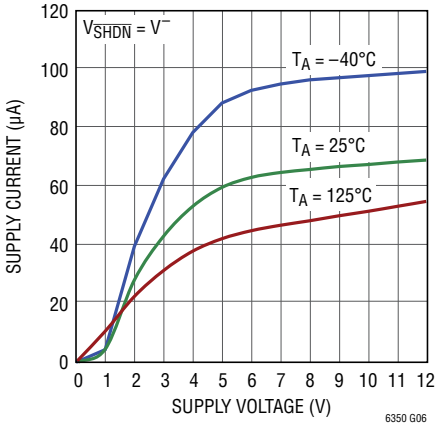
Supply Current vs Temperature



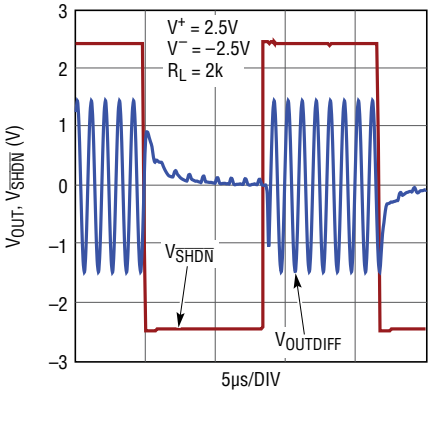
Supply Current vs $\overline{SHDN}$ Voltage



Supply Current in Shutdown vs Supply Voltage



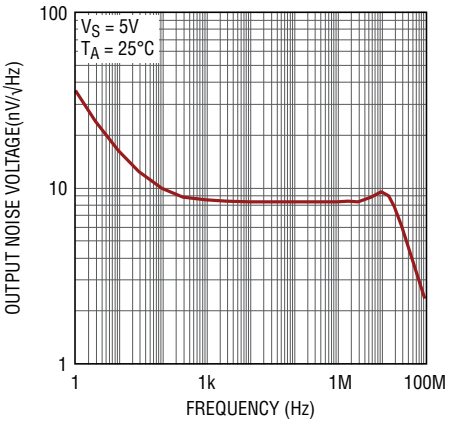
Turn-On and Turn-Off Transient Response



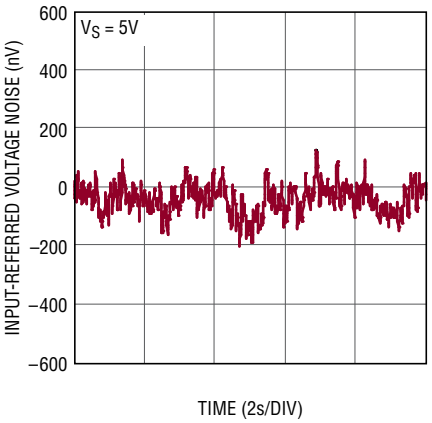
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V^+ = 5V, V^- = 0V, V_{+IN1} = V2 = Mid-Supply, $V_{\overline{SHDN}}$ = V^+, R_F = SHORT, R_G = OPEN, R_L = OPEN. See Figure 1.

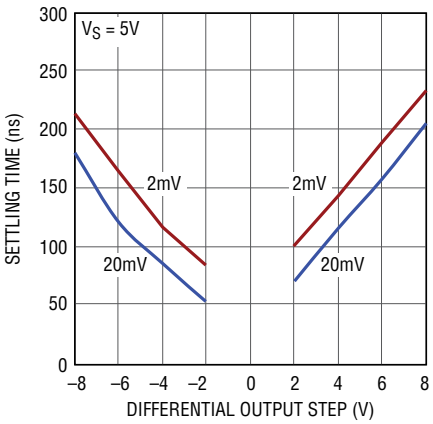
Differential Output Voltage Noise vs Frequency



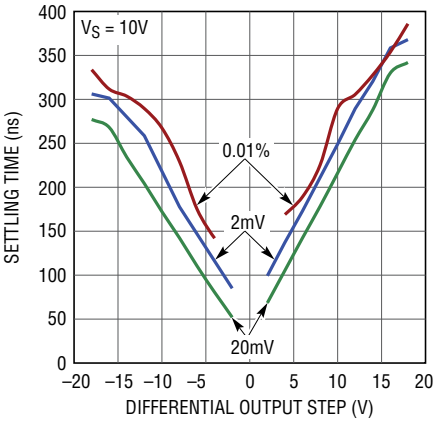
0.1Hz to 10Hz Differential Input-Referred Voltage Noise



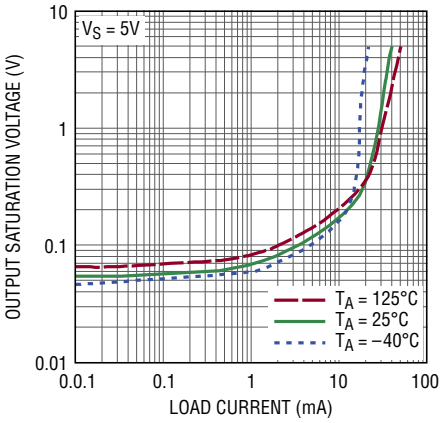
Output Settling Time vs Output Step



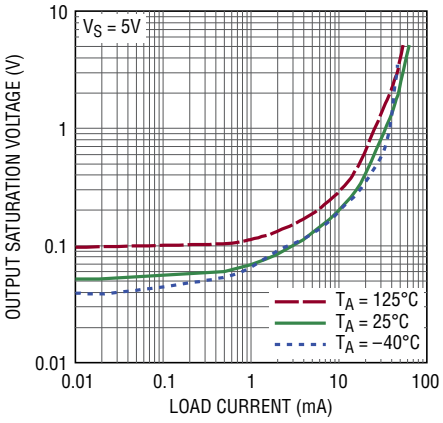
Output Settling Time vs Output Step



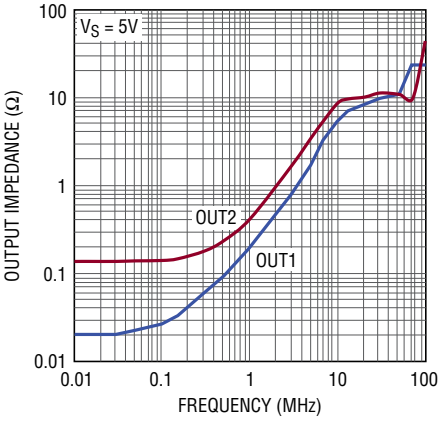
Output Saturation Voltage vs Load Current, Output Low, Either Output



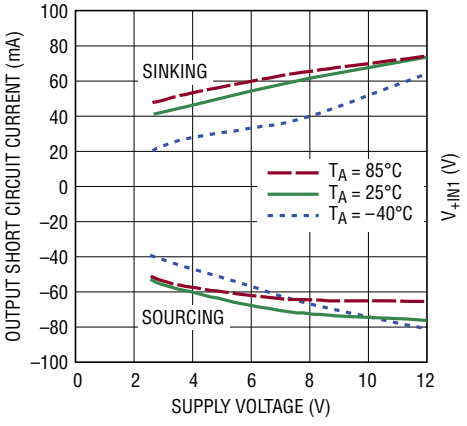
Output Saturation Voltage vs Load Current, Output High, Either Output



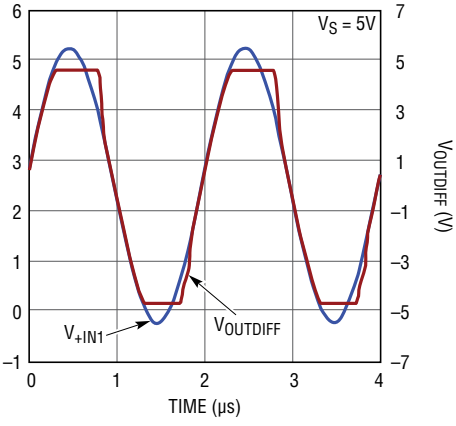
Output Impedance vs Frequency



Output Short-Circuit Current vs Supply Voltage, Either Output



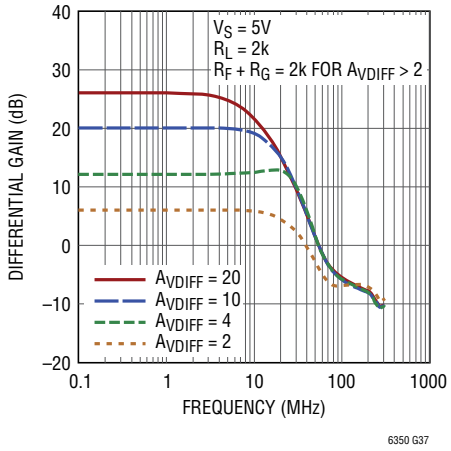
Overdrive Recovery



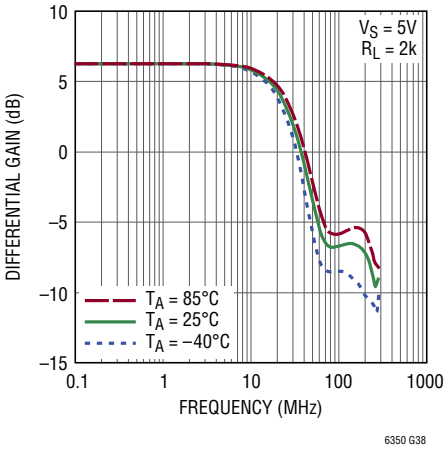
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V^+ = 5V, V^- = 0V, V_{+IN1} = V2 = Mid-Supply, $V_{\overline{SHDN}}$ = V^+, R_F = SHORT, R_G = OPEN, R_L = OPEN. See Figure 1.

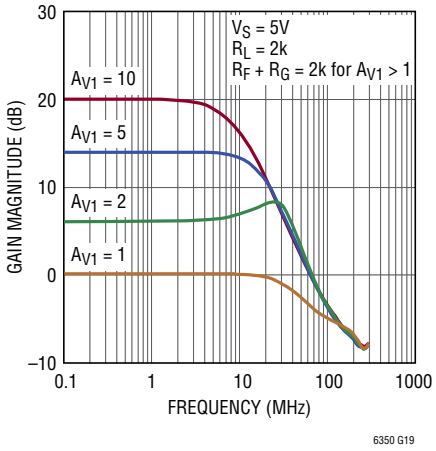
Differential Frequency Response vs Gain



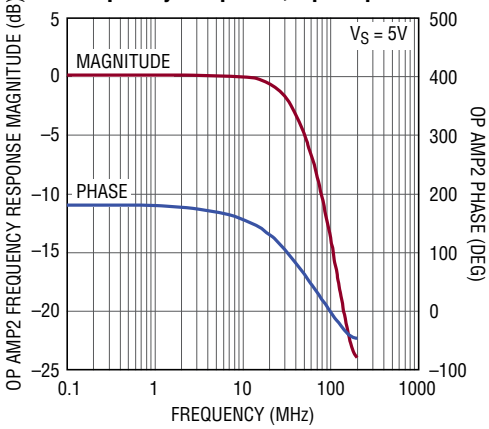
Differential Frequency Response vs Temperature



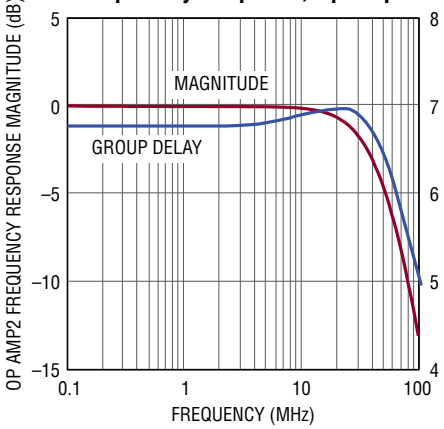
Closed-Loop Small-Signal Frequency Response, Op Amp 1



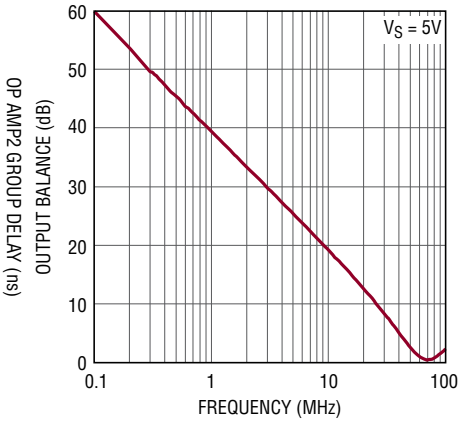
Closed-Loop Small-Signal Frequency Response, Op Amp 2



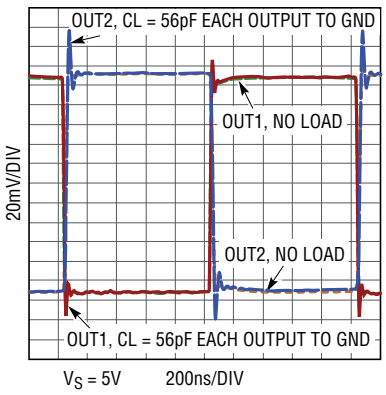
Closed-Loop Magnitude and Group Delay Response, Op Amp 2



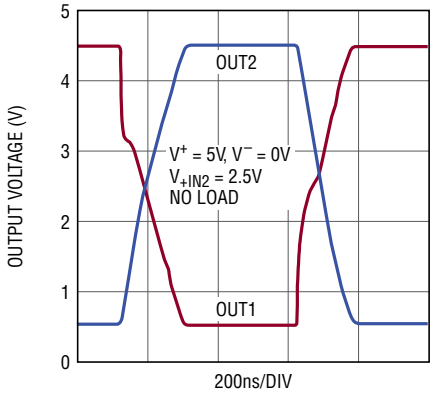
Output Balance vs Frequency



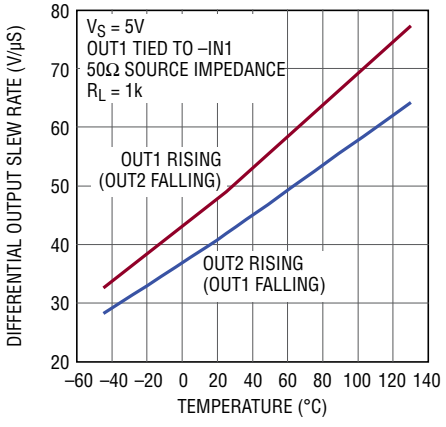
Small-Signal Step Response



Large-Signal Step Response



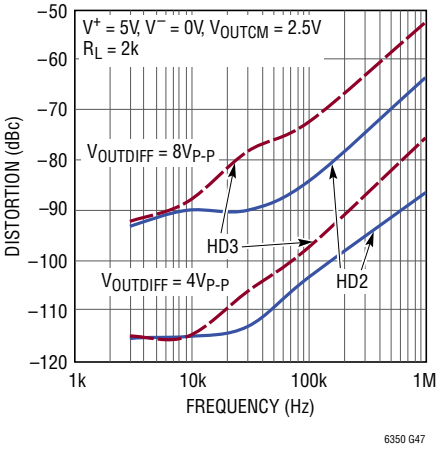
Differential Slew Rate vs Temperature



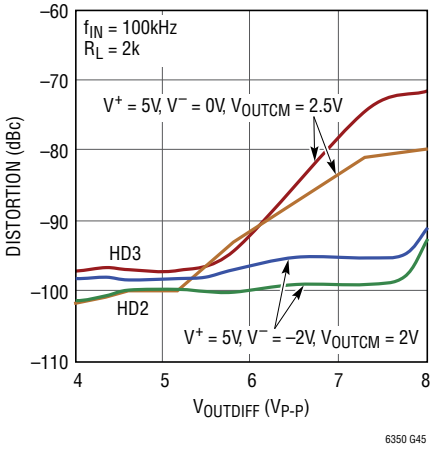
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V^+ = 5V, V^- = 0V, V_{+IN1} = V2 = Mid-Supply, $V_{\overline{SHDN}}$ = V^+, R_F = SHORT, R_G = OPEN, R_L = OPEN. See Figure 1.

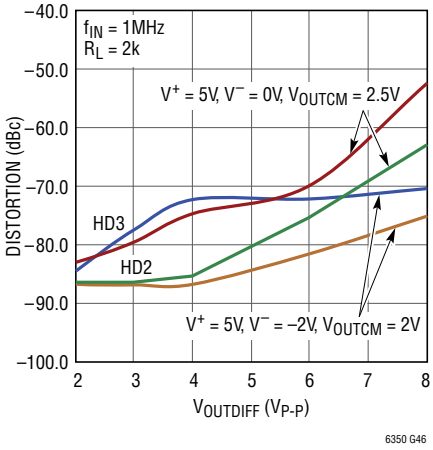
Harmonic Distortion vs Frequency



Harmonic Distortion vs Output Amplitude



Harmonic Distortion vs Output Amplitude



PIN FUNCTIONS

–IN1 (Pin 1): Inverting Input. Normally used to take feedback from OUT1.

+IN2 (Pin 2): High Impedance Input. Normally used as a reference input.

V^+ (Pin 3): Positive Power Supply.

OUT1 (Pin 4): Noninverting Output. In phase with +IN1.

OUT2 (Pin 5): Inverting Output.

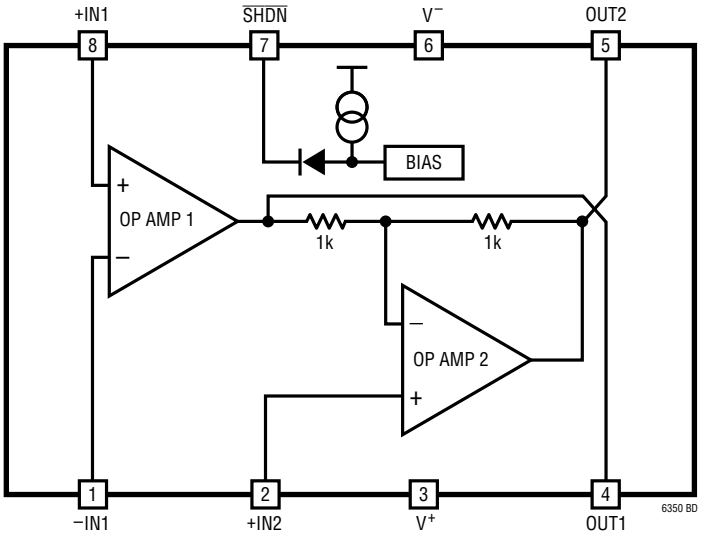
V^- (Pin 6): Negative Power Supply. Can be ground.

$\overline{SHDN}$ (Pin 7): Shutdown. If tied high or left floating, the part is enabled. If tied low, the part is disabled and draws less than 70µA of supply current.

+IN1 (Pin 8): High Impedance Input. Normally used as the single-ended input.

Exposed Pad (Pin 9, DD8 Package Only): Tie to V^-

BLOCK DIAGRAM



DC TEST CIRCUIT

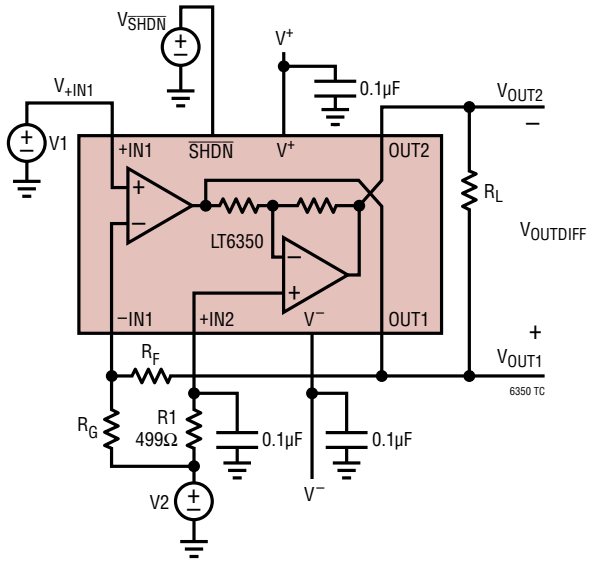


Figure 1. DC Test Circuit.

OPERATION

The LT6350 is a low noise single-ended to differential converter/ADC driver. It converts a high or low impedance, single-ended input signal to a low impedance, balanced differential output suitable for driving high performance differential sucessive approximation register (SAR) ADCs. The closed loop –3dB bandwidth for the typical gain-of-two configuration is 33MHz.

The LT6350 uses a two op amp topology as shown in the Block Diagram: at the input is one fully uncommitted op amp with both inputs and output brought out to pins. This is followed by an op amp internally hardwired and optimally compensated as a unity-gain inverter with its input connected to the output of the first op amp. The noninverting input of the inverting op amp is brought out to a pin and is used to set the output common mode voltage level. The outputs of the two op amps are therefore 180° out-of-phase and provide a low impedance differential drive for differential-input analog to digital converters. The outputs of the LT6350 can swing rail-to-rail and can source or sink a transient 45mA of current. The outputs are designed to drive 40pF to ground or 20pF differentially. Load capacitances larger than 40pF should be decoupled from each output with at least 25Ω of series resistance.

The LT6350 features very low noise op amps to support signal-to-noise ratios >110dB.

BASIC CONNECTIONS

A typical use of the LT6350 is to convert a high impedance, single-ended input signal into a low impedance differential output. The configuration for such an application is shown in Figure 2. Here, the input op amp is wired as a non-inverting buffer with a high input impedance at +IN1. At the outputs, V_{OUT1} follows the input, and V_{OUT2} provides an inverted copy of V_{OUT1} for an overall differential gain of two. The input op amp has a rail-to-rail input stage, and both outputs are rail-to-rail, typically swinging to within 55mV of the rails at each output in this configuration allowing $8V_{P-P}$ differential outputs from a single 5V rail. This provides a simple interface to differential input ADCs that accept a mid-rail input common mode voltage.

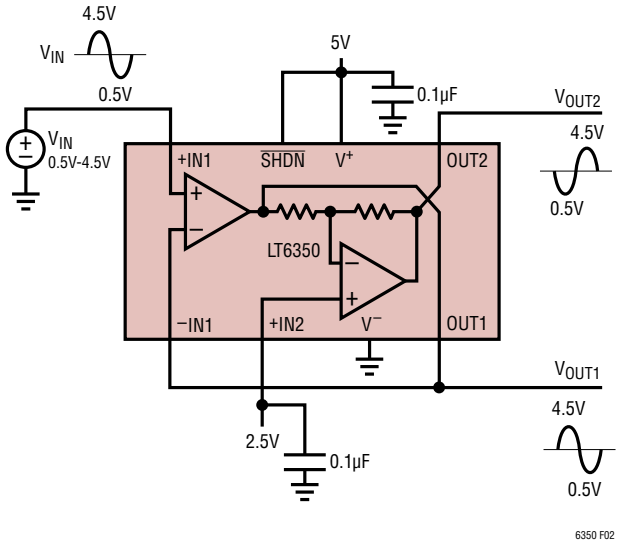


Figure 2. Basic Connections

DESIGN EQUATIONS AND ALTERNATIVE CONNECTIONS

Because the input op amp presents its output and both its inputs to LT6350 pins, alternative configurations are possible. Consider the general configuration shown in Figure 3.

Ordinary op amp analysis gives the equations for V_{OUT1} and V_{OUT2} given the input voltages V1, V2, V_{IN} and V_A:

$$V_{OUT1} = V_{IN} \bullet (1+R_F/R_G) - V1 \bullet (R_F/R_G)$$

$$V_{OUT1} = V_A \bullet (1+R_F/R_G) + V1$$

$$V_{OUT2} = -V_{OUT1} + 2 \bullet V2$$

If we define the differential and common mode output voltages as:

$$V_{OUTDIFF} \equiv V_{OUT1} - V_{OUT2}$$

and

$$V_{OUTCM} \equiv (V_{OUT1} + V_{OUT2})/2,$$

then combining the expressions for V_{OUT1} and V_{OUT2} with the definitions gives the resulting differential and common mode output voltages:

$$V_{OUTDIFF} = 2 \bullet (V_{IN} \bullet (1+R_F/R_G) - V1 \bullet (R_F/R_G) - V2) \quad (1)$$

$$V_{OUTDIFF} = 2 \bullet (V_A \bullet (1+R_F/R_G) + V1 - V2) \quad (2)$$

$$V_{OUTCM} = V2 \quad (3)$$

OPERATION

Notice that the output common mode voltage is determined simply by the voltage at +IN2. However, since the voltage applied at +IN2 does not affect the voltage at the V_{OUT1} output, a differential offset voltage will develop for $V_A = 0$ when V1 does not equal V2. The value of the offset voltage will be 2 • (V1 – V2), as can be seen in Equation 2. For lowest differential offset, therefore, the input signal to pin +IN1, V_{IN}, should be centered around the common mode voltage applied to pin +IN2. Often this voltage is provided by the ADC reference output. When the input is so centered and V1 = V2, Equation 2 reduces to:

$$V_{OUTDIFF} = 2 \bullet V_A \bullet (1+R_F/R_G)$$

The simple connection described in the Basic Connections section can be seen as a special case of the general circuit in Figure 3 where R_F is a short circuit, R_G is an open circuit, and the voltage at V_{IN} is centered around the voltage V2. If differential gain greater than two is needed, the values of R_F and R_G can be adjusted in accordance with Equation (2). Additional information about feedback networks is given in the next section and in the Input Amplifier (Op Amp 1) Feedback Components section.

Inverting Gain Connections/Interfacing to High Voltage Signals

Although the previous examples have assumed the input signal is applied at +IN1, it is also possible to use the input op amp in an inverting configuration by fixing the voltage V_{IN} and applying the input signal at V1 of Figure 3. Using the input op amp in the inverting configuration fixes its input common mode voltage at the voltage V_{IN}, which allows the input signal at V1 to traverse a swing beyond the LT6350 supply rails. To avoid unwanted differential offsets in this configuration V_{IN} should be chosen such that:

$$V_{IN} = V2/(1+(R_F/R_G))$$

Then Equation (1) reduces to:

$$V_{OUTDIFF} = -2 \bullet V1 \bullet (R_F/R_G))$$

Choosing $R_F = R_G$ with the input at V1 leads to the gain of –2 configuration.

A practical application for the inverting gain configuration is interfacing a high voltage op amp to a 5V differential SAR ADC. As seen in Figure 4, an industrial application might have sensed signals coming through an op amp running from ±15V rails. The LT6350 can easily interface the high voltage op amp to a 5V ADC by using the inverting gain configuration. For a clean interface, three conditions must be met:

1. $V_{OUTDIFF}$ = 0 when OUT_{HV} is centered at OUT_{HVNOM}.
2. $V_{OUT1} = V_{OUTCM}$ = V2 when OUT_{HV} is centered at OUT_{HVNOM}.
3. Full-scale signals at OUT_{HV} are translated at the output of the LT6350 into the appropriate full-scale range for the ADC.

Applying the above constraints to the design Equations (1) to (3) gives values for the ratio of R_F to R_G and for the value of V_{IN}:

$$R_F/R_G = (OUT_{MAX} - OUT_{MIN})/(OUT_{HVMAX} - OUT_{HVMIN})$$

$$V_{IN} = V2/(1+(R_F/R_G)) + (OUT_{HVNOM})/(1+(R_G/R_F))$$

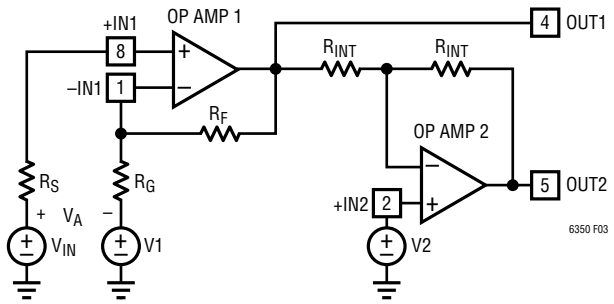


Figure 3. General Configuration

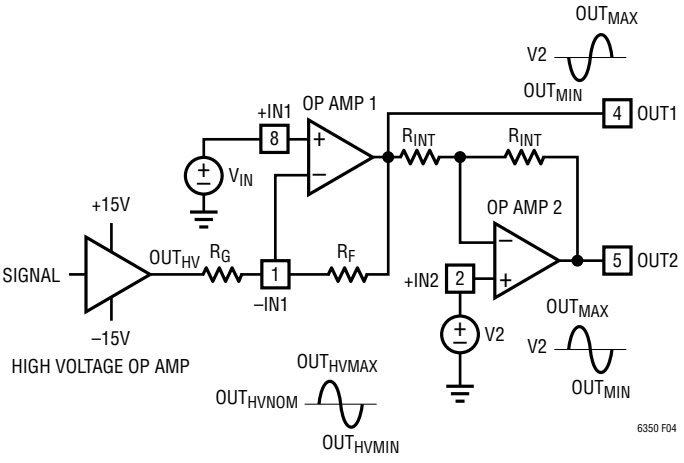


Figure 4. Interfacing to High Voltage Signals

APPLICATIONS INFORMATION

INPUT AMPLIFIER (OP AMP 1) CHARACTERISTICS

Figure 5 shows a simplified schematic of the LT6350's input amplifier. The input stage has NPN and PNP differential pairs operating in parallel. This topology allows the inputs to swing all the way from the negative supply rail to the positive supply rail. Both differential pairs are operational when the common mode voltage is at least 1.3V from either rail. As the common mode voltage swings higher than $V^+ – 1.3V$, current source I_1 saturates, and current in PNP differential pair Q1/Q4 drops to zero. Feedback is maintained through the NPN differential pair Q2/Q3, but the input stage transconductance, g_m, is reduced by a factor of 2. A similar effect occurs with I_2 when the common mode voltage swings within 1.3V of the negative rail. A precision, 2-point algorithm is used to maintain near constant offset voltage over the entire input range (see Offset Considerations).

Negative input bias current flows into the +IN1 and –IN1 inputs when the input common mode is centered between the rails. The magnitude of this current increases when the input common mode voltage is within 1.3V of the negative rail and only Q1/Q4 are active. The polarity of the current reverses when the input common mode voltage is within 1.3V of the positive rail and only Q2/Q3 are active. Typical total change in input bias current over the entire input common mode range is approximately 4µA. These changes in input bias current will generate corresponding changes in voltage across the source and gain-setting resistors. Because the LT6350 input offset current is less than the input bias current, matching the effective source and feedback resistances at the input pins will reduce total offset errors generated by changes in input bias current and will keep distortion to a minimum.

INPUT AMPLIFIER (OP AMP 1) FEEDBACK COMPONENTS

When feedback resistors are used to set gain in op amp 1, care should be taken to ensure that the pole formed by the feedback resistors and the total capacitance at the inverting input, –IN1, does not degrade stability. For instance, to set the LT6350 in a differential gain of +4, R_F and R_G of Figure 3 could be set to 1kΩ. If the total capacitance at –IN1 (LT6350 plus PC board) were 3pF, a new pole would be formed in the loop response at 106MHz, which could lead to ringing in the step response. A capacitor connected across the feedback resistor and having the same value

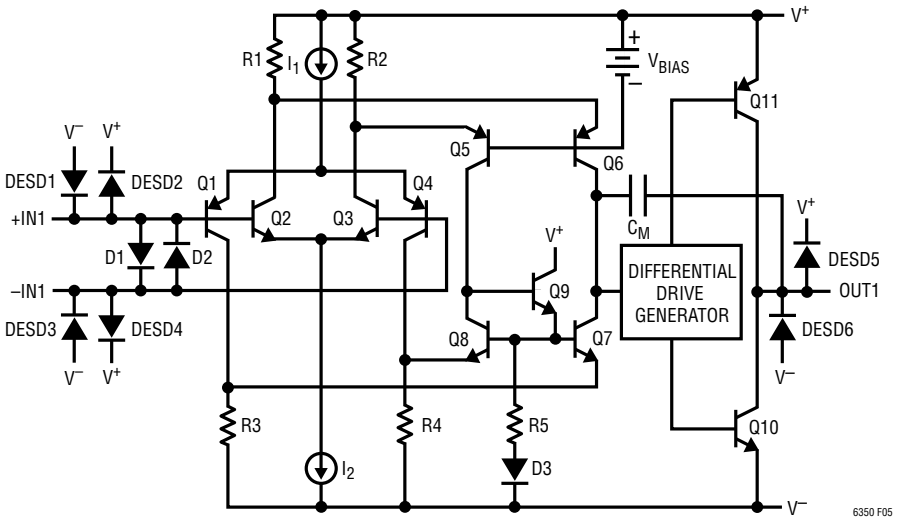


Figure 5. Input Amplifier (Op Amp 1) Simplified Schematic

APPLICATIONS INFORMATION

as the total –IN1 parasitic capacitance will eliminate any ringing or oscillation. Special care should be taken during layout, including using the shortest possible trace lengths and stripping the ground plane under the –IN1 pin, to minimize the parasitic capacitance introduced at that pin.

Input bias current induced DC voltage offsets in the input op amp can be minimized by matching the parallel impedance of R_F and R_G to the impedance of the source that drives +IN1. For example, in the typical gain-of-two application, when the input op amp is configured as a unity-gain buffer, choosing $R_F = R_S$ will minimize the differential offset at the output. Since nonzero values of R_F will contribute to the total output noise, R_F may be bypassed with a capacitor to reduce the noise bandwidth.

INVERTING AMPLIFIER (OP AMP 2) CHARACTERISTICS

The operational amplifier at pins OUT1, +IN2 and OUT2 is internally configured as a unity-gain inverter and provides on pin OUT2 an inverted copy of the voltage at pin OUT1. The voltage applied to pin +IN2 sets the output common mode voltage in accordance with Equation (3). The range of useful output common mode voltages is limited by the full-scale input range of A/D converters; values of output common mode near mid-rail are most useful. The op amp used for the inverting buffer therefore differs from the input op amp primarily in that its input common mode range is not rail-to-rail: the inverting op amp has an input stage that functions over the input range from V^- + 1.5V to V^+ – 0.1V.

The inverting op amp uses tightly matched, 1k on-chip resistors to set the gain of –1. Note that during output swings, current flows through these resistors, increasing the total power dissipation of the LT6350. The worst-case increase over quiescent power dissipation can be found by assuming that the full power supply voltage appears between OUT1 and OUT2. In this case the extra power dissipated in the internal feedback network will be $V_S^2/2k\Omega$.

Since the inverting op amp is permanently configured with a noise gain of two, the internal frequency compensation has been adjusted such that the GBW product of the inverting op amp is higher than that of the input op amp. This allows the closed-loop bandwidths of the two op amps to match more closely when the LT6350 is used in the typical differential gain of two configuration and increases the closed-loop differential bandwidth in that application.

The input referred voltage offset of the inverting op amp, which is equivalent to output common mode voltage offset, and which could contribute to differential voltage offset in accordance with Equation (2), is trimmed during manufacture to within ±125µV. To minimize the offset contribution of the input bias current into pin +IN2, an external 499Ω resistor should be installed at pin +IN2 for all applications. For more information, see the Setting The Output Common Mode and Offset Considerations sections.

INPUT PROTECTION

There are back-to-back diodes across the + and – inputs of both LT6350 op amps. The inputs of the LT6350 do not have internal resistors in series with the input transistors, a technique often used to protect the input transistors from excessive current flow during a differential overdrive condition. Adding series input resistors would significantly degrade the low noise performance. Therefore, if the voltage across the op amp input stages is allowed to exceed ±0.7V, steady-state current conducted though the protection diodes should be externally limited to ±20mA. The input diodes are rugged enough to handle transient currents due to amplifier slew rate overdrive or momentary clipping without protection resistors.

APPLICATIONS INFORMATION

Driving the input signal sufficiently beyond the power supply rails will cause the input transistors to saturate. When saturation occurs, the amplifier loses a stage of phase inversion and the output tries to invert. Diodes D1 and D2 (Figure 5) forward bias and hold the output within a diode drop of the input signal. With very heavy input overdrive the output of op amp 1 could invert. To avoid this inversion, limit the input overdrive to 0.5V beyond the power supply rails.

OUTPUT VOLTAGE RANGE

The outputs of the LT6350 typically swing to within 55mV of the upper and lower supply rails when driving a purely capacitive load such as at the switched-capacitor input stage of a SAR ADC. The LT6350 can therefore share a single 5V supply with the SAR ADC and drive a full $8V_{P-P}$ differential around an input common mode voltage between 2.055V and 2.945V. A modest negative supply can be added to allow the LT6350 to swing all the way to 0V in systems where the ADC requires a true 0V-referenced signal or when the input common mode range of the ADC is restricted to be lower than 2.055V. Some SAR ADCs use 2V as the input common mode voltage with a full-scale input signal range at each input of 0V to 4V. The outputs of the LT6350 can swing $7.78V_{P-P}$ differentially around a 2V common mode voltage, which is a loss of only 0.24dB of the full-scale range of such ADCs.

INTERFACING THE LT6350 TO A/D CONVERTERS

When driving an ADC, an additional single-pole passive RC filter added between the outputs of the LT6350 and the inputs of the ADC can sometimes improve system performance. This is because the sampling process of ADCs creates a charge transient at the ADC inputs that is caused by the switching in of the ADC sampling capacitor. This momentarily shorts the output of the amplifier as charge is transferred between amplifier and sampling capacitor. For an accurate representation of the input signal, the amplifier must recover and settle from this load transient before the acquisition period has ended. An RC network at the outputs of the driver helps decouple the sampling transient of the ADC from the amplifier reducing the demands on the amplifier's output stage (see Figure 6). The resistors at the inputs to the ADC minimize the sampling transients that charge the RC filter capacitors.

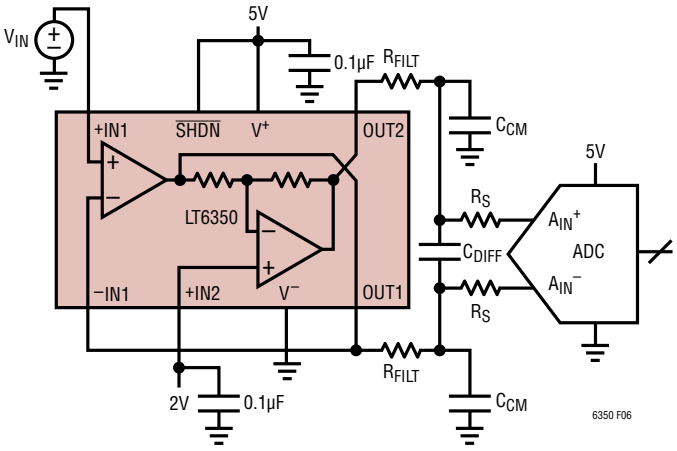


Figure 6. Driving an ADC

APPLICATIONS INFORMATION

The capacitance serves to provide the bulk of the charge during the sampling process, while the two resistors at the outputs of the LT6350 are used to dampen and attenuate any charge injected by the ADC. The RC filter can also be used to the additional benefit of band limiting broadband output noise. See the Noise Considerations section for more information.

The selection of the RC time constant depends on the ADC; but generally, longer time constants will improve SNR at the expense of longer settling time. Excessive settling time can introduce gain errors and can cause distortion if the filter components are not perfectly linear. Note also that too small of a resistor will not properly dampen the load transient of the sampling process, prolonging the time required for settling. 16-bit applications typically require a minimum settling time of eleven RC time constants of a first order filter.

Note that the filter's series resistance also serves to decouple the LT6350 outputs from load capacitance. The outputs of the LT6350 are designed to drive a maximum of 40pF to ground or 20pF differentially; higher values of filter capacitor should always be decoupled with filter resistors of at least 25Ω.

High quality resistors and capacitors should be used in the RC filter since these components can contribute to distortion. For lowest distortion, choose capacitors with a high quality dielectric, such as a C0G multilayer ceramic capacitor. Metal film surface mount resistors are more linear than carbon types.

SETTING THE OUTPUT COMMON MODE VOLTAGE

The output common mode voltage is set by the voltage applied to pin +IN2 in accordance with Equation (3). The usable output common mode range is determined by the input common mode range of the inverting op amp and is from V^- + 1.5V to V^+.

In single supply applications, the optimal common mode input range to the ADC is often determined by the ADC's reference. If the ADC has an output pin for setting the input common mode voltage, it can be directly tied to the +IN2 pin, as long as it is capable of providing the input current into +IN2 as listed in the Electrical Characteristics Table. Alternatively, +IN2 may be driven by an external precision reference such as the LT1790.

For lowest offset, the +IN2 pin should see 499Ω of driving resistance in all applications (see Offset Considerations). If the driving resistance is nominally less than 499Ω, additional resistance can be added to make up the difference. The resistor noise bandwidth can be reduced by bypassing the +IN2 pin to the ground plane with a chip ceramic capacitor of at least 0.1µF (see the Typical Application on the front page). The bypass capacitance also helps prevent AC signals on this pin from being inadvertently converted to differential signals.

$\overline{\text{SHDN}}$

If the $\overline{\text{SHDN}}$ pin (Pin 7), is pulled low within 300mV of the negative supply rail, the LT6350 will power down. The pin is connected through a diode to an internal current source of 20µA. When pulled below the shutdown threshold, the 20µA current will flow from the pin. If the pin is left open or pulled high (above V^- + 2V), the part will enter normal active operation, and the current into the pin will be very small due to the reverse-biased diode.

APPLICATIONS INFORMATION

In shutdown, all biasing current sources are shut off, and the output pins, OUT1 and OUT2, each appear as open collectors with non-linear capacitors in parallel and steering diodes to either supply. Because of the non-linear capacitance, the outputs still have the ability to sink and source small amounts of transient current if driven with significant voltage transients. The input protection diodes between +IN1 and +IN2 can still conduct if voltage transients at the input exceed 700mV. All other inputs also have ESD protection diodes that can conduct when the applied voltage exceeds 700mV. Using the $\overline{SHDN}$ feature to wire-OR outputs together is not recommended.

The turn-on and turn off times between the shutdown and active states are typically 400ns.

ESD

The LT6350 has ESD protection diodes on all inputs and outputs. The diodes are reverse biased during normal operation. If input pins are driven beyond either supply, large currents will flow through these diodes. If the current is transient and limited to 100mA or less, no damage to the device will occur.

OFFSET CONSIDERATIONS

For excellent offset and distortion performance, both the common mode and differential mode output voltage offsets are trimmed during manufacturing.

Figure 7 shows the contributors to DC offset voltage in the LT6350.

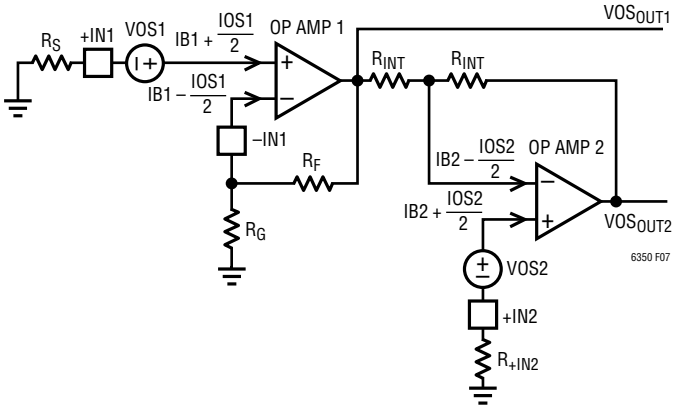


Figure 7. Offset Model

The resulting DC offset voltages at pin OUT1 and OUT2 can be calculated:

$$VOS_{OUT1} = VOS1 \bullet (1+R_F/R_G) + IB1 \bullet (R_F - R_S \bullet (1+R_F/R_G)) - (IOS1/2) \bullet (R_F + R_S \bullet (1+R_F/R_G))$$

$$VOS_{OUT2} = -VOS_{OUT1} + 2 \bullet VOS2 + IB2 \bullet (R_{INT} - 2 \bullet R_{+IN2}) - (IOS2/2) \bullet (R_{INT} + 2 \bullet R_{+IN2})$$

Using the above equations and Equations (2) and (3), the output common mode and output differential mode offsets can be found. The common mode offset is found to be:

$$VOS_{CM} = VOS2 + IB2 \bullet ((R_{INT}/2) - R_{+IN2}) - (IOS2/2) \bullet ((R_{INT}/2) + R_{+IN2})$$

APPLICATIONS INFORMATION

Because the input bias current into op amp 2 is much larger than the offset current, choosing R_{+IN2} to be $R_{INT}/2$ greatly reduces the offset contribution of op amp 2's input currents on all units. With $R_{+IN2} = R_{INT}/2$, VOS_{CM} reduces to:

$$VOS_{CM} = VOS2 – (IOS2/2) \bullet R_{INT}$$

VOS_{CM} is trimmed to within ±125µV with a 499Ω resistor installed at +IN2.

The value of V_{OS1} is trimmed to bring V_{OSDIFF} to ± 125µV. Because linear modulation of V_{OS1} with input common mode could degrade the common mode rejection ratio specification of op amp 1, and nonlinear modulation of V_{OS1} could cause nonlinear gain error (distortion), V_{OS1} is trimmed to a low constant value over as wide an input common mode range as possible. A precision, 2-point trim algorithm is used that results in V_{OS1} within ±125µV over the input range $V^- + 1.3V \le V_{+IN1} \le V^+$ and V_{OS1} within ±300µV over the input range $V^- \le V_{+IN1} \le V^+$. A negative supply below –1.3V can be used to extend the input range for which V_{OS1} is within ±125µV all the way down to ground.

As a result of the trim procedure, the lowest offsets, both common mode and differential mode, will occur with a 499Ω resistor at +IN2. This resistor can be bypassed with a capacitor to eliminate its noise contribution. The gain-setting resistor network (R_G and R_F) impedance should be matched to that of the source to minimize op amp 1's input bias current contributions to the offsets.

NOISE CONSIDERATIONS

A model showing the sources of output noise in the LT6350 is shown in Figure 8. The total output noise resulting from all contributors is governed by the equation:

The LT6350 uses very low noise op amps, resulting in a total differential output spot noise at 10kHz of 8.2nV/√Hz when the LT6350 is in the noninverting gain-of-two configuration shown in Figure 2. This is equivalent to the voltage noise of a 1015Ω resistor at the +IN1 input. For source resistors larger than about 1k, voltage noise due to the source resistance will start to dominate output noise. Source resistors larger than about 13k will interact with the input current noise and result in output noise that is resistor noise and amplifier current noise dominant.

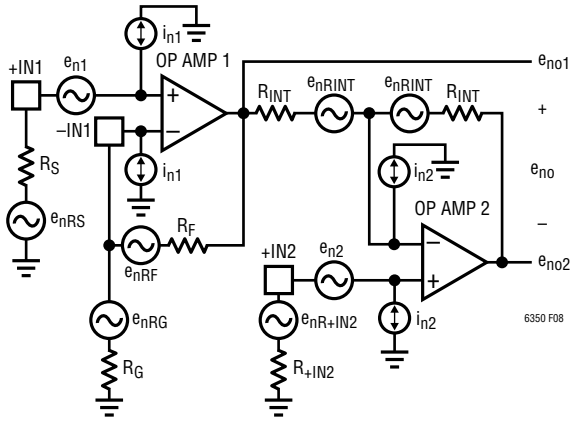


Figure 8. Noise Model

Note that the parallel combination of gain-setting resistors R_F and R_G behaves like the source resistance, R_S, from the point of view of noise calculations, and the value should be kept below about 1k to avoid increasing the output noise. Lower-value gain and feedback resistors,

$$e_{no} = \sqrt{(4 \bullet [e^2_{n1} + (i_{n1}R_S)^2 + e^2_{nRS}](1 + (R_F/R_G))^2 + 4 \bullet (i_{n1}R_F)^2 + 4e^2_{nRF}(1 + (R_F/R_G)) + 4e^2_{n2} + 4e^2_{nR+IN2} + 2e^2_{nRINT} + (i_{n2}R_{INT})^2 + 4 \bullet (i_{n2}R_{+IN2})^2)}$$

APPLICATIONS INFORMATION

R_G and R_F, will always result in lower output noise at the expense of increased distortion due to increased loading of op amp 1. Note that op amp 1 is loaded internally by the 1k input resistor to op amp 2, and therefore external loading should not be much heavier than 1k to avoid degrading distortion performance.

When using R_F equal to R_S (for low offsets) in the gain-of-two configuration, wideband noise can be substantially reduced by bypassing across R_F. For lowest output noise always bypass at the +IN2 pin with a capacitor of at least 0.1µF as seen in the Typical Application schematic on the front page. Alternatively, for systems that can tolerate output voltage offsets, omitting R_{+IN2} and R_F will minimize output noise at the expense of larger output offset voltage.

Using a single pole passive RC filter network at the output of the LT6350, as shown in Figure 6, reduces the output noise bandwidth and thereby increases the signal-to-noise ratio of the system. For example, in a typical system with output signals of $8V_{P-P}$, and a signal bandwidth of 100kHz, an RC output filter with R_{FILT} = 100Ω and C_{DIFF} = 6.8nF, slightly increases the output spot noise from $8.2nV\sqrt{Hz}$ to $8.4nV\sqrt{Hz}$, but will reduce the total integrated noise from 47µV (33MHz noise bandwidth) to 3.6µV (184kHz noise bandwidth) and improve the SNR from 96dB to 118dB. Keep in mind that long RC time constants in the output filter can increase the settling time at the inputs of the ADC; incomplete settling can cause gain errors or increase apparent crosstalk in multiplexed systems.

OUTPUT PHASE BALANCE

The topology of the LT6350 is that of a noninverting stage followed by an inverting stage. This topology presents a high impedance single-ended input and provides low impedance differential outputs. The output of the inverting buffer, OUT2, is slightly delayed with respect to the output of the noninverting buffer, OUT1. In the LT6350, the delay from OUT1 to OUT2 over an input bandwidth from DC to the differential f_{-3dB} frequency is a nearly constant 6.8ns, as shown in the group delay plot in the Typical Performance Characteristics section of this data sheet. The delay is equivalent to a small phase offset from the nominal 180° phase of the differential outputs. The size of the phase offset grows with frequency. The phase imbalance causes a small frequency-dependent common mode component to appear at the outputs. A practical measure of this effect can be found in the balance specification, which is defined to be the change in output common mode level caused by the presence of an output differential signal:

$$\text{Balance} \equiv ((V_{OUTDIFF}/V_{IN})/(V_{OUTCM}/V_{IN}))$$

The balance of the LT6350 at any frequency, f, can be approximated from the delay, t_d, between outputs:

$$\text{Balance (dB)} \cong 20 \bullet \log((4)/(2 \bullet \pi \bullet f \bullet t_d))$$

The approximation is very good from low frequencies up to frequencies where the balance approaches 20dB, about 10MHz for the LT6350. At DC, the balance is limited by the matching of the internal resistors that set the gain in the inverting buffer. 1% matching of the resistors limits the balance to 52dB at DC. At frequencies near the f_{-3dB} point of the differential transfer function, additional phase lag and gain rolloff also contribute to balance. See the balance plot in the Typical Performance Characteristics for a detailed picture of Balance vs Input Frequency.

APPLICATIONS INFORMATION

BOARD LAYOUT AND BYPASS CAPACITORS/DC1538A DEMOBOARD

For single-supply applications it is recommended that a high quality X5R or X7R, 0.1µF bypass capacitor be placed directly between the V^+ and the V^- pin; the V^- pin (including the Exposed Pad on the DD8 package) should be tied directly to a low impedance ground plane with minimal routing. For split power supplies, it is recommended that additional high quality X5R or X7R, 0.1µF capacitors be used to bypass pin V^+ to ground and V^- to ground, again with minimal routing. Small geometry (e.g., 0603) surface mount ceramic capacitors have a much higher self-resonant frequency than do leaded capacitors, and perform best with the LT6350.

The +IN2 pin should be bypassed to ground with a high quality ceramic capacitor of at least 0.1µF, both to reduce the noise bandwidth of the recommended DC offset balance resistor and to prevent changes in the common mode reference voltage from being converted into a differential output signal.

Stray parasitic capacitance at the –IN1 pin should be kept to a minimum to prevent degraded stability resulting in excessive ringing or oscillations. Traces at –IN1 should be kept as short as possible, and any ground plane should be stripped from under the pin and pin traces.

Because the outputs operate differentially, load impedances seen by both outputs (stray or intended) should be as balanced and symmetric as possible. This will help preserve the balanced operation that minimizes the generation of even-order harmonic distortion in the output stage and maximizes the rejection of common mode signals and noise.

The DC1538A demoboard has been designed for the evaluation of the LT6350 following the above layout practices. Its schematic and component placement are shown in Figures 9 and 10.

APPLICATIONS INFORMATION

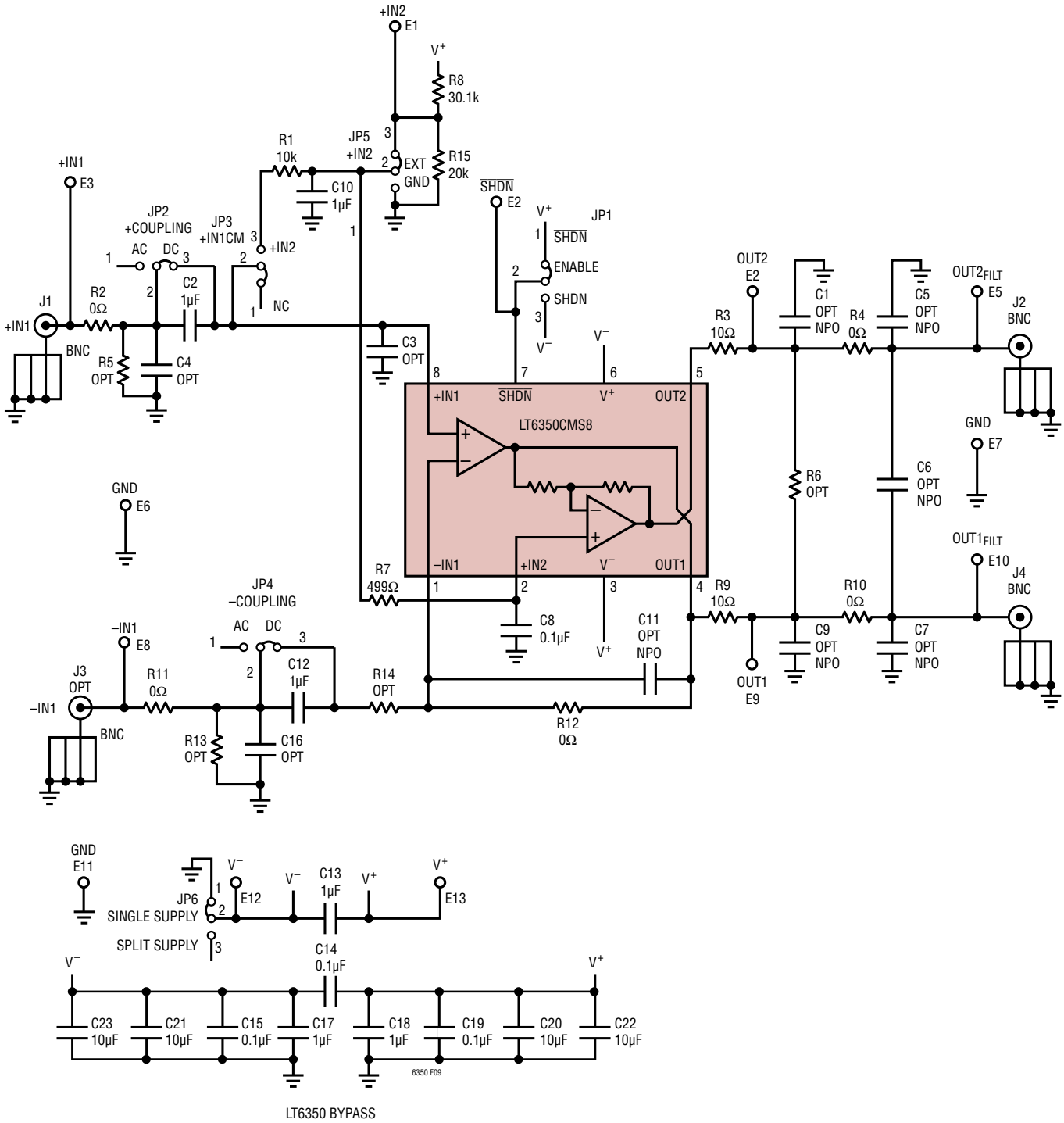


Figure 9. DC1538A Demoboard Schematic

APPLICATIONS INFORMATION

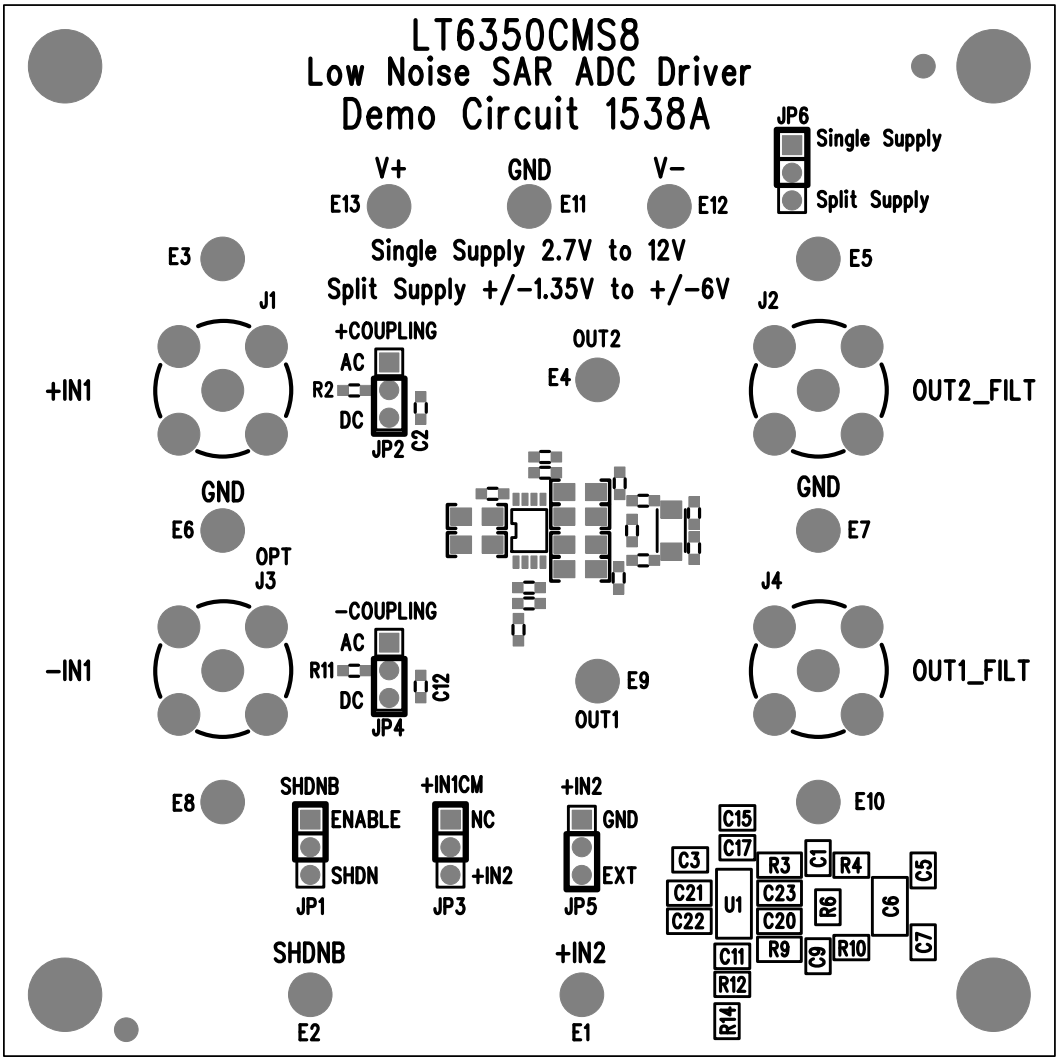


Figure 10. DC1538A Demoboard Layout

APPLICATIONS INFORMATION

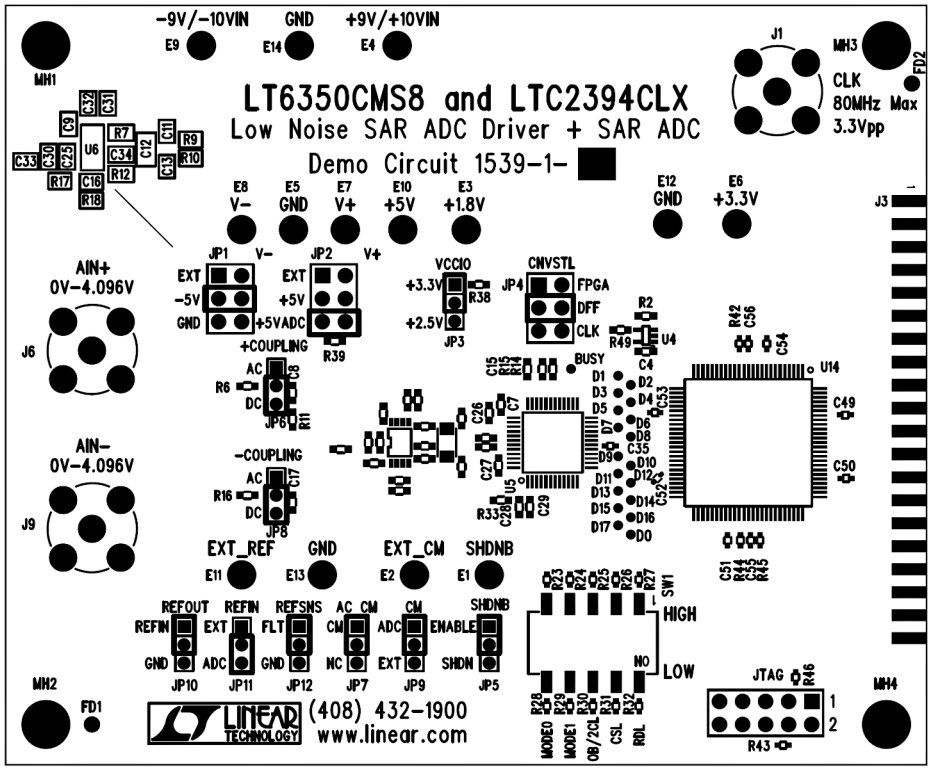


Figure 11. DC1539A Demoboard Layout

DRIVING THE LTC239X-16 / DC1539A DEMOBOARD

The DC1539A demoboard, shown in Figure 11, has been developed to demonstrate the interfacing of the LT6350 to the LTC239x-16 family of 16-bit SAR ADCs.

Spurious-free dynamic range of 102.2dB is achievable on the DC1539A as seen in the FFT in Figure 12.

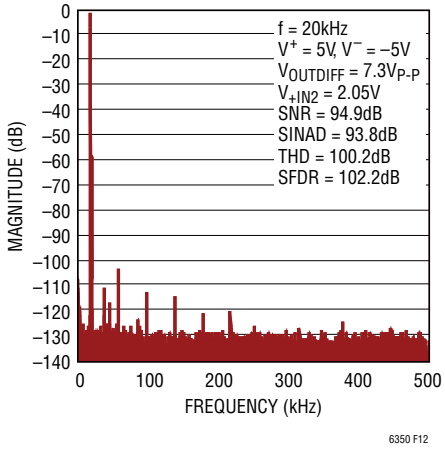


Figure 12. 8192-Point FFT LT6350 Driving the LTC2393-16 on the DC1539A Demoboard

APPLICATIONS INFORMATION

100kHz, 3RD-ORDER BUTTERWORTH FILTER

The LT6350 can be configured as a single-ended to differential filter incorporating feedback from the inverting output. Figure 13 shows the schematic of the configuration with values giving a 3rd Order Butterworth characteristic having a 100kHz –3dB point with a differential gain of four. Figure 14 shows the filter output response to 10MHz. As an option, to match the source impedance and preserve the low DC errors of the LT6350, connect a 2.10k series resistor at +IN1. To reduce the resistor noise, the +IN1 pin can be bypassed with a 0.1µF capacitor. For similar topologies please consult the LT1567 data sheet and design guide.

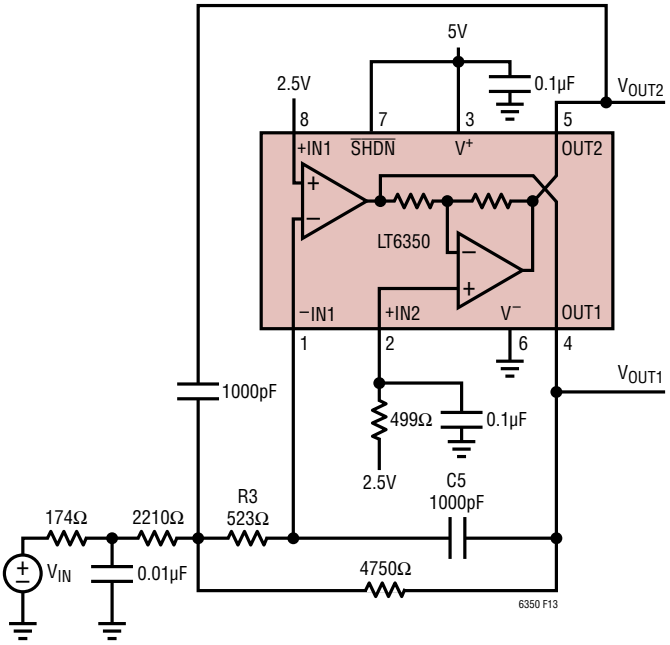


Figure 13. 100KHz, 3rd Order Butterworth Filter

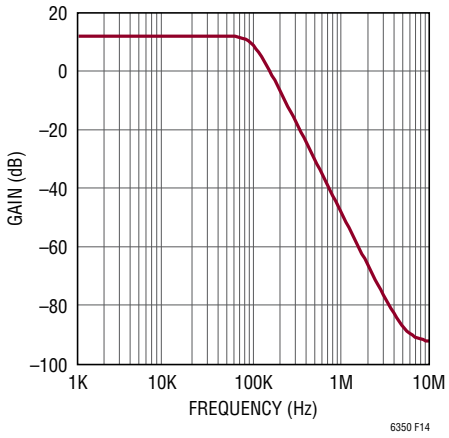


Figure 14. 100KHz, 3rd Order Butterworth Filter Response

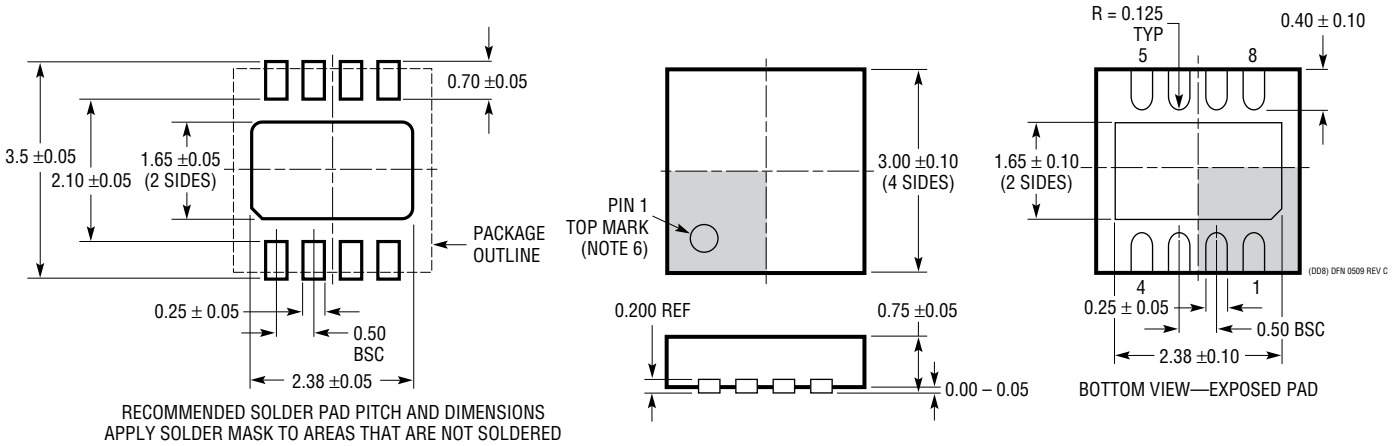
Low Noise, Low Power 1MΩ Single Supply Photodiode Differential Output Transimpedance Amplifier

The Typical Application on the back page shows the LT6350 applied as a differential output transimpedance amplifier. The LT6350 forces the BF862 ultralow noise JFET source to 3V, with R2 ensuring that the JFET has an I_{DRAIN} of 1mA. The JFET acts as a source follower, buffering the input of the LT6350 and making it suitable for the high impedance feedback element R1. The BF862 has a minimum I_{DSS} of 10mA and a pinchoff voltage between –0.3V and –1.2V. The JFET gate and OUT1 therefore sit at a point slightly higher than one pinchoff voltage below 3V, about mid-supply at 2.5V.

When the photodiode is illuminated, the current must come from OUT1 through R1 as in a normal transimpedance amplifier. Amplifier output noise density is dominated at low frequency by the 130nV/$\sqrt{Hz}$ of the feedback resistor, rising to 210nV/$\sqrt{Hz}$ at 1MHz. Note that because the JFET has a high g_m, approximately 1/30Ω, its attenuation looking into R2 is only about 1%. The closed-loop bandwidth using a 3pF photodiode was measured at approximately 1.35MHz. With the output taken differentially, the gain and the noise are both doubled.

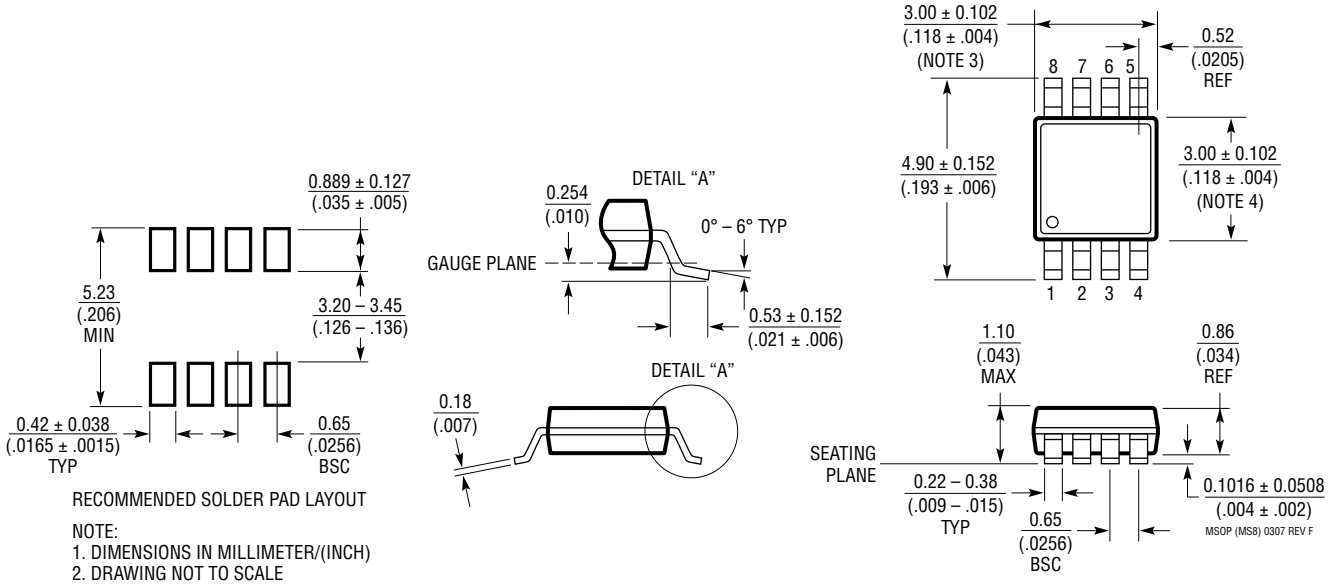
PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)



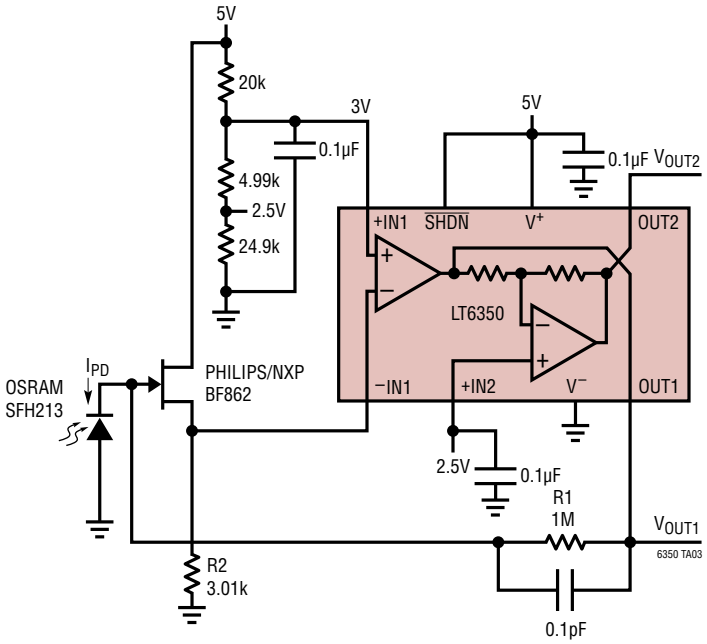
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

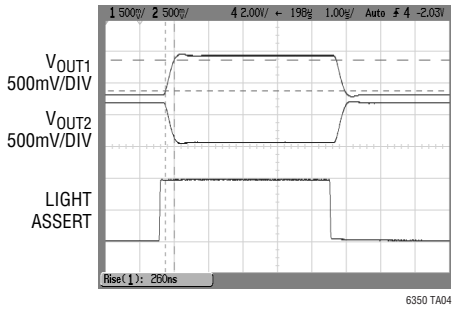
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/10	Updated Units on V_{OH} in Electrical Characteristics	4
B	05/10	Updated Note 2	5
		Updated Related Parts	28
C	06/13	Corrected curve labels on Input Bias Current vs Input Voltage graphs	7

TYPICAL APPLICATION

Low Noise, Low Power 1MΩ Single Supply Photodiode Transimpedance Amplifier





$V_{OUTDIFF}$ = ~ ±200mV + I_{PD} • 2MΩ
BW = 1.35MHz

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2391-16/ LTC2392-16/ LTC2393-16	16-Bit SAR ADCs	250ksps/500ksps/1Msps
LT6202/LT6203	Single/Dual 100MHz Rail-to-Rail Input/Output Ultralow Noise, Low Power Amplifiers	1.9nV/√Hz, 3mA Maximum, 100MHz Gain Bandwidth
LT1806/LT1807	Single/Dual 325MHz Low Noise/Low Distortion Rail-toRail Input/Output Amplifiers	2.5V Operation, 550µV Maximum V_{OS}, 3.5µV/√Hz
LTC6403	200MHz Low Noise, Low Distortion, Fully Differential Input/Output Amplifier/Driver	10.8mA Supply Current, –95dBc Distortion at 3MHz, $2V_{P-P}$ Output
LT1468/LT1469	Single/Dual 90MHz, 22V/µs 16-Bit Accurate Op Amp	±5V to ±15V Operation, VOS ≤ 75µV
LTC6246/LTC6247/ LTC6248	Single/Dual/Quad 180MHz Rail-to-Rail Low Power Op Amps	1mA/Amplifier, 4.2nV/√Hz
LTC1992/LTC1992-X	Fully Differential Input/Output Amplifiers	Programmable Gain or Fixed Gain (G = 1, 2, 5, 10)
LT1994	Low Noise, Low Distortion Fully Differential Input/Output Amplifier/Driver	Low Distortion, $2V_{P-P}$, 1MHz –94dBc, 13mA, Low Noise 3nV/√Hz

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