# CYV15G0403TB

# Independent Clock Quad HOTLink II™ Serializer

## Features

- **Second-generation HOTLink® technology**
- **Compliant to SMPTE 292M and SMPTE 259M video standards**
- **Quad channel video serializer**
  - **— 195- to 1500-Mbps serial data signaling rate**
  - **— Simultaneous operation at different signaling rates**
- **Supports half-rate and full-rate clocking**
- **Internal phase-locked loops (PLLs) with no external PLL components**
- **Redundant differential PECL-compatible serial outputs per channel**
  - **— No external bias resistors required**
  - **— Signaling-rate controlled edge-rates**
  - **— Internal source termination**
- **Synchronous LVTTL parallel interface**
- **JTAG boundary scan**
- **Built-In Self-Test (BIST) for at-speed link testing**
- **Low-power 2W @ 3.3V typical**
- **Single 3.3V supply**
- **Thermally enhanced BGA**
- **Pb-Free package option available**
- **0.25μ BiCMOS technology**

## Functional Description

The CYV15G0403TB Independent Clock Quad HOTLink II™ Serializer is a point-to-point or point-to-multipoint communications building block enabling transfer of data over a variety of high-speed serial links including SMPTE 292M and SMPTE 259M video applications. It supports signaling rates in the range of 195 to 1500 Mbps per serial link. All four channels are independent and can simultaneously operate at different rates. Each channel accepts 10-bit parallel characters in an Input Register and converts them to serial data. *Figure 1* illustrates typical connections between independent video coprocessors and corresponding CYV15G0403TB Serializer and CYV15G0404RB Reclocking Deserializer chips.

The CYV15G0403TB satisfies the SMPTE-259M and SMPTE-292M compliance as per SMPTE EG34-1999 Pathological Test Requirements.

As a second-generation HOTLink device, the CYV15G0403TB extends the HOTLink family with enhanced levels of integration and faster data rates, while maintaining serial-link compatibility (data and BIST) with other HOTLink devices. Each channel of the CYV15G0403TB Quad HOTLink II device independently accepts scrambled 10-bit transmission characters. These characters are serialized and output from dual Positive ECL (PECL) compatible differential transmission-line drivers at a bit-rate of either 10- or 20-times the input reference clock for that channel.

Each channel contains an independent BIST pattern generator. This BIST hardware allows at-speed testing of the high-speed serial data paths in each transmit section of this device, each receive section of a connected HOTLink II device, and across the interconnecting links.

The CYV15G0403TB is ideal for SMPTE applications where different data rates and serial interface standards are necessary for each channel. Some applications include multi-format routers, switchers, format converters, and cameras.

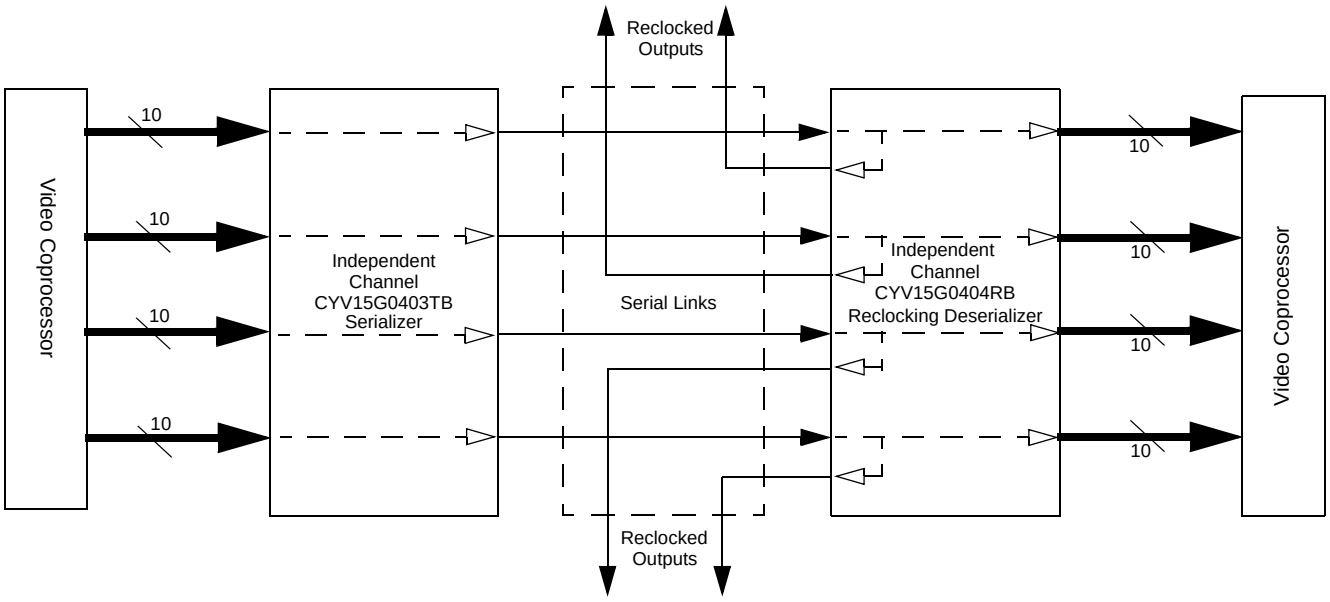
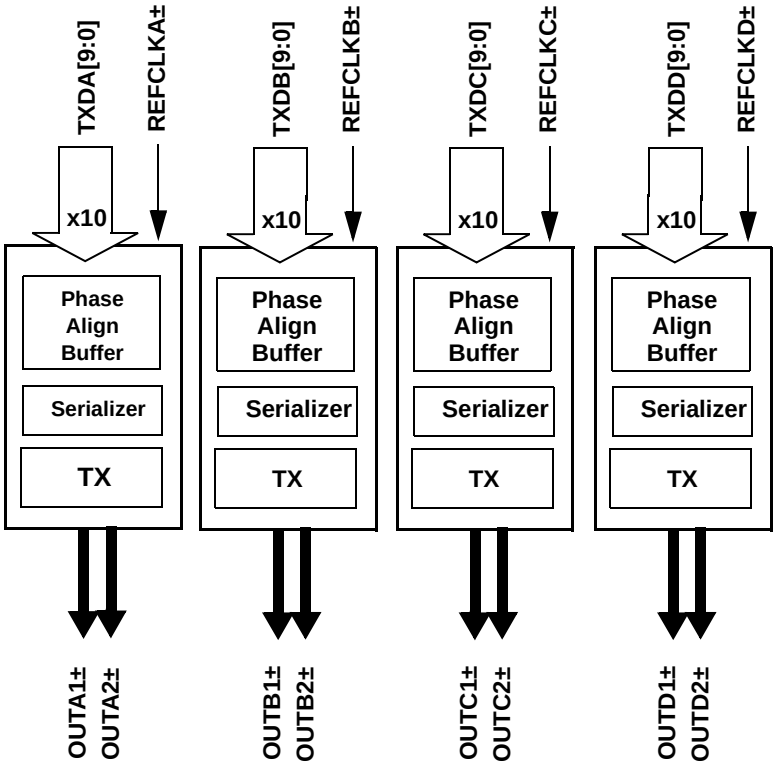



**Figure 1. HOTLink II™ System Connections**

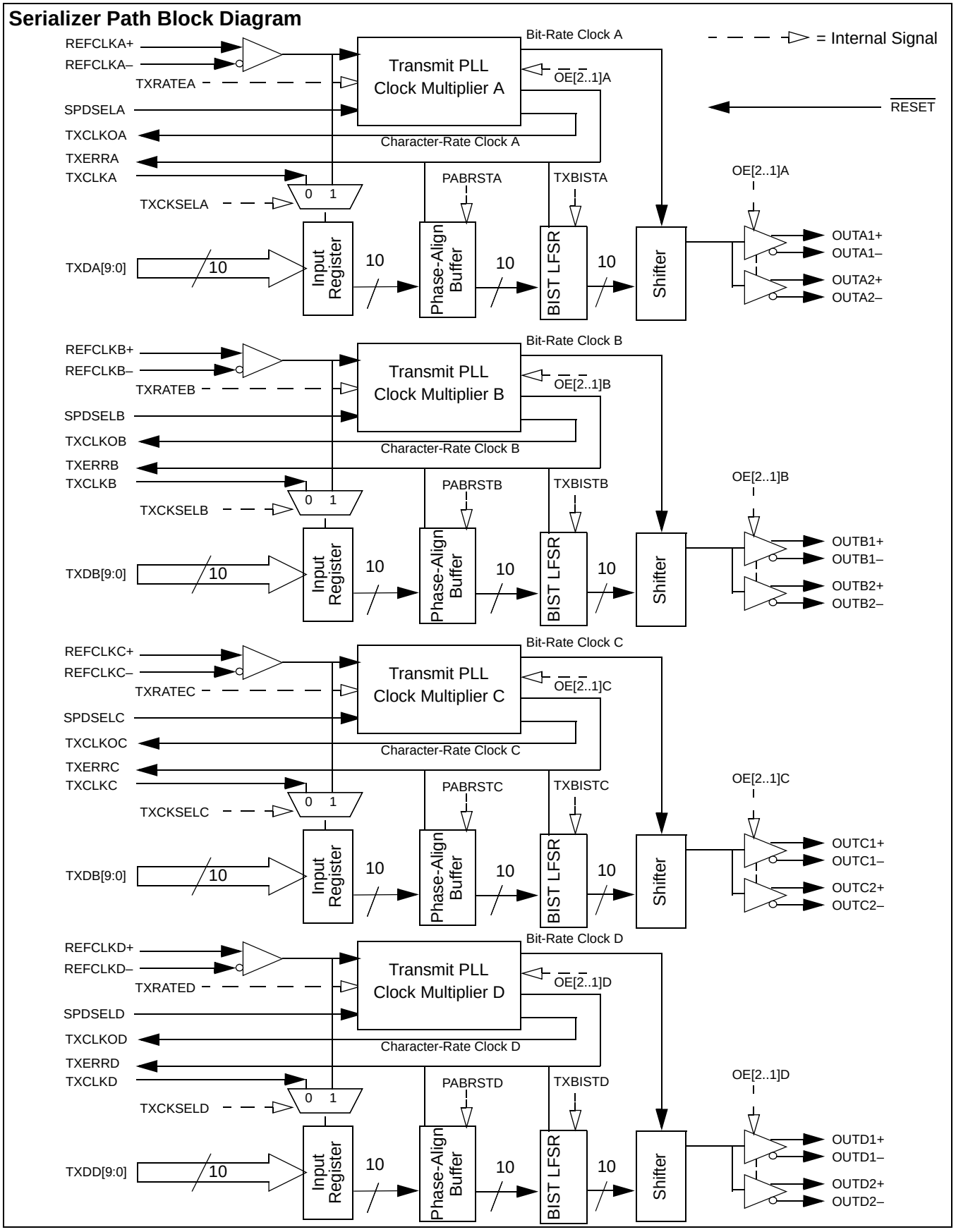
## CYV15G0403TB Serializer Logic Block Diagram






[+] Feedback

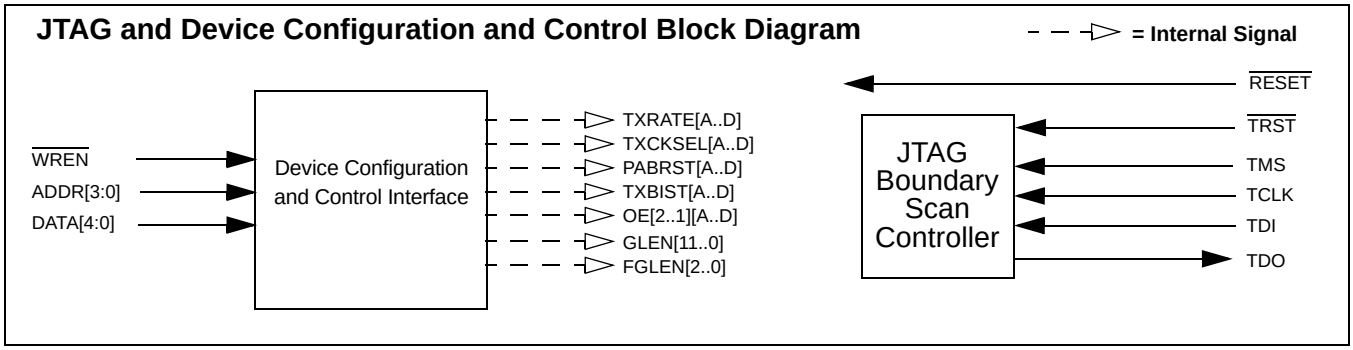
## Serializer Path Block Diagram






[+] Feedback

## JTAG and Device Configuration and Control Block Diagram






[+] Feedback

## Pin Configuration (Top View)[1]

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NC | OUT C1– | NC | OUT C2– | $V_{CC}$ | NC | OUT D1– | GND | GND | OUT D2– | GND | OUT A1– | GND | GND | OUT A2– | $V_{CC}$ | $V_{CC}$ | OUT B1– | $V_{CC}$ | OUT B2– |
| B | $V_{CC}$ | OUT C1+ | $V_{CC}$ | OUT C2+ | $V_{CC}$ | $V_{CC}$ | OUT D1+ | GND | NC | OUT D2+ | NC | OUT A1+ | GND | NC | OUT A2+ | $V_{CC}$ | NC | OUT B1+ | NC | OUT B2+ |
| C | TDI | TMS | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | NC | NC | GND | NC | NC | DATA [3] | DATA [1] | GND | NC | SPD SELD | $V_{CC}$ | NC | $\overline{TRST}$ | GND | TDO |
| D | TCLK | $\overline{RESET}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | SPD SELC | GND | GND | DATA [4] | DATA [2] | DATA [0] | GND | GND | NC | $V_{CC}$ | NC | NC | SCAN EN2 | TMEN3 |
| E | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | | | | | | | | | | | | | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |
| F | NC | NC | TX DC[0] | NC | | | | | | | | | | | | | NC | NC | TX CLKOB | NC |
| G | TX DC[7] | $\overline{WREN}$ | TX DC[4] | TX DC[1] | | | | | | | | | | | | | SPD SELB | NC | SPD SELA | NC |
| H | GND | GND | GND | GND | | | | | | | | | | | | | GND | GND | GND | GND |
| J | TX DC[9] | TX DC[5] | TX DC[2] | TX DC[3] | | | | | | | | | | | | | NC | NC | NC | NC |
| K | NC | REF CLKC– | TX DC[8] | TX CLKC | | | | | | | | | | | | | NC | NC | NC | NC |
| L | NC | REF CLKC+ | NC | TX DC[6] | | | | | | | | | | | | | NC | NC | NC | TX DB[6] |
| M | NC | NC | NC | TX ERRC | | | | | | | | | | | | | REF CLKB+ | REF CLKB– | TX ERRB | TX CLKB |
| N | GND | GND | GND | GND | | | | | | | | | | | | | GND | GND | GND | GND |
| P | NC | NC | NC | NC | | | | | | | | | | | | | TX DB[5] | TX DB[4] | TX DB[3] | TX DB[2] |
| R | NC | TX CLKOC | NC | NC | | | | | | | | | | | | | TX DB[1] | TX DB[0] | TX DB[9] | TX DB[7] |
| T | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | | | | | | | | | | | | | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |
| U | TX DD[0] | TX DD[1] | TX DD[2] | TX DD[9] | $V_{CC}$ | NC | NC | GND | TX DA[9] | ADDR [0] | REF CLKD– | TX DA[1] | GND | TX DA[4] | TX DA[8] | $V_{CC}$ | NC | TX DB[8] | NC | NC |
| V | TX DD[3] | TX DD[4] | TX DD[8] | NC | $V_{CC}$ | NC | NC | GND | NC | ADDR [2] | REF CLKD+ | TX CLKOA | GND | TX DA[3] | TX DA[7] | $V_{CC}$ | NC | NC | NC | NC |
| W | TX DD[5] | TX DD[7] | NC | NC | $V_{CC}$ | NC | NC | GND | ADDR [3] | ADDR [1] | NC | TX ERRA | GND | TX DA[2] | TX DA[6] | $V_{CC}$ | NC | REF CLKA+ | NC | NC |
| Y | TX DD[6] | TX CLKD | NC | NC | $V_{CC}$ | NC | NC | GND | TX CLKOD | NC | TX CLKA | NC | GND | TX DA[0] | TX DA[5] | $V_{CC}$ | TX ERRD | REF CLKA– | NC | NC |

**Note:**
1. NC = Do not connect.



[+] Feedback

## Pin Configuration (Bottom View)[1]

| | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | OUT B2– | $V_{CC}$ | OUT B1– | $V_{CC}$ | $V_{CC}$ | OUT A2– | GND | GND | OUT A1– | GND | OUT D2– | GND | GND | OUT D1– | NC | $V_{CC}$ | OUT C2– | NC | OUT C1– | NC |
| B | OUT B2+ | NC | OUT B1+ | NC | $V_{CC}$ | OUT A2+ | NC | GND | OUT A1+ | NC | OUT D2+ | NC | GND | OUT D1+ | $V_{CC}$ | $V_{CC}$ | OUT C2+ | $V_{CC}$ | OUT C1+ | $V_{CC}$ |
| C | TDO | GND | $\overline{TRST}$ | NC | $V_{CC}$ | SPD SELD | NC | GND | DATA [1] | DATA [3] | NC | NC | GND | NC | NC | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | TMS | TDI |
| D | TMEN3 | SCAN EN2 | NC | NC | $V_{CC}$ | NC | GND | GND | DATA [0] | DATA [2] | DATA [4] | GND | GND | SPD SELC | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $\overline{RESET}$ | TCLK |
| E | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | | | | | | | | | | | | | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |
| F | NC | TX CLKOB | NC | NC | | | | | | | | | | | | | NC | TX DC[0] | NC | NC |
| G | NC | SPD SELA | NC | SPD SELB | | | | | | | | | | | | | TX DC[1] | TX DC[4] | $\overline{WREN}$ | TX DC[7] |
| H | GND | GND | GND | GND | | | | | | | | | | | | | GND | GND | GND | GND |
| J | NC | NC | NC | NC | | | | | | | | | | | | | TX DC[3] | TX DC[2] | TX DC[5] | TX DC[9] |
| K | NC | NC | NC | NC | | | | | | | | | | | | | TX CLKC | TX DC[8] | REF CLKC– | NC |
| L | TX DB[6] | NC | NC | NC | | | | | | | | | | | | | TX DC[6] | NC | REF CLKC+ | NC |
| M | TX CLKB | TX ERRB | REF CLKB– | REF CLKB+ | | | | | | | | | | | | | TX ERRC | NC | NC | NC |
| N | GND | GND | GND | GND | | | | | | | | | | | | | GND | GND | GND | GND |
| P | TX DB[2] | TX DB[3] | TX DB[4] | TX DB[5] | | | | | | | | | | | | | NC | NC | NC | NC |
| R | TX DB[7] | TX DB[9] | TX DB[0] | TX DB[1] | | | | | | | | | | | | | NC | NC | TX CLKOC | NC |
| T | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | | | | | | | | | | | | | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |
| U | NC | NC | TX DB[8] | NC | $V_{CC}$ | TX DA[8] | TX DA[4] | GND | TX DA[1] | REF CLKD– | ADDR [0] | TX DA[9] | GND | NC | NC | $V_{CC}$ | TX DD[9] | TX DD[2] | TX DD[1] | TX DD[0] |
| V | NC | NC | NC | NC | $V_{CC}$ | TX DA[7] | TX DA[3] | GND | TX CLKOA | REF CLKD+ | ADDR [2] | NC | GND | NC | NC | $V_{CC}$ | NC | TX DD[8] | TX DD[4] | TX DD[3] |
| W | NC | NC | REF CLKA+ | NC | $V_{CC}$ | TX DA[6] | TX DA[2] | GND | TX ERRA | NC | ADDR [1] | ADDR [3] | GND | NC | NC | $V_{CC}$ | NC | NC | TX DD[7] | TX DD[5] |
| Y | NC | NC | REF CLKA– | TX ERRD | $V_{CC}$ | TX DA[5] | TX DA[0] | GND | NC | TX CLKA | NC | TX CLKOD | GND | NC | NC | $V_{CC}$ | NC | NC | TX CLKD | TX DD[6] |



[+] Feedback

## Pin Definitions
## CYV15G0403TB Quad HOTLink II Serializer

| Name | I/O Characteristics | Signal Description |
|---|---|---|
| **Transmit Path Data and Status Signals** | | |
| TXDA[9:0]<br>TXDB[9:0]<br>TXDC[9:0]<br>TXDD[9:0] | LVTTL Input, synchronous, sampled by the associated TXCLKx↑ or REFCLKx↑[2] | **Transmit Data Inputs**. TXDx[9:0] data inputs are captured on the rising edge of the transmit interface clock. The transmit interface clock is selected by the TXCKSELx latch via the device configuration interface. |
| TXERRA<br>TXERRB<br>TXERRC<br>TXERRD | LVTTL Output, synchronous to REFCLKx↑ [3], asynchronous to transmit channel enable / disable, asynchronous to loss or return of REFCLKx± | **Transmit Path Error**. TXERRx is asserted HIGH to indicate detection of a transmit Phase-Align Buffer underflow or overflow. If an underflow or overflow condition is detected, TXERRx, for the channel in error, is asserted HIGH and remains asserted until the transmit Phase-Align Buffer is re-centered with the PABRSTx latch via the device configuration interface. When TXBISTx = 0, the BIST progress is presented on the associated TXERRx output. The TXERRx signal pulses HIGH for one transmit-character clock period to indicate a pass through the BIST sequence once every 511 character times.<br>TXERRx is also asserted HIGH, when any of the following conditions is true:<br>• The TXPLL for the associated channel is powered down. This occurs when OE2x and OE1x for a given channel are both disabled by setting OE2x = 0 and OE1x = 0.<br>• The absence of the REFCLKx± signal. |
| **Transmit Path Clock Signals** | | |
| REFCLKA±<br>REFCLKB±<br>REFCLKC±<br>REFCLKD± | Differential LVPECL or single-ended LVTTL input clock | **Reference Clock**. REFCLKx± clock inputs are used as the timing references for the associated transmit PLL. These input clocks may also be selected to clock the transmit parallel interface. When driven by a single-ended LVCMOS or LVTTL clock source, connect the clock source to either the true or complement REFCLKx input, and leave the alternate REFCLKx input open (floating). When driven by an LVPECL clock source, the clock must be a differential clock, using both inputs. |
| TXCLKA<br>TXCLKB<br>TXCLKC<br>TXCLKD | LVTTL Clock Input, internal pull-down | **Transmit Path Input Clock**. When configuration latch TXCKSELx = 0, the associated TXCLKx input is selected as the character-rate input clock for the TXDx[9:0] input. In this mode, the TXCLKx input must be frequency-coherent to its associated TXCLKOx output clock, but may be offset in phase by any amount. Once initialized, TXCLKx is allowed to drift in phase as much as ±180 degrees. If the input phase of TXCLKx drifts beyond the handling capacity of the Phase Align Buffer, TXERRx is asserted to indicate the loss of data, and remains asserted until the Phase Align Buffer is initialized. The phase of the TXCLKx input clock relative to its associated REFCLKx± is initialized when the configuration latch PABRSTx is written as 0. When the associated TXERRx is deasserted, the Phase Align Buffer is initialized and input characters are correctly captured. |
| TXCLKOA<br>TXCLKOB<br>TXCLKOC<br>TXCLKOD | LVTTL Output | **Transmit Clock Output**. TXCLKOx output clock is synthesized by each channel's transmit PLL and operates synchronous to the internal transmit character clock. TXCLKOx operates at either the same frequency as REFCLKx± (TXRATEx = 0), or at twice the frequency of REFCLKx± (TXRATEx = 1). The transmit clock outputs have no fixed phase relationship to REFCLKx±. |
| **Device Control Signals** | | |
| $\overline{\text{RESET}}$ | LVTTL Input, asynchronous, internal pull-up | **Asynchronous Device Reset**. $\overline{\text{RESET}}$ initializes all state machines, counters, and configuration latches in the device to a known state. $\overline{\text{RESET}}$ must be asserted LOW for a minimum pulse width. When the reset is removed, all state machines, counters and configuration latches are at an initial state. See *Table 2* for the initialize values of the device configuration latches. |
| SPDSELA<br>SPDSELB<br>SPDSELC<br>SPDSELD | 3-Level Select[4] static control input | **Serial Rate Select**. The SPDSELx inputs specify the operating signaling-rate range of each channel's PLL.<br>LOW = 195–400 MBd<br>MID = 400–800 MBd<br>HIGH = 800–1500 MBd. |

**Notes:**
2. When REFCLKx± is configured for half-rate operation, these inputs are sampled relative to both the rising and falling edges of the associated REFCLKx±.
3. When REFCLKx± is configured for half-rate operation, these outputs are presented relative to both the rising and falling edges of the associated REFCLKx±.
4. 3-Level Select inputs are used for static configuration. These are ternary inputs that make use of logic levels of LOW, MID, and HIGH. The LOW level is usually implemented by direct connection to $V_{SS}$ (ground). The HIGH level is usually implemented by direct connection to $V_{CC}$ (power). The MID level is usually implemented by not connecting the input (left floating), which allows it to self bias to the proper level.



[+] Feedback

## Pin Definitions (continued)
## CYV15G0403TB Quad HOTLink II Serializer

| Name | I/O Characteristics | Signal Description |
|---|---|---|
| **Device Configuration and Control Bus Signals** | | |
| $\overline{\text{WREN}}$ | LVTTL input, asynchronous, internal pull-up | **Control Write Enable**. The $\overline{\text{WREN}}$ input writes the values of the DATA[4:0] bus into the latch specified by the address location on the ADDR[3:0] bus.[5] |
| ADDR[3:0] | LVTTL input asynchronous, internal pull-up | **Control Addressing Bus**. The ADDR[3:0] bus is the input address bus used to configure the device. The $\overline{\text{WREN}}$ input writes the values of the DATA[4:0] bus into the latch specified by the address location on the ADDR[3:0] bus.[5] *Table 2* lists the configuration latches within the device, and the initialization value of the latches upon the assertion of $\overline{\text{RESET}}$. *Table 3* shows how the latches are mapped in the device. |
| DATA[4:0] | LVTTL input asynchronous, internal pull-up | **Control Data Bus**. The DATA[4:0] bus is the input data bus used to configure the device. The $\overline{\text{WREN}}$ input writes the values of the DATA[4:0] bus into the latch specified by address location on the ADDR[3:0] bus.[5] *Table 2* lists the configuration latches within the device, and the initialization value of the latches upon the assertion of $\overline{\text{RESET}}$. *Table 3* shows how the latches are mapped in the device. |
| **Internal Device Configuration Latches** | | |
| TXCKSEL[A..D] | Internal Latch[6] | **Transmit Clock Select**. |
| TXRATE[A..D] | Internal Latch[6] | **Transmit PLL Clock Rate Select**. |
| TXBIST[A..D] | Internal Latch[6] | **Transmit Bist Disabled**. |
| OE2[A..D] | Internal Latch[6] | **Differential Serial Output Driver 2 Enable**. |
| OE1[A..D] | Internal Latch[6] | **Differential Serial Output Driver 1 Enable**. |
| PABRST[A..D] | Internal Latch[6] | **Transmit Clock Phase Alignment Buffer Reset**. |
| GLEN[11..0] | Internal Latch[6] | **Global Latch Enable**. |
| FGLEN[2..0] | Internal Latch[6] | **Force Global Latch Enable**. |
| **Factory Test Modes** | | |
| SCANEN2 | LVTTL input, internal pull-down | **Factory Test 2.** SCANEN2 input is for factory testing only. This input may be left as a NO CONNECT, or GND only. |
| TMEN3 | LVTTL input, internal pull-down | **Factory Test 3**. TMEN3 input is for factory testing only. This input may be left as a NO CONNECT, or GND only. |
| **Analog I/O** | | |
| OUTA1±<br>OUTB1±<br>OUTC1±<br>OUTD1± | CML Differential Output | **Primary Differential Serial Data Output**. The OUTx1± PECL-compatible CML outputs (+3.3V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules, and must be AC-coupled for PECL-compatible connections. |
| OUTA2±<br>OUTB2±<br>OUTC2±<br>OUTD2± | CML Differential Output | **Secondary Differential Serial Data Output**. The OUTx2± PECL-compatible CML outputs (+3.3V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules, and must be AC-coupled for PECL-compatible connections. |
| **JTAG Interface** | | |
| TMS | LVTTL Input, internal pull-up | **Test Mode Select**. Used to control access to the JTAG Test Modes. If maintained high for ≥5 TCLK cycles, the JTAG test controller is reset. |
| TCLK | LVTTL Input, internal pull-down | **JTAG Test Clock**. |
| TDO | 3-State LVTTL Output | **Test Data Out**. JTAG data output buffer. High-Z while JTAG test mode is not selected. |
| TDI | LVTTL Input, internal pull-up | **Test Data In**. JTAG data input port. |

**Notes:**
5. See *Device Configuration and Control Interface* for detailed information on the operation of the Configuration Interface.
6. See *Device Configuration and Control Interface* for detailed information on the internal latches.



[+] Feedback

## Pin Definitions (continued)
## CYV15G0403TB Quad HOTLink II Serializer

| Name | I/O Characteristics | Signal Description |
|---|---|---|
| $\overline{TRST}$ | LVTTL Input, internal pull-up | **JTAG reset signal**. When asserted (LOW), this input asynchronously resets the JTAG test access port controller. |
| **Power** | | |
| $V_{CC}$ | | **+3.3V Power**. |
| GND | | **Signal and Power Ground for all internal circuits**. |

## CYV15G0403TB HOTLink II Operation

The CYV15G0403TB is a highly configurable, independent clocking, quad-channel serializer designed to support reliable transfer of large quantities of digital video data, using high-speed serial links from multiple sources to multiple destinations. This device supports four 10-bit channels.

## CYV15G0403TB Transmit Data Path

### Input Register

The parallel input bus TXDx[9:0] can be clocked in using TXCLKx (TXCKSELx = 0) or REFCLKx (TXCKSELx = 1).

### Phase-Align Buffer

Data from each Input Register is passed to the associated Phase-Align Buffer, when the TXDx[9:0] input registers are clocked using TXCLKx (TXCKSELx = 0 and TXRATEx = 0). When the TXDx[9:0] input registers are clocked using REFCLKx± (TXCKSELx = 1) and REFCLKx± is a full-rate clock, the associated Phase Alignment Buffer in the transmit path is bypassed. These buffers are used to absorb clock phase differences between the TXCLKx input clock and the internal character clock for that channel.

Once initialized, TXCLKx is allowed to drift in phase as much as ±180 degrees. If the input phase of TXCLKx drifts beyond the handling capacity of the Phase Align Buffer, TXERRx is asserted to indicate the loss of data, and remains asserted until the Phase Align Buffer is initialized. The phase of the TXCLKx relative to its associated internal character rate clock is initialized when the configuration latch PABRSTx is written as 0. When the associated TXERRx is deasserted, the Phase Align Buffer is initialized and input characters are correctly captured.

If the phase offset, between the initialized location of the input clock and REFCLKx, exceeds the skew handling capabilities of the Phase-Align Buffer, an error is reported on that channel's TXERRx output. This output indicates an error continuously until the Phase-Align Buffer for that channel is reset. While the error remains active, the transmitter for that channel outputs a continuous "1001111000" character (LSB first) to indicate to the remote receiver that an error condition is present in the link.

### Transmit BIST

Each channel contains an internal pattern generator that can be used to validate both the link and device operation. These generators are enabled by the associated TXBISTx latch via the device configuration interface. When enabled, a register in the associated channel becomes a signature pattern generator by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character sequence. This provides a predictable yet pseudo-random sequence that can be matched to an identical LFSR in the attached Receiver(s).

A device reset ($\overline{RESET}$ sampled LOW) presets the BIST Enable Latches to disable BIST on all channels.

All data present at the associated TXDx[9:0] inputs are ignored when BIST is active on that channel.

### Transmit PLL Clock Multiplier

Each Transmit PLL Clock Multiplier accepts a character-rate or half-character-rate external clock at the associated REFCLKx± input, and that clock is multiplied by 10 or 20 (as selected by TXRATEx) to generate a bit-rate clock for use by the transmit shifter. It also provides a character-rate clock used by the transmit paths, and outputs this character rate clock as TXCLKOx.

Each clock multiplier PLL can accept a REFCLKx± input between 19.5 MHz and 150 MHz, however, this clock range is limited by the operating mode of the CYV15G0403TB clock multiplier (TXRATEx) and by the level on the associated SPDSELx input.

SPDSELx are 3-level select[4] inputs that select one of three operating ranges for the serial data outputs and inputs of the associated channel. The operating serial signaling-rate and allowable range of REFCLKx± frequencies are listed in *Table 1*.

**Table 1. Operating Speed Settings**

| SPDSELx | TXRATEx | REFCLKx± Frequency (MHz) | Signaling Rate (Mbps) |
|---|---|---|---|
| LOW | 1 | reserved | 195–400 |
| | 0 | 19.5–40 | |
| MID (Open) | 1 | 20–40 | 400–800 |
| | 0 | 40–80 | |
| HIGH | 1 | 40–75 | 800–1500 |
| | 0 | 80–150 | |

The REFCLKx± inputs are differential inputs with each input internally biased to 1.4V. If the REFCLKx+ input is connected to a TTL, LVTTL, or LVCMOS clock source, the input signal is recognized when it passes through the internally biased reference point. When driven by a single-ended TTL, LVTTL, or LVCMOS clock source, connect the clock source to either the true or complement REFCLKx input, and leave the alternate REFCLKx input open (floating).

When both the REFCLKx+ and REFCLKx– inputs are connected, the clock source must be a differential clock. This can either be a differential LVPECL clock that is DC-or AC-coupled or a differential LVTTL or LVCMOS clock.



[+] Feedback

By connecting the REFCLKx– input to an external voltage source, it is possible to adjust the reference point of the REFCLKx+ input for alternate logic levels. When doing so, it is necessary to ensure that the input differential crossing point remains within the parametric range supported by the input.

### Serial Output Drivers

The serial output interface drivers use differential Current Mode Logic (CML) drivers to provide source-matched drivers for 50Ω transmission lines. These drivers accept data from the Transmit Shifter, which shifts the data out LSB first. These drivers have signal swings equivalent to that of standard PECL drivers, and are capable of driving AC-coupled optical modules or transmission lines.

*Transmit Channels Enabled*

Each driver can be enabled or disabled separately via the device configuration interface.

When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both serial drivers for a channel are in this disabled state, the associated internal logic for that channel is also powered down. A device reset (RESET sampled LOW) disables all output drivers.

**Note**. When a disabled channel (i.e., both outputs disabled) is re-enabled:

- data on the serial outputs may not meet all timing specifications for up to 250 μs
- the state of the phase-align buffer cannot be guaranteed, and a phase-align reset is required if the phase-align buffer is used

## Device Configuration and Control Interface

The CYV15G0403TB is highly configurable via the configuration interface. This interface allows the device to be configured globally or allows each channel to be configured independently. *Table 2* lists the configuration latches within the device including the initialization value of the latches upon the assertion of RESET. *Table 3* shows how the latches are mapped in the device. Each row in the *Table 3* maps to a 5-bit latch bank. There are 16 such write-only latch banks. When WREN = 0, the logic value in DATA[4:0] is latched to the latch bank specified by the values in ADDR[3:0]. The second column of *Table 3* specifies the channels associated with the corresponding latch bank. For example, the first three latch banks (0,1 and 2) consist of configuration bits for channel A. The latch banks 12, 13 and 14 consist of Global configuration bits and the last latch bank (15) is the Mask latch bank that can be configured to perform bit-by-bit configuration.

### Global Enable Function

The global enable function, controlled by the GLENx bits, is a feature that can be used to reduce the number of write operations needed to setup the latch banks. This function is beneficial in systems that use a common configuration in multiple channels. The GLENx bit is present in bit 0 of latch banks 0 through 11 only. Its default value (1) enables the global update of the latch bank's contents. Setting the GLENx bit to 0 disables this functionality.

Latch Banks 12, 13, and 14 are used to load values in the related latch banks in a global manner. A write operation to latch bank 12 could do a global write to latch banks 0, 3, 6, and 9 depending on the value of GLENx in these latch banks; latch bank 13 could do a global write to latch banks 1, 4, 7 and 10; and latch banks 14 could do a global write to latch banks 2, 5, 8 and 11. The GLENx bit cannot be modified by a global write operation.

### Force Global Enable Function

FGLENx forces the global update of the target latch banks, but does not change the contents of the GLENx bits. If FGLENx = 1 for the associated global channel, FGLENx forces the global update of the target latch banks.

### Mask Function

An additional latch bank (15) is used as a global mask vector to control the update of the configuration latch banks on a bit-by-bit basis. A logic 1 in a bit location allows for the update of that same location of the target latch bank(s), whereas a logic 0 disables it. The reset value of this latch bank is FFh, thereby making its use optional by default. The mask latch bank is not maskable. The FGLEN functionality is not affected by the bit 0 value of the mask latch bank.

### Latch Types

There are two types of latch banks: static (S) and dynamic (D). Each channel is configured by 2 static and 1 dynamic latch banks. The S type contain those settings that normally do not change for a given application, whereas the D type controls the settings that could change during the application's lifetime. The first and second rows of each channel (address numbers 0, 1, 3, 4, 6, 7, 9, and 10) are the static control latches. The third row of latches for each channel (address numbers 2, 5, 8, and 11) are the dynamic control latches that are associated with enabling dynamic functions within the device.

Latch Bank 14 is also useful for those users that do not need the latch-based programmable feature of the device. This latch bank could be used in those applications that do not need to modify the default value of the static latch banks, and that can afford a global (i.e., not independent) control of the dynamic signals. In this case, this feature becomes available when ADDR[3:0] is left unchanged with a value of “1110” and WREN is left asserted. The signals present in DATA[4:0] effectively become global control pins, and for the latch banks 2, 5, 8 and 11.

### Static Latch Values

There are some latches in the table that have a static value (i.e. 1, 0, or X). The latches that have a ‘1’ or ‘0’ must be configured with their corresponding value each time that their associated latch bank is configured. The latches that have an ‘X’ are don’t cares and can be configured with any value.



[+] Feedback

**Table 2. Device Configuration and Control Latch Descriptions**

| Name | Signal Description |
|---|---|
| TXCKSELA<br>TXCKSELB<br>TXCKSELC<br>TXCKSELD | **Transmit Clock Select**. The initialization value of the TXCKSELx latch = 1. TXCKSELx selects the clock source used to write data into the Transmit Input Register. When TXCKSELx = 1, the associated input register TXDx[9:0] is clocked by REFCLKx↑. In this mode, the phase alignment buffer in the transmit path is bypassed. When TXCKSELx = 0, the associated TXCLKx↑ is used to clock in the input register TXDx[9:0]. |
| TXRATEA<br>TXRATEB<br>TXRATEC<br>TXRATED | **Transmit PLL Clock Rate Select**. The initialization value of the TXRATEx latch = 0. TXRATEx is used to select the clock multiplier for the Transmit PLL. When TXRATEx = 0, each transmit PLL multiples the associated REFCLKx± input by 10 to generate the serial bit-rate clock. When TXRATEx = 0, the TXCLKOx output clocks are full-rate clocks and follow the frequency and duty cycle of the associated REFCLKx± input. When TXRATEx = 1, each Transmit PLL multiplies the associated REFCLKx± input by 20 to generate the serial bit-rate clock. When TXRATEx = 1, the TXCLKOx output clocks are twice the frequency rate of the REFCLKx± input. When TXCLKSELx = 1 and TXRATEx = 1, the Transmit Data Inputs are captured using both the rising and falling edges of REFCLKx. TXRATEx = 1 and SPDSELx = LOW, is an invalid state and this combination is reserved. |
| TXBISTA<br>TXBISTB<br>TXBISTC<br>TXBISTD | **Transmit Bist Disabled**. The initialization value of the TXBISTx latch = 1. TXBISTx selects if the transmit BIST is disabled or enabled. When TXBISTx = 1, the transmit BIST function is disabled. When TXBISTx = 0, the transmit BIST function is enabled. |
| OE2A<br>OE2B<br>OE2C<br>OE2D | **Secondary Differential Serial Data Output Driver Enable**. The initialization value of the OE2x latch = 0. OE2x selects if the OUT2x± secondary differential output drivers are enabled or disabled. When OE2x = 1, the associated serial data output driver is enabled allowing data to be transmitted from the transmit shifter. When OE2x = 0, the associated serial data output driver is disabled. When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both serial drivers for a channel are in this disabled state, the associated internal logic for that channel is also powered down. A device reset (RESET sampled LOW) disables all output drivers. |
| OE1A<br>OE1B<br>OE1C<br>OE1D | **Primary Differential Serial Data Output Driver Enable**. The initialization value of the OE1x latch = 0. OE1x selects if the OUT1x± primary differential output drivers are enabled or disabled. When OE1x = 1, the associated serial data output driver is enabled allowing data to be transmitted from the transmit shifter. When OE1x = 0, the associated serial data output driver is disabled. When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both serial drivers for a channel are in this disabled state, the associated internal logic for that channel is also powered down. A device reset (RESET sampled LOW) disables all output drivers. |
| PABRSTA<br>PABRSTB<br>PABRSTC<br>PABRSTD | **Transmit Clock Phase Alignment Buffer Reset**. The initialization value of the PABRSTx latch = 1. The PABRSTx is used to re-center the Transmit Phase Align Buffer. When the configuration latch PABRSTx is written as a 0, the phase of the TXCLKx input clock relative to its associated REFCLKx+/- is initialized. PABRST is an asynchronous input, but is sampled by each TXCLKx↑ to synchronize it to the internal clock domain. PABRSTx is a self clearing latch. This eliminates the requirement of writing a 1 to complete the initialization of the Phase Alignment Buffer. |
| GLEN[11..0] | **Global Enable**. The initialization value of the GLENx latch = 1. The GLENx is used to reconfigure several channels simultaneously in applications where several channels may have the same configuration. When GLENx = 1 for a given address, that address is allowed to participate in a global configuration. When GLENx = 0 for a given address, that address is disabled from participating in a global configuration. |
| FGLEN[2..0] | **Force Global Enable**. The initialization value of the FGLENx latch is NA. The FGLENx latch forces a GLobal ENable no matter what the setting is on the GLENx latch. If FGLENx = 1 for the associated Global channel, FGLEN forces the global update of the target latch banks. |

**Device Configuration Strategy**

The following is a series of ordered events needed to load the configuration latches on a per channel basis:

1. Pulse $\overline{\text{RESET}}$ Low after device power-up. This operation resets all four channels.
2. Set the static latch banks for the target channel. May be performed using a global operation, if the application permits it.
3. Set the dynamic bank of latches for the target channel. Enable the output drivers. May be performed using a global operation, if the application permits it. [Required step.]
4. Reset the Phase Alignment Buffer for the target channel. May be performed using a global operation, if the application permits it. [Optional if phase align buffer is bypassed.]



[+] Feedback

**Table 3. Device Control Latch Configuration Table**

| ADDR | Channel | Type | DATA4 | DATA3 | DATA2 | DATA1 | DATA0 | Reset Value |
|---|---|---|---|---|---|---|---|---|
| 0 (0000b) | A | S | X | X | 0 | X | GLEN0 | 11111 |
| 1 (0001b) | A | S | X | 0 | TXCKSELA | TXRATEA | GLEN1 | 01101 |
| 2 (0010b) | A | D | TXBISTA | OE2A | OE1A | PABRSTA | GLEN2 | 10011 |
| 3 (0011b) | B | S | X | X | 0 | X | GLEN3 | 11111 |
| 4 (0100b) | B | S | X | 0 | TXCKSELB | TXRATEB | GLEN4 | 01101 |
| 5 (0101b) | B | D | TXBISTB | OE2B | OE1B | PABRSTB | GLEN5 | 10011 |
| 6 (0110b) | C | S | X | X | 0 | X | GLEN6 | 11111 |
| 7 (0111b) | C | S | X | 0 | TXCKSELC | TXRATEC | GLEN7 | 01101 |
| 8 (1000b) | C | D | TXBISTC | OE2C | OE1C | PABRSTC | GLEN8 | 10011 |
| 9 (1001b) | D | S | X | X | 0 | X | GLEN9 | 11111 |
| 10 (1010b) | D | S | X | 0 | TXCKSELD | TXRATED | GLEN10 | 01101 |
| 11 (1011b) | D | D | TXBISTD | OE2D | OE1D | PABRSTD | GLEN11 | 10011 |
| 12 (1100b) | GLOBAL | S | X | X | 0 | X | FGLEN0 | N/A |
| 13 (1101b) | GLOBAL | S | X | 0 | TXCKSELGL | TXRATEGL | FGLEN1 | N/A |
| 14 (1110b) | GLOBAL | D | TXBISTGL | OE2GL | OE1GL | PABRSTGL | FGLEN2 | N/A |
| 15 (1111b) | MASK | D | D4 | D3 | D2 | D1 | D0 | 11111 |

## JTAG Support

The CYV15G0403TB contains a JTAG port to allow system level diagnosis of device interconnect. Of the available JTAG modes, boundary scan, and bypass are supported. This capability is present only on the LVTTL inputs and outputs and the REFCLKx± clock input. The high-speed serial inputs and outputs are not part of the JTAG test chain.

### 3-Level Select Inputs

Each 3-Level select inputs reports as two bits in the scan register. These bits report the LOW, MID, and HIGH state of the associated input as 00, 10, and 11 respectively

### JTAG ID

The JTAG device ID for the CYV15G0403TB is ‘0C810069’x.



[+] Feedback

## Maximum Ratings

Above which the useful life may be impaired. User guidelines only, not tested

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +3.8V

DC Voltage Applied to LVTTL Outputs in High-Z State .....–0.5V to $V_{CC}$ + 0.5V

Output Current into LVTTL Outputs (LOW).....60 mA

DC Input Voltage.....–0.5V to $V_{CC}$ + 0.5V

Static Discharge Voltage.....> 2000 V (per MIL-STD-883, Method 3015)

Latch-up Current.....> 200 mA

### Power-up Requirements

The CYV15G0403TB requires one power-supply. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | +3.3V ±5% |

## CYV15G0403TB DC Electrical Characteristics

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| **LVTTL-compatible Outputs** | | | | | |
| $V_{OHT}$ | Output HIGH Voltage | $I_{OH}$ = –4 mA, $V_{CC}$ = Min. | 2.4 | | V |
| $V_{OLT}$ | Output LOW Voltage | $I_{OL}$ = 4 mA, $V_{CC}$ = Min. | | 0.4 | V |
| $I_{OST}$ | Output Short Circuit Current | $V_{OUT}$ = 0V[7], $V_{CC}$ = 3.3V | –20 | –100 | mA |
| $I_{OZL}$ | High-Z Output Leakage Current | $V_{OUT}$ = 0V, $V_{CC}$ | –20 | 20 | µA |
| **LVTTL-compatible Inputs** | | | | | |
| $V_{IHT}$ | Input HIGH Voltage | | 2.0 | $V_{CC}$ + 0.3 | V |
| $V_{ILT}$ | Input LOW Voltage | | –0.5 | 0.8 | V |
| $I_{IHT}$ | Input HIGH Current | REFCLKx Input, $V_{IN}$ = $V_{CC}$ | | 1.5 | mA |
| | | Other Inputs, $V_{IN}$ = $V_{CC}$ | | +40 | µA |
| $I_{ILT}$ | Input LOW Current | REFCLKx Input, $V_{IN}$ = 0.0V | | –1.5 | mA |
| | | Other Inputs, $V_{IN}$ = 0.0V | | –40 | µA |
| $I_{IHPDT}$ | Input HIGH Current with internal pull-down | $V_{IN}$ = $V_{CC}$ | | +200 | µA |
| $I_{ILPUT}$ | Input LOW Current with internal pull-up | $V_{IN}$ = 0.0V | | –200 | µA |
| **LVDIFF Inputs: REFCLKx±** | | | | | |
| $V_{DIFF}$[8] | Input Differential Voltage | | 400 | $V_{CC}$ | mV |
| $V_{IHHP}$ | Highest Input HIGH Voltage | | 1.2 | $V_{CC}$ | V |
| $V_{ILLP}$ | Lowest Input LOW voltage | | 0.0 | $V_{CC}$/2 | V |
| $V_{COMREF}$[9] | Common Mode Range | | 1.0 | $V_{CC}$ – 1.2V | V |
| **3-Level Inputs** | | | | | |
| $V_{IHH}$ | Three-Level Input HIGH Voltage | Min. ≤ $V_{CC}$ ≤ Max. | 0.87 * $V_{CC}$ | $V_{CC}$ | V |
| $V_{IMM}$ | Three-Level Input MID Voltage | Min. ≤ $V_{CC}$ ≤ Max. | 0.47 * $V_{CC}$ | 0.53 * $V_{CC}$ | V |
| $V_{ILL}$ | Three-Level Input LOW Voltage | Min. ≤ $V_{CC}$ ≤ Max. | 0.0 | 0.13 * $V_{CC}$ | V |
| $I_{IHH}$ | Input HIGH Current | $V_{IN}$ = $V_{CC}$ | | 200 | µA |
| $I_{IMM}$ | Input MID current | $V_{IN}$ = $V_{CC}$/2 | –50 | 50 | µA |
| $I_{ILL}$ | Input LOW current | $V_{IN}$ = GND | | –200 | µA |
| **Differential CML Serial Outputs: OUTA1±, OUTA2±, OUTB1±, OUTB2±, OUTC1±, OUTC2±, OUTD1±, OUTD2±** | | | | | |
| $V_{OHC}$ | Output HIGH Voltage ($V_{cc}$ Referenced) | 100Ω differential load | $V_{CC}$ – 0.5 | $V_{CC}$ – 0.2 | V |
| | | 150Ω differential load | $V_{CC}$ – 0.5 | $V_{CC}$ – 0.2 | V |
| $V_{OLC}$ | Output LOW Voltage ($V_{CC}$ Referenced) | 100Ω differential load | $V_{CC}$ – 1.4 | $V_{CC}$ – 0.7 | V |
| | | 150Ω differential load | $V_{CC}$ – 1.4 | $V_{CC}$ – 0.7 | V |

**Notes:**

7. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
8. This is the minimum difference in voltage between the true and complement inputs required to ensure detection of a logic-1 or logic-0. A logic-1 exists when the true (+) input is more positive than the complement (–) input. A logic-0 exists when the complement (–) input is more positive than true (+) input.
9. The common mode range defines the allowable range of REFCLKx+ and REFCLKx– when REFCLKx+ = REFCLKx–. This marks the zero-crossing between the true and complement inputs as the signal switches between a logic-1 and a logic-0.

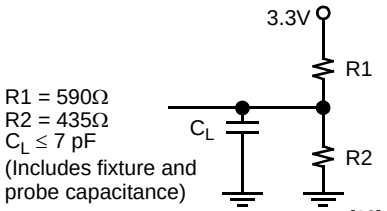


[+] Feedback

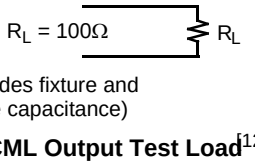
## CYV15G0403TB DC Electrical Characteristics (continued)

| Parameter | Description | Test Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{ODIF}$ | Output Differential Voltage \|(OUT+) – (OUT–)\| | 100Ω differential load | | 450 | 900 | mV |
| | | 150Ω differential load | | 560 | 1000 | mV |
| **Power Supply** | | | | **Typ.** | **Max.** | |
| $I_{CC}$ [10,11] | Max Power Supply Current | REFCLKx = MAX | Commercial | 640 | 820 | mA |
| $I_{CC}$ [10,11] | Typical Power Supply Current | REFCLKx = 125 MHz | Commercial | 610 | 790 | mA |

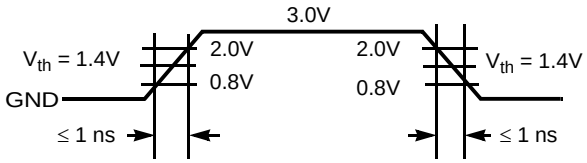
## AC Test Loads and Waveforms



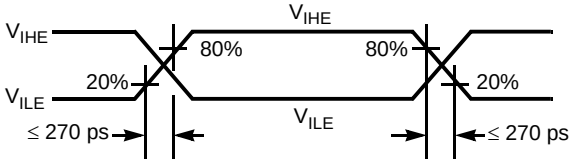

**(a) LVTTL Output Test Load**[12]




**(b) CML Output Test Load**[12]




**(c) LVTTL Input Test Waveform**[13]




**(d) CML/LVPECL Input Test Waveform**

## CYV15G0403TB AC Electrical Characteristics

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| **CYV15G0403TB Transmitter LVTTL Switching Characteristics** Over the Operating Range | | | | |
| $f_{TS}$ | TXCLKx Clock Cycle Frequency | 19.5 | 150 | MHz |
| $t_{TXCLK}$ | TXCLKx Period=1/$f_{TS}$ | 6.66 | 51.28 | ns |
| $t_{TXCLKH}$ [14] | TXCLKx HIGH Time | 2.2 | | ns |
| $t_{TXCLKL}$ [14] | TXCLKx LOW Time | 2.2 | | ns |
| $t_{TXCLKR}$ [14, 15, 16, 17] | TXCLKx Rise Time | 0.2 | 1.7 | ns |
| $t_{TXCLKF}$ [14, 15, 16, 17] | TXCLKx Fall Time | 0.2 | 1.7 | ns |
| $t_{TXDS}$ | Transmit Data Set-up Time to TXCLKx↑ (TXCKSELx = 0) | 2.2 | | ns |
| $t_{TXDH}$ | Transmit Data Hold Time from TXCLKx↑ (TXCKSELx = 0) | 1.0 | | ns |
| $f_{TOS}$ | TXCLKOx Clock Frequency = 1x or 2x REFCLKx Frequency | 19.5 | 150 | MHz |
| $t_{TXCLKO}$ | TXCLKOx Period = 1/$f_{TOS}$ | 6.66 | 51.28 | ns |
| $t_{TXCLKOD}$ | TXCLKO Duty Cycle centered at 60% HIGH time | –1.9 | 0 | ns |
| **CYV15G0403TB REFCLKx Switching Characteristics** Over the Operating Range | | | | |
| $f_{REF}$ | REFCLKx Clock Frequency | 19.5 | 150 | MHz |

**Notes:**

10. Maximum $I_{CC}$ is measured with $V_{CC}$ = MAX, $T_A$ = 25°C, with all channels and Serial Line Drivers enabled, sending a continuous alternating 01 pattern, and outputs unloaded.
11. Typical $I_{CC}$ is measured under similar conditions except with $V_{CC}$ = 3.3V, $T_A$ = 25°C, with all channels enabled and one Serial Line Driver per channel sending a continuous alternating 01 pattern. The redundant outputs on each channel are powered down.
12. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only.
13. The LVTTL switching threshold is 1.4V. All timing references are made relative to where the signal edges cross the threshold voltage.
14. Tested initially and after any design or process changes that may affect these parameters, but not 100% tested.
15. The ratio of rise time to falling time must not vary by greater than 2:1.
16. For a given operating frequency, neither rise or fall specification can be greater than 20% of the clock-cycle period or the data sheet maximum time.
17. All transmit AC timing parameters measured with 1 ns typical rise time and fall time.



[+] Feedback

## CYV15G0403TB AC Electrical Characteristics (continued)

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{REFCLK}$ | REFCLKx Period = $1/f_{REF}$ | 6.6 | 51.28 | ns |
| $t_{REFH}$ | REFCLKx HIGH Time (TXRATEx = 1)(Half Rate) | 5.9 | | ns |
| | REFCLKx HIGH Time (TXRATEx = 0)(Full Rate) | 2.9[14] | | ns |
| $t_{REFL}$ | REFCLKx LOW Time (TXRATEx = 1)(Half Rate) | 5.9 | | ns |
| | REFCLKx LOW Time (TXRATEx = 0)(Full Rate) | 2.9[14] | | ns |
| $t_{REFD}$[18] | REFCLKx Duty Cycle | 30 | 70 | % |
| $t_{REFR}$ [14, 15, 16, 17] | REFCLKx Rise Time (20%–80%) | | 2 | ns |
| $t_{REFF}$[14, 15, 16, 17] | REFCLKx Fall Time (20%–80%) | | 2 | ns |
| $t_{TREFDS}$ | Transmit Data Set-up Time to REFCLKx - Full Rate (TXRATEx = 0, TXCKSELx = 1) | 2.4 | | ns |
| | Transmit Data Set-up Time to REFCLKx - Half Rate (TXRATEx = 1, TXCKSELx = 1) | 2.3 | | ns |
| $t_{TREFDH}$ | Transmit Data Hold Time from REFCLKx - Full Rate (TXRATEx = 0, TXCKSELx = 1) | 1.0 | | ns |
| | Transmit Data Hold Time from REFCLKx - Half Rate (TXRATEx = 1, TXCKSELx = 1) | 1.6 | | ns |
| **CYV15G0403TB Bus Configuration Write Timing Characteristics** Over the Operating Range | | | | |
| $t_{DATAH}$ | Bus Configuration Data Hold | 0 | | ns |
| $t_{DATAS}$ | Bus Configuration Data Setup | 10 | | ns |
| $t_{WRENP}$ | Bus Configuration WREN Pulse Width | 10 | | ns |
| **CYV15G0403TB JTAG Test Clock Characteristics** Over the Operating Range | | | | |
| $f_{TCLK}$ | JTAG Test Clock Frequency | | 20 | MHz |
| $t_{TCLK}$ | JTAG Test Clock Period | 50 | | ns |
| **CYV15G0403TB Device RESET Characteristics** Over the Operating Range | | | | |
| $t_{RST}$ | Device RESET Pulse Width | 30 | | ns |

**CYV15G0403TB Transmit Serial Outputs and TX PLL Characteristics** Over the Operating Range

| Parameter | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_B$ | Bit Time | | 660 | 5128 | ps |
| $t_{RISE}$[14] | CML Output Rise Time 20–80% (CML Test Load) | SPDSELx = HIGH | 50 | 270 | ps |
| | | SPDSELx = MID | 100 | 500 | ps |
| | | SPDSELx =LOW | 180 | 1000 | ps |
| $t_{FALL}$[14] | CML Output Fall Time 80–20% (CML Test Load) | SPDSELx = HIGH | 50 | 270 | ps |
| | | SPDSELx = MID | 100 | 500 | ps |
| | | SPDSELx =LOW | 180 | 1000 | ps |

## PLL Characteristics

| Parameter | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **CYV15G0403TB Transmitter Output PLL Characteristics** | | | | | | |
| $t_{JTGENSD}$[14, 19] | Transmit Jitter Generation - SD Data Rate | REFCLKx = 27 MHz | | 200 | | ps |
| $t_{JTGENHD}$[14, 19] | Transmit Jitter Generation - HD Data Rate | REFCLKx = 148.5 MHz | | 76 | | ps |
| $t_{TXLOCK}$ | Transmit PLL lock to REFCLKx± | | | | 200 | µs |

**Notes:**

18. The duty cycle specification is a simultaneous condition with the $t_{REFH}$ and $t_{REFL}$ parameters. This means that at faster character rates the REFCLKx± duty cycle cannot be as large as 30%–70%.
19. While sending BIST data at the corresponding data rate, after 10,000 histogram hits on a digital sampling oscilloscope, time referenced to REFCLKx± input.

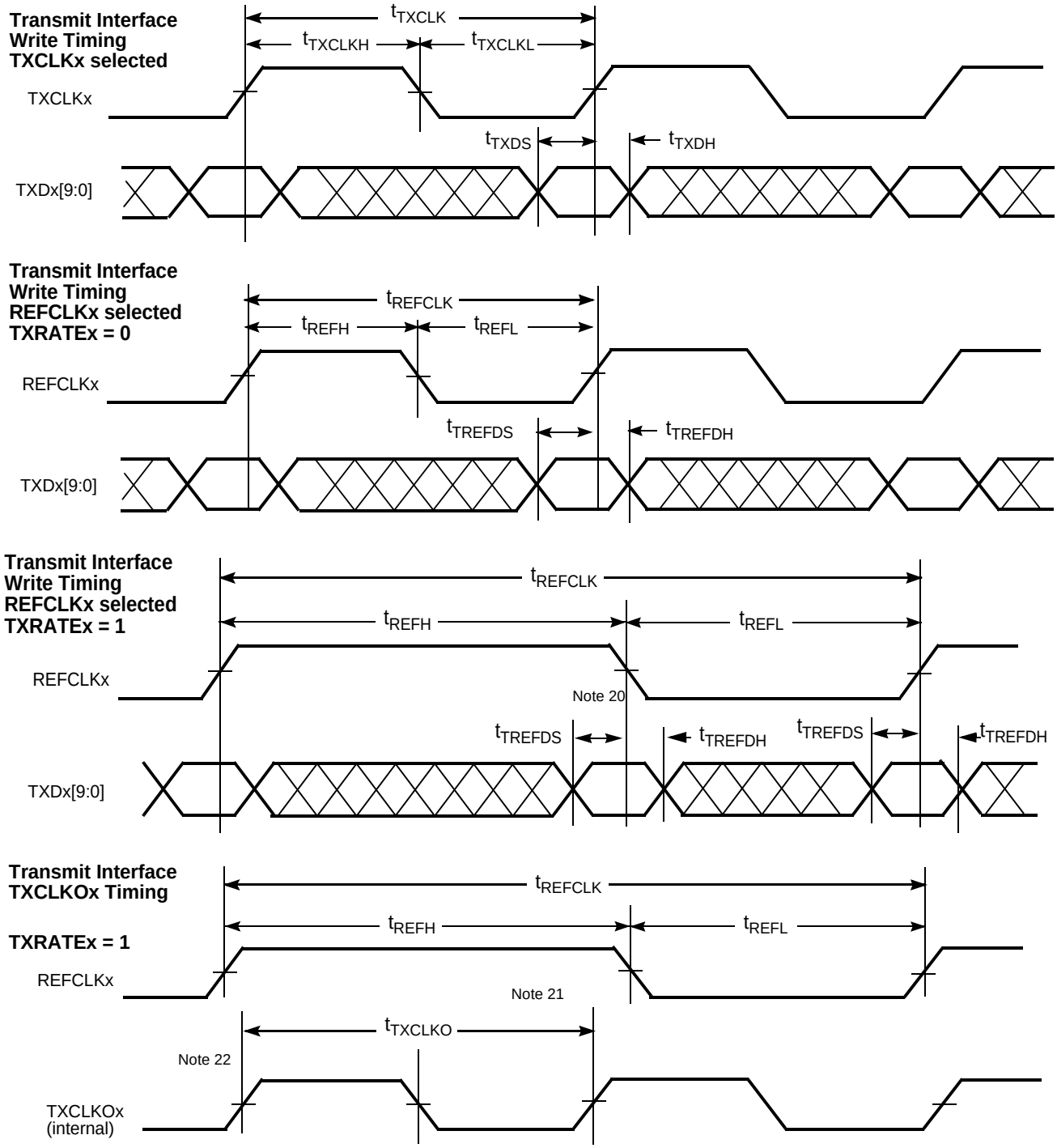


[+] Feedback

## Capacitance [14]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{INTTL}$ | TTL Input Capacitance | $T_A$ = 25°C, $f_0$ = 1 MHz, $V_{CC}$ = 3.3V | 7 | pF |
| $C_{INPECL}$ | PECL input Capacitance | $T_A$ = 25°C, $f_0$ = 1 MHz, $V_{CC}$ = 3.3V | 4 | pF |

## CYV15G0403TB HOTLink II Transmitter Switching Waveforms



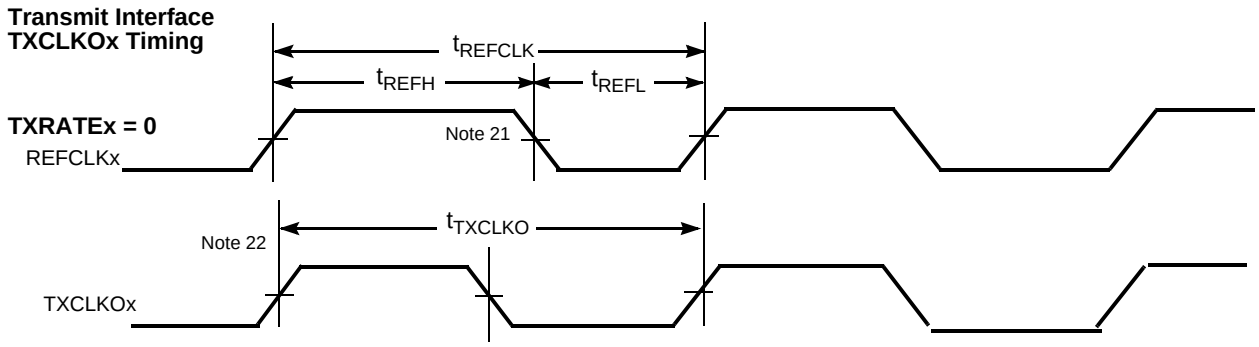

**Notes:**

20. When REFCLKx± is configured for half-rate operation (TXRATEx = 1) and data is captured using REFCLKx instead of a TXCLKx clock. Data is captured using both the rising and falling edges of REFCLKx.
21. The TXCLKOx output remains at the character rate regardless of the state of TXRATEx and does not follow the duty cycle of REFCLKx±.

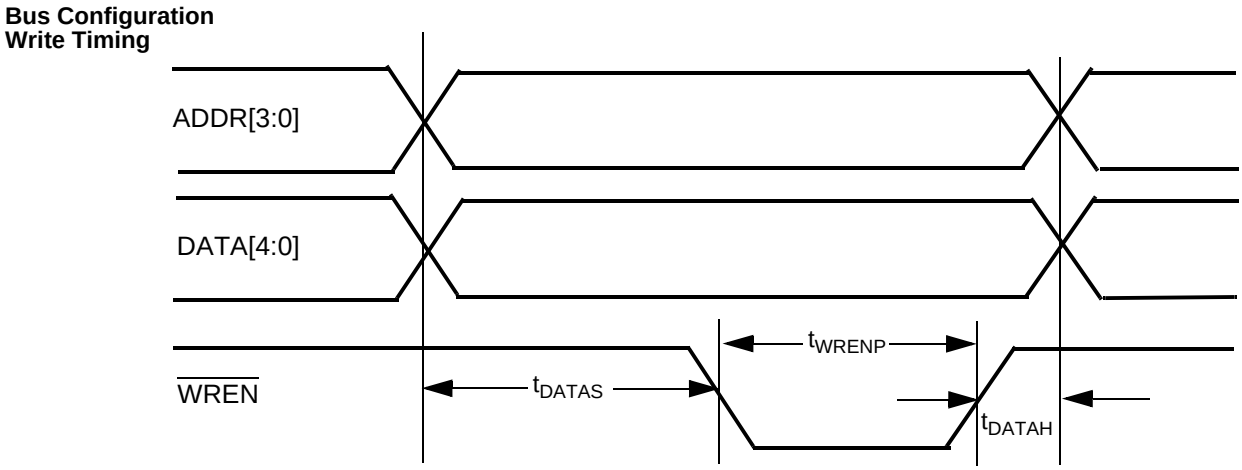


[+] Feedback

## CYV15G0403TB HOTLink II Transmitter Switching Waveforms (continued)




## CYV15G0403TB HOTLink II Bus Configuration Switching Waveforms




**Note:**
22. The rising edge of TXCLKOx output has no direct phase relationship to the REFCLKx± input.



[+] Feedback

**Table 4. Package Coordinate Signal Allocation**

| Ball ID | Signal Name | Signal Type | Ball ID | Signal Name | Signal Type | Ball ID | Signal Name | Signal Type |
|---|---|---|---|---|---|---|---|---|
| A01 | NC | NO CONNECT | C07 | NC | NO CONNECT | F17 | NC | NO CONNECT |
| A02 | OUTC1– | CML OUT | C08 | GND | GROUND | F18 | NC | NO CONNECT |
| A03 | NC | NO CONNECT | C09 | NC | NO CONNECT | F19 | TXCLKOB | LVTTL OUT |
| A04 | OUTC2– | CML OUT | C10 | NC | NO CONNECT | F20 | NC | NO CONNECT |
| A05 | VCC | POWER | C11 | DATA[3] | LVTTL IN PU | G01 | TXDC[7] | LVTTL IN |
| A06 | NC | NO CONNECT | C12 | DATA[1] | LVTTL IN PU | G02 | $\overline{\text{WREN}}$ | LVTTL IN PU |
| A07 | OUTD1– | CML OUT | C13 | GND | GROUND | G03 | TXDC[4] | LVTTL IN |
| A08 | GND | GROUND | C14 | NC | NO CONNECT | G04 | TXDC[1] | LVTTL IN |
| A09 | GND | GROUND | C15 | SPDSELD | 3-LEVEL SEL | G17 | SPDSELB | 3-LEVEL SEL |
| A10 | OUTD2– | CML OUT | C16 | VCC | POWER | G18 | NC | NO CONNECT |
| A11 | GND | GROUND | C17 | NC | NO CONNECT | G19 | SPDSELA | 3-LEVEL SEL |
| A12 | OUTA1– | CML OUT | C18 | $\overline{\text{TRST}}$ | LVTTL IN PU | G20 | NC | NO CONNECT |
| A13 | GND | GROUND | C19 | GND | GROUND | H01 | GND | GROUND |
| A14 | GND | GROUND | C20 | TDO | LVTTL 3-S OUT | H02 | GND | GROUND |
| A15 | OUTA2– | CML OUT | D01 | TCLK | LVTTL IN PD | H03 | GND | GROUND |
| A16 | VCC | POWER | D02 | $\overline{\text{RESET}}$ | LVTTL IN PU | H04 | GND | GROUND |
| A17 | VCC | POWER | D03 | VCC | POWER | H17 | GND | GROUND |
| A18 | OUTB1– | CML OUT | D04 | VCC | POWER | H18 | GND | GROUND |
| A19 | VCC | POWER | D05 | VCC | POWER | H19 | GND | GROUND |
| A20 | OUTB2– | CML OUT | D06 | VCC | POWER | H20 | GND | GROUND |
| B01 | VCC | POWER | D07 | SPDSELC | 3-LEVEL SEL | J01 | TXDC[9] | LVTTL IN |
| B02 | OUTC1+ | CML OUT | D08 | GND | GROUND | J02 | TXDC[5] | LVTTL IN |
| B03 | VCC | POWER | D09 | GND | GROUND | J03 | TXDC[2] | LVTTL IN |
| B04 | OUTC2+ | CML OUT | D10 | DATA[4] | LVTTL IN PU | J04 | TXDC[3] | LVTTL IN |
| B05 | VCC | POWER | D11 | DATA[2] | LVTTL IN PU | J17 | NC | NO CONNECT |
| B06 | VCC | POWER | D12 | DATA[0] | LVTTL IN PU | J18 | NC | NO CONNECT |
| B07 | OUTD1+ | CML OUT | D13 | GND | GROUND | J19 | NC | NO CONNECT |
| B08 | GND | GROUND | D14 | GND | GROUND | J20 | NC | NO CONNECT |
| B09 | NC | NO CONNECT | D15 | NC | NO CONNECT | K01 | NC | NO CONNECT |
| B10 | OUTD2+ | CML OUT | D16 | VCC | POWER | K02 | REFCLKC– | PECL IN |
| B11 | NC | NO CONNECT | D17 | NC | NO CONNECT | K03 | TXDC[8] | LVTTL IN |
| B12 | OUTA1+ | CML OUT | D18 | NC | NO CONNECT | K04 | TXCLKC | LVTTL IN PD |
| B13 | GND | GROUND | D19 | SCANEN2 | LVTTL IN PD | K17 | NC | NO CONNECT |
| B14 | NC | NO CONNECT | D20 | TMEN3 | LVTTL IN PD | K18 | NC | NO CONNECT |
| B15 | OUTA2+ | CML OUT | E01 | VCC | POWER | K19 | NC | NO CONNECT |
| B16 | VCC | POWER | E02 | VCC | POWER | K20 | NC | NO CONNECT |
| B17 | NC | NO CONNECT | E03 | VCC | POWER | L01 | NC | NO CONNECT |
| B18 | OUTB1+ | CML OUT | E04 | VCC | POWER | L02 | REFCLKC+ | PECL IN |
| B19 | NC | NO CONNECT | E17 | VCC | POWER | L03 | NC | NO CONNECT |
| B20 | OUTB2+ | CML OUT | E18 | VCC | POWER | L04 | TXDC[6] | LVTTL IN |
| C01 | TDI | LVTTL IN PU | E19 | VCC | POWER | L17 | NC | NO CONNECT |
| C02 | TMS | LVTTL IN PU | E20 | VCC | POWER | L18 | NC | NO CONNECT |
| C03 | VCC | POWER | F01 | NC | NO CONNECT | L19 | NC | NO CONNECT |



[+] Feedback

**Table 4. Package Coordinate Signal Allocation** (continued)

| Ball ID | Signal Name | Signal Type |
|---|---|---|
| C04 | VCC | POWER |
| C05 | VCC | POWER |
| C06 | NC | NO CONNECT |
| M03 | NC | NO CONNECT |
| M04 | TXERRC | LVTTL OUT |
| M17 | REFCLKB+ | PECL IN |
| M18 | REFCLKB– | PECL IN |
| M19 | TXERRB | LVTTL OUT |
| M20 | TXCLKB | LVTTL IN PD |
| N01 | GND | GROUND |
| N02 | GND | GROUND |
| N03 | GND | GROUND |
| N04 | GND | GROUND |
| N17 | GND | GROUND |
| N18 | GND | GROUND |
| N19 | GND | GROUND |
| N20 | GND | GROUND |
| P01 | NC | NO CONNECT |
| P02 | NC | NO CONNECT |
| P03 | NC | NO CONNECT |
| P04 | NC | NO CONNECT |
| P17 | TXDB[5] | LVTTL IN |
| P18 | TXDB[4] | LVTTL IN |
| P19 | TXDB[3] | LVTTL IN |
| P20 | TXDB[2] | LVTTL IN |
| R01 | NC | NO CONNECT |
| R02 | TXCLKOC | LVTTL OUT |
| R03 | NC | NO CONNECT |
| R04 | NC | NO CONNECT |
| R17 | TXDB[1] | LVTTL IN |
| R18 | TXDB[0] | LVTTL IN |
| R19 | TXDB[9] | LVTTL IN |
| R20 | TXDB[7] | LVTTL IN |
| T01 | VCC | POWER |
| T02 | VCC | POWER |
| T03 | VCC | POWER |
| T04 | VCC | POWER |
| T17 | VCC | POWER |
| T18 | VCC | POWER |
| T19 | VCC | POWER |
| T20 | VCC | POWER |
| U01 | TXDD[0] | LVTTL IN |
| U02 | TXDD[1] | LVTTL IN |
| F02 | NC | NO CONNECT |
| F03 | TXDC[0] | LVTTL IN |
| F04 | NC | NO CONNECT |
| U03 | TXDD[2] | LVTTL IN |
| U04 | TXDD[9] | LVTTL IN |
| U05 | VCC | POWER |
| U06 | NC | NO CONNECT |
| U07 | NC | NO CONNECT |
| U08 | GND | GROUND |
| U09 | TXDA[9] | LVTTL IN |
| U10 | ADDR [0] | LVTTL IN PU |
| U11 | REFCLKD– | PECL IN |
| U12 | TXDA[1] | LVTTL IN |
| U13 | GND | GROUND |
| U14 | TXDA[4] | LVTTL IN |
| U15 | TXDA[8] | LVTTL IN |
| U16 | VCC | POWER |
| U17 | NC | NO CONNECT |
| U18 | TXDB[8] | LVTTL IN |
| U19 | NC | NO CONNECT |
| U20 | NC | NO CONNECT |
| V01 | TXDD[3] | LVTTL IN |
| V02 | TXDD[4] | LVTTL IN |
| V03 | TXDD[8] | LVTTL IN |
| V04 | NC | NO CONNECT |
| V05 | VCC | POWER |
| V06 | NC | NO CONNECT |
| V07 | NC | NO CONNECT |
| V08 | GND | GROUND |
| V09 | NC | NO CONNECT |
| V10 | ADDR [2] | LVTTL IN PU |
| V11 | REFCLKD+ | PECL IN |
| V12 | TXCLKOA | LVTTL OUT |
| V13 | GND | GROUND |
| V14 | TXDA[3] | LVTTL IN |
| V15 | TXDA[7] | LVTTL IN |
| V16 | VCC | POWER |
| V17 | NC | NO CONNECT |
| V18 | NC | NO CONNECT |
| V19 | NC | NO CONNECT |
| V20 | NC | NO CONNECT |
| W01 | TXDD[5] | LVTTL IN |
| W02 | TXDD[7] | LVTTL IN |
| L20 | TXDB[6] | LVTTL IN |
| M01 | NC | NO CONNECT |
| M02 | NC | NO CONNECT |
| W03 | NC | NO CONNECT |
| W04 | NC | NO CONNECT |
| W05 | VCC | POWER |
| W06 | NC | NO CONNECT |
| W07 | NC | NO CONNECT |
| W08 | GND | GROUND |
| W09 | ADDR [3] | LVTTL IN PU |
| W10 | ADDR [1] | LVTTL IN PU |
| W11 | NC | NO CONNECT |
| W12 | TXERRA | LVTTL OUT |
| W13 | GND | GROUND |
| W14 | TXDA[2] | LVTTL IN |
| W15 | TXDA[6] | LVTTL IN |
| W16 | VCC | POWER |
| W17 | NC | NO CONNECT |
| W18 | REFCLKA+ | PECL IN |
| W19 | NC | NO CONNECT |
| W20 | NC | NO CONNECT |
| Y01 | TXDD[6] | LVTTL IN |
| Y02 | TXCLKD | LVTTL IN PD |
| Y03 | NC | NO CONNECT |
| Y04 | NC | NO CONNECT |
| Y05 | VCC | POWER |
| Y06 | NC | NO CONNECT |
| Y07 | NC | NO CONNECT |
| Y08 | GND | GROUND |
| Y09 | TXCLKOD | LVTTL OUT |
| Y10 | NC | NO CONNECT |
| Y11 | TXCLKA | LVTTL IN PD |
| Y12 | NC | NO CONNECT |
| Y13 | GND | GROUND |
| Y14 | TXDA[0] | LVTTL IN |
| Y15 | TXDA[5] | LVTTL IN |
| Y16 | VCC | POWER |
| Y17 | TXERRD | LVTTL OUT |
| Y18 | REFCLKA– | PECL IN |
| Y19 | NC | NO CONNECT |
| Y20 | NC | NO CONNECT |



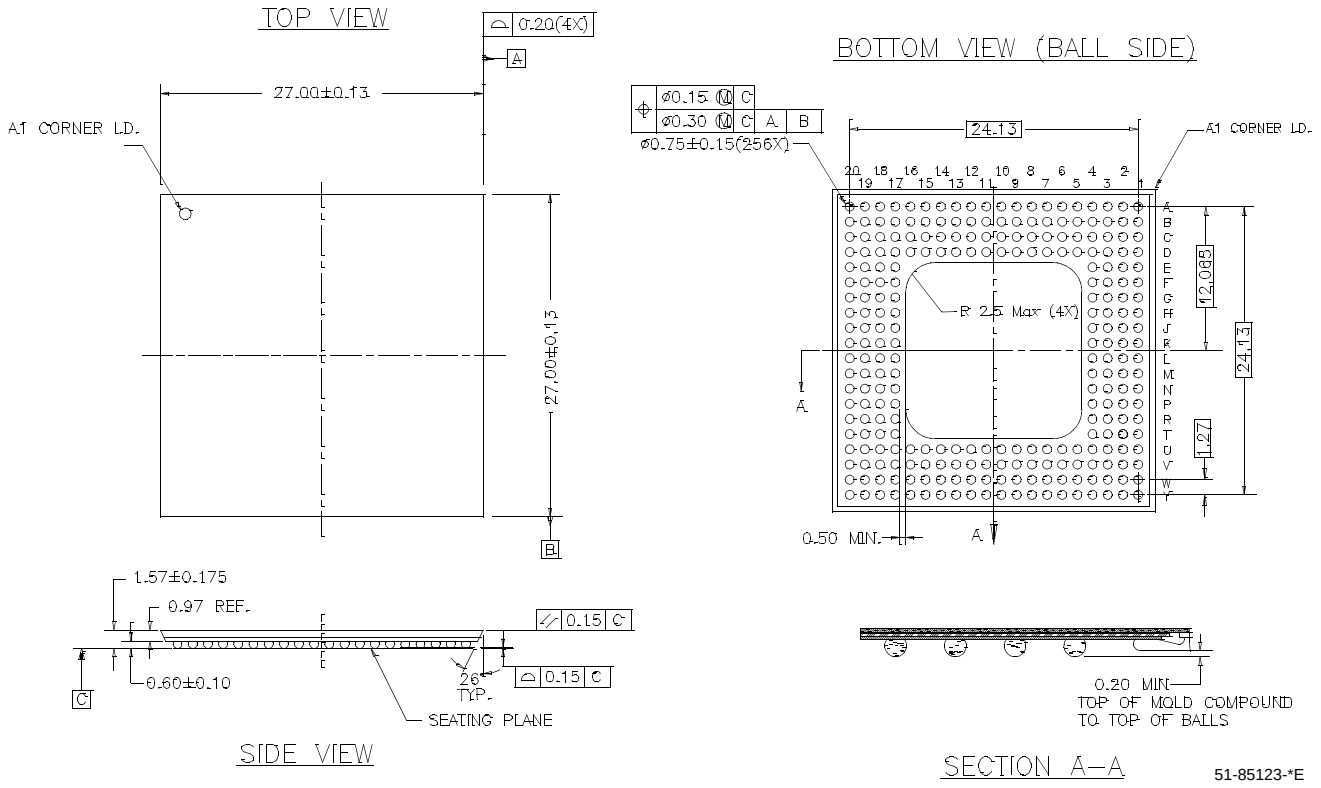
[+] Feedback

## Ordering Information

| Speed | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| Standard | CYV15G0403TB-BGC | BL256 | 256-Ball Thermally Enhanced Ball Grid Array | Commercial |
| Standard | CYV15G0403TB-BGXC | BL256 | Pb-Free 256-Ball Thermally Enhanced Ball Grid Array | Commercial |

## Package Diagram

**256-Lead L2 Ball Grid Array (27 x 27 x 1.57 mm) BL256**




HOTLink is a registered trademark and HOTLink II is a trademark of Cypress Semiconductor. All product and company names mentioned in this document may be the trademarks of their respective holders.



© Cypress Semiconductor Corporation, 2005. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges

[+] Feedback

## Document History Page

| Document Title: CYV15G0403TB Independent Clock Quad HOTLink II™ Serializer<br>Document Number: 38-02104 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **ISSUE DATE** | **ORIG. OF CHANGE** | **DESCRIPTION OF CHANGE** |
| ** | 246850 | See ECN | FRE | New Data Sheet |
| *A | 338721 | See ECN | SUA | Added Pb-Free package option availability |
| *B | 384307 | See ECN | AGT | Revised setup and hold times ($t_{TXDH}$, $t_{TREFDS}$, $t_{TREFDH}$) |



[+] Feedback

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

**Данный компонент на территории Российской Федерации**

**Вы можете приобрести в компании MosChip.**

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

**Офис по работе с юридическими лицами:**

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9