



#### 100V N-CHANNEL ENHANCEMENT MODE MOSFET

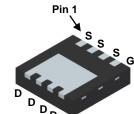
## **Product Summary**

BV <sub>DSS</sub>	R <sub>DS(ON)</sub> Max	I <sub>D</sub> Max T <sub>C</sub> = +25°C
100V	15mΩ @ V <sub>GS</sub> = 10V	34A
	19.5mΩ @ V <sub>GS</sub> = 6V	32A

# **Description and Applications**

This new generation N-Channel Enhancement Mode MOSFET is designed to minimize  $R_{DS(ON)}$  and yet maintain superior switching performance. This device is ideal for use in Notebook battery power management and Load switch.

- Backlighting
- Power Management Functions
- **DC-DC Converters**







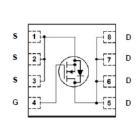
**Bottom View** 

# **Features and Benefits**

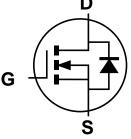
- 100% Unclamped Inductive Switch (UIS) Test in Production
- High Conversion Efficiency
- Low R<sub>DS(ON)</sub> Minimizes On State Losses
- Low Input Capacitance
- Fast Switching Speed
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)

#### **Mechanical Data**

- Case: V-DFN3333-8 (Type B)
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Below Diagram Terminals: Finish -NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 @4
- Weight: 0.03 grams (Approximate)



Top View Internal Schematic



**Equivalent Circuit** 

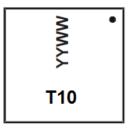
#### **Ordering Information** (Note 4)

Part Number	Case	Packaging
DMT10H015LCG-7	V-DFN3333-8 (Type B)	2,000/Tape & Reel
DMT10H015LCG-13	V-DFN3333-8 (Type B)	3,000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

# **Marking Information**



T10 = Product Type Marking Code YYWW = Date Code Marking YY = Year (ex: 18 = 2018)WW = Week (01 to 53)



## **Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V <sub>DSS</sub>	100	V
Gate-Source Voltage			V <sub>GSS</sub>	±20	V
Continuous Drain Current, V <sub>GS</sub> = 10V (Note 6)	Steady State	$T_A = +25^{\circ}C$ $T_A = +70^{\circ}C$	I <sub>D</sub>	9.4 7.5	А
Continuous Drain Current, V <sub>GS</sub> = 10V	Steady State	$T_{C} = +25^{\circ}C$ $T_{C} = +100^{\circ}C$	I <sub>D</sub>	34 21	А
Maximum Continuous Body Diode Forward Current (Note 6)			I <sub>S</sub>	1.6	Α
Pulsed Drain Current (10μs Pulse, Duty Cycle = 1%)			I <sub>DM</sub>	54	Α
Avalanche Current, L = 3mH (Note 8)			I <sub>AS</sub>	7.5	Α
Avalanche Energy, L = 3mH (Note 8)			E <sub>AS</sub>	85	mJ

# Thermal Characteristics (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P <sub>D</sub>	1	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	118	°C/W
Total Power Dissipation (Note 6)	P <sub>D</sub>	2.1	W
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	59	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.5	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

# Electrical Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

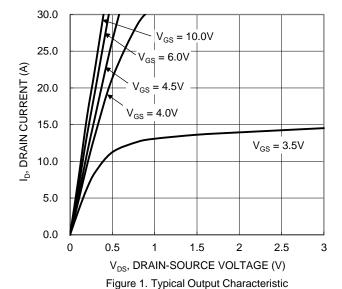
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	100	1	_	V	$V_{GS} = 0V$ , $I_D = 1mA$	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>			1	μΑ	$V_{DS} = 80V, V_{GS} = 0V$	
Gate-Source Leakage	I <sub>GSS</sub>	_	_	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	1.4	2	3.5	٧	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	
			12.1	15	mΩ	$V_{GS} = 10V, I_D = 20A$	
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	l	15	19.5	11122	$V_{GS} = 6V, I_D = 20A$	
	, ,	_	18.9	26	mΩ	$V_{GS} = 4.5V, I_D = 5A$	
Diode Forward Voltage	V <sub>SD</sub>	_	0.9	1.3	V	$V_{GS} = 0V, I_{S} = 20A$	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	Ciss	_	1871	_		$V_{DS} = 50V$ , $V_{GS} = 0V$ f = 1MHz	
Output Capacitance	Coss	l	261	_	pF		
Reverse Transfer Capacitance	Crss		6.9	_			
Gate Resistance	Rg	_	0.75	_	Ω	$V_{DS} = 0V$ , $V_{GS} = 0V$ , $f = 1MHz$	
Total Gate Charge	Qg	_	33.3	_		V 50V L 40A	
Gate-Source Charge	Qgs	_	6.9	_	$N_{DD} = 50V, I_{D} = 10A,$		
Gate-Drain Charge	$Q_{gd}$	_	5.1	_		$V_{GS} = 10V$	
Turn-On Delay Time	t <sub>D(ON)</sub>	_	6.5	_			
Turn-On Rise Time	t <sub>R</sub>	_	7	_		$V_{DD} = 50V, V_{GS} = 10V,$	
Turn-Off Delay Time	t <sub>D(OFF)</sub>	_	19.7	_	ns	$I_D = 10A$ , $R_g = 6\Omega$	
Turn-Off Fall Time	t <sub>F</sub>		8.1	_			
Reverse Recovery Time	t <sub>RR</sub>	1	37.9	_	ns	1 100 di/dt 1000/up	
Reverse Recovery Charge	Q <sub>RR</sub>	_	51.9	_	nC	$I_F = 10A$ , di/dt = 100A/ $\mu$ s	

5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout. 6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

7. Short duration pulse test used to minimize self-heating effect.

8. Guaranteed by design. Not subject to product testing.





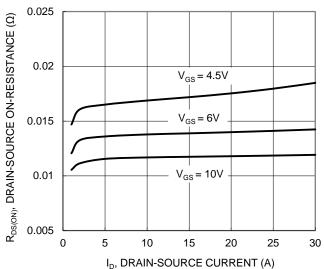


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

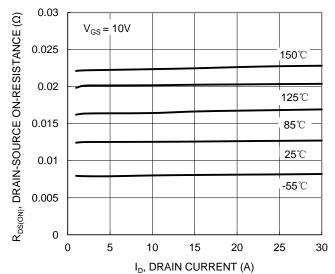
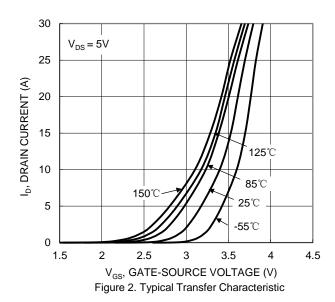


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature



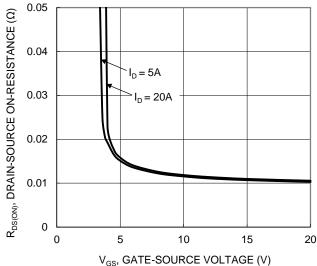


Figure 4. Typical Transfer Characteristic

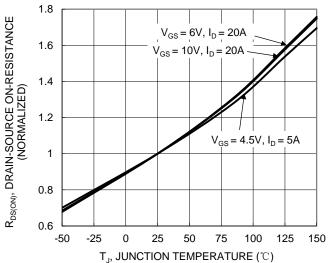


Figure 6. On-Resistance Variation with Junction Temperature



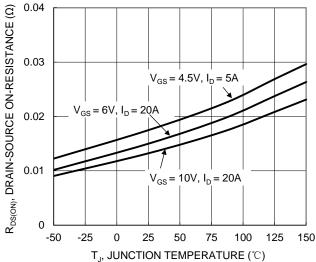
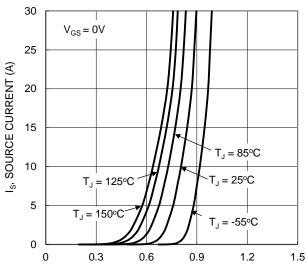


Figure 7. On-Resistance Variation with Junction
Temperature



V<sub>SD</sub>, SOURCE-DRAIN VOLTAGE (V) Figure 9. Diode Forward Voltage vs. Current

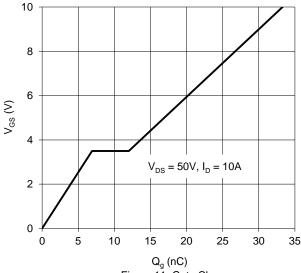


Figure 11. Gate Charge

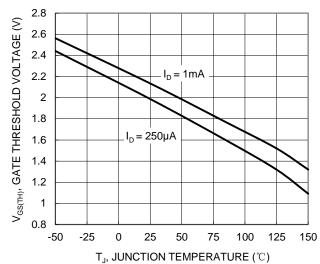


Figure 8. Gate Threshold Variation vs. Junction Temperature

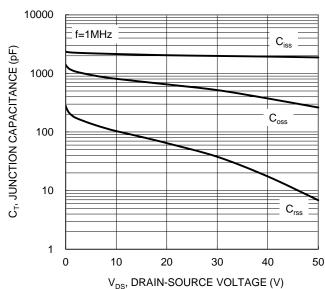


Figure 10. Typical Junction Capacitance

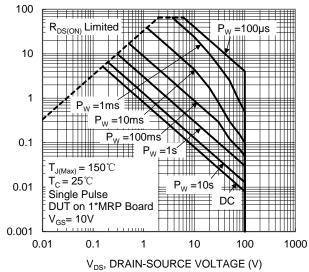


Figure 12. SOA, Safe Operation Area

ID, DRAIN CURRENT (A)



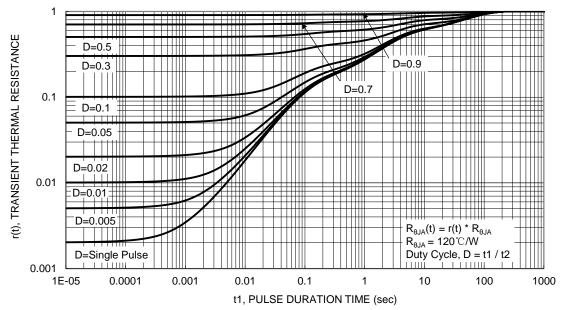
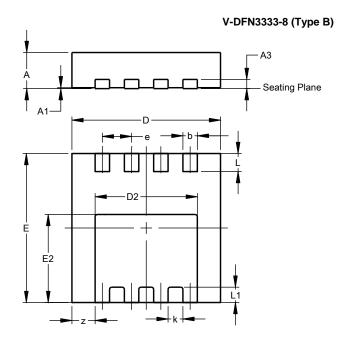


Figure 13. Transient Thermal Resistance



# **Package Outline Dimensions**

Please see http://www.diodes.com/package-outlines.html for the latest version.

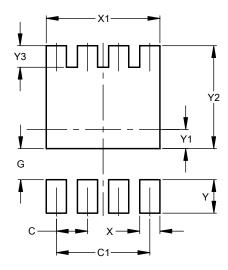


V-DFN3333-8					
(Type B)					
Dim	Min	Max	Тур		
Α	0.75	0.85	0.80		
A1	0.00	0.05	0.02		
A3			0.203		
b	0.27	0.37	0.32		
D	3.25	3.35	3.30		
D2	2.17	2.37	2.27		
Е	3.25	3.35	3.30		
E2	1.85	2.05	1.95		
е			0.65		
k	-		0.33		
L	0.35	0.45	0.40		
L1	-		0.34		
Z	-		0.515		
All Dimensions in mm					

# **Suggested Pad Layout**

Please see http://www.diodes.com/package-outlines.html for the latest version.

# V-DFN3333-8 (Type B)



Dimensions	Value (in mm)		
C	0.650		
C1	1.950		
G	0.650		
X	0.420		
X1	2.370		
Υ	0.700		
Y1	0.400		
Y2	2.150		
Y3 0.450			



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