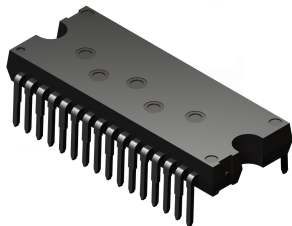
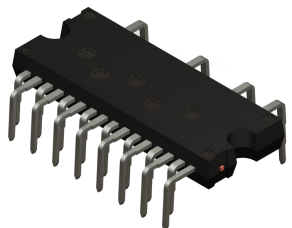


## SLLIMM™-nano 2<sup>nd</sup> series IPM, 3-phase inverter, 3 A, 1.6 Ω max., 600 V, N-channel MDmesh™ DM2 Power MOSFET



N2DIP-26L type L



N2DIP-26L type Z

### Features

- IPM 3 A, 600 V,  $R_{DS(on)} = 1.6 \Omega$ , 3-phase Power MOSFET inverter bridge including control ICs for gate driving
- Optimized for low electromagnetic interference
- 3.3 V, 5 V, 15 V CMOS/TTL input comparators with hysteresis and pull-down/pull-up resistors
- Undervoltage lockout
- Internal bootstrap diode
- Interlocking function
- Shutdown function
- Comparator for fault protection against overtemperature and overcurrent
- Op-amp for advanced current sensing
- Optimized pinout for easy board layout
- NTC for temperature control (UL 1434 CA 2 and 4)
- Isolation ratings of 1500 Vrms/min.
- UL recognition: UL 1557 file, E81734

### Applications

- 3-phase inverters for motor drives
- Dish washers, refrigerator compressors, heating systems, air-conditioning fans, draining and recirculation pumps

### Description

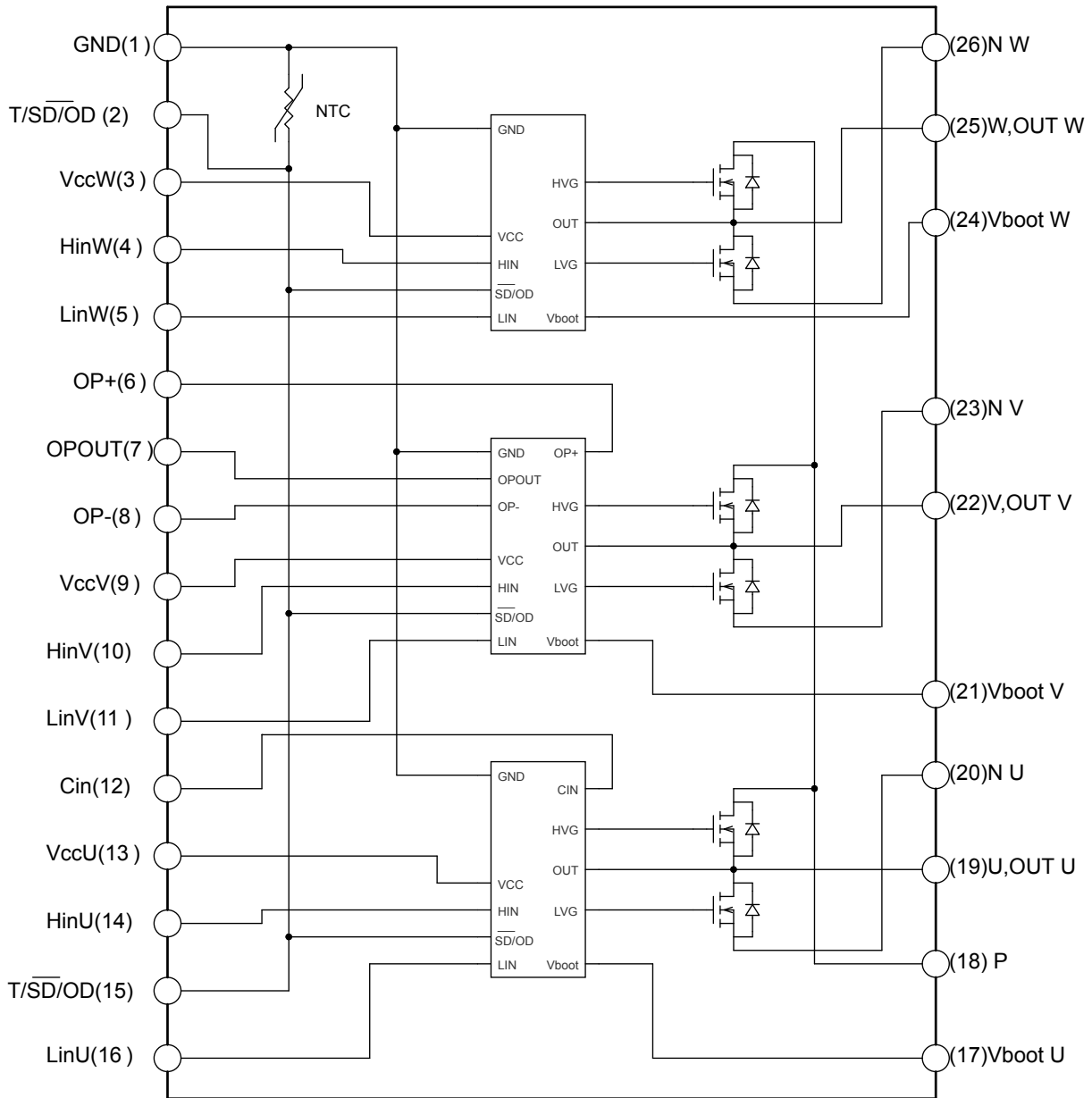
This SLLIMM (small low-loss intelligent molded module)-nano provides a compact, high-performance AC motor drive in a simple, rugged design. It is composed of six N-channel MDmesh™ DM2 Power MOSFETs with intrinsic fast-recovery diode and three half-bridge HVICs for gate driving, providing low electromagnetic interference (EMI) characteristics with optimized switching speed. The package is designed to allow a better and easy screw on heatsink. It is optimized for thermal performance and compactness in built-in motor applications, or other low-power applications where assembly space is limited. This IPM includes an operational amplifier, completely uncommitted, and a comparator that can be used to design a fast and efficient protection circuit. SLLIMM™ is a trademark of STMicroelectronics.



Product status links	
	<a href="#">STIPQ3M60T-HL</a>
	<a href="#">STIPQ3M60T-HZ</a>
Product summary	
STIPQ3M60T-HL	
Order code	STIPQ3M60T-HL
Marking	IPQ3M60T-HL
Package	N2DIP-26L type L
Packing	Tube
STIPQ3M60T-HZ	
Order code	STIPQ3M60T-HZ
Marking	IPQ3M60T-HZ
Package	N2DIP-26L type Z
Packing	Tube

# 1 Internal schematic diagram and pin configuration

Figure 1. Internal schematic diagram



GIPD120120170806SA

**Table 1. Pin description**

Pin	Symbol	Description
1	GND	Ground
2	T/SD/OD	NTC thermistor terminal/shutdown logic input (active low)/open-drain (comparator output)
3	V <sub>CC</sub> W	Low-voltage power supply W phase
4	HIN W	High-side logic input for W phase
5	LIN W	Low-side logic input for W phase
6	OP+	Op-amp non-inverting input
7	OP <sub>OUT</sub>	Op-amp output
8	OP-	Op-amp inverting input
9	V <sub>CC</sub> V	Low-voltage power supply V phase
10	HIN V	High-side logic input for V phase
11	LIN V	Low-side logic input for V phase
12	CIN	Comparator input
13	V <sub>CC</sub> U	Low-voltage power supply for V phase
14	HIN U	High-side logic input for V phase
15	T/SD/OD	NTC thermistor terminal/shutdown logic input (active low)/open-drain (comparator output)
16	LIN U	Low-side logic input for U phase
17	V <sub>boot</sub> U	Bootstrap voltage for U phase
18	P	Positive DC input
19	U, OUT <sub>U</sub>	U phase output
20	N <sub>U</sub>	Negative DC input for U phase
21	V <sub>boot</sub> V	Bootstrap voltage for V phase
22	V, OUT <sub>V</sub>	V phase output
23	N <sub>V</sub>	Negative DC input for V phase
24	V <sub>boot</sub> W	Bootstrap voltage for W phase
25	W, OUT <sub>W</sub>	W phase output
26	N <sub>W</sub>	Negative DC input for W phase

## 2 Electrical ratings

$T_J = 25\text{ °C}$  unless otherwise specified

### 2.1 Absolute maximum ratings

**Table 2. Inverter part**

Symbol	Parameter	Value	Unit
$V_{DSS}$	MOSFET blocking voltage (or drain-source voltage) for each MOSFET ( $V_{IN}^{(1)} = 0$ )	600	V
$\pm I_D$	Continuous drain current for each MOSFET ( $T_C = 25\text{ °C}$ )	3	A
$\pm I_{DP}^{(2)}$	Peak drain current for each MOSFET (less than 1 ms)	6	A
$P_{TOT}$	Total power dissipation for each MOSFET ( $T_C = 25\text{ °C}$ )	11.7	W

1. Applied among  $HINx$ ,  $LINx$  and  $GND$  for  $x = U, V, W$

2. Pulse width limited by maximum junction temperature

**Table 3. Control part**

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Low voltage power supply	-0.3	21	V
$V_{boot}$	Bootstrap voltage	-0.3	620	V
$V_{OUT}$	Output voltage applied among $OUT_U$ , $OUT_V$ , $OUT_W - GND$	$V_{boot} - 21$	$V_{boot} + 0.3$	V
$V_{CIN}$	Comparator input voltage	-0.3	$V_{CC} + 0.3$	V
$V_{op+}$	Op-amp non-inverting input	-0.3	$V_{CC} + 0.3$	V
$V_{op-}$	Op-amp inverting input	-0.3	$V_{CC} + 0.3$	V
$V_{IN}$	Logic input voltage applied among $HINx$ , $LINx$ and $GND$	-0.3	15	V
$V_{T/SD/OD}$	Open-drain voltage	-0.3	15	V
$dV_{out}/dt$	Allowed output slew rate		50	V/ns

**Table 4. Total system**

Symbol	Parameter	Value	Unit
$V_{ISO}$	Isolation withstand voltage applied on each pin and heatsink plate (AC voltage, $t = 60\text{ s}$ )	1500	Vrms
$T_J$	Power chip operating junction temperature range	-40 to 150	°C
$T_C$	Module case operation temperature range	-40 to 125	°C

## 2.2 Thermal data

**Table 5. Thermal data**

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Thermal resistance junction-case single MOSFET	10.7	°C/W

### 3 Electrical characteristics

$T_J = 25\text{ °C}$  unless otherwise noted.

#### 3.1 Inverter part

**Table 6. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{DSS}$	Zero-gate voltage drain current	$V_{DS} = 600\text{ V}$ , $V_{CC} = 15\text{ V}$ , $V_{boot} = 15\text{ V}$			1	mA
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{CC} = V_{boot} = 15\text{ V}$ , $V_{IN}^{(1)} = 0\text{ V}$ , $I_D = 1\text{ mA}$	600			V
$R_{DS(on)}$	Static drain source turn-on resistance	$V_{CC} = V_{boot} = 15\text{ V}$ , $V_{IN}^{(1)} = 0\text{ to }5\text{ V}$ , $I_D = 1.5\text{ A}$		1.35	1.6	$\Omega$
$V_{SD}$	Drain-source diode forward voltage	$V_{IN}^{(1)} = 0$ "logic state", $I_D = 3\text{ A}$		1.4	1.9	V

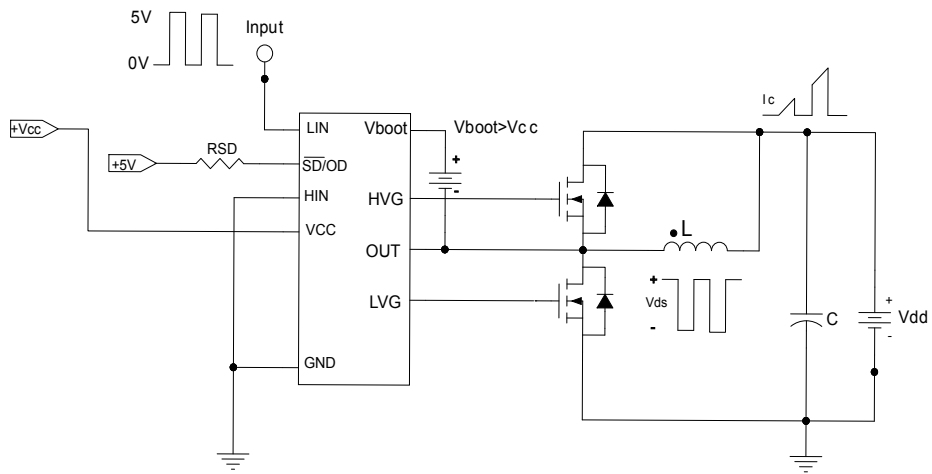
1. Applied among  $HINx$ ,  $LINx$  and  $GND$  for  $x = U, V, W$ .

**Table 7. Inductive load switching time and energy**

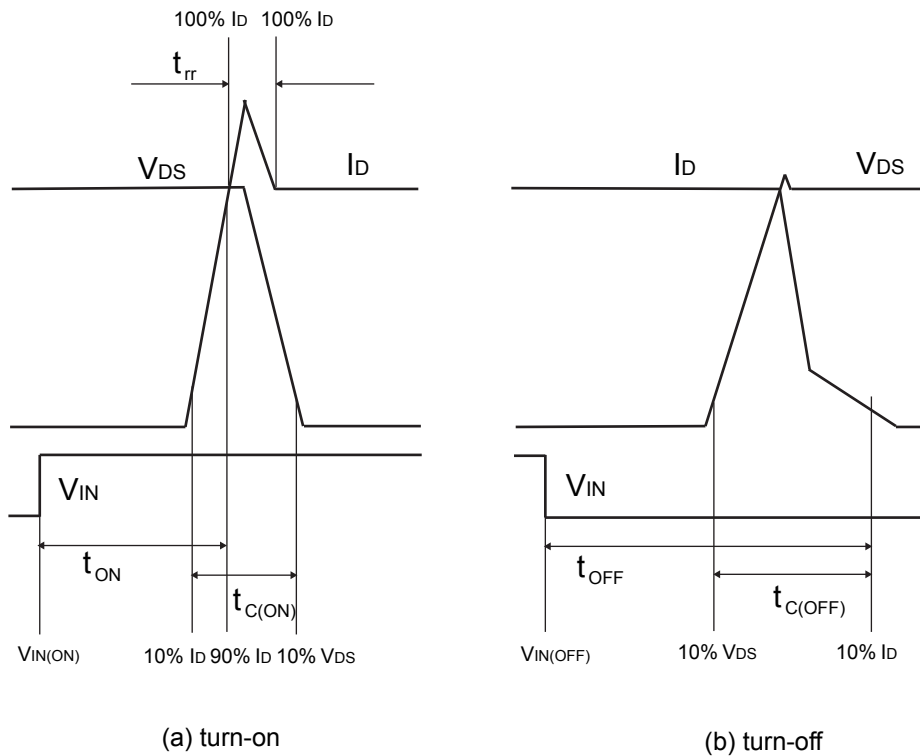
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{on}^{(1)}$	Turn-on time	$V_{DD} = 300\text{ V}$ , $V_{CC} = V_{boot} = 15\text{ V}$ , $V_{IN}^{(2)} = 0\text{ to }5\text{ V}$ , $I_C = 1.5\text{ A}$ (see <a href="#">Figure 3. Switching time definition</a> )	-	220	-	ns
$t_{c(on)}^{(1)}$	Crossover time (on)		-	72	-	
$t_{off}^{(1)}$	Turn-off time		-	225	-	
$t_{c(off)}^{(1)}$	Crossover time (off)		-	29	-	
$t_{rr}$	Reverse recovery time		-	79	-	$\mu\text{J}$
$E_{on}$	Turn-on switching energy		-	47	-	
$E_{off}$	Turn-off switching energy		-	3.9	-	

1.  $t_{ON}$  and  $t_{OFF}$  include the propagation delay time of the internal drive.  $t_{C(ON)}$  and  $t_{C(OFF)}$  are the switching times of the MOSFET itself under the internally given gate driving conditions.

2. Applied among  $HINx$ ,  $LINx$  and  $GND$  for  $x = U, V, W$ .

**Figure 2. Switching time test circuit**


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**Figure 3. Switching time definition**


AM09223V2

Figure 3. Switching time definition refers to HIN, LIN inputs (active high).

### 3.2 Control part

**Table 8. Low-voltage power supply ( $V_{CC} = 15\text{ V}$  unless otherwise specified)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC\_hys}$	$V_{CC}$ UV hysteresis		1.2	1.5	1.8	V
$V_{CC\_thON}$	$V_{CC}$ UV turn-ON threshold		11.5	12	12.5	V
$V_{CC\_thOFF}$	$V_{CC}$ UV turn-OFF threshold		10	10.5	11	V
$I_{qccu}$	Undervoltage quiescent supply current	$V_{CC} = 10\text{ V}$ , $T/\overline{SD}/OD = 5\text{ V}$ , $LIN = HIN = CIN = 0\text{ V}$			150	$\mu\text{A}$
$I_{qcc}$	Quiescent current	$V_{CC} = 10\text{ V}$ , $T/\overline{SD}/OD = 5\text{ V}$ , $LIN = HIN = CIN = 0\text{ V}$			1	mA
$V_{ref}$	Internal comparator (CIN) reference voltage		0.51	0.54	0.56	V

**Table 9. Bootstrapped voltage ( $V_{CC} = 15\text{ V}$  unless otherwise specified)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BS\_hys}$	$V_{BS}$ UV hysteresis		1.2	1.5	1.8	V
$V_{BS\_thON}$	$V_{BS}$ UV turn-ON threshold		11.1	11.5	12.1	V
$V_{BS\_thOFF}$	$V_{BS}$ UV turn-OFF threshold		9.8	10	10.6	V
$I_{QBSU}$	Undervoltage $V_{BS}$ quiescent current	$V_{BS} < 9\text{ V}$ , $T/\overline{SD}/OD = 5\text{ V}$ , $LIN = 0\text{ V}$ and $HIN = 5\text{ V}$ , $CIN = 0$		70	110	$\mu\text{A}$
$I_{QBS}$	$V_{BS}$ quiescent current	$V_{BS} = 15\text{ V}$ , $T/\overline{SD}/OD = 5\text{ V}$ , $LIN = 0\text{ V}$ and $HIN = 5\text{ V}$ , $CIN = 0$		200	300	$\mu\text{A}$
$R_{DS(on)}$	Bootstrap driver on-resistance	LVG ON		120		$\Omega$

**Table 10. Logic inputs ( $V_{CC} = 15\text{ V}$  unless otherwise specified)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{il}$	Low logic level voltage				0.8	V
$V_{ih}$	High logic level voltage		2.25			V
$I_{HINh}$	HIN logic "1" input bias current	$HIN = 15\text{ V}$	20	40	100	$\mu\text{A}$
$I_{HINl}$	HIN logic "0" input bias current	$HIN = 0\text{ V}$			1	$\mu\text{A}$
$I_{LINl}$	LIN logic "1" input bias current	$LIN = 15\text{ V}$	20	40	100	$\mu\text{A}$
$I_{LINh}$	LIN logic "0" input bias current	$LIN = 0\text{ V}$			1	$\mu\text{A}$
$I_{SDh}$	$\overline{SD}$ logic "0" input bias current	$\overline{SD} = 15\text{ V}$	220	295	370	$\mu\text{A}$
$I_{SDl}$	$\overline{SD}$ logic "1" input bias current	$\overline{SD} = 0\text{ V}$			3	$\mu\text{A}$
Dt	Dead time	See <a href="#">Section 3.3 Waveform definitions</a>		180		ns



**Table 11. Op-amp characteristics ( $V_{CC} = 15\text{ V}$  unless otherwise specified)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{io}$	Input offset voltage	$V_{ic} = 0\text{ V}$ , $V_o = 7.5\text{ V}$			6	mV
$I_{io}$	Input offset current	$V_{ic} = 0\text{ V}$ , $V_o = 7.5\text{ V}$		4	40	nA
$I_{ib}$	Input bias current <sup>(1)</sup>			100	200	nA
$V_{OL}$	Low-level output voltage	$R_L = 10\text{ k}\Omega$ to $V_{CC}$		75	150	mV
$V_{OH}$	High-level output voltage	$R_L = 10\text{ k}\Omega$ to GND	14	14.7		V
$I_o$	Output short-circuit current	Source, $V_{id} = +1\text{ V}$ , $V_o = 0\text{ V}$	16	30		mA
		Sink, $V_{id} = -1\text{ V}$ , $V_o = V_{CC}$	50	80		mA
SR	Slew rate	$V_i = 1$ to $4\text{ V}$ , $C_L = 100\text{ pF}$ , unity gain	2.5	3.8		V/ $\mu\text{s}$
GBWP	Gain bandwidth product	$V_o = 7.5\text{ V}$	8	12		MHz
$A_{vd}$	Large signal voltage gain	$R_L = 2\text{ k}\Omega$	70	85		dB
SVR	Supply voltage rejection ratio	vs. $V_{CC}$	60	75		dB
CMRR	Common mode rejection ratio		55	70		dB

1. The direction of the input current is out of the IC.

**Table 12. Sense comparator characteristics ( $V_{CC} = 15\text{ V}$  unless otherwise specified)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{ib}$	Input bias current	$V_{CIN} = 1\text{ V}$			1	$\mu\text{A}$
$V_{od}$	Open-drain low level output voltage	$I_{od} = 3\text{ mA}$			0.5	V
$R_{ON\_OD}$	Open-drain low level output resistance	$I_{od} = 3\text{ mA}$		166		$\Omega$
$R_{PD\_SD}$	$\overline{SD}$ pull-down resistor <sup>(1)</sup>			125		k $\Omega$
$t_{d\_comp}$	Comparator delay	T/ $\overline{SD}$ /OD pulled to $5\text{ V}$ through $100\text{ k}\Omega$ resistor		90	130	ns
SR	Slew rate	$C_L = 180\text{ pF}$ , $R_{pu} = 5\text{ k}\Omega$		60		V/ $\mu\text{s}$
$t_{sd}$	Shutdown to high-/low-side driver propagation delay	$V_{OUT} = 0$ , $V_{boot} = V_{CC}$ , $V_{IN} = 0$ to $3.3\text{ V}$	50	125	200	ns
$t_{isd}$	Comparator triggering to high-/low-side driver turn-off propagation delay	Measured applying a voltage step from $0\text{ V}$ to $3.3\text{ V}$ to pin CIN	50	200	250	

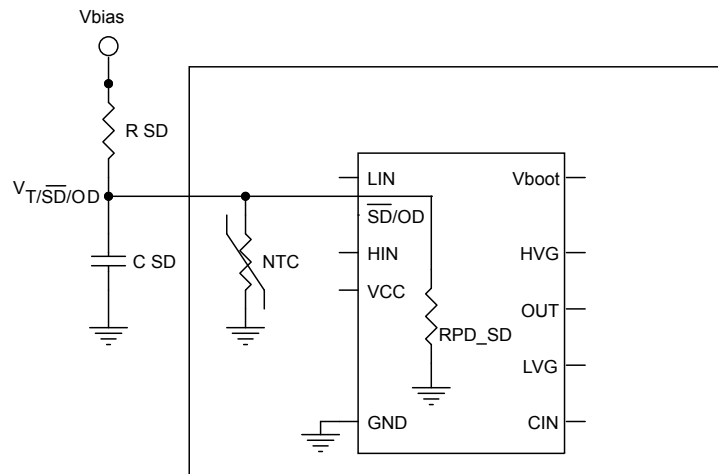
1. Equivalent values are the result of the resistances of three drivers in parallel.

**Table 13. Truth table**

Conditions	Logic input ( $V_I$ )			Output	
	$\overline{T/SD/OD}$	LIN	HIN	LVG	HVG
Shutdown enable half-bridge tri-state	L	X <sup>(1)</sup>	X <sup>(1)</sup>	L	L
Interlocking half-bridge tri-state	H	H	H	L	L
0 "logic state" half-bridge tri-state	H	L	L	L	L
1 "logic state" low-side direct driving	H	H	L	H	L
1 "logic state" high-side direct driving	H	L	H	L	H

1. X: do not care.

### 3.2.1 NTC thermistor

**Figure 4. Internal structure of  $\overline{SD}$  and NTC**


$R_{PD\_SD}$ : equivalent value as result of resistances of three drivers in parallel.

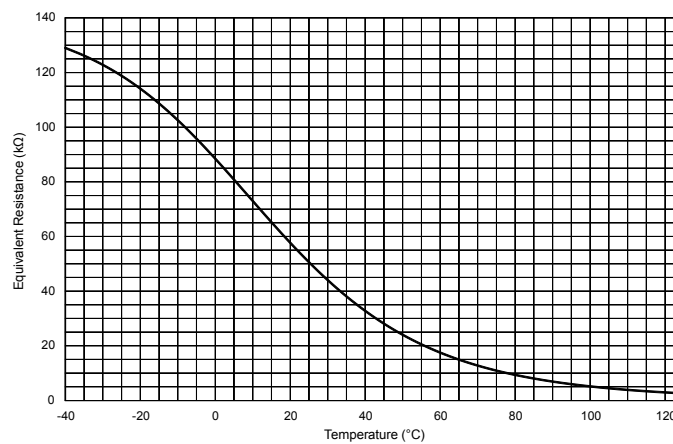
**Figure 5. Equivalent resistance ( $NTC//R_{PD\_SD}$ )**


Figure 6. Equivalent resistance (NTC//R<sub>PD\_SD</sub>) zoom

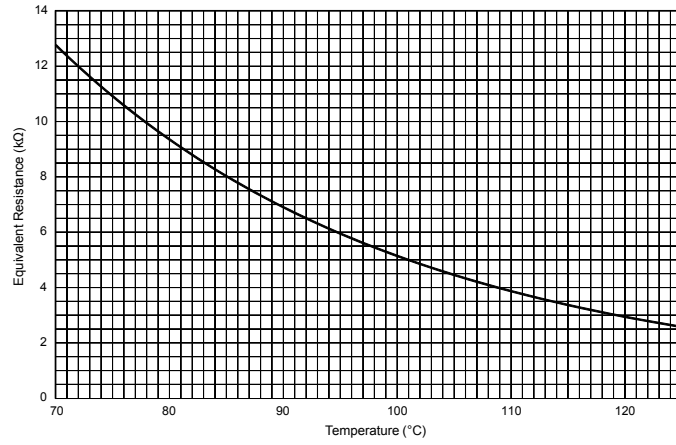
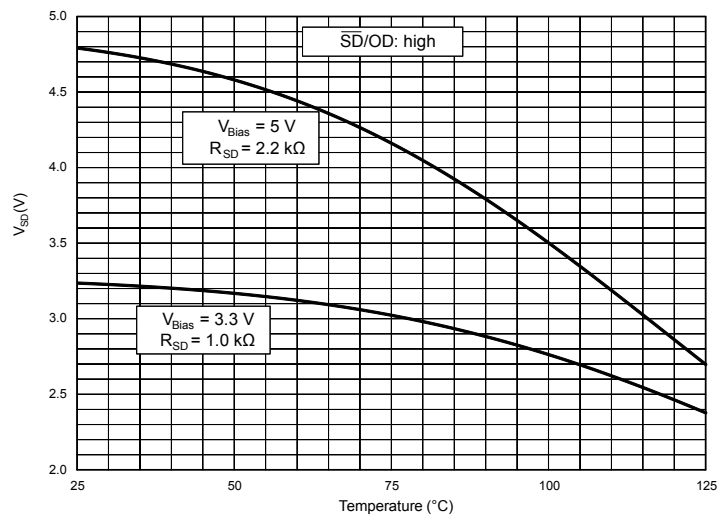
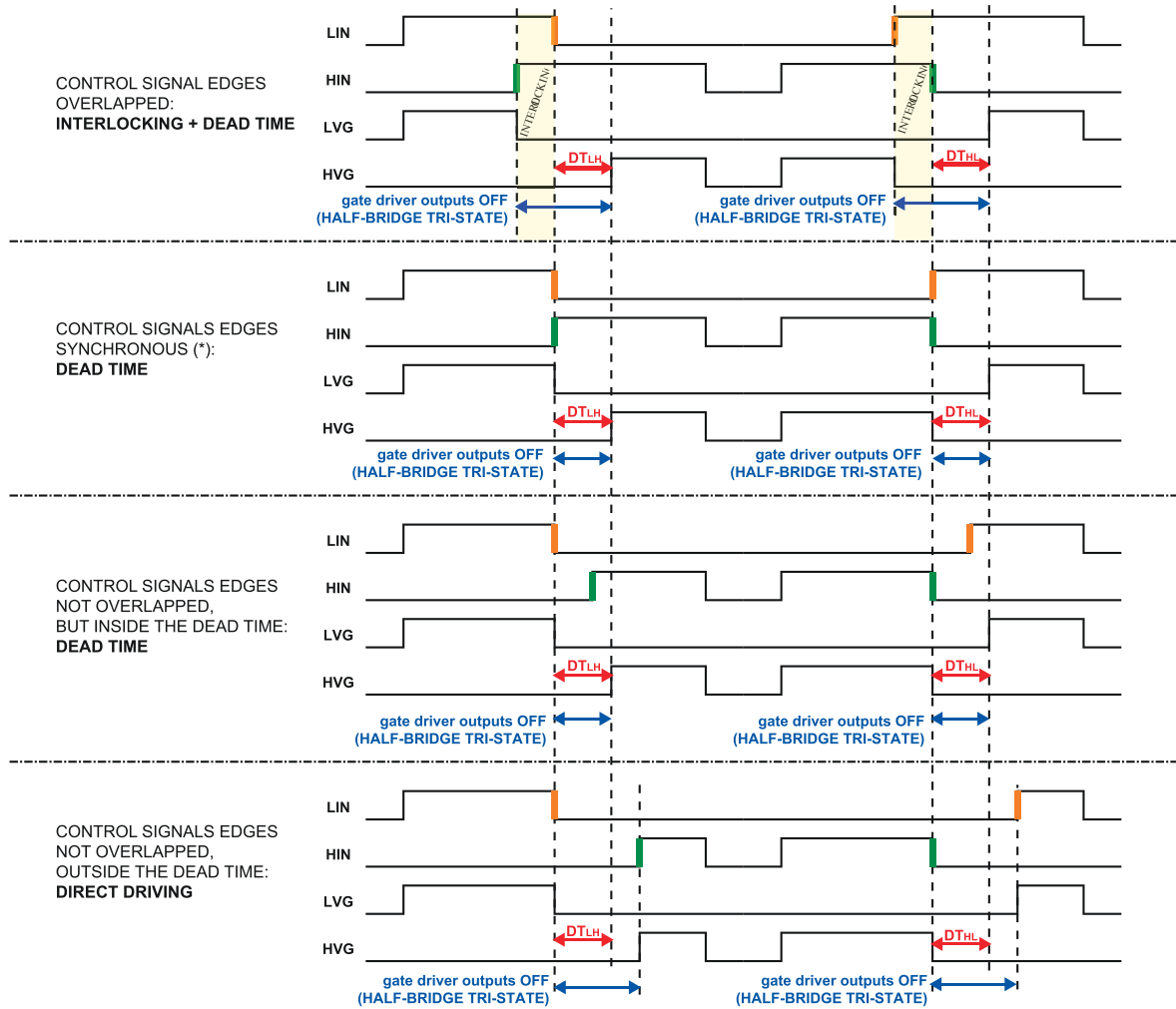


Figure 7. Voltage of T/SD/OD pin according to NTC temperature



### 3.3 Waveform definitions

**Figure 8. Dead time and interlocking waveform definitions**


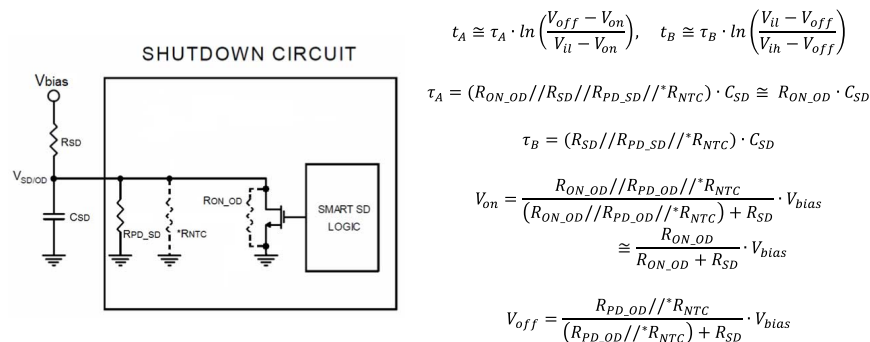
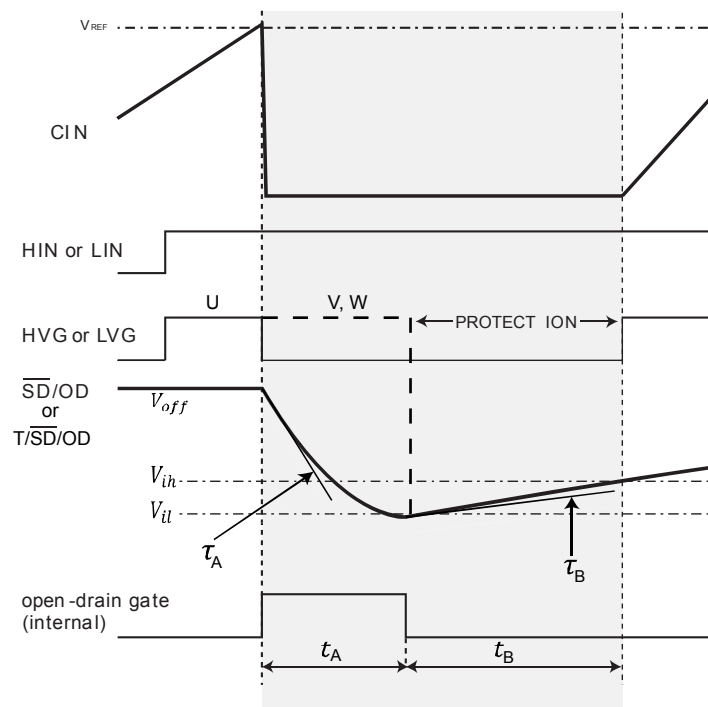
## 4 Shutdown function

The device is equipped with three half-bridge IC gate drivers and integrates a comparator for fault detection. The comparator has an internal voltage reference  $V_{REF}$  connected to the inverting input, while the non-inverting input pin (CIN) can be connected to an external shunt resistor for current monitoring.

Since the comparator is embedded in the U IC gate driver, in case of fault it disables directly the U outputs, whereas the shutdown of V and W IC gate drivers depends on the RC value of the external SD circuitry, which fixes the disabling time.

For an effective design of the shutdown circuit, please refer to Application note AN4966.

**Figure 9. Shutdown timing waveforms**



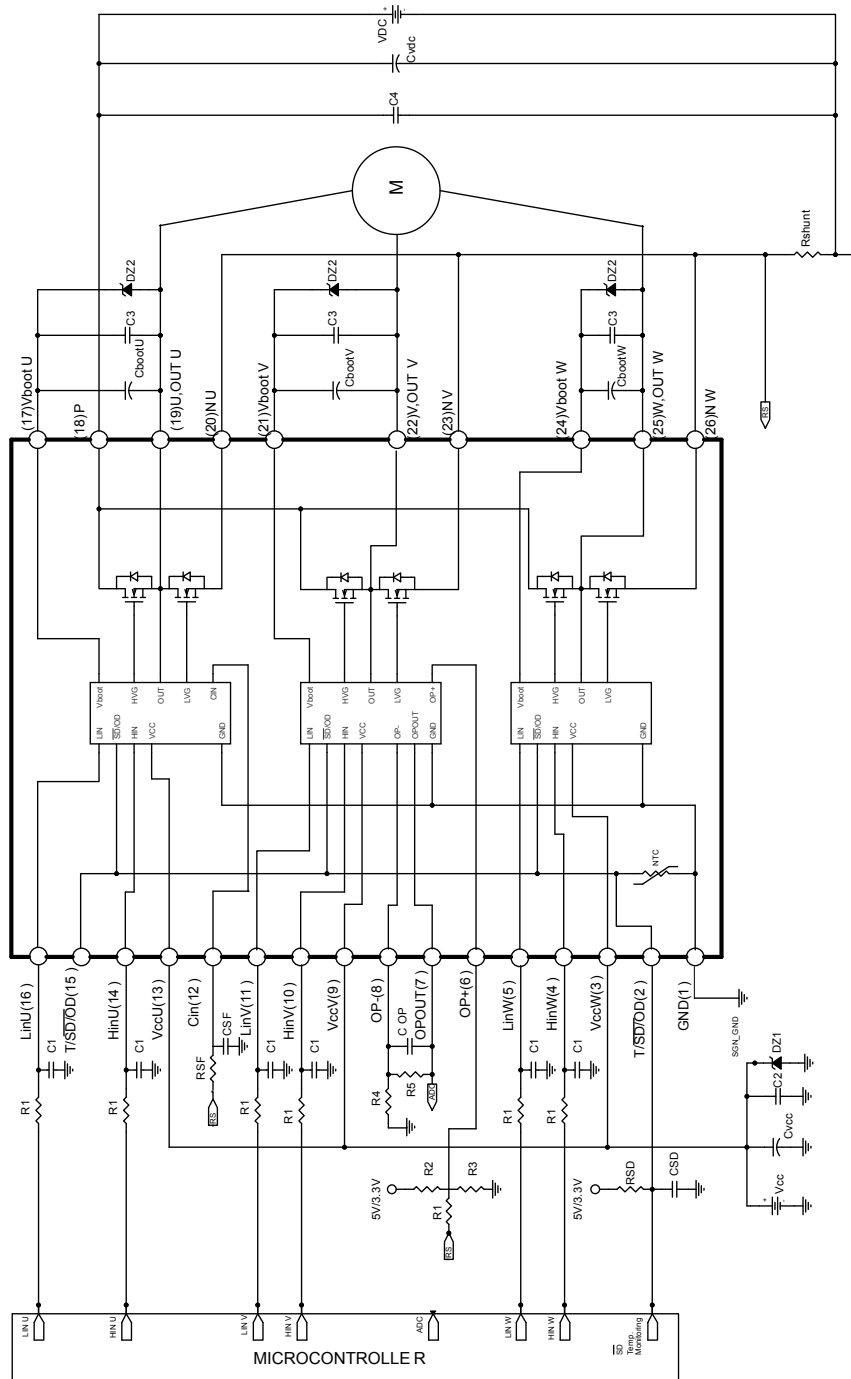
$R_{SD}$  and  $C_{SD}$  external circuitry must be designed to ensure  $V_{on} < V_{il}$  &  $V_{off} > V_{ih}$

Please refer to AN4966 for further details.

\*  $R_{NTC}$  to be considered only when the NTC is internally connected to the T/SD/OD pin.

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## 5 Application circuit example

**Figure 10. Application circuit example**


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Application designers are free to use a different scheme according to the specifications of the device.

## 5.1 Guidelines

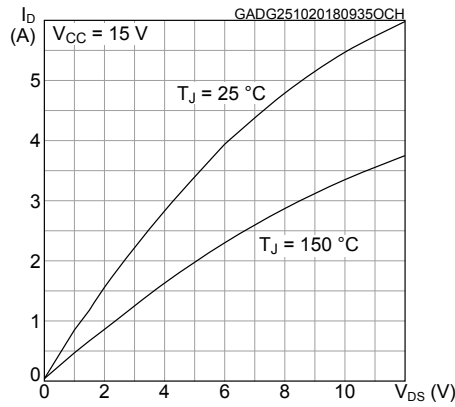
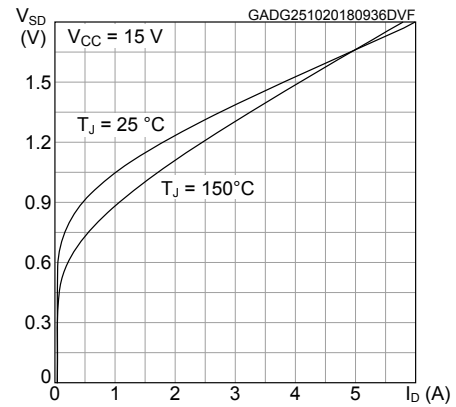
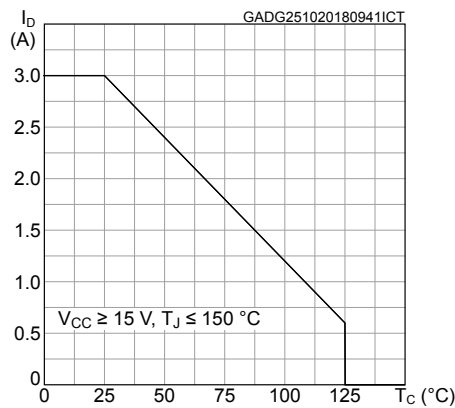
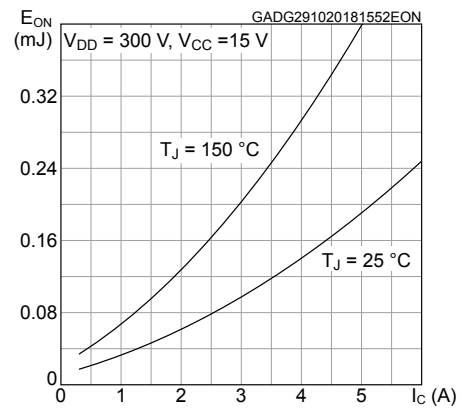
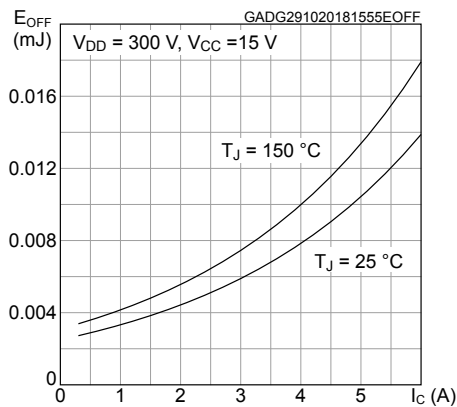
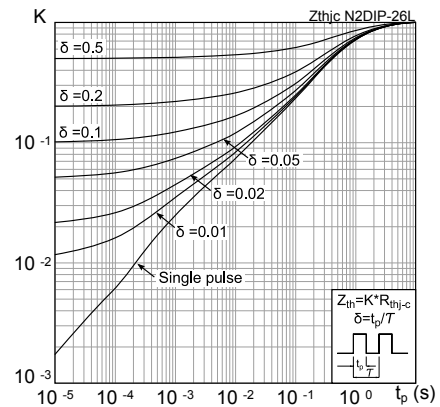
- Input signals HIN, LIN are active high logic. A 375 k $\Omega$  (typ.) pull-down resistor is built-in for each input. To avoid input signal oscillation, the wiring of each input should be as short as possible, and the use of RC filters ( $R_1$ ,  $C_1$ ) on each input signal is suggested. The filters should be with a time constant of about 100 ns and placed as close as possible to the IPM input pins.
- The use of a bypass capacitor  $C_{VCC}$  (aluminum or tantalum) can reduce the transient circuit demand on the power supply. Also, to reduce any high-frequency switching noise distributed on the power lines, a decoupling capacitor  $C_2$  (100 to 220 nF, with low ESR and low ESL) should be placed as close as possible to the Vcc pin and in parallel with the bypass capacitor.
- The use of an RC filter ( $R_{SF}$ ,  $C_{SF}$ ) is recommended to prevent protection circuit malfunction. The time constant ( $R_{SF} \times C_{SF}$ ) should be set to 1  $\mu$ s and the filter must be placed as close as possible to the  $C_{IN}$  pin.
- The  $\overline{SD}$  is an input/output pin (open-drain type if it is used as output). A built-in thermistor NTC is internally connected between the  $\overline{SD}$  pin and GND. The voltage  $V_{SD-GND}$  decreases as the temperature increases, due to the pull-up resistor  $R_{SD}$ . In order to keep the voltage always higher than the high-level logic threshold, the pull-up resistor should be set to 1 k $\Omega$  or 2.2 k $\Omega$  for 3.3 V or 5 V MCU power supply, respectively. The  $C_{SD}$  capacitor of the filter on  $\overline{SD}$  should be fixed no higher than 3.3 nF in order to assure the SD activation time  $\tau_A \leq 500$  ns. Besides, the filter should be placed as close as possible to the SD pin.
- The decoupling capacitor  $C_3$  (from 100 to 220 nF, ceramic with low ESR and low ESL), in parallel with each  $C_{boot}$ , filters high-frequency disturbance. Both  $C_{boot}$  and  $C_3$  (if present) should be placed as close as possible to the U, V, W and  $V_{boot}$  pins. Bootstrap negative electrodes should be connected to U, V, W terminals directly and separated from the main output wires.
- To avoid overvoltage on the Vcc pin, a Zener diode (Dz1) can be used. Similarly on the  $V_{boot}$  pin, a Zener diode (Dz2) can be placed in parallel with each  $C_{boot}$ .
- The use of the decoupling capacitor  $C_4$  (100 to 220 nF, with low ESR and low ESL) in parallel with the electrolytic capacitor  $C_{vdc}$  is useful to prevent surge destruction. Both capacitors  $C_4$  and  $C_{vdc}$  should be placed as close as possible to the IPM ( $C_4$  has priority over  $C_{vdc}$ ).
- By integrating an application-specific type HVIC inside the module, direct coupling to the MCU terminals without an optocoupler is possible.
- Low-inductance shunt resistors have to be used for phase leg current sensing.
- In order to avoid malfunctions, the wiring on N pins, the shunt resistor and  $PWR\_GND$  should be as short as possible.
- The connection of  $SGN\_GND$  to  $PWR\_GND$  on one point only (close to the shunt resistor terminal) can reduce the impact of power ground fluctuation.

These guidelines ensure the specifications of the device for application designs. For further details, please refer to the relevant application note.

**Table 14. Recommended operating conditions**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{PN}$	Supply voltage	Applied among P-Nu, Nv, Nw		300	500	V
$V_{CC}$	Control supply voltage	Applied to $V_{CC-GND}$	13.5	15	18	V
$V_{BS}$	High-side bias voltage	Applied to $V_{BOOTx-OUT}$ for $x = U, V, W$	13		18	V
$t_{dead}$	Blanking time to prevent arm-short	For each input signal	1.5			$\mu$ s
$f_{PWM}$	PWM input signal	-40 $^{\circ}$ C < $T_C$ < 100 $^{\circ}$ C -40 $^{\circ}$ C < $T_J$ < 125 $^{\circ}$ C			25	kHz
$T_C$	Case operation temperature				100	$^{\circ}$ C

## 6 Electrical characteristics (curves)

**Figure 11. Output characteristics**

**Figure 12. Diode  $V_{SD}$  vs drain current**

**Figure 13.  $I_D$  vs case temperature**

**Figure 14.  $E_{ON}$  switching energy vs drain current**

**Figure 15.  $E_{OFF}$  switching energy vs drain current**

**Figure 16. Thermal impedance for MOSFET**


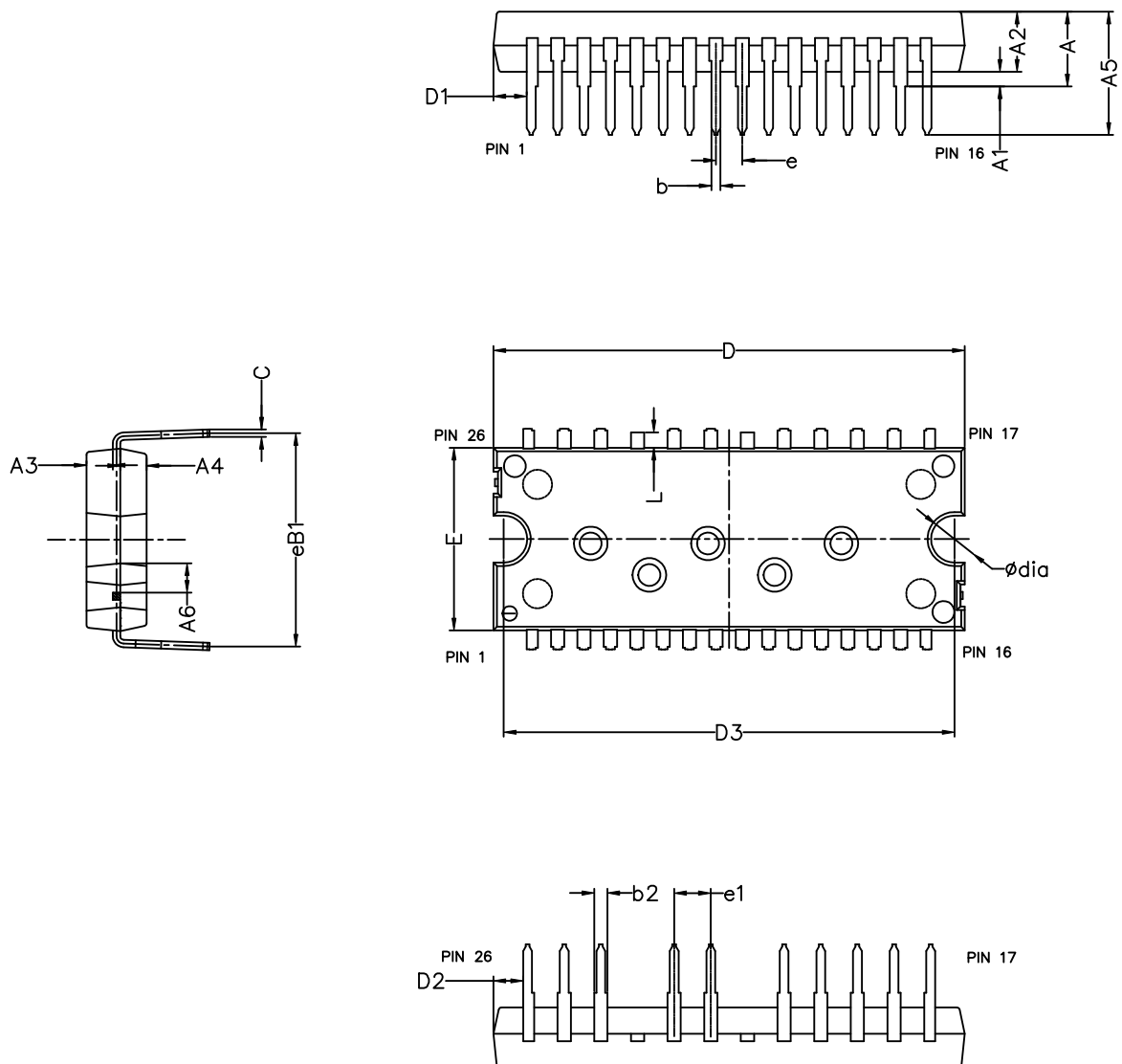


## 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK®** packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 7.1 N2DIP-26L type L package information

Figure 17. N2DIP-26L type L package outline



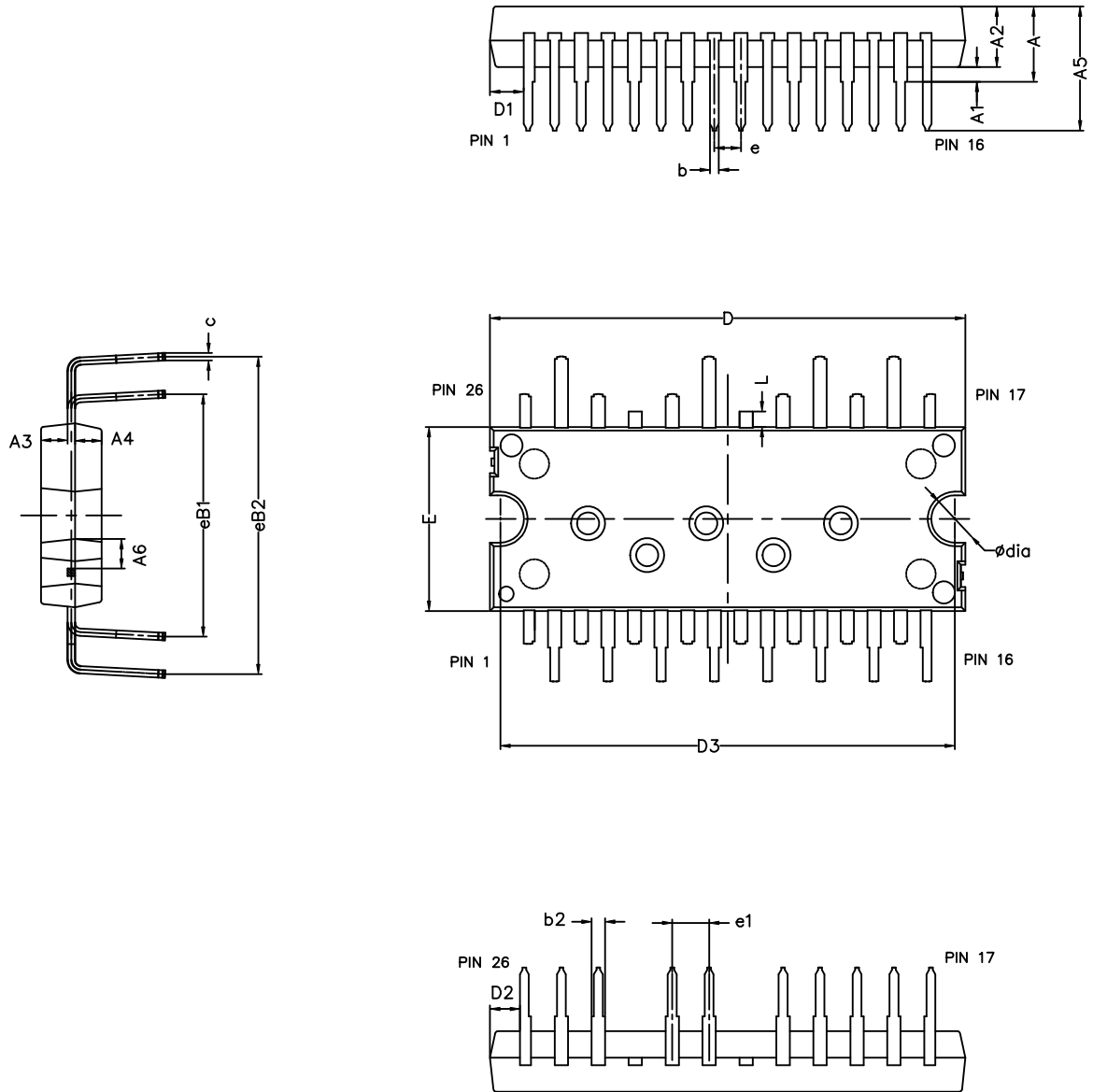
8558322\_typeL\_rev3

**Table 15. N2DIP-26L type L mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.80	5.10	5.40
A1	0.80	1.00	1.20
A2	4.00	4.10	4.20
A3	1.70	1.80	1.90
A4	1.70	1.80	1.90
A5	8.10	8.40	8.70
A6	1.75		
b	0.53		0.72
b2	0.83		1.02
c	0.46		0.59
D	32.05	32.15	32.25
D1	2.10		
D2	1.85		
D3	30.65	30.75	30.85
E	12.35	12.45	12.55
e	1.70	1.80	1.90
e1	2.40	2.50	2.60
eB1	14.25	14.55	14.85
L	0.85	1.05	1.25
Dia	3.10	3.20	3.30

## 7.2 N2DIP-26L type Z package information

Figure 18. N2DIP-26L type Z package outline



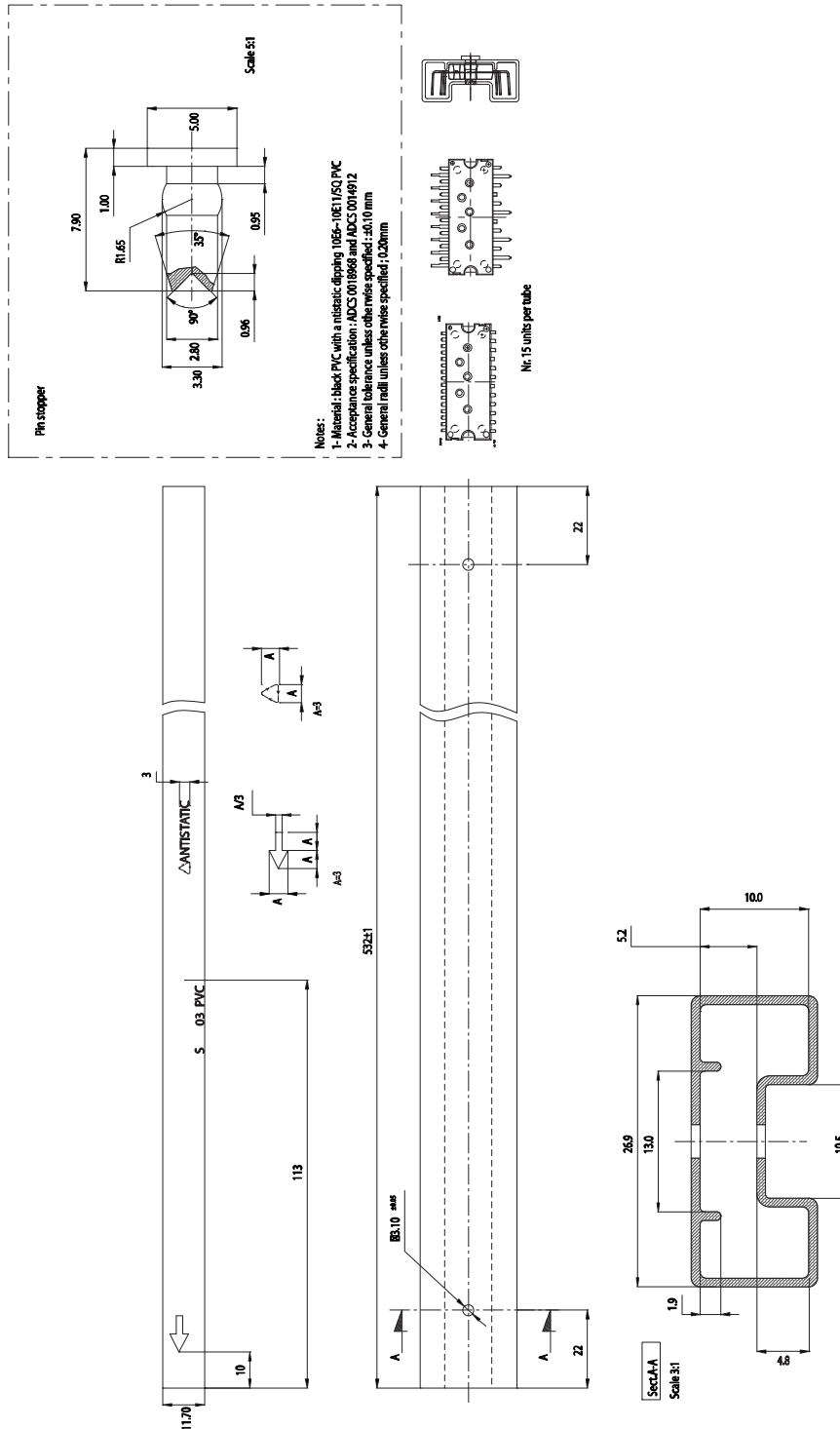
8558322\_typeZ\_rev3

**Table 16. N2DIP-26L type Z mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.80	5.10	5.40
A1	0.80	1.00	1.20
A2	4.00	4.10	4.20
A3	1.70	1.80	1.90
A4	1.70	1.80	1.90
A5	8.10	8.40	8.70
A6	1.75		
b	0.53		0.72
b2	0.83		1.02
c	0.46		0.59
D	32.05	32.15	32.25
D1	2.10		
D2	1.85		
D3	30.65	30.75	30.85
E	12.35	12.45	12.55
e	1.70	1.80	1.90
e1	2.40	2.50	2.60
eB1	16.10	16.40	16.70
eB2	21.18	21.48	21.78
L	0.85	1.05	1.25
Dia	3.10	3.20	3.30

### 7.3 N2DIP-26L packing information

Figure 19. N2DIP-26L tube (dimensions are in mm)



## Revision history

**Table 17. Document revision history**

Date	Revision	Changes
17-Jan-2017	1	Initial release.
27-Jun-2017	2	Document status promoted from preliminary data to production data. Updated features in cover page. Minor text changes.
07-Nov-2018	3	Updated package silhouette on cover page. Updated <a href="#">Section 2 Electrical ratings</a> and <a href="#">Section 3 Electrical characteristics</a> . Updated <a href="#">Section 4 Shutdown function</a> . Added <a href="#">Section 6 Electrical characteristics (curves)</a> . Minor text changes

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