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74LVT245, 74LVTH245

Low Voltage Octal Bidirectional Transceiver with 3-STATE Inputs/Outputs

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH245), also available without bushold feature (74LVT245)
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink, $-32\text{mA}/+64\text{mA}$
- Latch-up performance exceeds 500mA
- ESD performance:
 - Human-body model > 2000V
 - Machine model > 200V
 - Charged-device model > 1000V

General Description

The LVT245 and LVTH245 contain eight non-inverting bidirectional buffers with 3-STATE outputs and are intended for bus-oriented applications. The Transmit/Receive (T/\bar{R}) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

The LVTH245 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These transceivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT245 and LVTH245 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

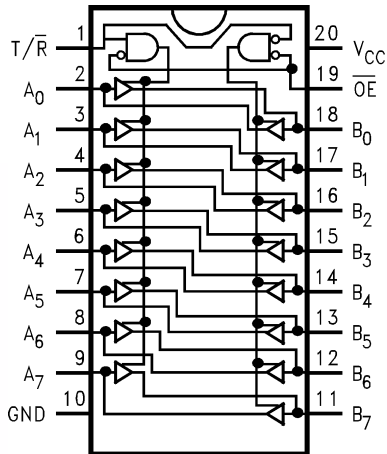
Ordering Information

| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74LVT245WM | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74LVT245SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74LVT245MSA | MSA20 | 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide |
| 74LVT245MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74LVTH245WM | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74LVTH245SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74LVTH245MSA | MSA20 | 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide |
| 74LVTH245MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

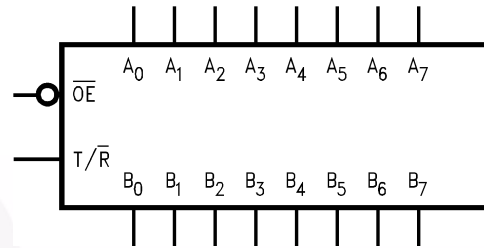
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram

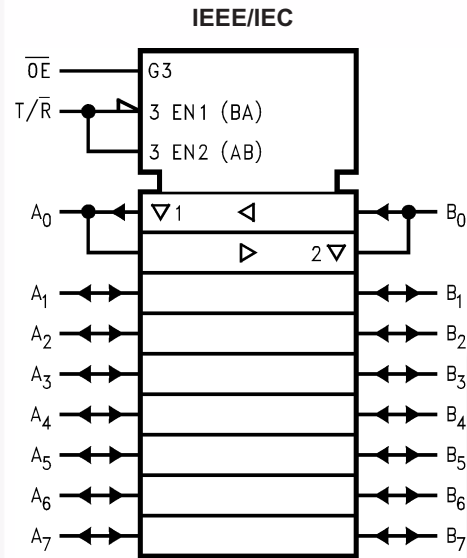


Logic Symbols



Pin Description

| Pin Names | Description |
|------------------|----------------------------------|
| \overline{OE} | Output Enable Input |
| T/\overline{R} | Transmit/Receive Input |
| A_0-A_7 | Side A Inputs or 3-STATE Outputs |
| B_0-B_7 | Side B Inputs or 3-STATE Outputs |



Truth Table

| Inputs | | Outputs |
|-----------------|------------------|---------------------|
| \overline{OE} | T/\overline{R} | |
| L | L | Bus B Data to Bus A |
| L | H | Bus A Data to Bus B |
| H | X | HIGH-Z State |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|-----------|---|-----------------|
| V_{CC} | Supply Voltage | -0.5V to +4.6V |
| V_I | DC Input Voltage | -0.5V to +7.0V |
| V_O | DC Output Voltage Output in 3-STATE | -0.5V to +7.0V |
| | Output in HIGH or LOW State ⁽¹⁾ | -0.5V to +7.0V |
| I_{IK} | DC Input Diode Current, $V_I < GND$ | -50mA |
| I_{OK} | DC Output Diode Current, $V_O < GND$ | -50mA |
| I_O | DC Output Current, $V_O > V_{CC}$ Output at HIGH State | 64mA |
| | Output at LOW State | 128mA |
| I_{CC} | DC Supply Current per Supply Pin | ±64mA |
| I_{GND} | DC Ground Current per Ground Pin | ±128mA |
| T_{STG} | Storage Temperature | -65°C to +150°C |

Note:

- I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Min | Max | Units |
|-----------------------|---|-----|-----|-------|
| V_{CC} | Supply Voltage | 2.7 | 3.6 | V |
| V_I | Input Voltage | 0 | 5.5 | V |
| I_{OH} | HIGH-Level Output Current | | -32 | mA |
| I_{OL} | LOW-Level Output Current | | 64 | mA |
| T_A | Free-Air Operating Temperature | -40 | 85 | °C |
| $\Delta t / \Delta V$ | Input Edge Rate, $V_{IN} = 0.8V-2.0V$, $V_{CC} = 3.0V$ | 0 | 10 | ns/V |

DC Electrical Characteristics

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = -40°C to +85°C | | Units | |
|-------------------------------------|---|---------------------|---|--|----------------------------------|-------|----|
| | | | | Min. | Max. | | |
| V _{IK} | Input Clamp Diode Voltage | 2.7 | I _I = -18mA | | -1.2 | V | |
| V _{IH} | Input HIGH Voltage | 2.7-3.6 | V _O ≤ 0.1V or | 2.0 | | V | |
| V _{IL} | Input LOW Voltage | 2.7-3.6 | V _O ≥ V _{CC} - 0.1V | | 0.8 | | |
| V _{OH} | Output HIGH Voltage | 2.7-3.6 | I _{OH} = -100μA | V _{CC} - 0.2 | | V | |
| | | 2.7 | I _{OH} = -8mA | 2.4 | | | |
| | | 3.0 | I _{OH} = -32mA | 2.0 | | | |
| V _{OL} | Output LOW Voltage | 2.7 | I _{OL} = 100μA | | 0.2 | V | |
| | | | I _{OL} = 24mA | | 0.5 | | |
| | | 3.0 | I _{OL} = 16mA | | 0.4 | | |
| | | | I _{OL} = 32mA | | 0.5 | | |
| | | | I _{OL} = 64mA | | 0.55 | | |
| I _{I(HOLD)} ⁽²⁾ | Bushold Input Minimum Drive | 3.0 | V _I = 0.8V | 75 | | μA | |
| | | | V _I = 2.0V | -75 | | | |
| I _{I(OD)} ⁽²⁾ | Bushold Input Over-Drive, Current to Change State | 3.0 | ⁽³⁾ | 500 | | μA | |
| | | | ⁽⁴⁾ | -500 | | | |
| I _I | Input Current | 3.6 | V _I = 5.5V | | 10 | μA | |
| | | Control Pins | 3.6 | V _I = 0V or V _{CC} | | | ±1 |
| | | | Data Pins | 3.6 | V _I = 0V | | |
| | | | | | V _I = V _{CC} | | |
| I _{OFF} | Power Off Leakage Current | 0 | 0V ≤ V _I or V _O ≤ 5.5V | | ±100 | μA | |
| I _{PU/PD} | Power Up/Down, 3-STATE Current | 0-1.5V | V _O = 0.5V to V _{CC} , V _I = GND to V _{CC} | | ±100 | μA | |
| I _{OZL} | 3-STATE Output Leakage Current | 3.6 | V _O = 0.5V | | -5 | μA | |
| I _{OZL} ⁽²⁾ | 3-STATE Output Leakage Current | 3.6 | V _O = 0.0V | | -5 | μA | |
| I _{OZH} | 3-STATE Output Leakage Current | 3.6 | V _O = 3.0V | | 5 | μA | |
| I _{OZH} ⁽²⁾ | 3-STATE Output Leakage Current | 3.6 | V _O = 3.6V | | 5 | μA | |
| I _{OZH} ⁺ | 3-STATE Output Leakage Current | 3.6 | V _{CC} < V _O ≤ 5.5V | | 10 | μA | |
| I _{CCH} | Power Supply Current | 3.6 | Outputs HIGH | | 0.19 | mA | |
| I _{CCL} | Power Supply Current | 3.6 | Outputs LOW | | 5 | mA | |
| I _{CCZ} | Power Supply Current | 3.6 | Outputs Disabled | | 0.19 | mA | |
| I _{CCZ} ⁺ | Power Supply Current | 3.6 | V _{CC} ≤ V _O ≤ 5.5V, Outputs Disabled | | 0.19 | mA | |
| ΔI _{CC} | Increase in Power Supply Current ⁽⁵⁾ | 3.6 | One Input at V _{CC} - 0.6V, Other Inputs at V _{CC} or GND | | 0.2 | mA | |

Notes:

- Applies to Bushold versions only (LVTH245).
- An external driver must source at least the specified current to switch from LOW-to-HIGH.
- An external driver must sink at least the specified current to switch from HIGH-to-LOW.
- This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics⁽⁶⁾

| Symbol | Parameter | V _{CC} (V) | Conditions C _L = 50 pF, R _L = 500Ω | T _A = 25°C | | | Units |
|------------------|---|------------------------|---|-----------------------|------|------|-------|
| | | | | Min. | Typ. | Max. | |
| V _{OLP} | Quiet Output Maximum Dynamic V _{OL} | 3.3 | (7) | | 0.8 | | V |
| V _{OLV} | Quiet Output Minimum Dynamic V _{OL} | 3.3 | (7) | | -0.8 | | V |

Notes:

6. Characterized in SOIC package. Guaranteed parameter, but not tested.
 7. Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

| Symbol | Parameter | T _A = -40°C to +85°C, C _L = 50 pF, R _L = 500Ω | | | | Units |
|---------------------------------------|--------------------------------------|---|------|------------------------|------|-------|
| | | V _{CC} = 3.3V ± 0.3V | | V _{CC} = 2.7V | | |
| | | Min. | Max. | Min. | Max. | |
| t _{PLH} | Propagation Delay | 1.2 | 3.6 | 1.2 | 4.0 | ns |
| t _{PHL} | | 1.2 | 3.5 | 1.2 | 4.0 | |
| t _{PZH} | Output Enable Time | 1.3 | 5.5 | 1.3 | 7.1 | ns |
| t _{PZL} | | 1.7 | 5.7 | 1.7 | 6.7 | |
| t _{PHZ} | Output Disable | 2.0 | 5.9 | 2.0 | 6.5 | ns |
| t _{PLZ} | | 2.0 | 5.0 | 2.0 | 5.1 | |
| t _{OSSL} , t _{OSHL} | Output to Output Skew ⁽⁸⁾ | | 1.0 | | 1.0 | ns |

Note:

8. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSHL}).

Capacitance⁽⁹⁾

| Symbol | Parameter | Conditions | Typical | Units |
|------------------|--------------------|--|---------|-------|
| C _{IN} | Input Capacitance | V _{CC} = 0V, V _I = 0V or V _{CC} | 4 | pF |
| C _{OUT} | Output Capacitance | V _{CC} = 3.0V, V _O = 0V or V _{CC} | 8 | pF |

Note:

9. Capacitance is measured at frequency f = 1MHz, per MIL-STD-883, Method 3012.

Physical Dimensions



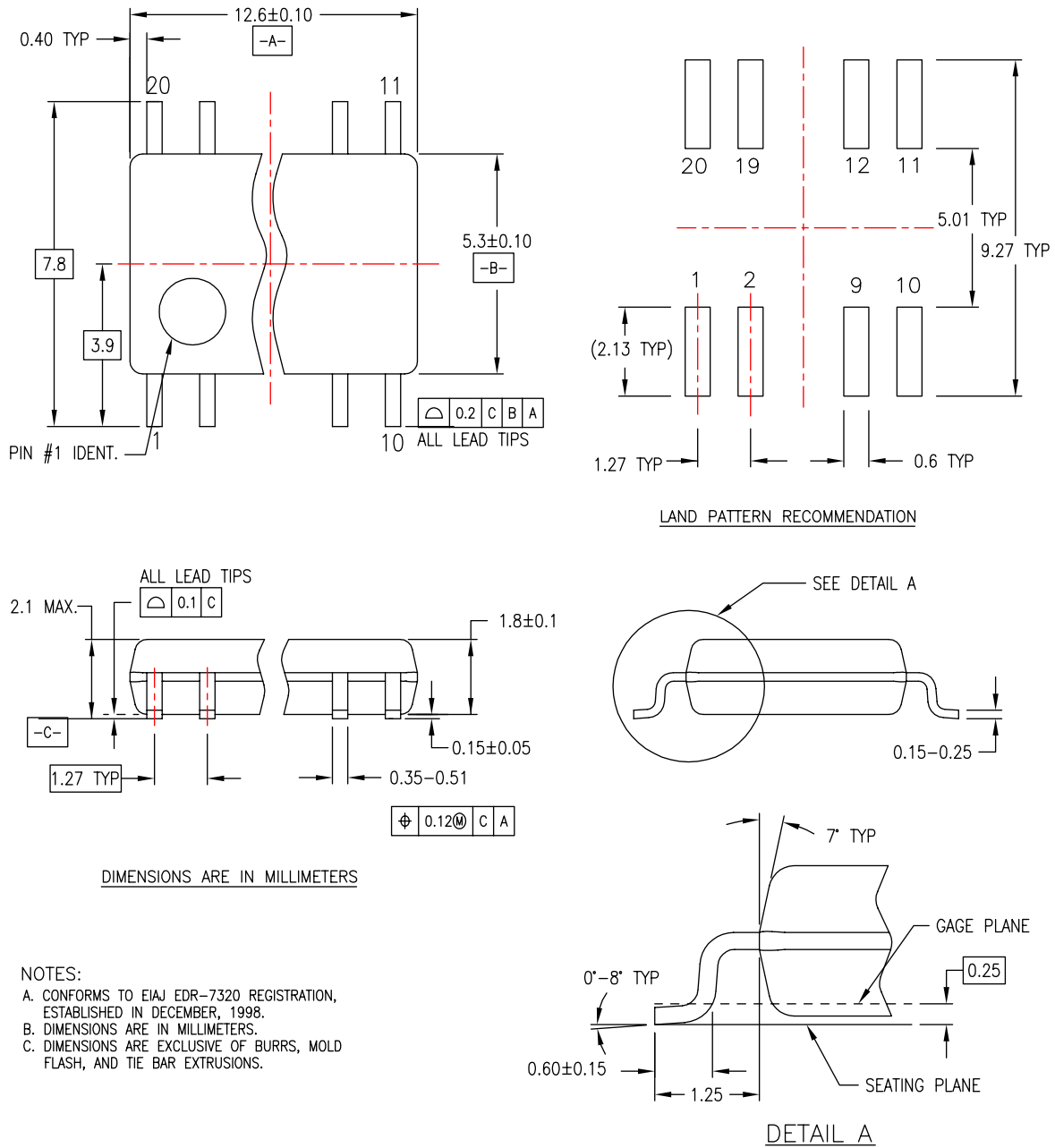
Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

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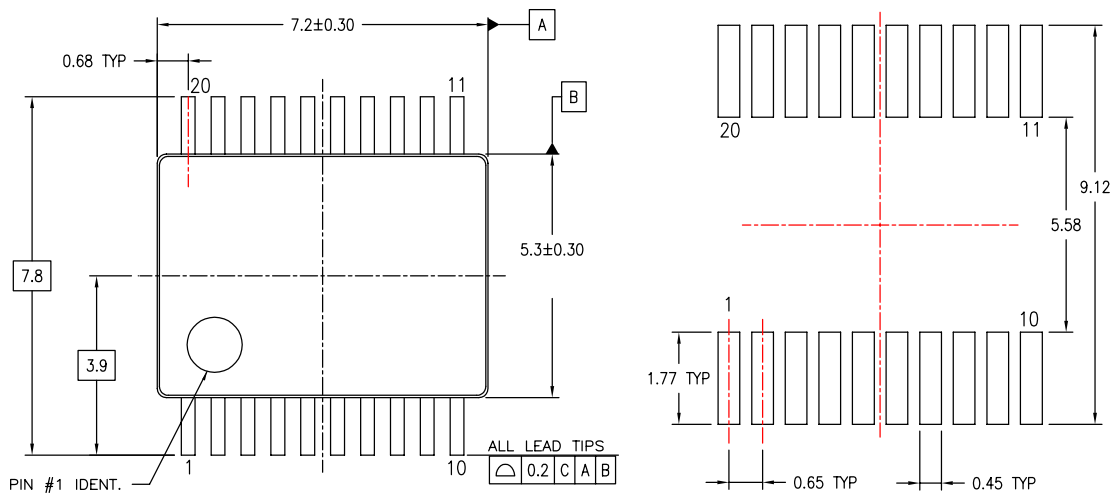
Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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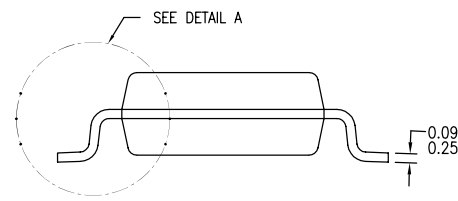
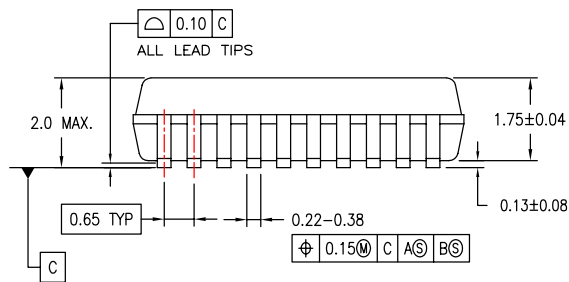
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Physical Dimensions (Continued)



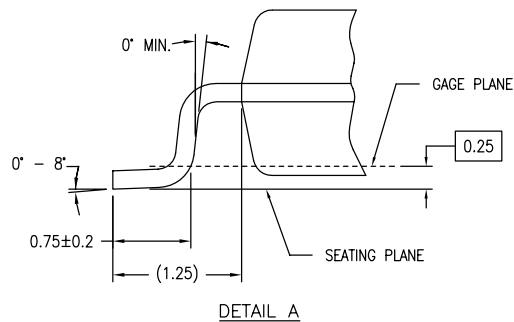
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NOTES:

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- D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M - 1994.



MSA20REVB

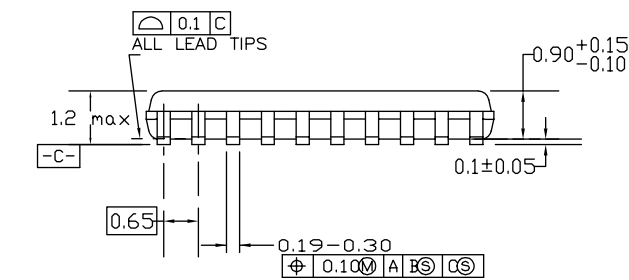
Figure 3. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide

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Physical Dimensions (Continued)



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- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

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Figure 4. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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