International Rectifier

Data Sheet No. PD60233 revB

IR2277S/IR2177S(PbF)

Phase Current Sensor IC for AC motor control

Features

- Floating channel up to 600 V for IR2177 & 1200 V for IR2277
- Synchronous sampling measurement system
- High PWM noise (ripple) rejection capability
- Digital PWM output
- Fast Over Current detection
- Suitable for bootstrap power supplies
- Low sensing latency (<7.5 μsec @20kHz)
- Ratiometric analog output suitable for DSP A/D interface

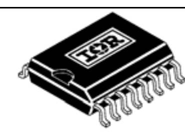
Product Summary

V_{OFFSET} (max)	IR2277	1200 V
	IR2177	600 V
V_{in} range		±250mV
Bootstrap supply range		8-20 V
Floating channel quiescent current (max)		2.2 mA
Sensing latency (max)		7.5 µsec (@20kHz)
Throughput		40ksample/sec (@20kHz)
Over Current threshold (max)		±470 mV

Description

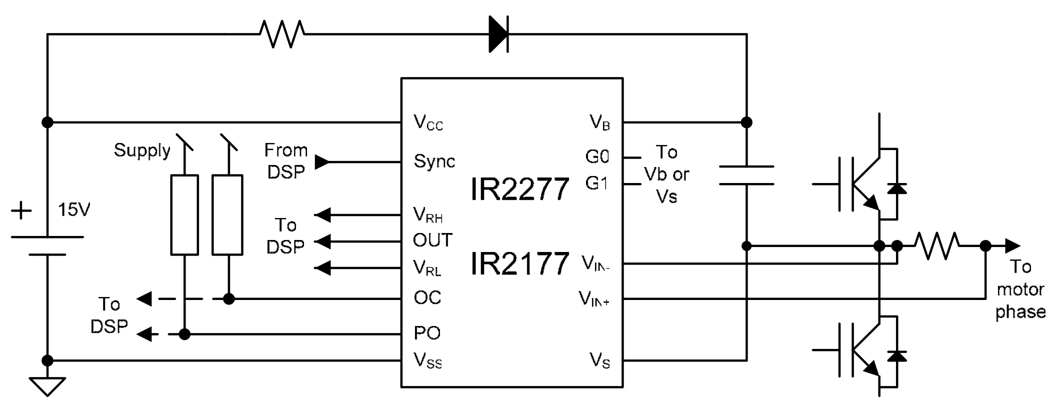
IR2177/IR2277 is a high voltage, high speed, single phase current sensor interface for AC motor drive applications. The current is sensed by an external shunt resistor. The IC converts the analog voltage into a time interval through a precise circuit that also performs a very good ripple rejection showing small group delay. The time interval is level shifted and given to the output both as a PWM signal (PO) and analog voltage (OUT). The analog voltage is proportional to the measured current and is ratio metric with respect to an externally provided voltage reference. The max throughput is 40 ksample/sec suitable for up to 20 kHz asymmetrical PWM modulation and max delay is <7.5 μsec (@20kHz). Also a fast over current signal is provided for IGBT protection.

Package



16-Lead SOIC
(wide body)

Typical Connection



(Please refer to Lead Assignments for correct pin configuration. This diagram shows electrical connections only)

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{SS}, all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High Side Floating Supply Voltage	IR2277	- 0.3	1225	V
		IR2177	- 0.3	625	
V_S	High Side Floating Ground Voltage		V_B - 25	V_B + 0.3	V
V_{in+} / V_{in-}	High-Side Inputs Voltages		V_S - 5	V_B + 0.3	V
G0 / G1	High-Side Range Selectors		V_S - 0.3	V_B + 0.3	V
V_{CC}	Low-Side Fixed Supply Voltage		- 0.3	25	V
Sync	Low-Side Input Synchronization Signal		- 0.3	V_{CC} + 0.3	V
V_{RH}/V_{RL}	DSP Reference High and Low Voltages		- 0.3	V_{CC} + 0.3	V
Out	Analog Output Voltage		- 0.3	V_{CC} + 0.3	V
PO	PWM Output		- 0.3	V_{CC} + 0.3	V
OC	Over Current Output Voltage		- 0.3	V_{CC} + 0.3	V
dV_S/dt	Allowable Offset Voltage Slew Rate			50	V/ns
P_D	Maximum Power Dissipation			250	mW
R_{thJA}	Thermal Resistance, Junction to Ambient			90	ºC/W
T_J	Junction Temperature		-40	125	ºC
T_S	Storage Temperature		-55	150	ºC
T_L	Lead Temperature (Soldering, 10 seconds)			300	ºC

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to V_{ss}. The V_s offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition		Min.	Max.	Units
V_{BS}	High Side Floating Supply Voltage (V_B- V_S)		V_S + 8.0	V_S + 20	V
V_S	High Side Floating Ground Voltage	IR2277	-5	1200	V
		IR2177		600	
V_{in+} / V_{in-}	High-Side Inputs Voltages		V_S - 5.0	V_S + 5.0	V
G0 / G1	High-Side Range Selectors		Note 1	Note1	
V_{CC}	Low Side Logic Fixed Supply Voltage		8	20	V
Sync	Low-Side Input Synchronization Signal		V_{SS}	V_{CC}	V
f_{sync}	Sync Input Frequency	Using PO	4	20	kHz
		Using OUT	8	20	
PO	PWM Output		-0.3	Note 2	V
OC	Over Current Output Voltage		-0.3	Note 2	V
V_{RH}	OUT Reference High Voltage		3	V_{CC}-2.5	V
V_{RL}	OUT Reference Low Voltage		V_{SS}	V_{RH}-3	V
T_A	Ambient Temperature		-40	125	ºC

Note 1: Shorted to V_S or V_B

Note 2: Pull-Up Resistor to V_{CC}

Static Electrical Characteristics

V_{CC}, V_{BS} = 15V unless otherwise specified. Temp=27°C; V_{in}=V_{in+} - V_{in}.

Pin: V_{CC}, V_{SS}, V_B, V_S

Symbol	Definition		Min.	Typ.	Max.	Units	Test Conditions
I_{QBS}	Quiescent V_{BS} supply current			1	2.2	mA	f_{sync} = 10kHz, 20kHz
I_{QCC}	Quiescent V_{CC} supply current				6	mA	f_{sync} = 10kHz, 20kHz
I_{LK}	Offset supply leakage current	IR2277			50	µA	V_B = V_S = 1200V
		IR2177			50		V_B = V_S = 600V

Pin: V_{in+}, V_{in-}, Sync, G0, G1, OC

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{inmax}	Maximum input voltage before saturation		250		mV	
V_{inmin}	Minimum input voltage before saturation		-250		mV	
V_{IH}	Sync Input High threshold	2.2			V	See Figure 1
V_{IL}	Sync Input Low threshold			0.8	V	See Figure 1
V_{hy}	Sync Input Hysteresis	0.2			V	See Figure 1
I_{vinp}	V_{in+} input current	-18		-6	µA	f_{sync} = 4kHz to 20kHz
I_{pu}	G0, G1 pull-up Current	-20		-8	µA	G1, G0 = V_B-5V
$\|V_{octh}\|$	Over Current Activation Threshold	300		470	mV	
R_{Sync}	SYNC to V_{SS} internal pull-down	6		12	kΩ	
R_{onOC}	Over Current On Resistance	25		75	Ω	@ I = 2mA See Figure 3

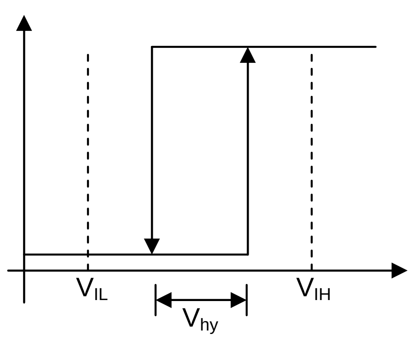


Figure 1: Sync input thresholds

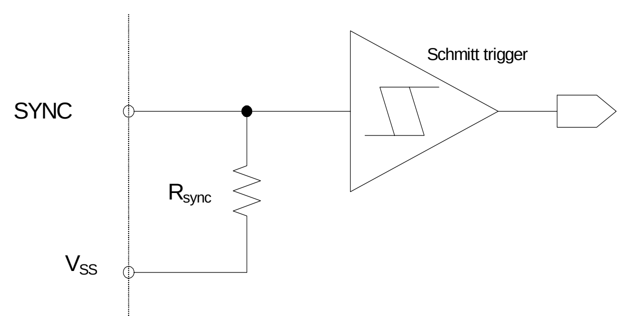


Figure 2: Sync input circuit

Pin: PO

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{POs}	Input offset voltage measured by PWM output	-50		20	mV	$R_{pull-up}$=500 Ω f_{sync} = 4, 20kHz $V_{threshold}$=2.75V Ext supply=5V (See Figure 6)
ΔV_{POs} / ΔTj	Input offset voltage temperature drift		TBD		µV/°C	
ΔV_{POs}	Δoffset between samples on channel1 and channel2 measured at PO (See Note1)	-10		10	mV	f_{sync} = 10kHz See Figure 6
G_p	PWM Output Gain	-38	-40.5	-42.5	%/V	V_{in}=±250mV
ΔG_p / ΔTj	PWM Output Gain Temperature Drift		TBD		%/(V*ºC)	
CMRR PO	PO Output common mode (V_S) rejection		0.2		m%/V	V_s-V_{ss} = 0, 600V f_{sync} = 10kHz
V_{POlin}	PO Linearity		0.07	0.2	%	10kHz
Δ V_{lin}/ ΔTj	PO Linearity Temperature Drift		TBD		%/ºC	10kHz
V_{thPO}	PO threshold for OC reset	0.8		1.6	V	OC active (See Figure 4)
PSRR PO	PSRR for PO Output			0.2	%/V	V_{CC}=V_{BS}= 8,20V
R_{onPO}	PO On Resistance	25		75	Ω	@ I = 2mA See Figure 3

Note1: Refer to PO output description for channels definition

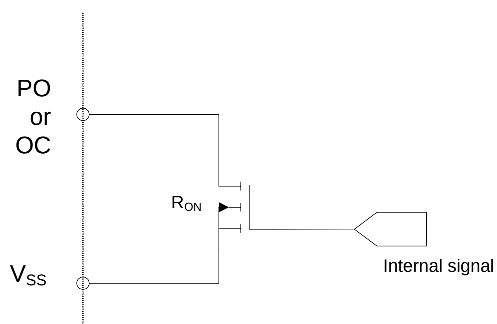


Figure 3: PO and OC open collector circuit

Pin: OUT, VRH, VRL

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
R_{REF}	V_{RH} to V_{RL} input resistance	36		84	kΩ	
V_{aos}	Input offset voltage measured by analog output	-100		50	mV	f_{sync} = 8kHz, 20 kHz
$\Delta V_{aos} / \Delta Tj$	Input offset voltage temperature drift		TBD		µV / ºC	Measured by analog output
ΔV_{aos}	Δoffset between samples on channel1 and channel2 measured at OUT (Note1)					f_{sync} = 8kHz, 20 kHz
G_a	Analog Output Gain	-20%	2VR	+20%	V/V	$V_R=V_{RH}-V_{RL}$=3V
$\Delta G_a / \Delta Tj$	Analog Output Gain Temperature Drift		TBD		$^oC^{-1}$	
CMRR OUT	Analog Output common mode (V_S offset) rejection		100		dB	Vs-Vss=0V, 600V f_{sync} = 10kHz
V_{OUTlin}	Out Linearity		0.3	0.7	%	f_{sync} = 8kHz, 20kHz
$\Delta V_{lin} / \Delta Tj$	Out Linearity Temperature Drift		TBD		%/ºC	f_{sync} = 8kHz, 20kHz
PSRR OUT	PSRR for Analog Output	30		100	dB	$V_{CC}= V_{BS}$ =8V, 20V
V_{OUTl}	Vout Low Saturation	0		50	mV	V_{in}= -500mV
V_{OUTh}	Vout High Saturation	V_{RH}+0.2		V_{RH}+0.7	V	V_{in} = +500mV

Note1: Refer to PO output description for channels definition

AC Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V unless otherwise specified. Temp=27°C.

Symbol	Definition		Min.	Typ.	Max.	Units	Test Conditions
f_{sync}	PWM frequency	PO	4		20	kHz	
		OUT	8		20		
f_{out}	Throughput			$2 \cdot f_{sync}$		ksample/sec	
BW	Bandwidth (@ -3 dB)			f_{sync}		kHz	
GD	Group Delay (input filter)			$\frac{1}{4 \cdot f_{sync}}$		µs	
D_{min}	Minimum Duty Cycle (Note 1)			10		%	V_{in}=+V_{inmax}
D_{max}	Maximum Duty Cycle (Note 1)			30		%	V_{in}=-V_{inmin}
t_{dOCon}	De-bounce time of OC		2.7	3.5	4.7	µs	See Figure 4
T_{OCoff}	Time to reset OC forcing PO				0.5	µs	See Figure 4
C_{load}	Analog output load capacitor		0		50	nF	NOTE 2
SL_{OUT}	Analog output (OUT) Slew Rate		0.2		1	V/µs	$C_{out} \leq 5$ nF
t_{settl}	Output settling time (1%)		5		30	µs	$C_{out} \leq 5$ nF
MD	Measure Delay				$\frac{0.30}{2 \cdot f_{sync}}$	µs	
SR	Step response (max time to reach steady state) for PO output		$\frac{0.51}{f_{sync}}$		$\frac{1.3}{f_{sync}}$	µs	See Figure 5
SR_{OUT}	Step response (max time to reach steady state) for OUT output		$\frac{0.51}{f_{sync}} + t_{settl}$		$\frac{1.3}{f_{sync}} + t_{settl}$	µs	See Figure 5

Note 1: negative logic, see Figure 4 on page 7
Note 2: Cload < 5 nF avoids overshoot

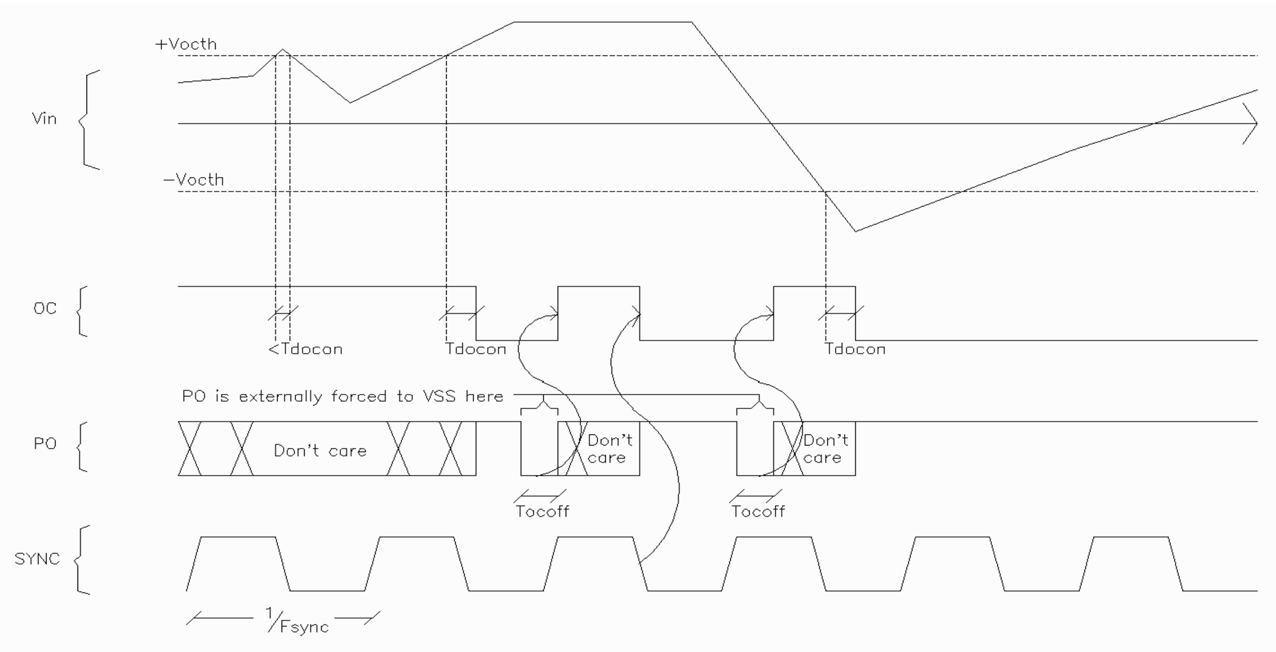


Figure 4: OC timing diagram

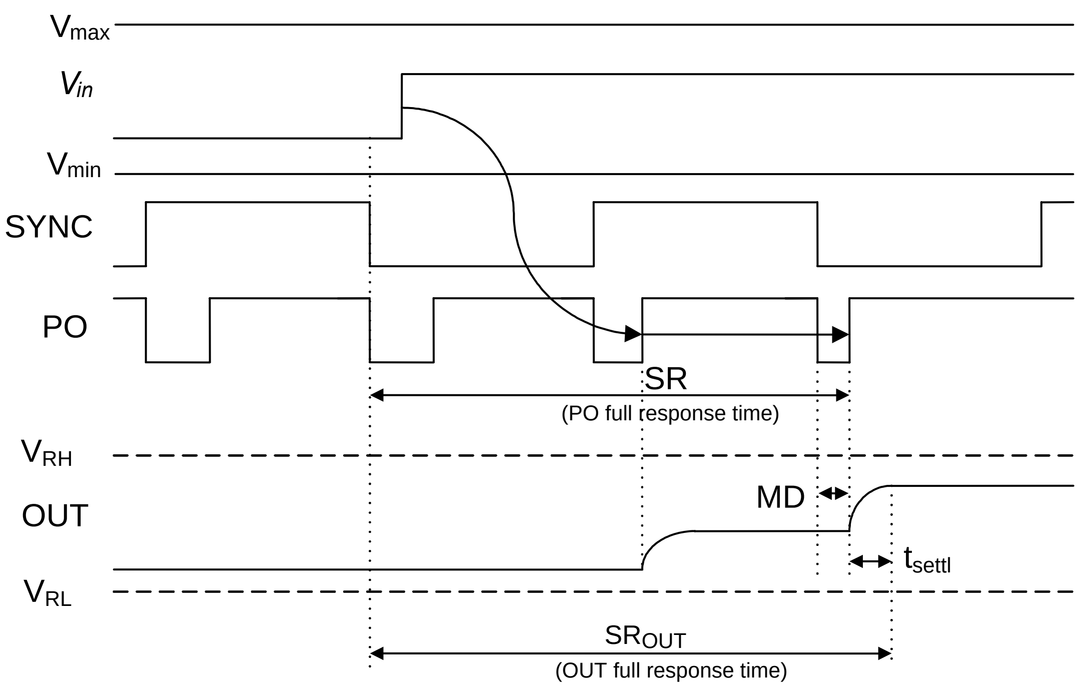


Figure 5: timing diagram

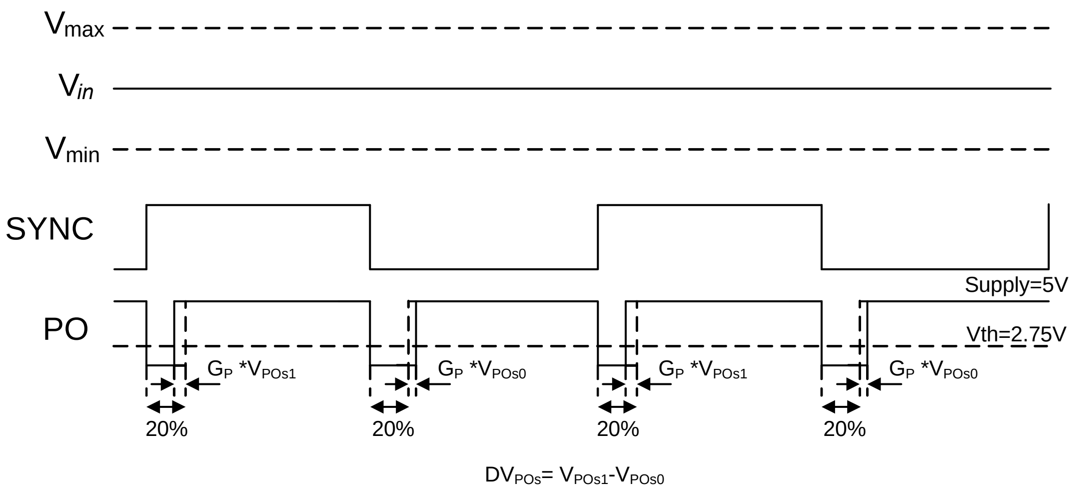
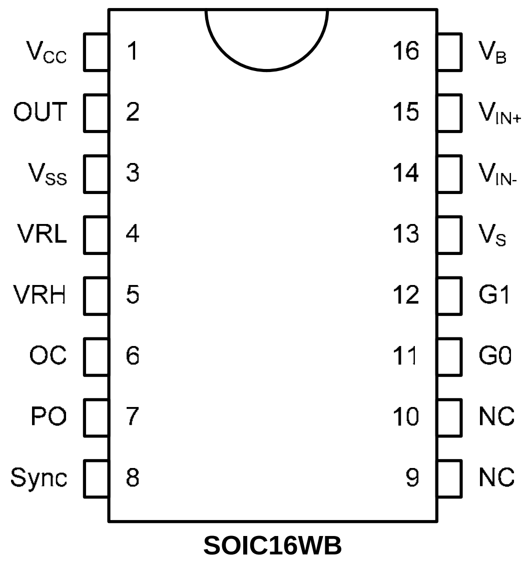


Figure 6: ∆offset between two consecutive samples measured at PO

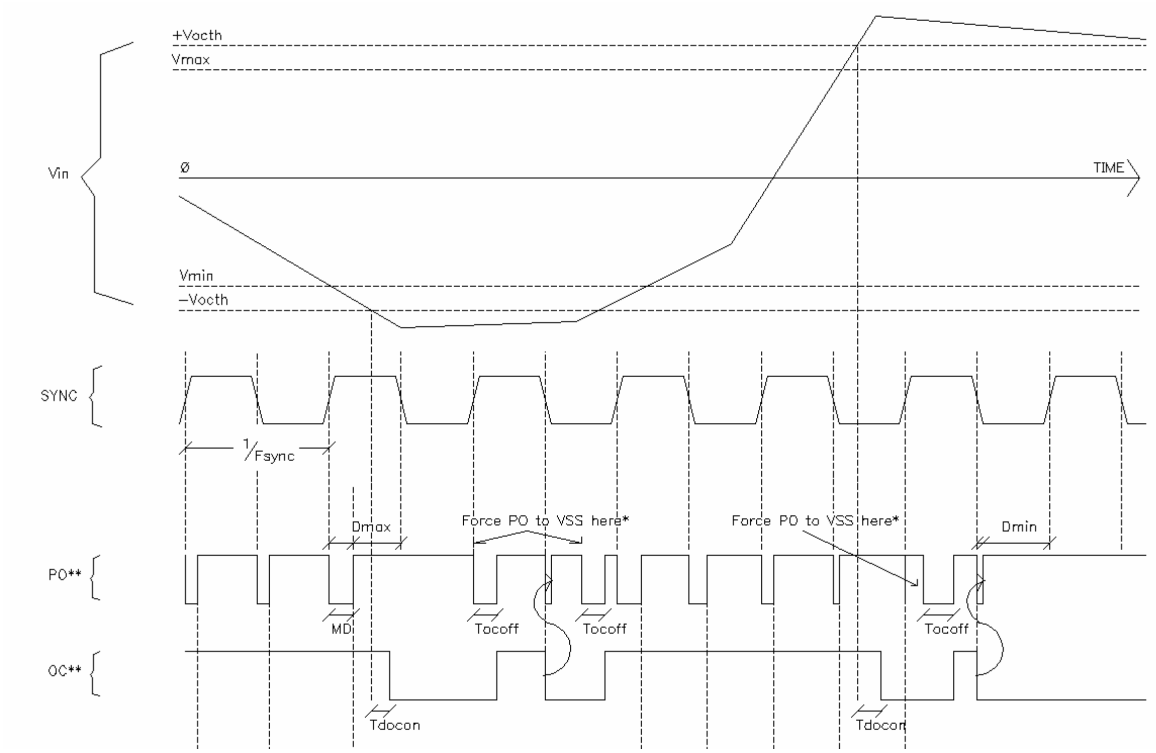
Lead Assignments



Lead Definitions

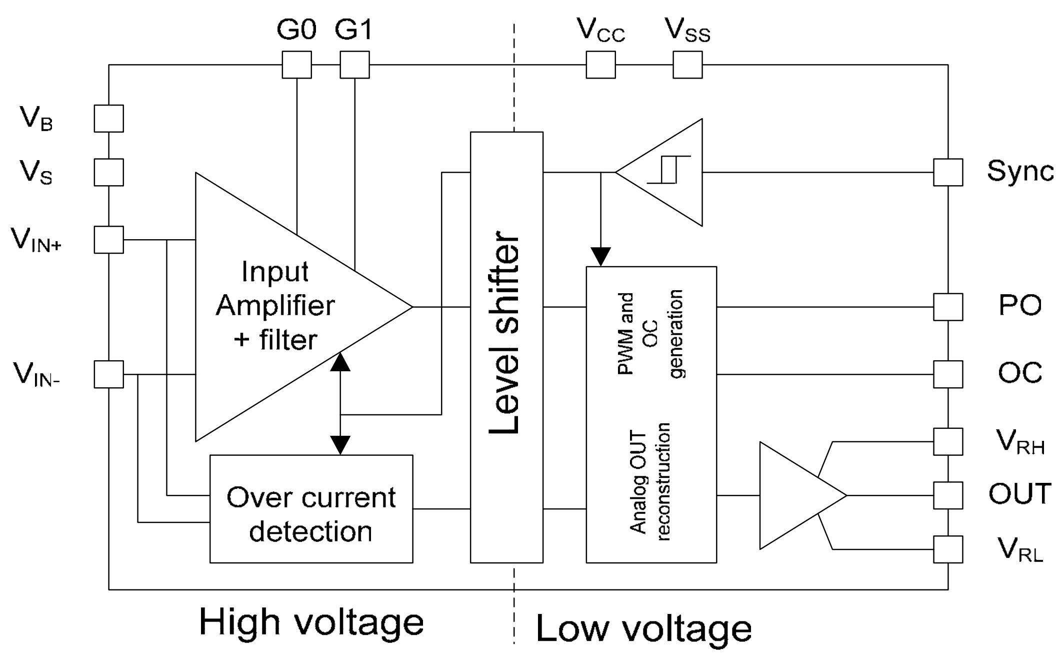
Pin	Symbol	Description
1	V_{CC}	Low side voltage supply
2	OUT	Analog output
3	V_{SS}	Low side ground supply
4	V_{RL}	Lower rail of A/D voltage range
5	V_{RH}	Higher rail of A/D voltage range
6	OC	Over current signal (open drain)
7	PO	PWM output (open drain)
8	Sync	DSP synchronization signal
9	NC	No connection
10	NC	No connection
11	G0	Integrator gain lsb
12	G1	Integrator gain msb
13	V_S	High side return
14	V_{IN-}	Negative sense input
15	V_{IN+}	Positive sense input
16	V_B	High side supply

Timing and logic state diagrams description



** See OC and PO detailed descriptions below in this document

Functional block diagram



1 Device Description

1.1 SYNC input

Sync input clocks the whole device. In order to make the device work properly it must be synchronous with the triangular PWM carrier as shown in Figure 8.
SYNC pin is internally pulled-down (10 kΩ) to V_{SS}.

1.2 PWM Output (PO)

PWM output is an open collector output (active low). It must be pulled-up to proper supply with an external resistor (suggested value between 500Ω and 10kΩ).

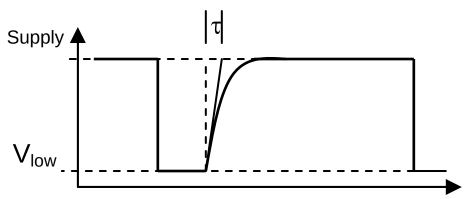


Figure 7: PO rising and falling slopes

PO pull-up resistor determines the rising slope of the PO output and the lower value of PO as shown in Figure 7, where $\tau = RC$, C is the total PO pin capacitance and R is the pull-up resistance.

$$V_{low} = Supply \cdot \frac{R_{on}}{R_{on} + R_{pull-up}}$$

where R_{on} is the internal open collector resistance and $R_{pull-up}$ is the external pull-up resistance.

PO duty cycle is defined for active low logic by the following formula:

Eq. 1 $$D_n = \frac{T_{off\_cycle\_n+1}}{T_{cycle\_n}}$$

PO duty cycle (D_n) swings between 10% and 30%. Zero input voltage corresponds to 20% duty cycle.

A residual offset can be read in PO duty cycle according to V_{POs} (see Static electrical characteristics).

According to
Figure 8, it can be assumed that odd cycles are represented by SYNC at high level (let's name channel 1 the output related to this state of SYNC) and even cycles represented by SYNC at low level (channel 2).
The two channels are independent in order to provide the correct duty cycle value of PO even for non-50% duty cycle of SYNC signal. Small variation of SYNC duty cycle are then allowed and automatically corrected when calculating the duty cycle using **Eq. 1**.
However, channel 1 and channel 2 can have a difference in offset value which is specified in ΔV_{POS} (see Static electrical characteristics).
To implement a correct offset compensation of PO duty cycle and analog OUT, each channel must be compensated separately.

1.3 Over Current output (OC)

OC output is an open drain pin (active low).
A simplified block diagram of the over current circuit is shown in the
Figure 9.

Over current is detected when $|V_{in}|=|V_{inp}-V_{inm}|>V_{OCth}$. If an event of over current lasts longer than t_{dOCon}, OC pin is forced to V_{SS} and remains latched until PO is externally forced low for at least t_{OCoff} (see timing on Figure 4). During an over current event (OC is low), PO is off (pulled-up by external resistor).
If OC is reset by PO and over current is still active, OC pin will be forced low again by the next edge of SYNC signal.
To reset OC state PO must be forced to V_{SS} for at least T_{OCoff}.

- Autoreset function

The autoreset function consists in clearing automatically the OC fault.
To enable the autoreset function, simply short circuit the OC pin with the PO pin.

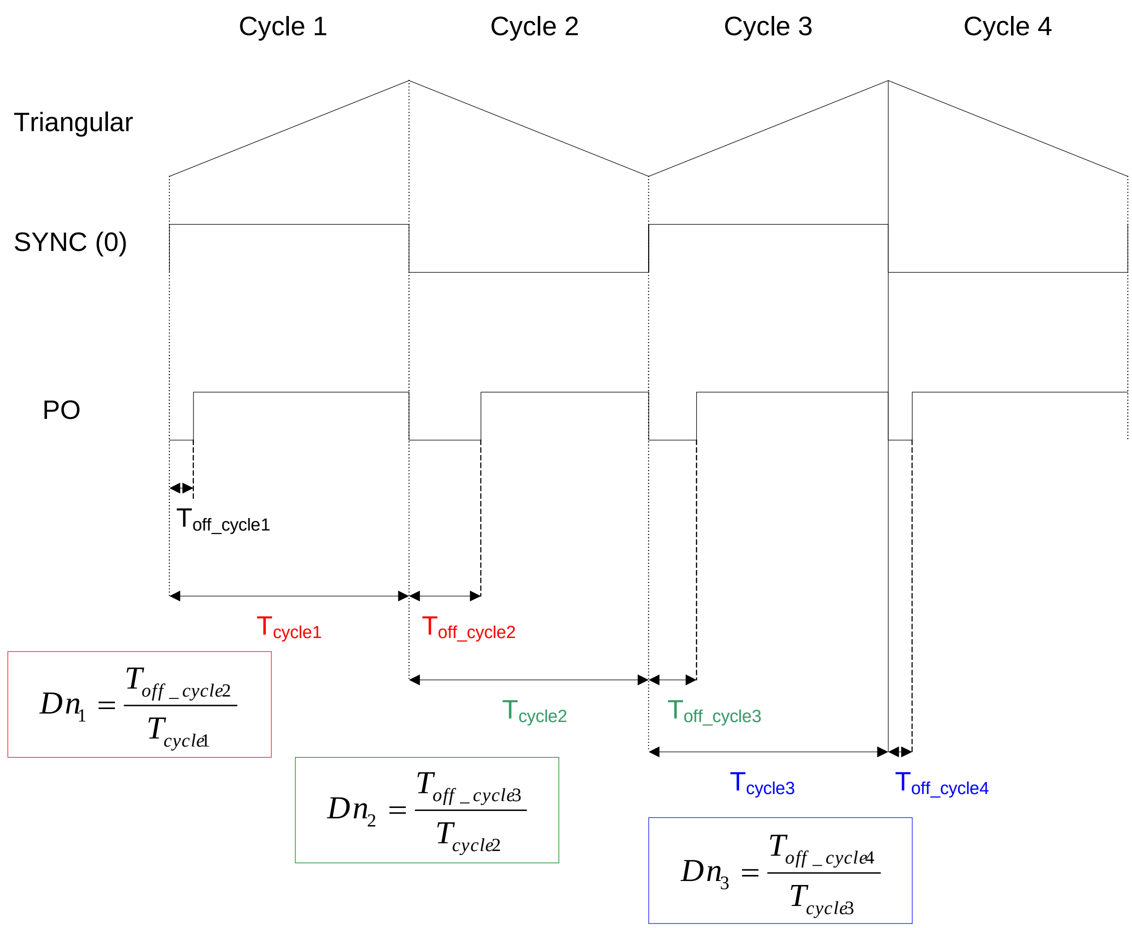


Figure 8: PO Duty Cycle

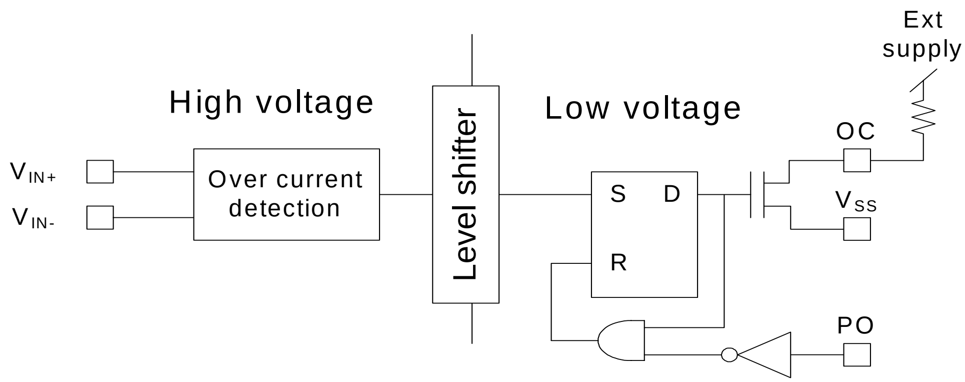


Figure 9: Over current block diagram

1.4 Analog Output (OUT)

The analog output is internally buffered and capable of driving capacitive loads ranging up to 50nF.

V_{RH} and V_{RL} set the dynamic range and gain of OUT pin.

Additional circuitry to protect A/D converter input against excessive voltage is not required.

Hereafter follow some definitions (see Figure 10 and following).

- $\boldsymbol{V_{in} = V_{inp} - V_{inm}}$
- **Input referred analog offset (V_{aos}):** It is the input that gives an output that equals $OUT = \frac{V_{RH} + V_{RL}}{2}$ (referred to V_{SS}).
- **Gain:** It is defined by the ratio $G_a = \frac{\Delta OUT}{\Delta V_{in}}$.
- **Linearity:** It is defined by the maximum difference between the ideal OUT/V_{in} curve and the measured curve depurated of the offset voltage and the gain error.

The analog output is also defined by some dynamic characteristics (see figure 8):

- **Slew Rate (SL_{OUT}).** The maximum slope of OUT measured in V/µs
- **Settling time (t_{settl}).** Time needed by the analog output (OUT) to reach 90% of final value.
- **Measure delay (MD).** It is defined by the time interval between the actual SYNC edge and PO rising edge.
- **Step response (SR).** Is the time needed by Output to reach the final value after a step of the input.
  Is always within the following range:

$$\frac{1}{2 \cdot f_{SYNC}} + MD + t_{settl} \leq SROUT \leq \frac{1}{f_{SYNC}} + MD + t_{settl}$$

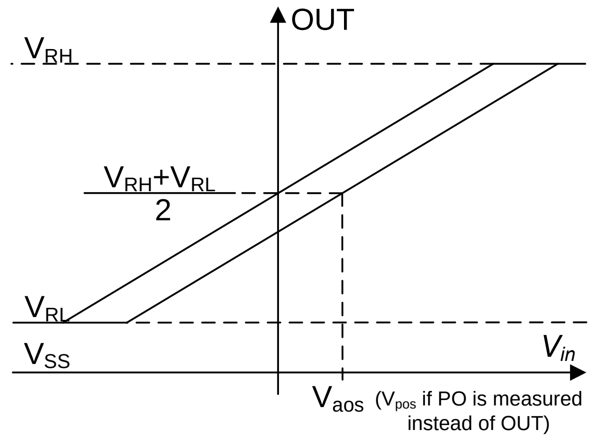


Figure 10: Input offset definition

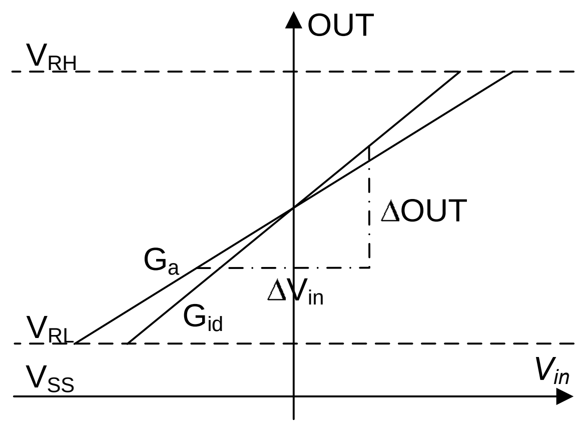


Figure 11: Gain definition

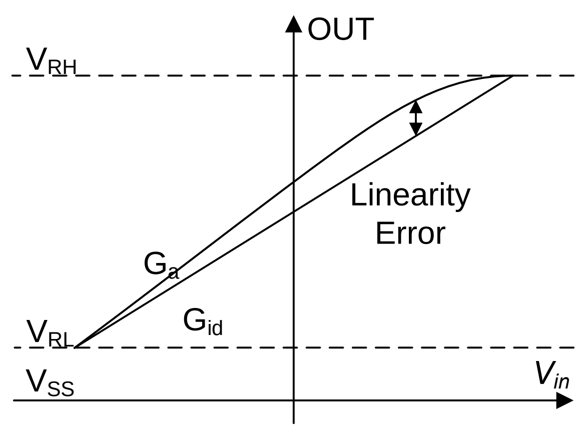


Figure 12: Linearity error definition

1.5 DC transfer functions

The working principle of the device can be easily explained by Figure 13, in which the main signals are represented.

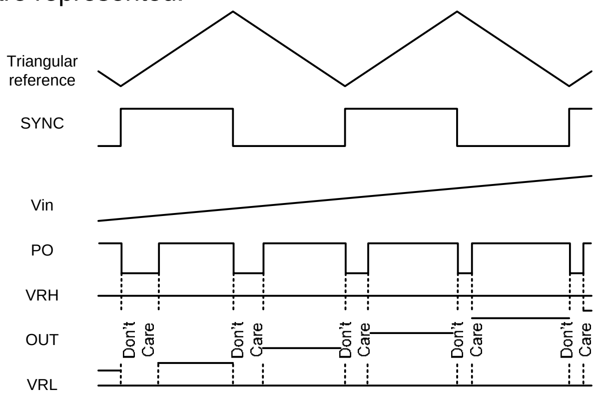


Figure 13: Main current sensor signals and outputs

PWM out (PO pin) gives a duty cycle which is inversely proportional to the input signal while the OUT pin gives the analog converted output.
Eq. 2 gives the resulting D_n of the PWM output (PO pin):

Eq. 2 $$D_n = 20\% - 40\frac{\%}{V} \cdot V_{in}$$

where $V_{in} = V_{inp} - V_{inm}$

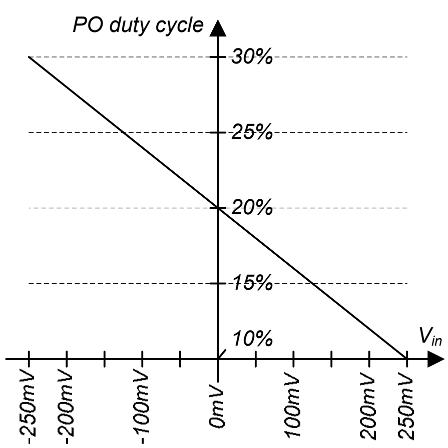


Figure 14: PO Duty Cycle (D_n)

The Voltage-to-Time conversion (V_{in} to PO) must be reconstructed (see Functional Block Diagram) to give an analog voltage output at OUT pin.
OUT pin swings from V_{RL} to V_{RH}, so the analog output (referred to V_{SS}) follows Eq. 3:

Eq. 3 $$OUT = 2 \cdot (V_{RH} - V_{RL}) \cdot V_{in} + \frac{V_{RH} + V_{RL}}{2}$$

The same equation can be referred to V_{RL}, as follows in Eq. 4:

Eq. 4
$$OUT - V_{RL} = 2 \cdot (V_{RH} - V_{RL}) \cdot V_{in} + \frac{V_{RH} - V_{RL}}{2}$$

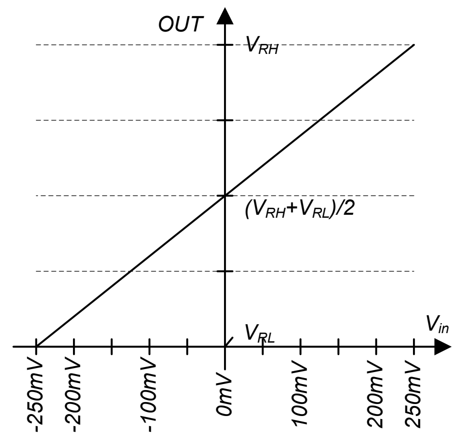


Figure 15: ideal OUT/V_{in} transfer function

Filter AC characteristic

IR2177/2277 signal path can be considered as composed by three stages in series (see Figure 17). The first two stages perform the filtering action.
Stage 1 (input filter) implements the filtering action originating the transfer function shown in Figure 18.
The input filter is a self-adaptive reset integrator which performs an accurate ripple cancellation. This stage extracts automatically the PWM frequency from Sync signal and puts transmission zeros at even harmonics, rejecting the unwanted PWM noise.
The following timing diagram shows the principle by which even harmonics are rejected (Figure 16).

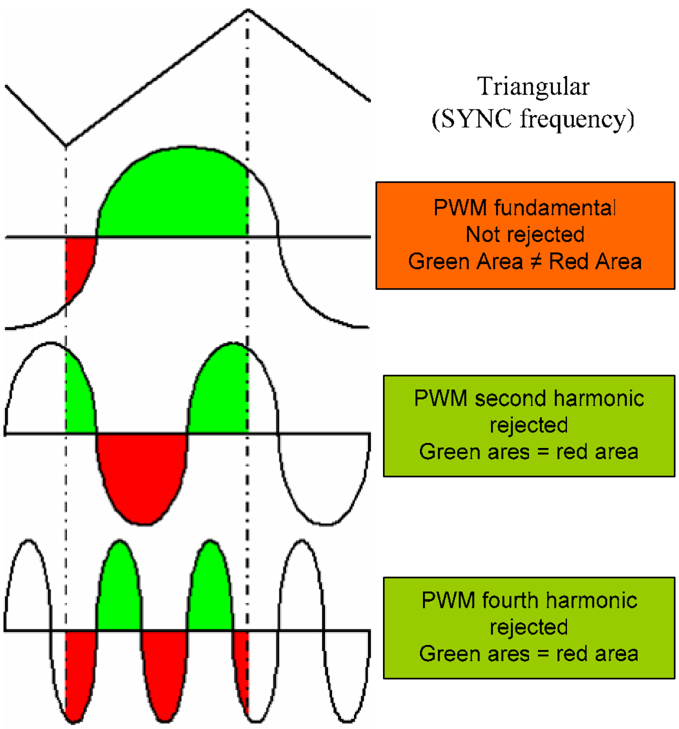


Figure 16: Even harmonic cancellation principle

As can be seen from Figure 18, the odd harmonics are rejected as a first order low pass filter with a single pole placed in f_{PWM}.
The input filter group delay in the pass-band is very low (see GD on AC electrical characteristics) due to the beneficial action of the zeroes.

The second stage samples the result of the first stage at double Sync frequency. This action can be used to fully remove the odd harmonics from the input signal.
To perform this cancellation it is necessary a shift of 90 degrees of the SYNC signal with respect to the triangular carrier edges (SYNC2).
The following timing diagrams show the principle of odd harmonics cancellation (Figure 19), in which SYNC2 allows the sampling of stage 1 output during odd harmonic zero crossings.
Odd harmonic cancellation using SYNC2 (i.e. 90 degree shifted SYNC signal) signal will introduce Tsync/4 additional propagation delay.

Anther way to obtain the same result (odd harmonics cancellation) can be achieved by controller computing the average of two consecutive PO results using SYNC1 (SYNC is in this case aligned to triangular edges, i.e. 0 degree shift).
This method is suitable for most symmetric (center aligned) PWM schemes.

For this particular PWM scheme another suitable solution is driving the IR2x77 with a half frequency SYNC signal ($f_{sync}=f_{PWM}/2$).
In this case the cut frequency of the input filter is reduced by half allowing zeroes to be put at f_{PWM} multiples (i.e. even and odd harmonics cancellation, no more computational effort needed by the controller).

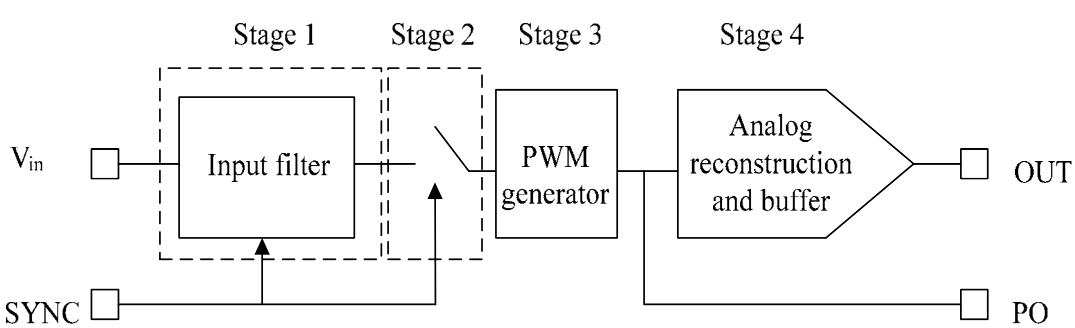


Figure 17: Simplified block diagram

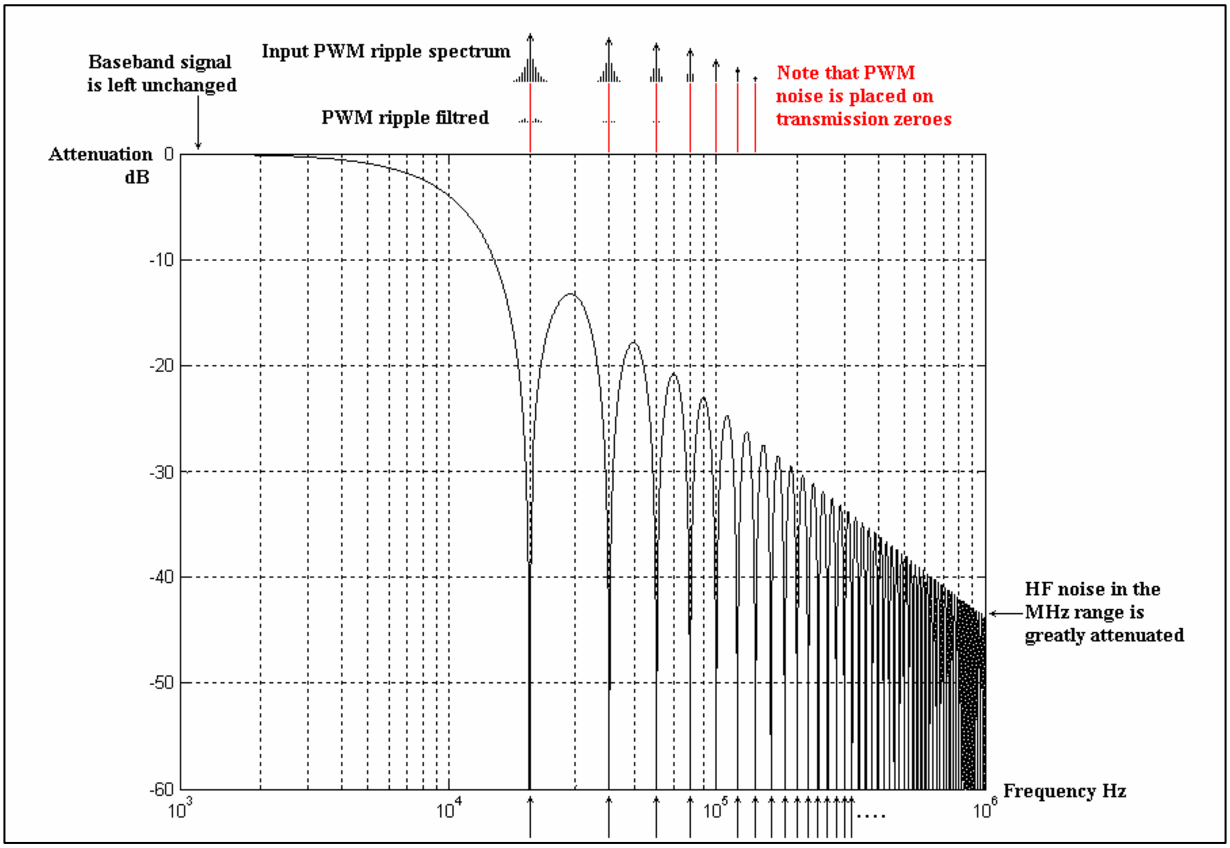


Figure 18: Input filter transfer function (10 kHz PWM)

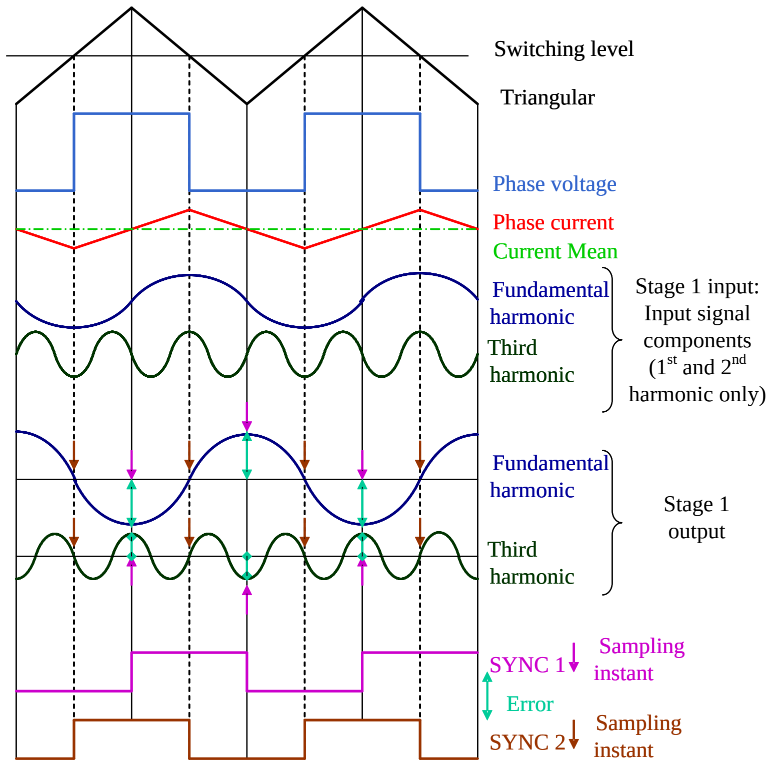


Figure 19: Even harmonic cancellation principle

1.6 Input filter gain setting

G0 and G1 pins are used to change the time constant of the integrators of the high side input filter.
To avoid internal saturation of the input filter, G0 and G1 must be connect according to SYNC frequency as shown in Table 1. A too small time constant may saturate the internal integrator, while a large time constant may reduce accuracy.
G0 and G1 do not affect the overall current sensor gain.

f_{PWM}	G0	G1
> 16 kHz *	V_B	V_B
16 / 10 kHz	V_S	V_B
10 / 6 kHz	V_B	V_S
< 6 kHz	V_S	V_S

*→ 40 kHz

Table 1: G0, G1 gain settings

2 Sizing tips

2.1 Bootstrap supply

The $V_{BS1,2,3}$ voltage provides the supply to the high side drivers circuitry of the IR2277S/IR2177S. V_{BS} supply sit on top of the V_S voltage and so it must be floating.
The bootstrap method to generate V_{BS} supply can be used with IR2277S/IR2177S current sensors. The bootstrap supply is formed by a diode and a capacitor connected as in Figure 20.

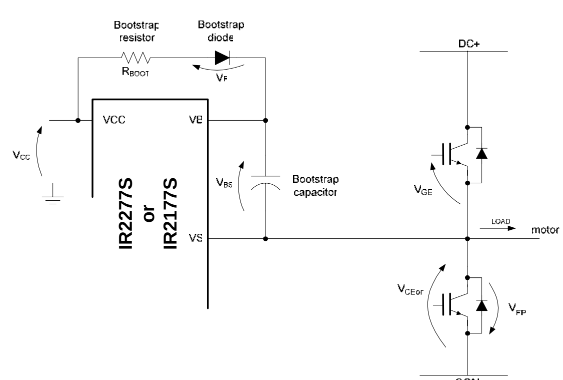


Figure 20: bootstrap supply schematic

This method has the advantage of being simple and low cost but may force some limitations on duty-cycle and on-time since they are limited by the requirement to refresh the charge in the bootstrap capacitor.
Proper capacitor choice can reduce drastically these limitations.

Bootstrap capacitor sizing

Given the maximum admitted voltage drop for V_{BS}, namely ΔV_{BS}, the influencing factors contributing to V_{BS} decrease are:

- Floating section quiescent current (***I_{QBS}***);
- Floating section leakage current (***I_{LK}***)
- Bootstrap diode leakage current (***I_{LK_DIODE}***);
- Charge required by the internal level shifters (***Q_{LS}***); typical 20nC
- Bootstrap capacitor leakage current (***I_{LK_CAP}***);
- High side on time (***T_{HON}***).

I_{LK_CAP} is only relevant when using an electrolytic capacitor and can be ignored if other types of capacitors are used. It is strongly recommend using at least one low ESR ceramic capacitor (paralleling electrolytic and low ESR ceramic may result in an efficient solution).

Then we have:

$$Q_{TOT} = Q_{LS} + (I_{QBS} + +I_{LK} + I_{LK\_DIODE} + I_{LK\_CAP}) \cdot T_{HON}$$

The minimum size of bootstrap capacitor is then:

$$C_{BOOT\min} = \frac{Q_{TOT}}{\Delta V_{BS}}$$

Some important considerations

a) <u>Voltage ripple</u>

There are three different cases making the bootstrap circuit get conductive (see Figure 20)

- $I_{LOAD} < 0$; the load current flows in the low side IGBT displaying relevant V_{CEon}

$$V_{BS} = V_{CC} - V_F - V_{CEon}$$

In this case we have the lowest value for V_{BS}. This represents the worst case for the bootstrap capacitor sizing. When the IGBT is turned off the Vs node is pushed up by the load current until the high side freewheeling diode get forwarded biased

- $I_{LOAD} = 0$; the IGBT is not loaded while being on and V_{CE} can be neglected

$$V_{BS} = V_{CC} - V_F$$

- $I_{LOAD} > 0$; the load current flows through the freewheeling diode

$$V_{BS} = V_{CC} - V_F + V_{FP}$$

In this case we have the highest value for V_{BS}. Turning on the high side IGBT, I_{LOAD} flows into it and V_S is pulled up.

b) <u>Bootstrap Resistor</u>

A resistor (R_{boot}) is placed in series with the bootstrap diode (see Figure 20) to limit the current when the bootstrap capacitor is initially charged. We suggest not exceeding some Ohms (typically 5, maximum 10 Ohms) to avoid increasing the V_{BS} time-constant. The minimum on time for charging the bootstrap capacitor or for refreshing its charge must be verified against this time-constant.

c) <u>Bootstrap Capacitor</u>

For high T_{HON} designs where an electrolytic tank capacitor is used, its ESR must be considered. This parasitic resistance develops a voltage divider with R_{boot} generating a voltage step on V_{BS} at the first charge of bootstrap capacitor. The voltage step and the related speed (dV_{BS}/dt) should be limited. As a general rule, ESR should meet the following constraint:

$$\frac{ESR}{ESR + R_{BOOT}} \cdot V_{CC} \le 3V$$

Parallel combination of small ceramic and large electrolytic capacitors is normally the best compromise, the first acting as fast charge tank for the gate charge only and limiting the dV_{BS}/dt by reducing the equivalent resistance while the second keeps the V_{BS} voltage drop inside the desired ΔV_{BS}.

d) <u>Bootstrap Diode</u>

The diode must have a BV> 600V (or 1200V depending on application) and a fast recovery time (t_{rr} < 100 ns) to minimize the amount of charge fed back from the bootstrap capacitor to V_{CC} supply.

3 PCB LAYOUT TIPS

3.1 Distance from H to L voltage

The IR2277S/IR2177S package (wide body) maximizes the distance between floating (from DC- to DC+) and low voltage pins (V_{SS}). It is strongly recommended to place components tied to floating voltage in the respective high voltage portions of the device (V_B, V_S) side.

3.2 Ground plane

Ground plane must NOT be placed under or nearby the high voltage floating side to minimize noise coupling.

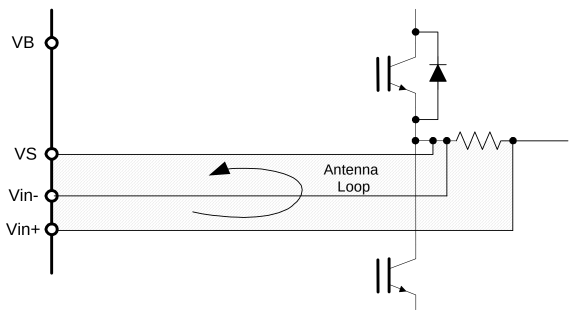


Figure 21: antenna loops

3.3 Antenna loops and inputs connection

Current loops behave like antennas able to receive EM noise. In order to reduce EM coupling loops must be reduced as much as possible. Figure 21 shows the high side shunt loops.
Moreover it is strongly suggested to use Kelvin connections for V_{in+} and V_{in-} to shunt paths and star-connect V_S to V_{in-} close to the shunt resistor as explained in Fig. 22.

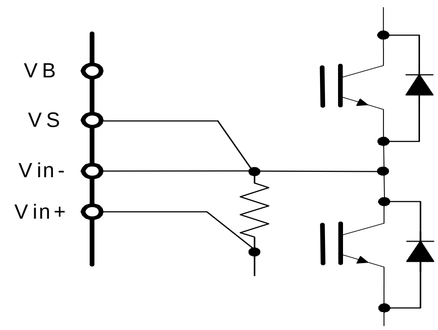
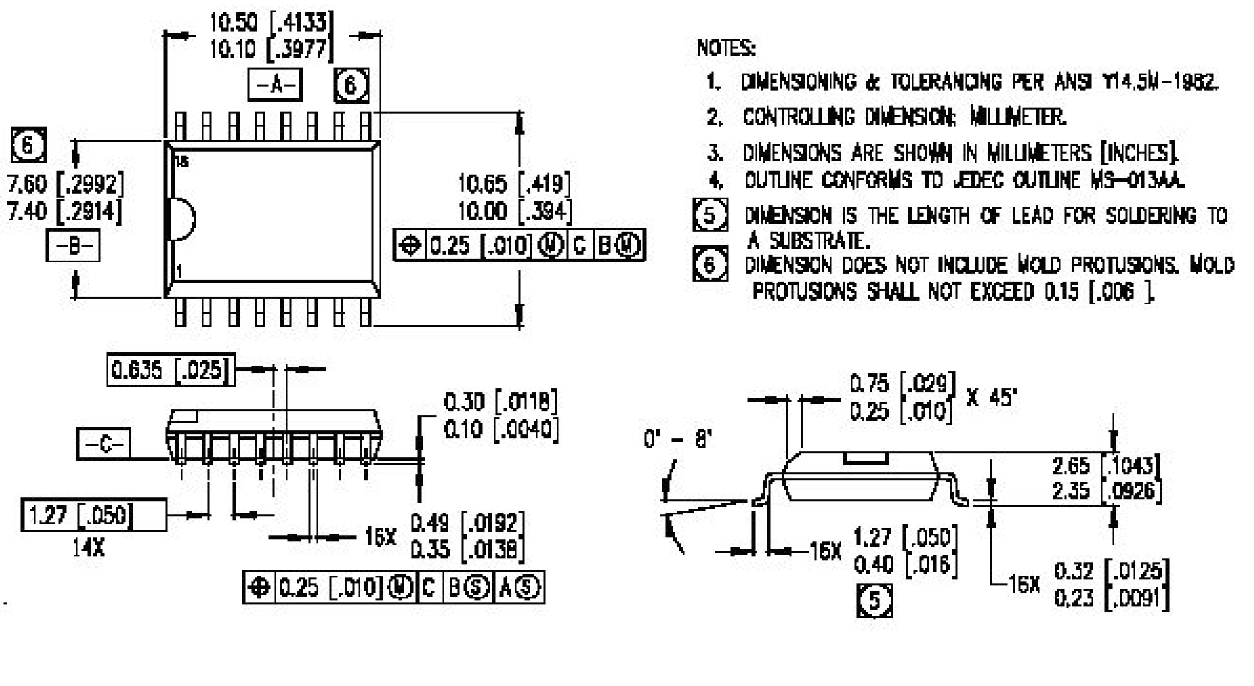


Figure 22: Recommended shunt connection

3.4 Supply capacitors

The supply capacitors must be placed as close as possible to the device pins (V_{CC} and V_{SS} for the ground tied supply, V_B and V_S for the floating supply) in order to minimize parasitic traces inductance/resistance

Case Outline



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