A Microchip Technology Company

16 Mbit (x8) Multi-Purpose Flash Plus

SST39VF1681 / SST39VF1682

Data Sheet

The SST39VF1681 / SST39VF1682 are 2M x8 CMOS Multi-Purpose Flash Plus (MPF+) manufactured with SST proprietary, high performance CMOS Super-Flash® technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39VF1681 / SST39VF1682 write (Program or Erase) with a 2.7-3.6V power supply. These devices conforms to JEDEC standard pinouts for x8 memories.

Features

- **Organized as 2M x8**
- **Single Voltage Read and Write Operations**
  - 2.7-3.6V
- **Superior Reliability**
  - Endurance: 100,000 Cycles (Typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption (typical values at 5 MHz)**
  - Active Current: 9 mA (typical)
  - Standby Current: 3 µA (typical)
  - Auto Low Power Mode: 3 µA (typical)
- **Hardware Block-Protection/WP# Input Pin**
  - Top Block-Protection (top 64 KByte) for SST39VF1682
  - Bottom Block-Protection (bottom 64 KByte) for SST39VF1681
- **Sector-Erase Capability**
  - Uniform 4 KByte sectors
- **Block-Erase Capability**
  - Uniform 64 KByte blocks
- **Chip-Erase Capability**
- **Erase-Suspend/Erase-Resume Capabilities**
- **Hardware Reset Pin (RST#)**
- **Security-ID Feature**
  - SST: 128 bits; User: 128 bits
- **Fast Read Access Time:**
  - 70 ns
- **Latched Address and Data**
- **Fast Erase and Byte-Program:**
  - Sector-Erase Time: 18 ms (typical)
  - Block-Erase Time: 18 ms (typical)
  - Chip-Erase Time: 40 ms (typical)
  - Byte-Program Time: 7 µs (typical)
- **Automatic Write Timing**
  - Internal V_{PP} Generation
- **End-of-Write Detection**
  - Toggle Bits
  - Data# Polling
- **CMOS I/O Compatibility**
- **JEDEC Standard**
  - Flash EEPROM Pinouts and Command sets
- **Packages Available**
  - 48-ball TFBGA (6mm x 8mm)
  - 48-lead TSOP (12mm x 20mm)
- **All devices are RoHS compliant**

Product Description

The SST39VF168x devices are 2M x8 CMOS Multi-Purpose Flash Plus (MPF+) manufactured with SST's proprietary, high performance CMOS SuperFlash® technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39VF168x write (Program or Erase) with a 2.7-3.6V power supply. These devices conform to JEDEC standard pinouts for x8 memories.

Featuring high performance Byte-Program, the SST39VF168x devices provide a typical Byte-Program time of 7 µsec. These devices use Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent write, they have on-chip hardware and Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with a guaranteed typical endurance of 100,000 cycles. Data retention is rated at greater than 100 years.

The SST39VF168x devices are suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, they significantly improve performance and reliability, while lowering power consumption. They inherently use less energy during Erase and Program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. These devices also improve flexibility while lowering the cost for program, data, and configuration storage applications.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

To meet high density, surface mount requirements, the SST39VF168x are offered in both 48-ball TFBGA and 48-lead TSOP packages. See Figures 2 and 3 for pin assignments.

Block Diagram

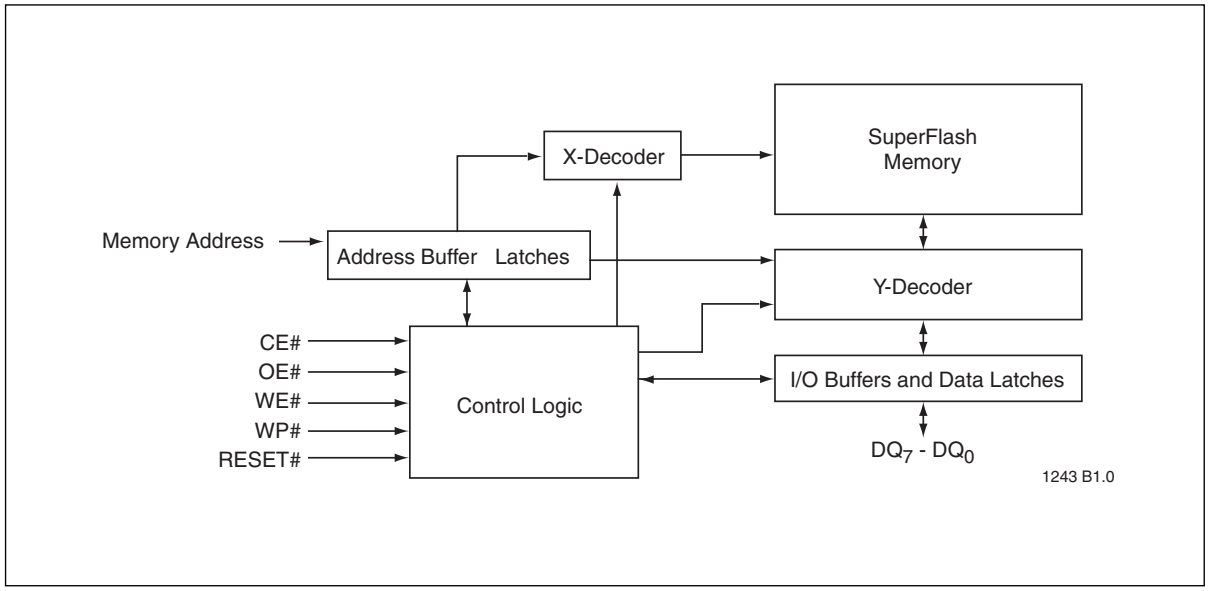

Figure 1: SST39VF1681 / SST39VF1682 Block Diagram

Pin Description

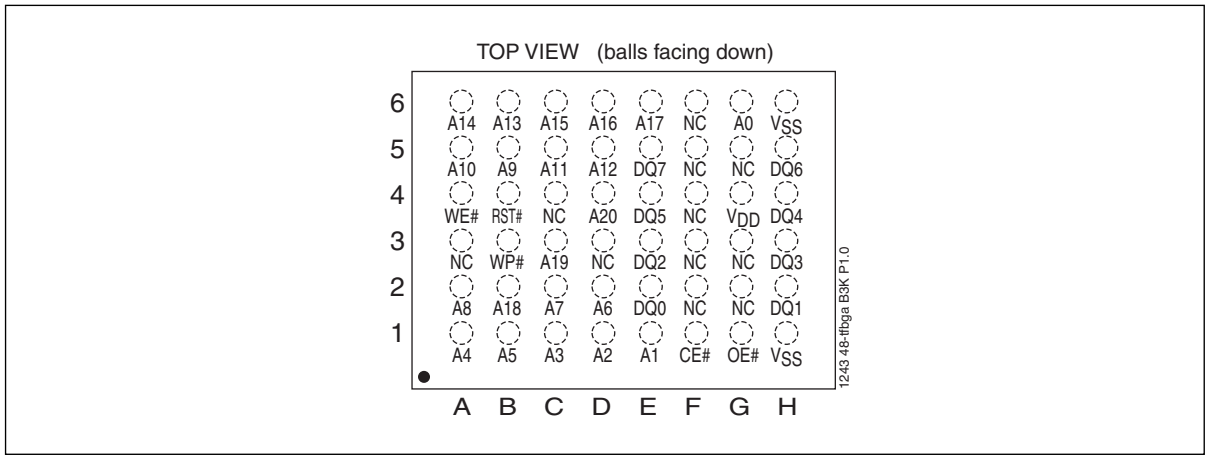

Figure 2: Pin Assignments for 48-lead TFBGA

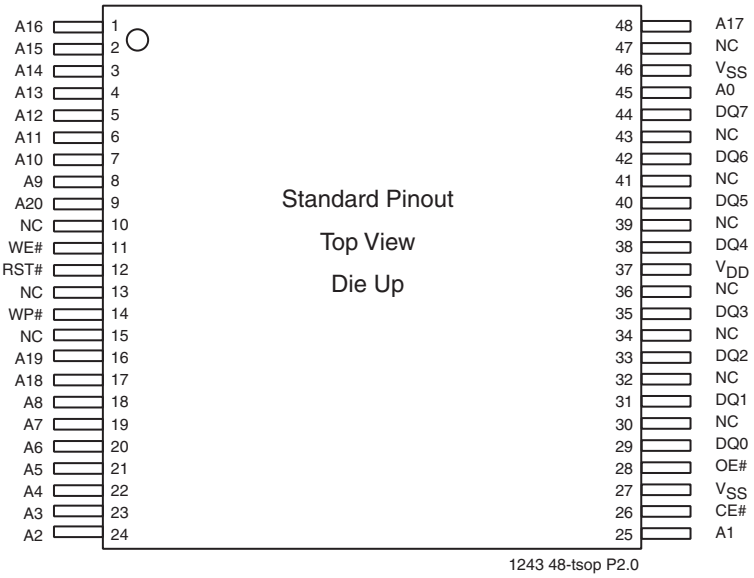

Figure 3: Pin Assignments for 48-lead TSOP

Table 1: Pin Description

Symbol	Pin Name	Functions
A_{MS}[1]-A_0	Address Inputs	To provide memory addresses. During Sector-Erase A_{MS}-A_{12} address lines will select the sector. During Block-Erase A_{MS}-A_{16} address lines will select the block.
DQ_7-DQ_0	Data Input/output	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.
WP#	Write Protect	To protect the top/bottom boot block from Erase/Program operation when grounded.
RST#	Reset	To reset and return the device to Read mode.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the Write operations.
V_{DD}	Power Supply	To provide power supply voltage: 2.7-3.6V
V_{SS}	Ground	
NC	No Connection	Unconnected pins.

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1. A_{MS} = Most significant address
   A_{MS} = A_{20} for SST39VF1681/1682

Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

The SST39VF168x also have the **Auto Low Power** mode which puts the device in a near standby mode after data has been accessed with a valid Read operation. This reduces the I_{DD} active read current from typically 9 mA to typically 3 µA. The Auto Low Power mode reduces the typical I_{DD} active read current to the range of 2 mA/MHz of Read cycle time. The device exits the Auto Low Power mode with any address transition or control signal transition used to initiate another Read cycle, with no access time penalty. Note that the device does not enter Auto-Low Power mode after power-up with CE# held steadily low, until the first address transition or CE# is driven high.

Read

The Read operation of the SST39VF168x is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 4).

Byte-Program Operation

The SST39VF168x are programmed on a byte-by-byte basis. Before programming, the sector where the byte exists must be fully erased. The Program operation is accomplished in three steps. The first step is the three-byte load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte-Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed within 10 µs. See Figures 5 and 6 for WE# and CE# controlled Program operation timing diagrams and Figure 20 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands issued during the internal Program operation are ignored. During the command sequence, WP# should be statically held high or low.

Sector/Block-Erase Operation

The Sector- (or Block-) Erase operation allows the system to erase the device on a sector-by-sector (or block-by-block) basis. The SST39VF168x offer both Sector-Erase and Block-Erase mode. The sector architecture is based on uniform sector size of 4 KByte. The Block-Erase mode is based on uniform block size of 64 KByte. The Sector-Erase operation is initiated by executing a six-byte command sequence with Sector-Erase command (50H) and sector address (SA) in the last bus cycle. The Block-Erase operation is initiated by executing a six-byte command sequence with Block-Erase command (30H) and block address (BA) in the last bus cycle. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (30H or 50H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase operation can be determined using either Data# Polling or Toggle Bit methods. See Figures 10 and 11 for

timing waveforms and Figure 24 for the flowchart. Any commands issued during the Sector- or Block-Erase operation are ignored. When WP# is low, any attempt to Sector- (Block-) Erase the protected block will be ignored. During the command sequence, WP# should be statically held high or low.

Erase-Suspend/Erase-Resume Commands

The Erase-Suspend operation temporarily suspends a Sector- or Block-Erase operation thus allowing data to be read from any memory location, or program data into any sector/block that is not suspended for an Erase operation. The operation is executed by issuing one byte command sequence with Erase-Suspend command (B0H). The device automatically enters read mode typically within 20 µs after the Erase-Suspend command had been issued. Valid data can be read from any sector or block that is not suspended from an Erase operation. Reading at address location within erase-suspended sectors/blocks will output DQ_2 toggling and DQ_6 at "1". While in Erase-Suspend mode, a Byte-Program operation is allowed except for the sector or block selected for Erase-Suspend.

To resume Sector-Erase or Block-Erase operation which has been suspended the system must issue Erase Resume command. The operation is executed by issuing one byte command sequence with Erase Resume command (30H) at any address in the last Byte sequence.

Chip-Erase Operation

The SST39VF168x provide a Chip-Erase operation, which allows the user to erase the entire memory array to the "1" state. This is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command (10H) at address AAAH in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 6 for the command sequence, Figure 10 for timing diagram, and Figure 24 for the flowchart. Any commands issued during the Chip-Erase operation are ignored. When WP# is low, any attempt to Chip-Erase will be ignored. During the command sequence, WP# should be statically held high or low.

Write Operation Status Detection

The SST39VF168x provide two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

When the SST39VF168x are in the internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce true data. Note that even though DQ_7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read DQ_7 will pro-

duce a '0'. Once the internal Erase operation is completed, DQ_7 will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-, Block- or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 7 for Data# Polling timing diagram and Figure 21 for a flowchart.

Toggle Bits (DQ6 and DQ2)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating "1"s and "0"s, i.e., toggling between 1 and 0. When the internal Program or Erase operation is completed, the DQ_6 bit will stop toggling. The device is then ready for the next operation. For Sector-, Block-, or Chip-Erase, the toggle bit (DQ_6) is valid after the rising edge of sixth WE# (or CE#) pulse. DQ_6 will be set to "1" if a Read operation is attempted on an Erase-Suspended Sector/Block. If Program operation is initiated in a sector/block not selected in Erase-Suspend mode, DQ_6 will toggle.

An additional Toggle Bit is available on DQ_2, which can be used in conjunction with DQ_6 to check whether a particular sector is being actively erased or erase-suspended. Table 2 shows detailed status bits information. The Toggle Bit (DQ_2) is valid after the rising edge of the last WE# (or CE#) pulse of Write operation. See Figure 8 for Toggle Bit timing diagram and Figure 21 for a flowchart.

Table 2: Write Operation Status

Status		DQ_7	DQ_6	DQ_2
Normal Operation	Standard Program	DQ_7#	Toggle	No Toggle
	Standard Erase	0	Toggle	Toggle
Erase-Suspend Mode	Read from Erase Suspended Sector/Block	1	1	Toggle
	Read from Non- Erase Suspended Sector/Block	Data	Data	Data
	Program	DQ_7#	Toggle	N/A

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Note: DQ_7 and DQ_2 require a valid address when reading status information.

Data Protection

The SST39VF168x provide both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Hardware Block Protection

The SST39VF1682 supports top hardware block protection, which protects the top 64 KByte block of the device. The SST39VF1681 supports bottom hardware block protection, which protects the bottom 64 KByte block of the device. The Boot Block address ranges are described in Table 3. Program and Erase operations are prevented on the 64 KByte when WP# is low. If WP# is left floating, it is internally held high via a pull-up resistor, and the Boot Block is unprotected, enabling Program and Erase operations on that block.

Table 3: Boot Block Address Ranges

Product	Address Range
Bottom Boot Block	
SST39VF1681	000000H-00FFFFH
Top Boot Block	
SST39VF1682	1F0000H-1FFFFFH

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Hardware Reset (RST#)

The RST# pin provides a hardware method of resetting the device to read array data. When the RST# pin is held low for at least T_{RP}, any in-progress operation will terminate and return to Read mode. When no internal Program/Erase operation is in progress, a minimum period of T_{RHR} is required after RST# is driven high before a valid Read can take place (see Figure 16).

The Erase or Program operation that has been interrupted needs to be re-initiated after the device resumes normal operation mode to ensure data integrity.

Software Data Protection (SDP)

The SST39VF168x provide the JEDEC approved Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte sequence. These devices are shipped with the Software Data Protection permanently enabled. See Table 6 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode within T_{RC}.

Common Flash Memory Interface (CFI)

The SST39VF168x also contain the CFI information to describe the characteristics of the device. In order to enter the CFI Query mode, the system must write three-byte sequence, same as product ID entry command with 98H (CFI Query command) to address AAAH in the last byte sequence. Once the device enters the CFI Query mode, the system can read CFI data at the addresses given in Tables 7 through 9. The system must write the CFI Exit command to return to Read mode from the CFI Query mode.

Product Identification

The Product Identification mode identifies the devices as the SST39VF1681 and SST39VF1682, and manufacturer as SST. Users may use the software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, see Table 6 for software operation, Figure 12 for the software ID Entry and Read timing diagram, and Figure 22 for the software ID Entry command sequence flowchart.

Table 4: Product Identification

	Address	Data
Manufacturer's ID	0000H	BFH
Device ID		
SST39VF1681	0001H	C8H
SST39VF1682	0001H	C9H

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Product Identification Mode Exit/CFI Mode Exit

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the software ID Exit command sequence, which returns the device to the Read mode. This command may also be used to reset the device to the Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. Please note that the software ID Exit/CFI Exit command is ignored during an internal Program or Erase operation. See Table 6 for software command codes, Figure 14 for timing waveform, and Figures 22 and 23 for flowcharts.

Security ID

The SST39VF168x devices offer a 256-bit Security ID space which is divided into two 128-bit segments. The first segment is programmed and locked at SST with a random 128-bit number. The user segment is left un-programmed for the customer to program as desired.

To program the user segment of the Security ID, the user must use the Security ID Byte-Program command. To detect end-of-write for the SEC ID, read the toggle bits. Do not use Data# Polling. Once this is complete, the Sec ID should be locked using the User Sec ID Program Lock-Out. This disables any future corruption of this space. Note that regardless of whether or not the Sec ID is locked, neither Sec ID segment can be erased.

The Security ID space can be queried by executing a three-byte command sequence with Enter-Sec-ID command (88H) at address AAAH in the last byte sequence. Execute the Exit-Sec-ID command to exit this mode. Refer to Table 6 for more details.

Operations

Table 5: Operation Modes Selection

Mode	CE#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Program	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Erase	V_{IL}	V_{IH}	V_{IL}	X[1]	Sector or block address, XXH for Chip-Erase
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{OUT}	X
	X	X	V_{IH}	High Z/ D_{OUT}	X
Product Identification					
Software Mode	V_{IL}	V_{IL}	V_{IH}		See Table 6

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1. X can be V_{IL} or V_{IH}, but no other value.

Table 6: Software Command Sequence

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data
Byte-Program	AAAH	AAH	555H	55H	AAAH	A0H	BA[2]	Data				
Sector-Erase	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	SA_X[3]	50H
Block-Erase	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	BA_X[3]	30H
Chip-Erase	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	AAAH	10H
Erase-Suspend	XXXXH	B0H										
Erase-Resume	XXXXH	30H										
Query Sec ID[4]	AAAH	AAH	555H	55H	AAAH	88H						
User Security ID Byte-Program	AAAH	AAH	555H	55H	AAAH	A5H	BA[5]	Data				
User Security ID Program Lock-Out	AAAH	AAH	555H	55H	AAAH	85H	XXH[5]	00H				
Software ID Entry[6,7]	AAAH	AAH	555H	55H	AAAH	90H						
CFI Query Entry	AAAH	AAH	555H	55H	AAAH	98H						
Software ID Exit[8,9] /CFI Exit/Sec ID Exit	AAAH	AAH	555H	55H	AAAH	F0H						
Software ID Exit[8,9] /CFI Exit/Sec ID Exit	XXH	F0H										

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1. Address format A_{11}-A_0 (Hex).
   Addresses A_{20}-A_{12} can be V_{IL} or V_{IH}, but no other value, for Command sequence for SST39VF1681/1682.
2. BA = Program Byte Address
3. SA_X for Sector-Erase; uses A_{MS}-A_{12} address lines
   BA_X, for Block-Erase; uses A_{MS}-A_{16} address lines
   A_{MS} = Most significant address
   A_{MS} = A_{20} for SST39VF1681/1682

4. With A_{MS}-A_5 = 0; Sec ID is read with A_4-A_0,
   SST ID is read with A_4 = 0 (Address range = 00000H to 0000FH),
   User ID is read with A_4 = 1 (Address range = 00010H to 0001FH).
   Lock Status is read with A_7-A_0 = 0000FFH. Unlocked: DQ_3 = 1 / Locked: DQ_3 = 0.
5. Valid Byte Addresses for Sec ID are from 000000H-00000FH and 000020H-00002FH.
6. The device does not remain in Software Product ID Mode if powered down.
7. With A_{MS}-A_1 =0; SST Manufacturer ID = 00BFH, is read with A_0 = 0,
   SST39VF1681 Device ID = C8H, is read with A_0 = 1,
   SST39VF1682 Device ID = C9H, is read with A_0 = 1,
   A_{MS} = Most significant address
   A_{MS} = A_{20} for SST39VF1681/1682
8. Both Software ID Exit operations are equivalent
9. If users never lock after programming, Sec ID can be programmed over the previously unprogrammed bits (data=1) using the Sec ID mode again (the programmed “0” bits cannot be reversed to “1”).

Table 7: CFI Query Identification String[1]

Address	Data	Data
10H	51H	Query Unique ASCII string “QRY”
11H	52H	
12H	59H	
13H	01H	Primary OEM command set
14H	07H	
15H	00H	Address for Primary Extended Table
16H	00H	
17H	00H	Alternate OEM command set (00H = none exists)
18H	00H	
19H	00H	Address for Alternate OEM extended Table (00H = none exits)
1AH	00H	

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1. Refer to CFI publication 100 for more details.

Table 8: System Interface Information

Address	Data	Data
1BH	27H	V_{DD} Min (Program/Erase) DQ_7-DQ_4: Volts, DQ_3-DQ_0: 100 millivolts
1CH	36H	V_{DD} Max (Program/Erase) DQ_7-DQ_4: Volts, DQ_3-DQ_0: 100 millivolts
1DH	00H	V_{PP} min. (00H = no V_{PP} pin)
1EH	00H	V_{PP} max. (00H = no V_{PP} pin)
1FH	03H	Typical time out for Byte-Program 2^N µs (2^3 = 8 µs)
20H	00H	Typical time out for min. size buffer program 2^N µs (00H = not supported)
21H	04H	Typical time out for individual Sector/Block-Erase 2^N ms (2^4 = 16 ms)
22H	05H	Typical time out for Chip-Erase 2^N ms (2^5 = 32 ms)
23H	01H	Maximum time out for Byte-Program 2^N times typical (2^1 x 2^3 = 16 µs)
24H	00H	Maximum time out for buffer program 2^N times typical
25H	01H	Maximum time out for individual Sector/Block-Erase 2^N times typical (2^1 x 2^4 = 32 ms)
26H	01H	Maximum time out for Chip-Erase 2^N times typical (2^1 x 2^5 = 64 ms)

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Table 9: Device Geometry Information

Address	Data	Data
27H	15H	Device size = 2^N Bytes (15H = 21; 2^{21} = 2 MByte)
28H	00H	Flash Device Interface description; 00H = x8-only asynchronous interface
29H	00H	
2AH	00H	Maximum number of byte in multi-byte write = 2^N (00H = not supported)
2BH	00H	
2CH	02H	Number of Erase Sector/Block sizes supported by device
2DH	FFH	Sector Information (y + 1 = Number of sectors; z x 256B = sector size)
2EH	01H	y = 511 + 1 = 512 sectors (01FF = 511
2FH	10H	
30H	00H	z = 16 x 256 Bytes = 4 KByte/sector (0010H = 16)
31H	1FH	Block Information (y + 1 = Number of blocks; z x 256B = block size)
32H	00H	y = 31 + 1 = 32 blocks (1F = 31)
33H	00H	
34H	01H	z = 256 x 256 Bytes = 64 KByte/block (0100H = 256)

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Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -2.0V to V_{DD}+2.0V
Voltage on A_9 Pin to Ground Potential . . . . . -0.5V to 13.2V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) . . . . . 240°C
Output Short Circuit Current[1] . . . . . 50 mA

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

Table 10: Operating Range

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	2.7-3.6V
Industrial	-40°C to +85°C	2.7-3.6V

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Table 11: AC Conditions of Test[1]

Input Rise/Fall Time	Output Load
5ns	C_L = 30 pF

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1. See Figures 18 and 19

Table 12: DC Operating Characteristics V_{DD} = 2.7-3.6V[1]

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	Power Supply Current Read[3]		18	mA	Address input=V_{ILT}/V_{IHT}[2], at f=5 MHz, V_{DD}=V_{DD} Max CE#=V_{IL}, OE#=WE#=V_{IH}, all I/Os open
	Program and Erase		35	mA	CE#=WE#=V_{IL}, OE#=V_{IH}
I_{SB}	Standby V_{DD} Current		20	µA	CE#=V_{IHC}, V_{DD}=V_{DD} Max
I_{ALP}	Auto Low Power		20	µA	CE#=V_{ILC}, V_{DD}=V_{DD} Max All inputs=V_{SS} or V_{DD}, WE#=V_{IHC}
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LIW}	Input Leakage Current on WP# pin and RST#		10	µA	WP#=GND to V_{DD} or RST#=GND to V_{DD}
I_{LO}	Output Leakage Current		10	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IL}	Input Low Voltage		0.8	V	V_{DD}=V_{DD} Min
V_{ILC}	Input Low Voltage (CMOS)		0.3	V	V_{DD}=V_{DD} Max
V_{IH}	Input High Voltage	0.7V_{DD}		V	V_{DD}=V_{DD} Max
V_{IHC}	Input High Voltage (CMOS)	V_{DD}-0.3		V	V_{DD}=V_{DD} Max
V_{OL}	Output Low Voltage		0.2	V	I_{OL}=100 µA, V_{DD}=V_{DD} Min
V_{OH}	Output High Voltage	V_{DD}-0.2		V	I_{OH}=-100 µA, V_{DD}=V_{DD} Min

T12.8 25040

1. Typical conditions for the Active Current shown on the front page of the data sheet are average values at 25°C (room temperature), and V_{DD} = 3V. Not 100% tested.
2. See Figure 18
3. The I_{DD} current listed is typically less than 2mA/MHz, with OE# at V_{IH}. Typical V_{DD} is 3V.

Table 13: Recommended System Power-up Timings

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Program/Erase Operation	100	µs

T13.0 25040

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 14: Capacitance (Ta = 25°C, f=1 MHz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

T14.0 25040

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 15: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1,2]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

T15.2 25040

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. N_{END} endurance rating is qualified as a 10,000 cycle minimum for the whole device. A sector- or block-level rating would result in a higher minimum specification.

AC Characteristics

Table 16: Read Cycle Timing Parameters V_{DD} = 2.7-3.6V

Symbol	Parameter	SST39VF168x-70		Units
		Min	Max	
T_{RC}	Read Cycle Time	70		ns
T_{CE}	Chip Enable Access Time		70	ns
T_{AA}	Address Access Time		70	ns
T_{OE}	Output Enable Access Time		35	ns
T_{CLZ}[1]	CE# Low to Active Output	0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		ns
T_{CHZ}[1]	CE# High to High-Z Output		20	ns
T_{OHZ}[1]	OE# High to High-Z Output		20	ns
T_{OH}[1]	Output Hold from Address Change	0		ns
T_{RP}[1]	RST# Pulse Width	500		ns
T_{RHR}[1]	RST# High before Read	50		ns
T_{RY}[1,2]	RST# Pin Low to Read Mode		20	µs

T16.1 25040

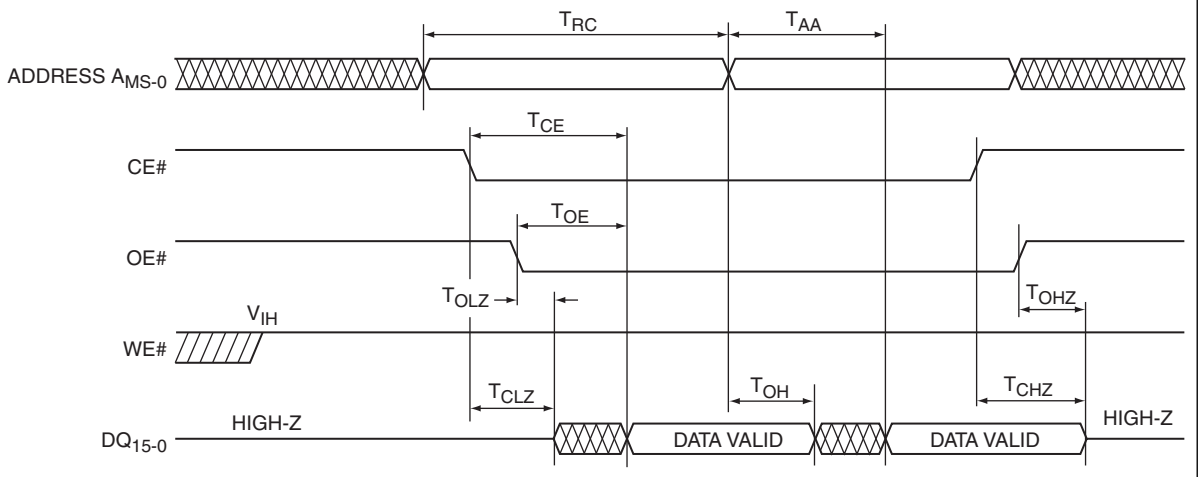
1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. This parameter applies to Sector-Erase, Block-Erase, and Program operations. This parameter does not apply to Chip-Erase operations.

Table 17: Program/Erase Cycle Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{BP}	Byte-Program Time		10	µs
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	30		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	10		ns
T_{CP}	CE# Pulse Width	40		ns
T_{WP}	WE# Pulse Width	40		ns
T_{WPH}[1]	WE# Pulse Width High	30		ns
T_{CPH}[1]	CE# Pulse Width High	30		ns
T_{DS}	Data Setup Time	30		ns
T_{DH}[1]	Data Hold Time	0		ns
T_{IDA}[1]	Software ID Access and Exit Time	150		ns
T_{SE}	Sector-Erase		25	ms
T_{BE}	Block-Erase		25	ms
T_{SCE}	Chip-Erase		50	ms

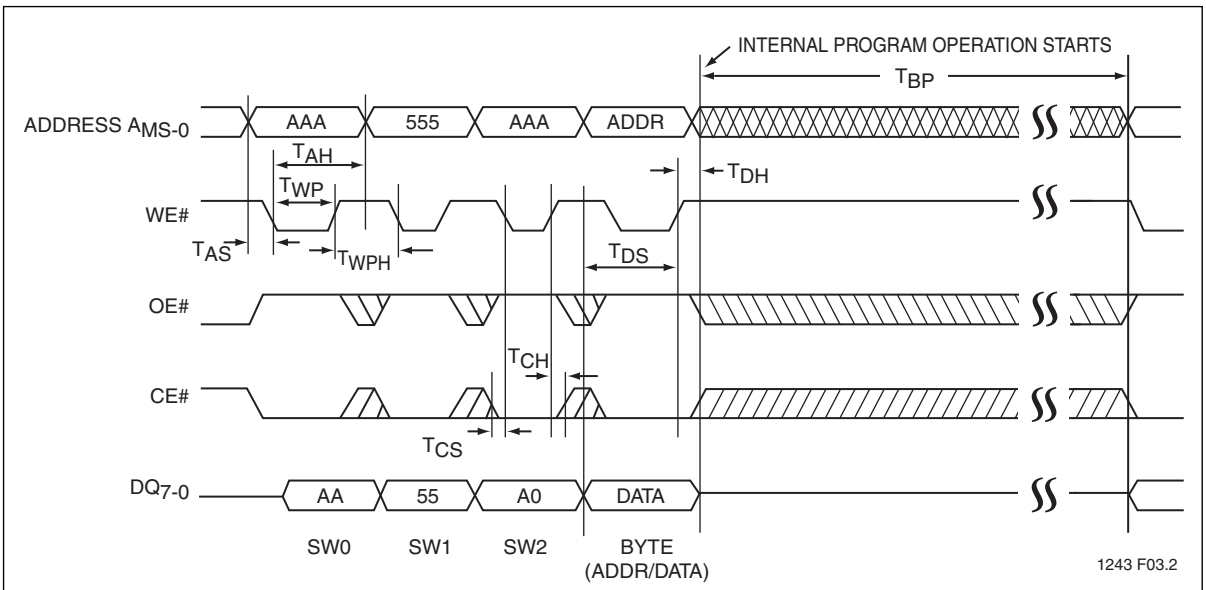
T17.0 25040

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



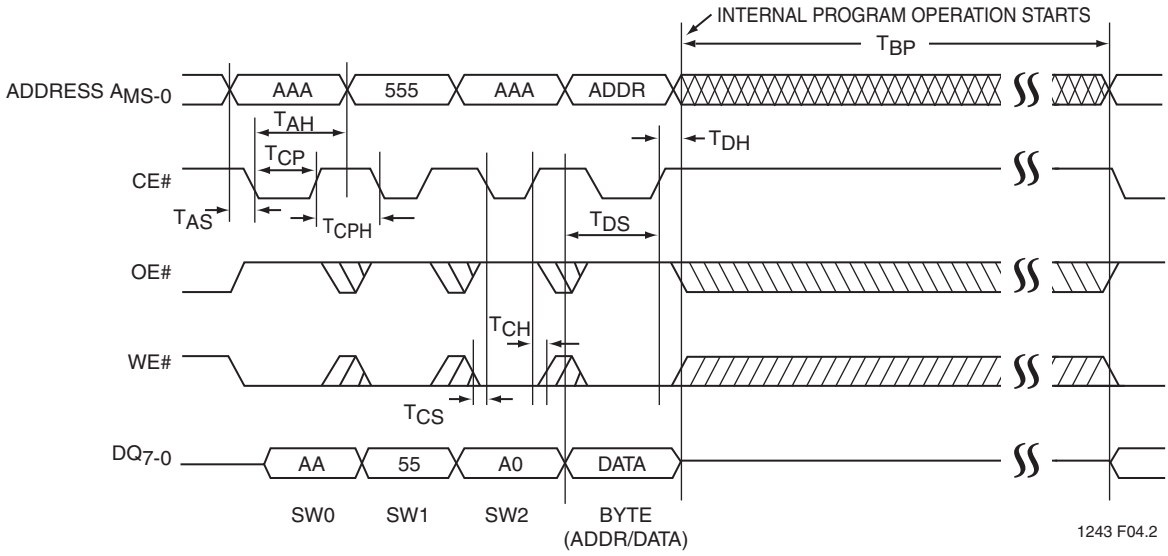
Note: A_{MS} = Most Significant Address
$A_{MS} = A_{20}$ for SST39VF168x

Figure 4: Read Cycle Timing Diagram



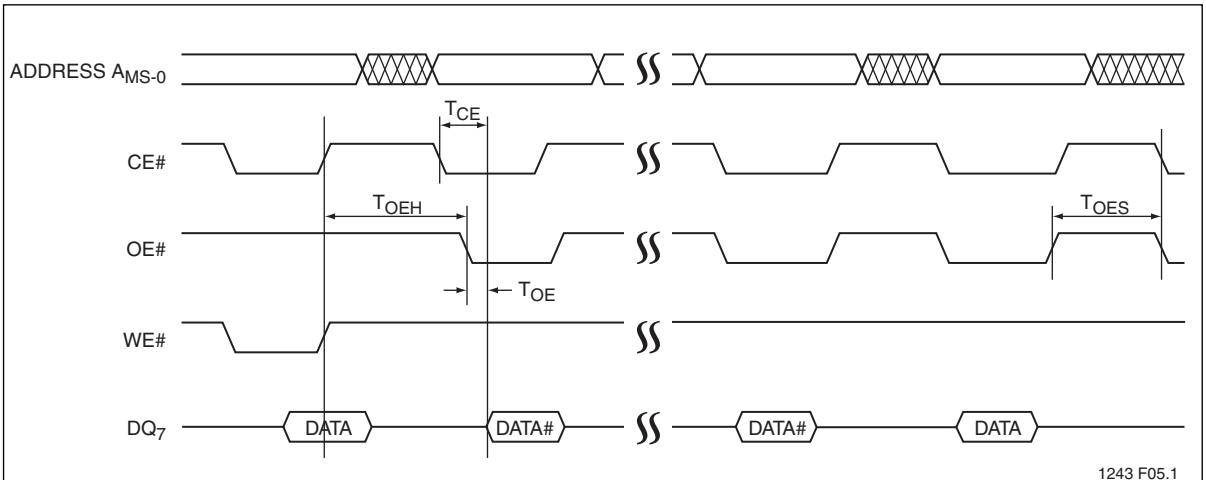
Note: A_{MS} = Most Significant Address
$A_{MS} = A_{20}$ for SST39VF168x
WP# must be held in proper logic state (V_{IL} or V_{IH}) 1 µs prior to and 1 µs after the command sequence.
X can be V_{IL} or V_{IH}, but no other value.

Figure 5: WE# Controlled Program Cycle Timing Diagram



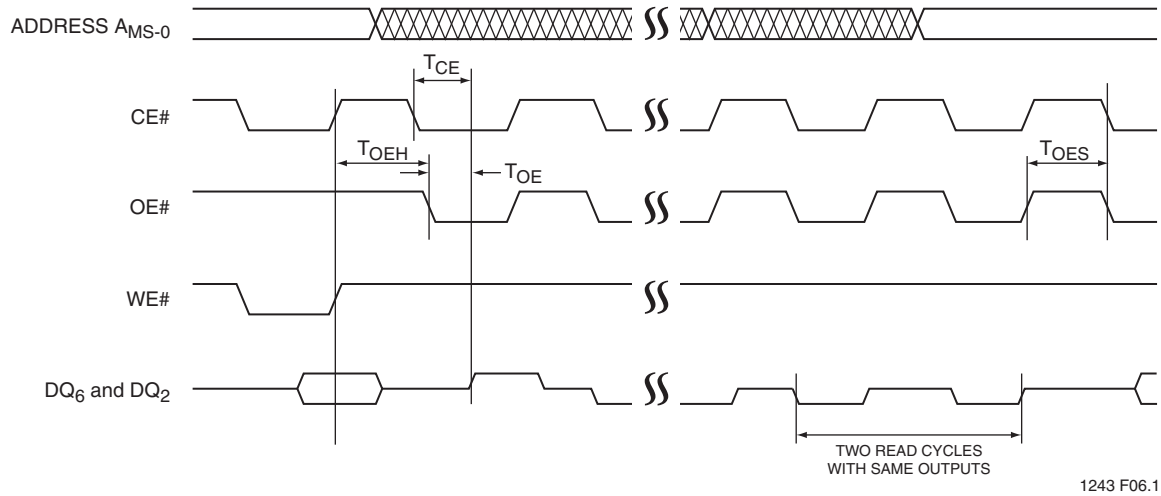
Note: A_{MS} = Most Significant Address
$A_{MS} = A_{20}$ for SST39VF168x
WP# must be held in proper logic state (V_{IL} or V_{IH}) 1 µs prior to and 1 µs after the command sequence.
X can be V_{IL} or V_{IH}, but no other value.

Figure 6: CE# Controlled Program Cycle Timing Diagram



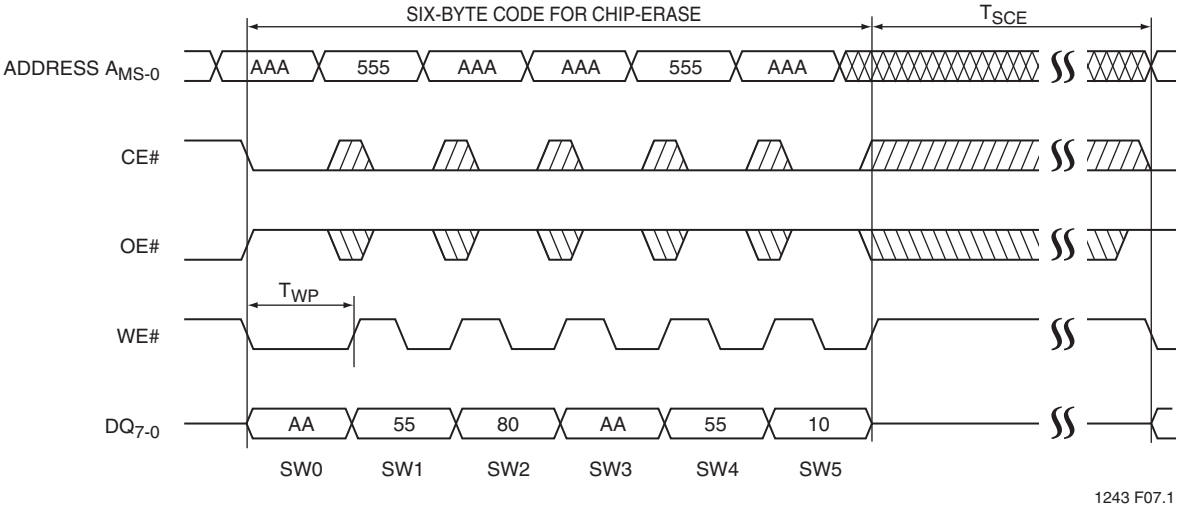
Note: A_{MS} = Most Significant Address
$A_{MS} = A_{20}$ for SST39VF168x

Figure 7: Data# Polling Timing Diagram



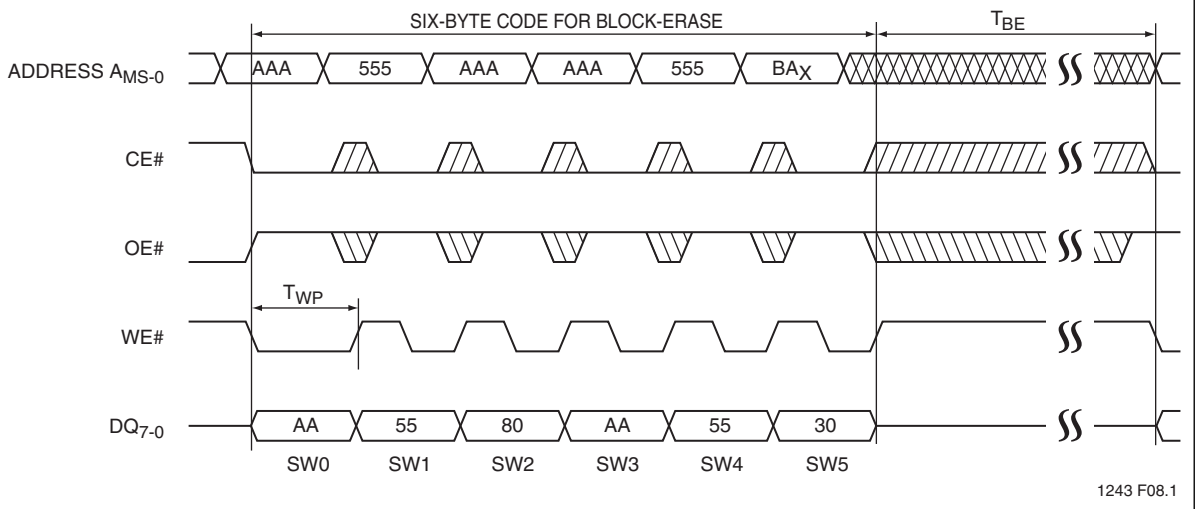
Note: A_{MS} = Most Significant Address
$A_{MS} = A_{20}$ for SST39VF168x

Figure 8: Toggle Bits Timing Diagram



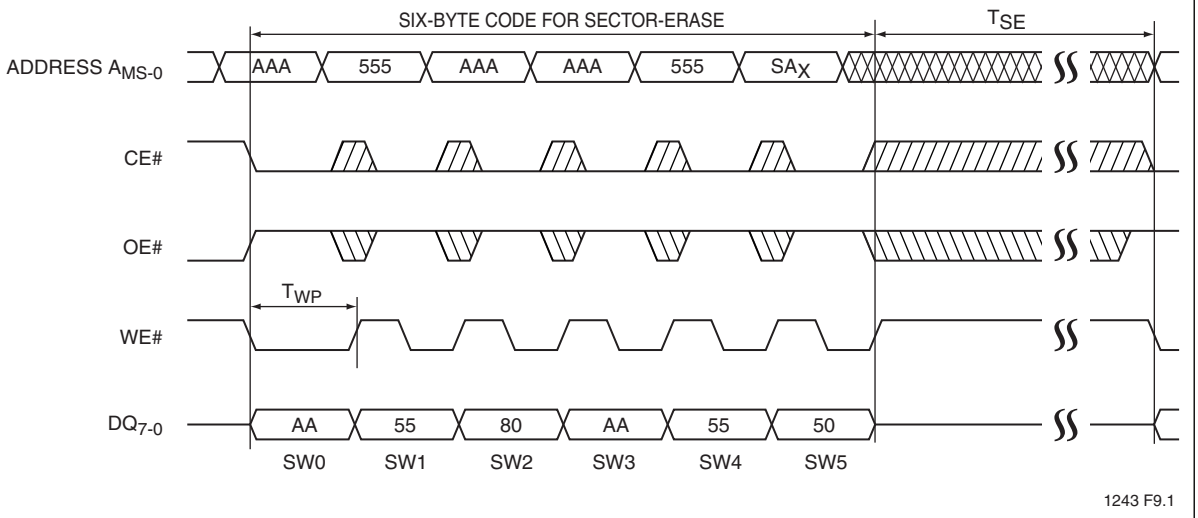
Note: This device also supports CE# controlled Chip-Erase operation.
The WE# and CE# signals are interchangeable as long as minimum timings are meet. (See Table 17.)
A_{MS} = Most Significant Address
$A_{MS} = A_{20}$ for SST39VF168x
WP# must be held in proper logic state (V_{IL} or V_{IH}) 1 µs prior to and 1 µs after the command sequence.
X can be V_{IL} or V_{IH}, but no other value.

Figure 9: WE# Controlled Chip-Erase Timing Diagram



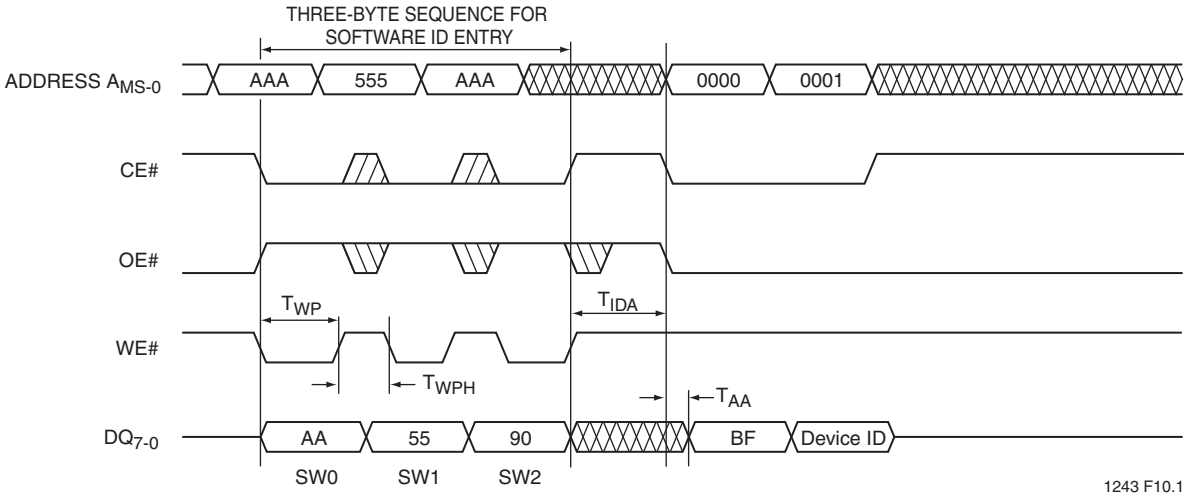
Note: This device also supports CE# controlled Chip-Erase operation.
The WE# and CE# signals are interchangeable as long as minimum timings are meet. (See Table 17.)
BA_X = Block Address
A_{MS} = Most Significant Address
A_{MS} = A_{20} for SST39VF168x
WP# must be held in proper logic state (V_{IL} or V_{IH}) 1 µs prior to and 1 µs after the command sequence.
X can be V_{IL} or V_{IH}, but no other value.

Figure 10: WE# Controlled Block-Erase Timing Diagram



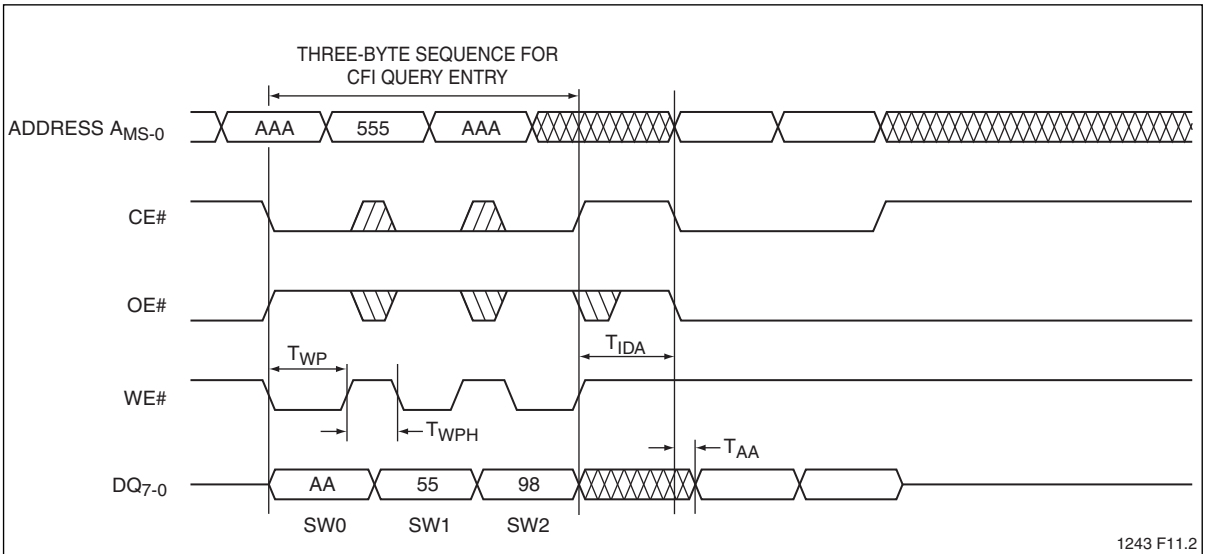
Note: This device also supports CE# controlled Chip-Erase operation.
The WE# and CE# signals are interchangeable as long as minimum timings are meet. (See Table 17.)
SA_X = Sector Address
A_{MS} = Most Significant Address
A_{MS} = A_{20} for SST39VF168x
WP# must be held in proper logic state (V_{IL} or V_{IH}) 1 µs prior to and 1 µs after the command sequence.
X can be V_{IL} or V_{IH}, but no other value.

Figure 11: WE# Controlled Sector-Erase Timing Diagram



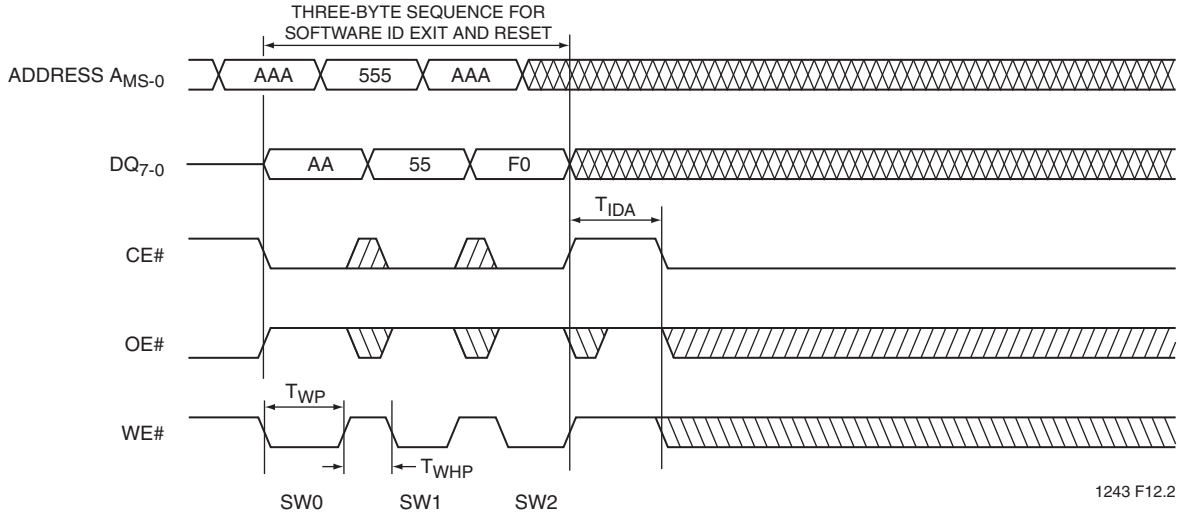
Note: Device ID - See Table 4 on page 9
A_{MS} = Most Significant Address
A_{MS} = A_{20} for SST39VF168x
WP# must be held in proper logic state (V_{IL} or V_{IH}) 1 µs prior to and 1 µs after the command sequence.
X can be V_{IL} or V_{IH}, but no other value.

Figure 12: Software ID Entry and Read



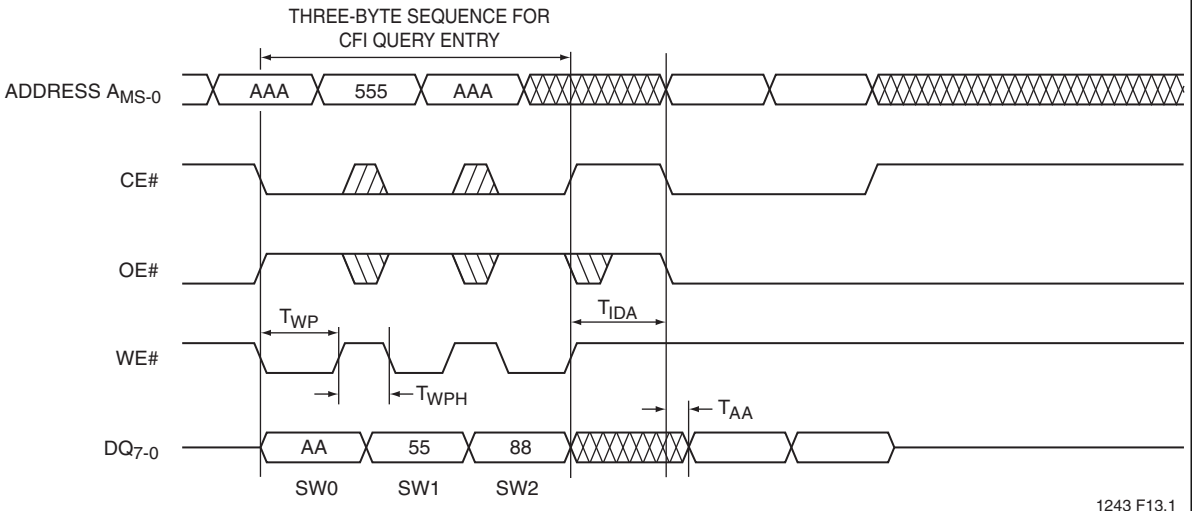
Note: A_{MS} = Most Significant Address
A_{MS} = A_{20} for SST39VF168x
WP# must be held in proper logic state (V_{IL} or V_{IH}) 1 µs prior to and 1 µs after the command sequence.
X can be V_{IL} or V_{IH}, but no other value.

Figure 13: CFI Query Entry and Read



Note: A_{MS} = Most Significant Address
$A_{MS} = A_{20}$ for SST39VF168x
WP# must be held in proper logic state (V_{IL} or V_{IH}) 1 µs prior to and 1 µs after the command sequence.
X can be V_{IL} or V_{IH}, but no other value.

Figure 14: Software ID Exit/CFI Exit



Note: A_{MS} = Most Significant Address
$A_{MS} = A_{20}$ for SST39VF168x
WP# must be held in proper logic state (V_{IL} or V_{IH}) 1 µs prior to and 1 µs after the command sequence.
X can be V_{IL} or V_{IH}, but no other value.

Figure 15: Sec ID Entry

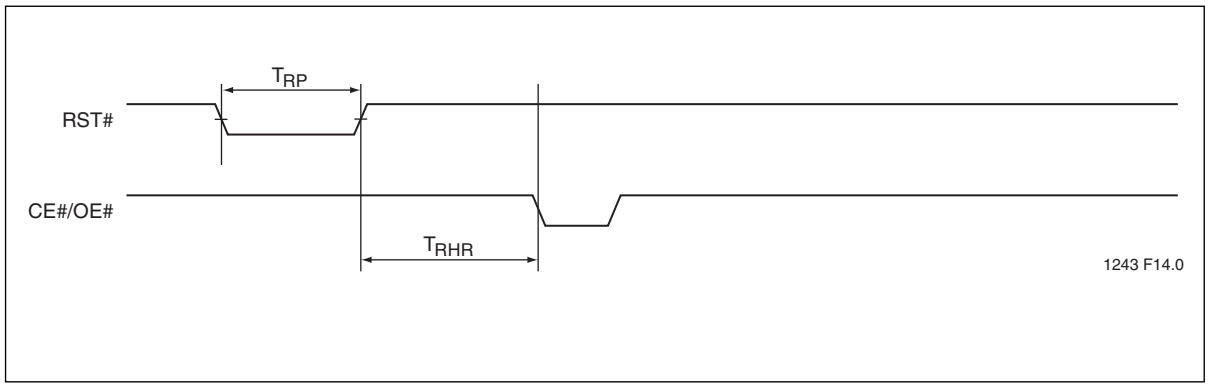


Figure 16: RST# Timing Diagram (When no internal operation is in progress)

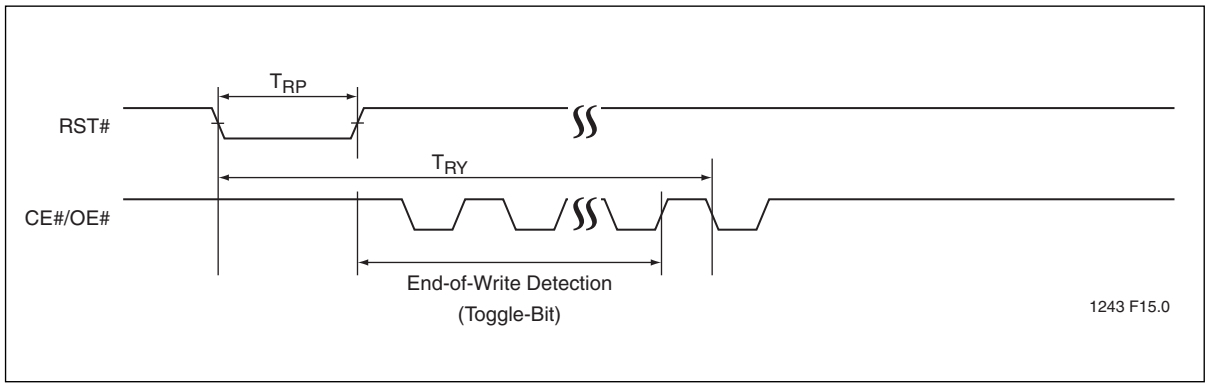
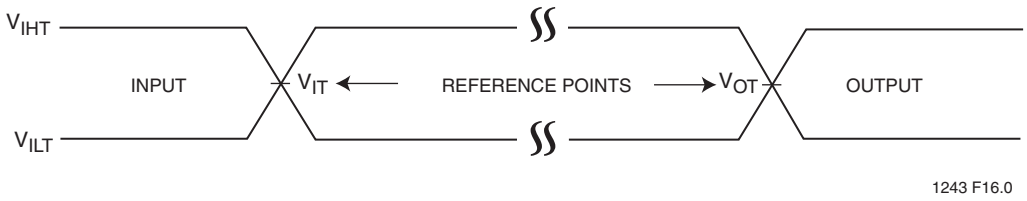


Figure 17: RST# Timing Diagram (During Program or Erase operation)



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

Figure 18: AC Input/Output Reference Waveforms

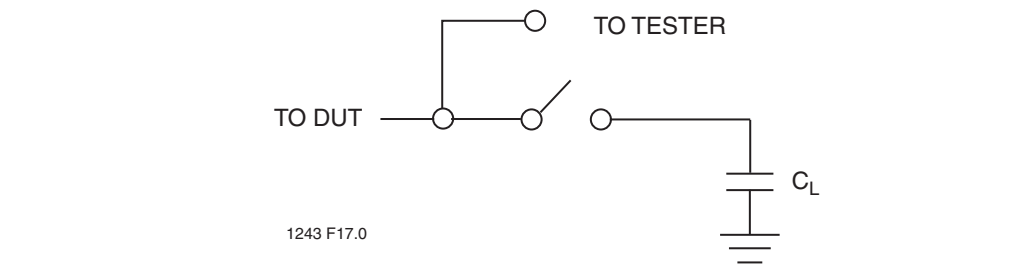


Figure 19: A Test Load Example

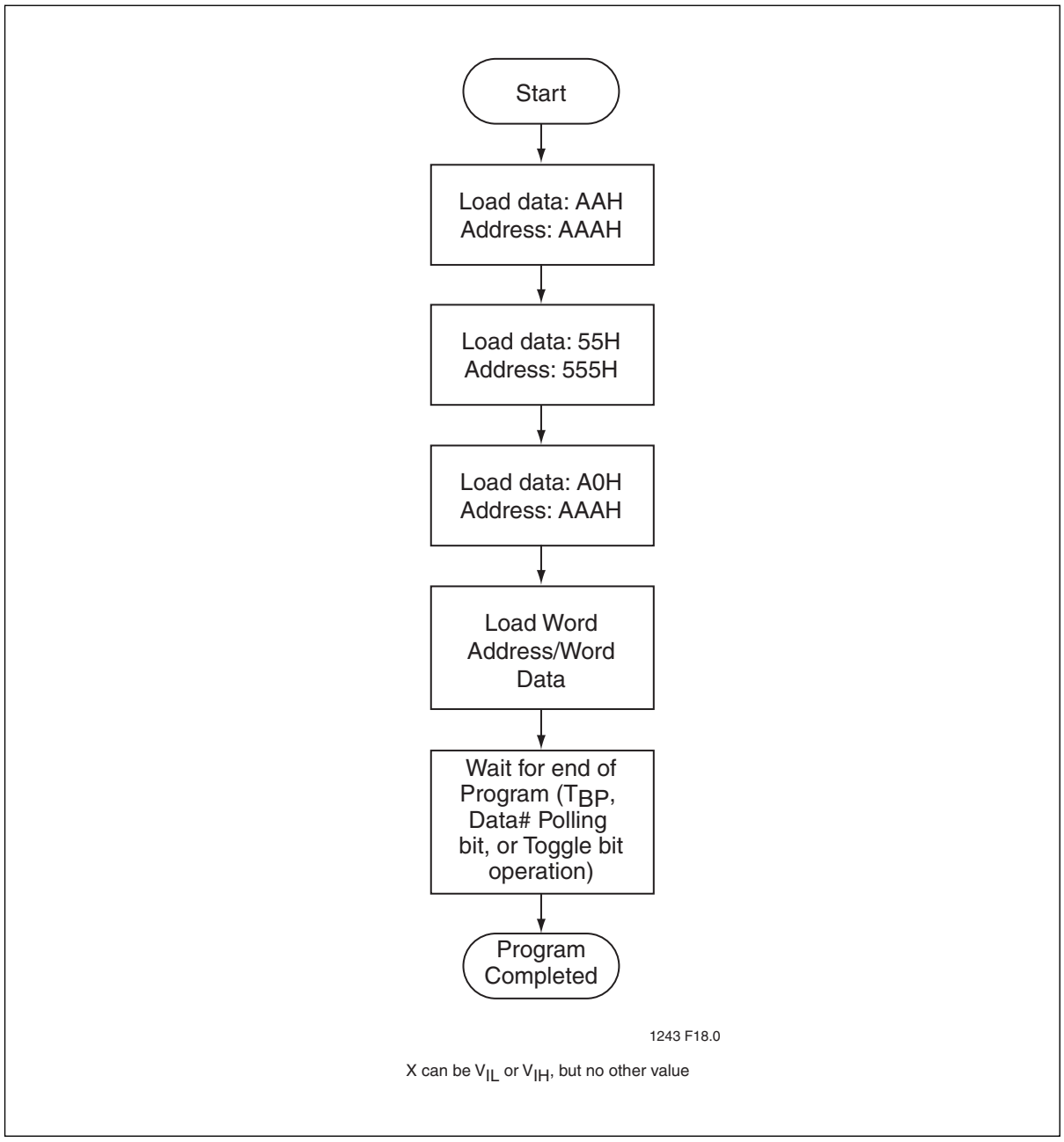


Figure 20: Byte-Program Algorithm

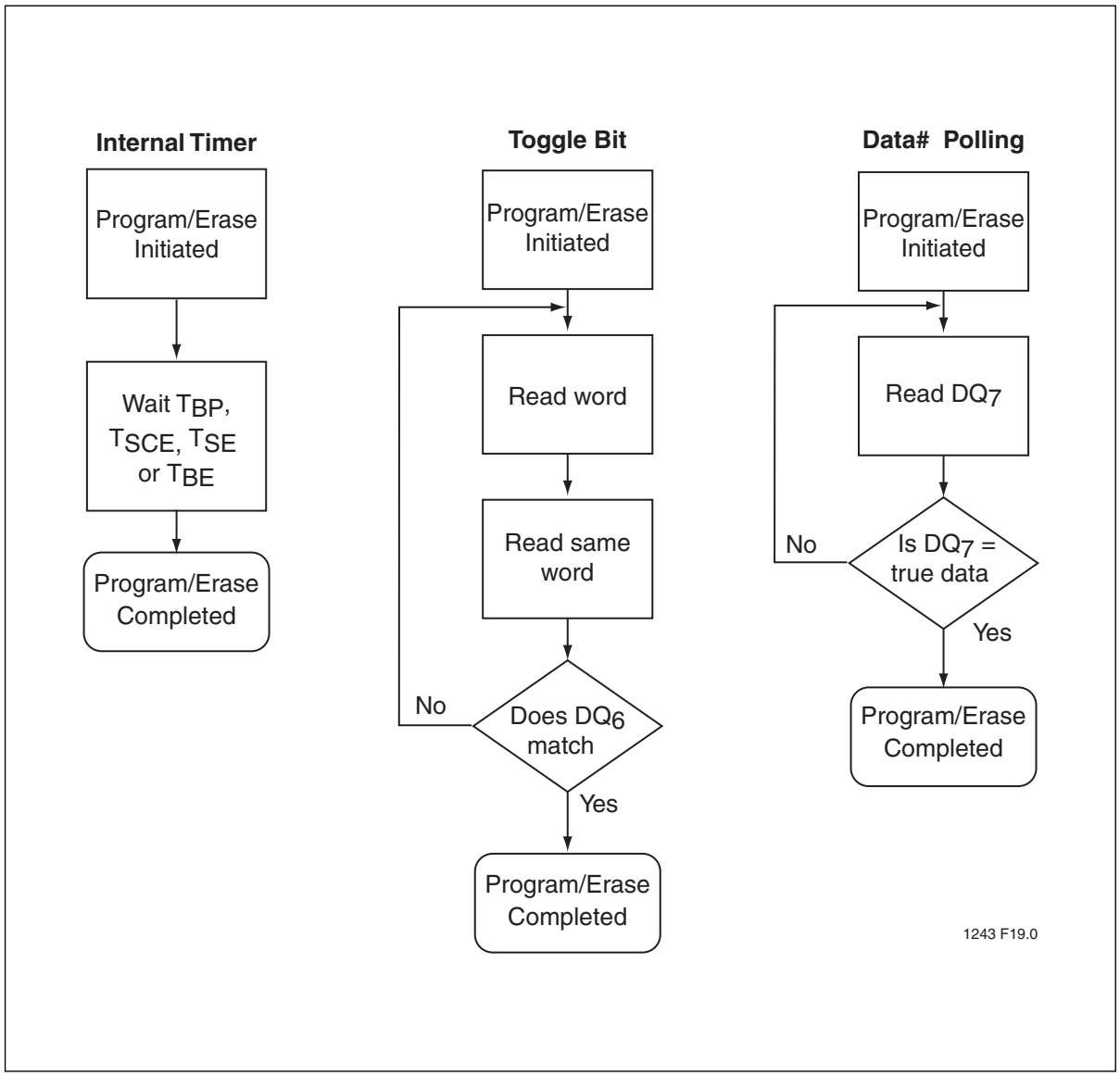


Figure 21: Wait Options

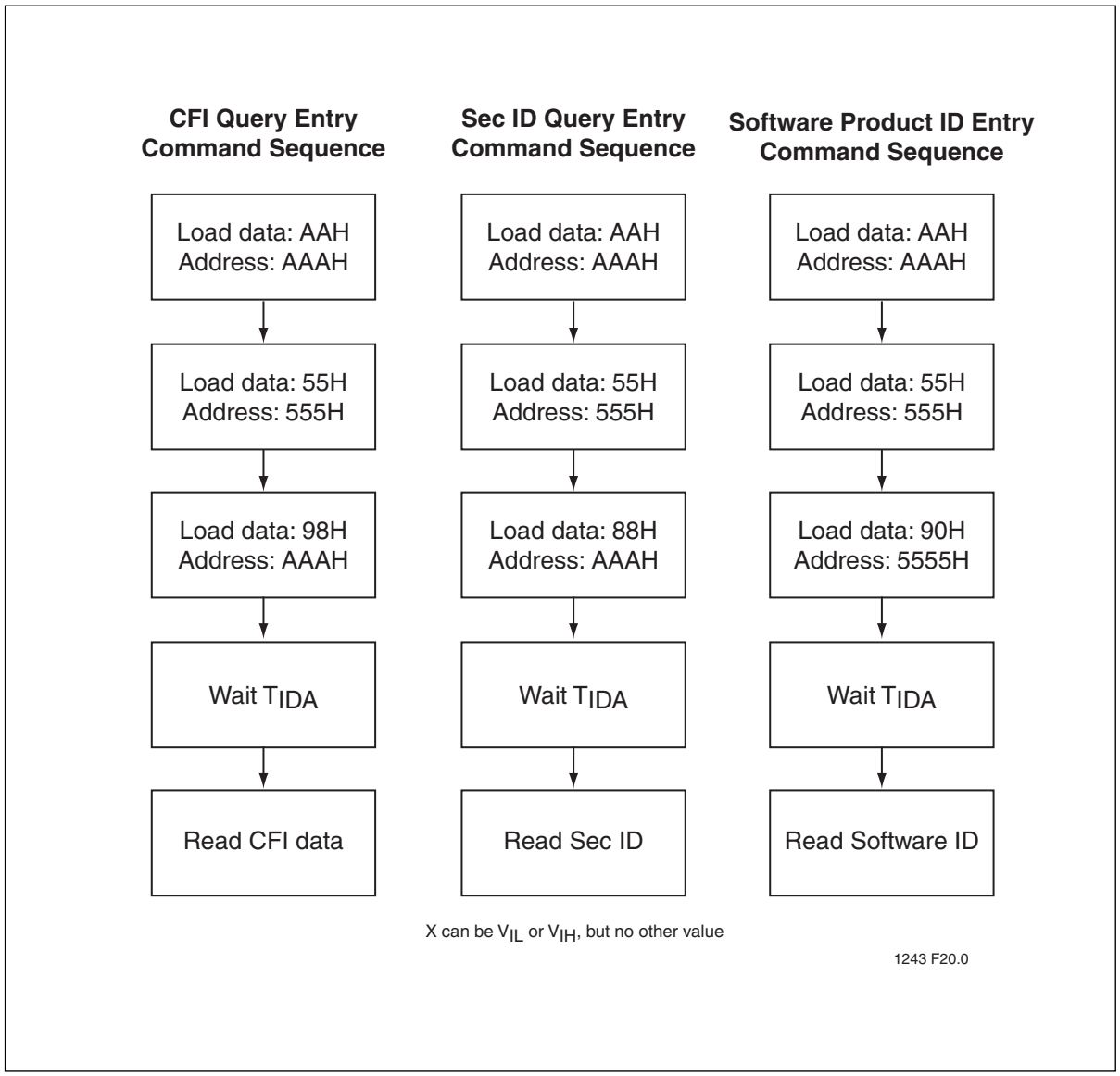


Figure 22: Software ID/CFI Entry Command Flowcharts

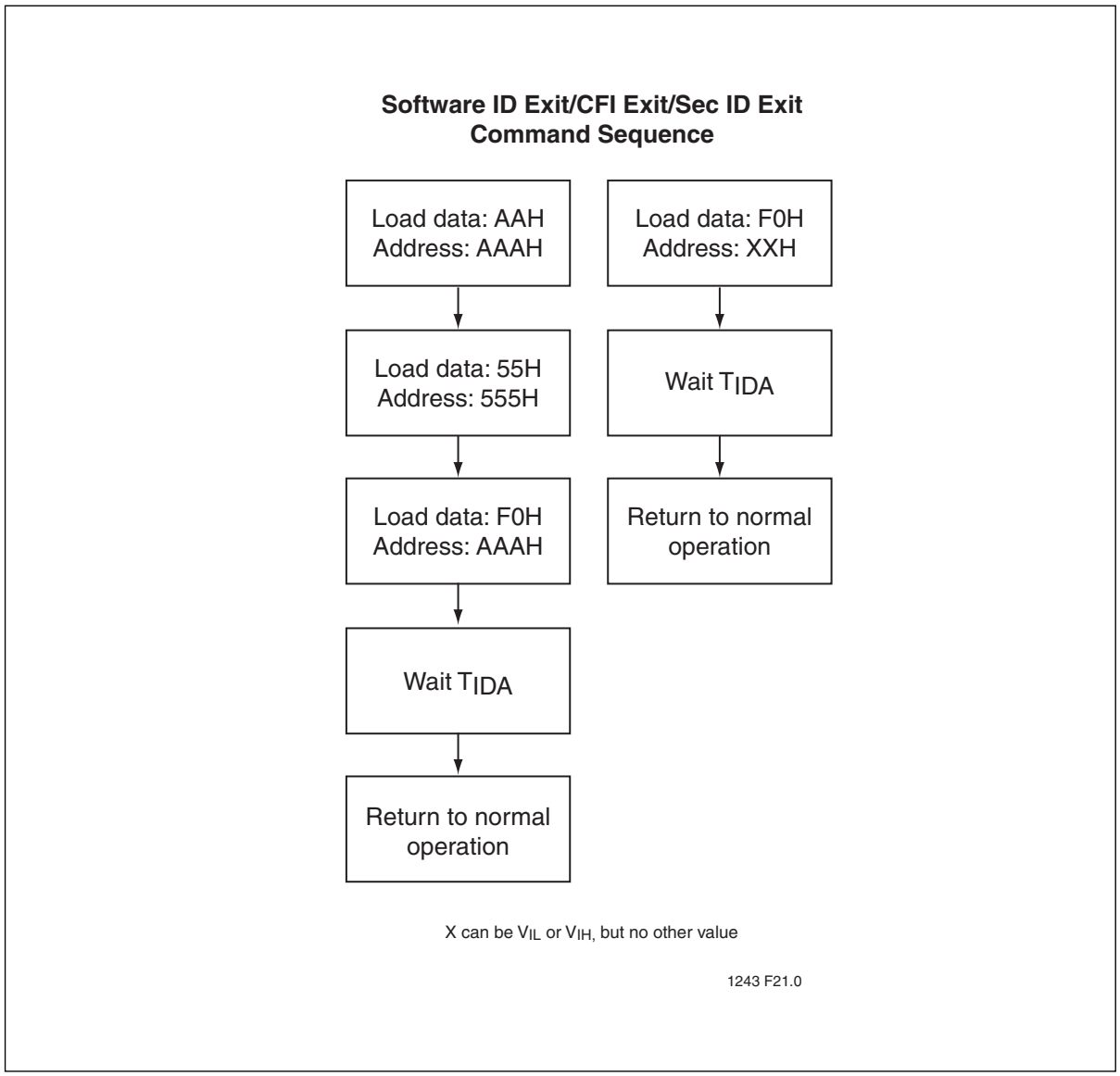


Figure 23: Software ID/CFI Exit Command Flowcharts

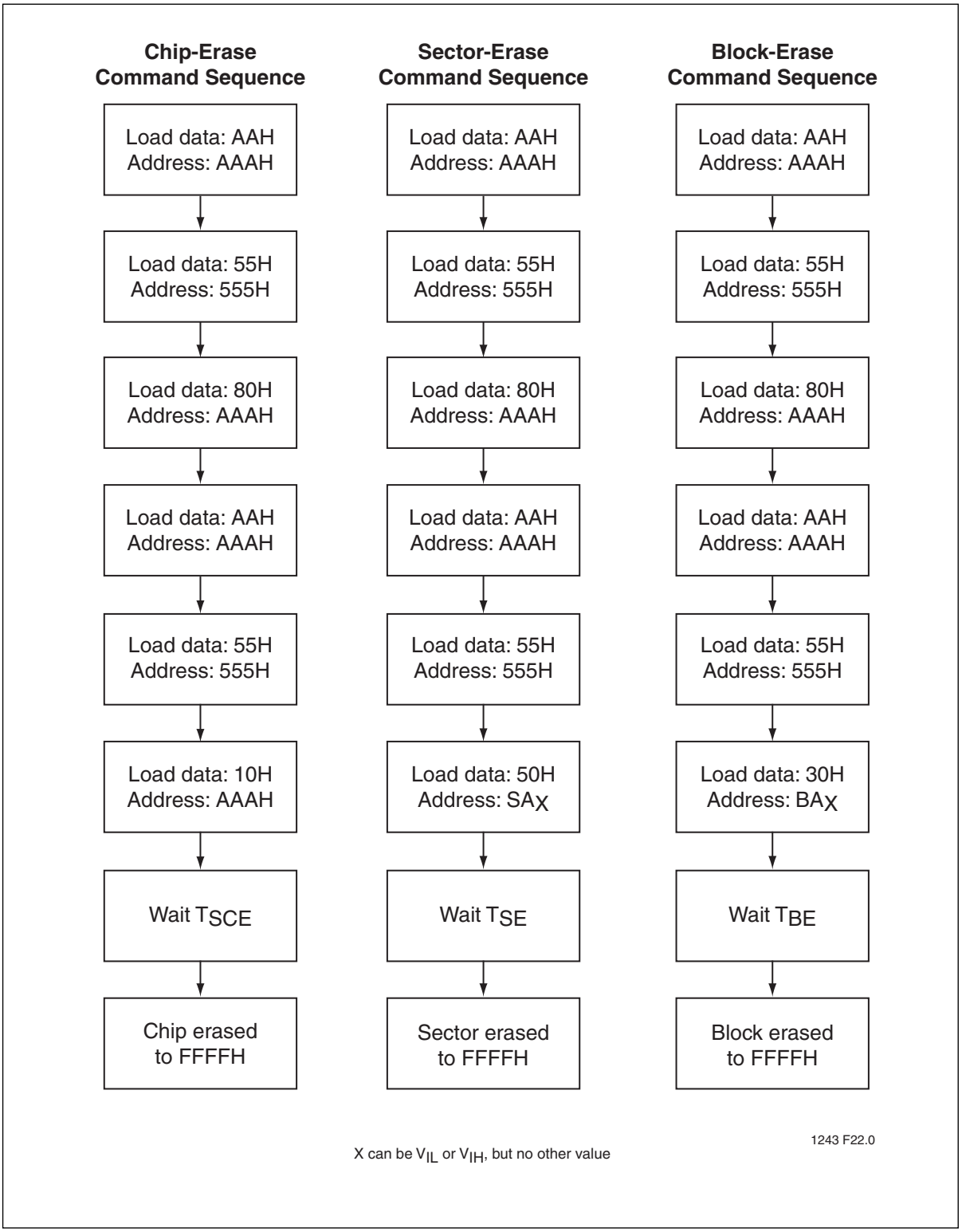
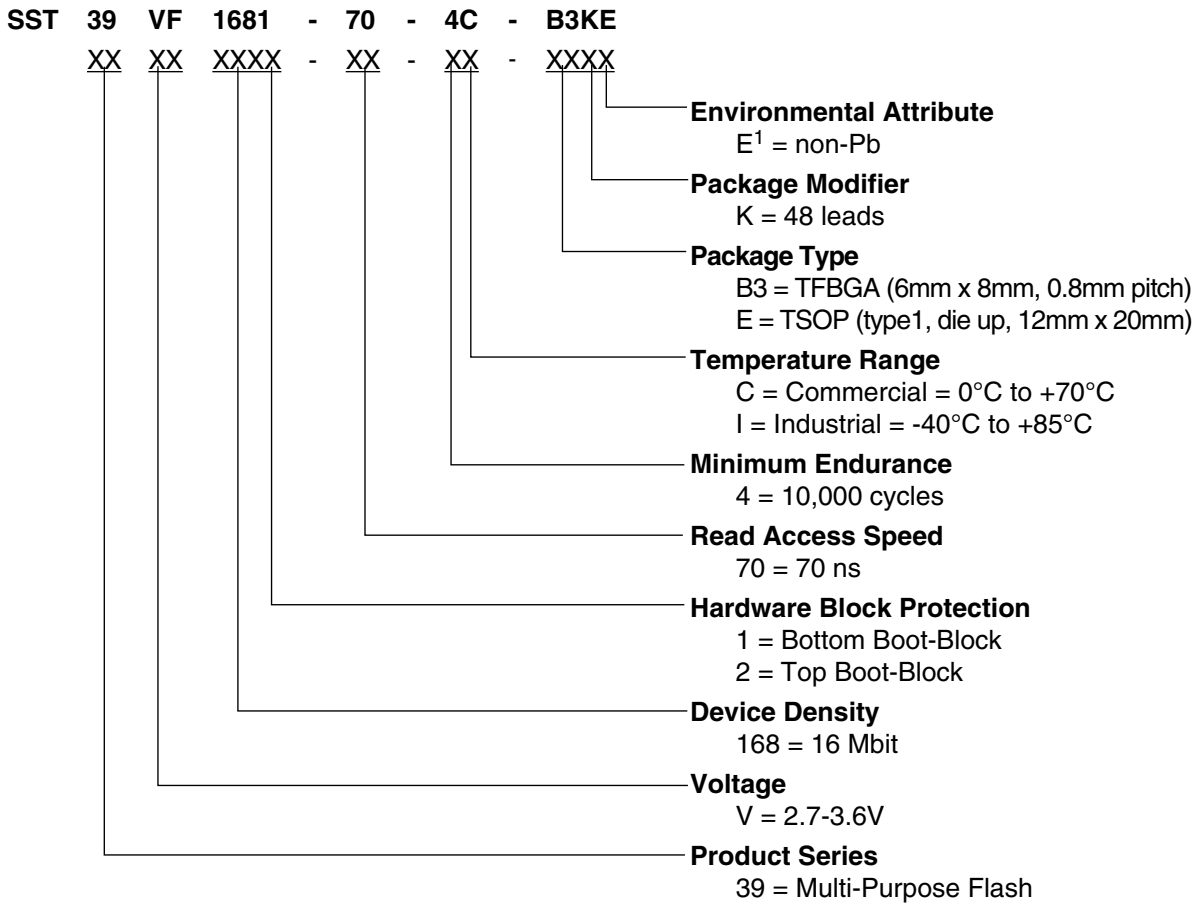


Figure 24: Erase Command Sequence

Product Ordering Information



1. Environmental suffix “E” denotes non-Pb solder. SST non-Pb solder devices are “RoHS Compliant”.

Valid Combinations for SST39VF1681

SST39VF1681-70-4C-EKE	SST39VF1681-70-4C-B3KE
SST39VF1681-70-4I-EKE	SST39VF1681-70-4I-B3KE

Valid Combinations for SST39VF1682

SST39VF1682-70-4C-EKE	SST39VF1682-70-4C-B3KE
SST39VF1682-70-4I-EKE	SST39VF1682-70-4I-B3KE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Packaging Diagrams

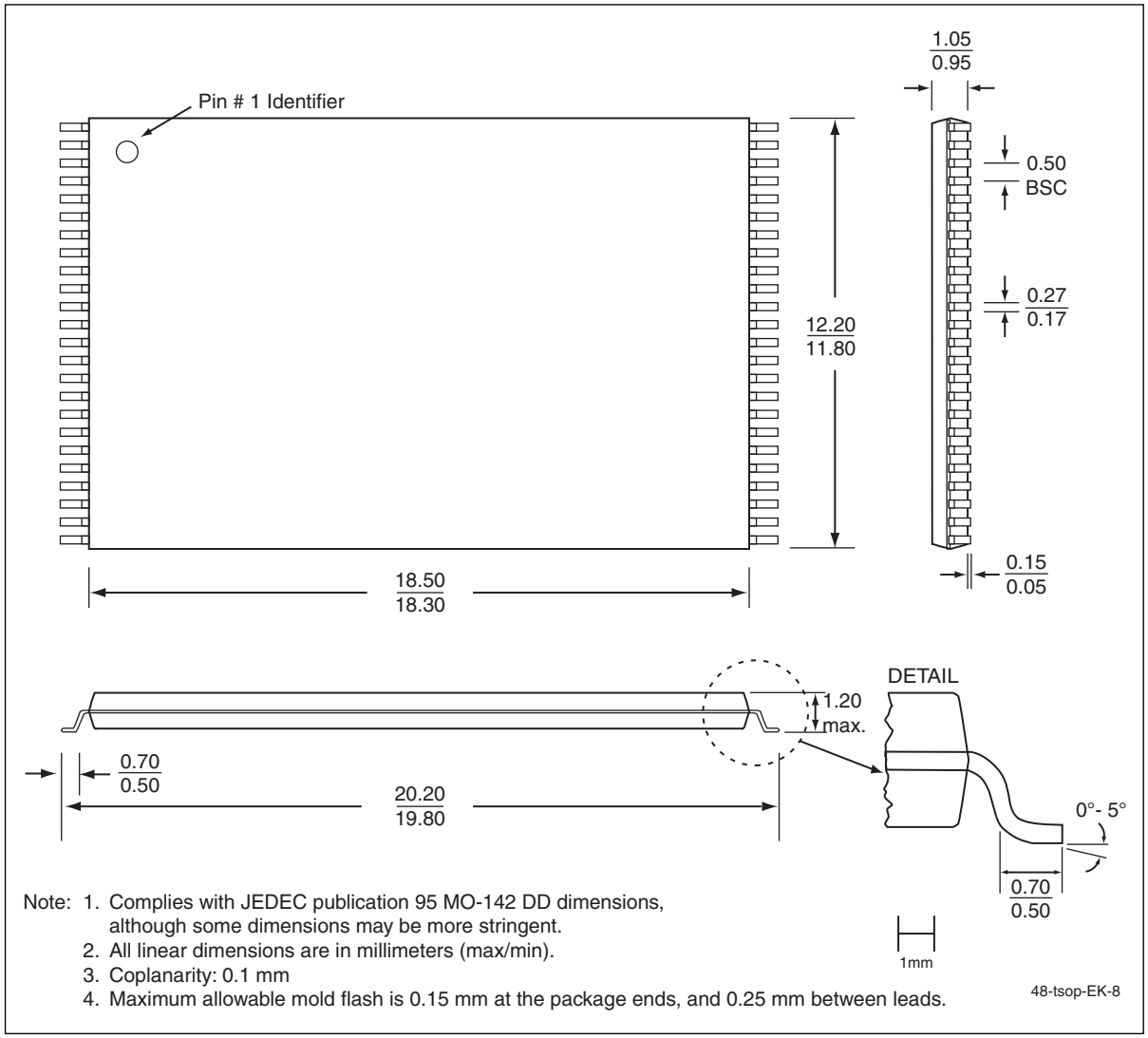
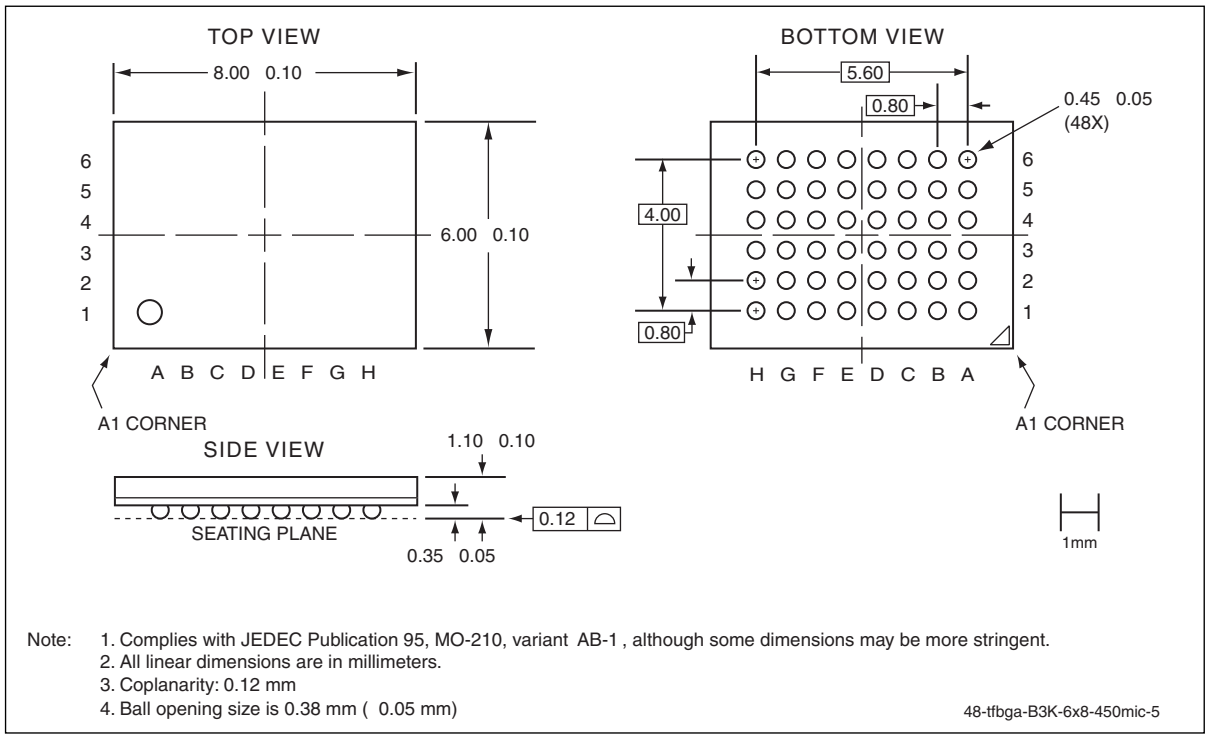


Figure 25: 48-lead Thin Small Outline Package (TSOP) 12mm x 20mm
SST Package Code: EK



Note: 1. Complies with JEDEC Publication 95, MO-210, variant AB-1 , although some dimensions may be more stringent.
2. All linear dimensions are in millimeters.
3. Coplanarity: 0.12 mm
4. Ball opening size is 0.38 mm (0.05 mm)

48-tfbga-B3K-6x8-450mic-5

Figure 26: 48-ball Thin-profile, Fine-pitch Ball Grid Array (TFBGA) 6mm x 8mm
SST Package Code: B3K

Table 18: Revision History

Number	Description	Date
00	• Initial release	May 2003
01	• Change product number from 166x to 168x	Sep 2003
02	• Added B3K package and associated MPNs (See page 31) • Removed 90 ns Commercial temperature for the EK and EKE packages	Oct 2003
03	• 2004 Data Book • Updated B3K package diagram	Nov 2003
A	• Updated document status to “Data Sheet.” • Removed all 90ns information. Edited “Features” on page 1, “Product Ordering Information” on page 31, and Table 16 on page 15. • Updated T_{IDA} information in Table 17 on page 16 • Applied new document format • Released document under the letter revision system • Updated spec number from S71243 to DS25040	May 2011

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