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July 2014

#### FDMS86202

# N-Channel Shielded Gate PowerTrench® MOSFET 120 V, 64 A, 7.2 m $\Omega$

#### **Features**

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 7.2 m $\Omega$  at  $V_{GS}$  = 10 V,  $I_D$  = 13.5 A
- Max  $r_{DS(on)}$  = 10.3 m $\Omega$  at  $V_{GS}$  = 6 V,  $I_D$  = 11.5 A
- $\blacksquare$  Advanced Package and Silicon combination for low  $r_{\text{DS}(\text{on})}$  and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

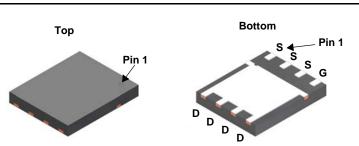
# General Description This N-Channel MOSFET is

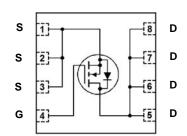
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

#### **Application**

■ DC-DC Conversion







Power 56

#### MOSFET Maximum Ratings T<sub>A</sub> = 25 °C unless otherwise noted

Symbol	Parameter	Ratings	Units			
$V_{DS}$	Drain to Source Voltage			120	V	
$V_{GS}$	Gate to Source Voltage			±20	V	
	Drain Current -Continuous	T <sub>C</sub> = 25 °C		64		
I <sub>D</sub>	-Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	13.5	Α	
	-Pulsed		(Note 4)	240		
E <sub>AS</sub>	Single Pulse Avalanche Energy		(Note 3)	600	mJ	
В	Power Dissipation	T <sub>C</sub> = 25 °C		156	W	
$P_{D}$	Power Dissipation	T <sub>A</sub> = 25 °C	(Note 1a)	2.7	VV	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature	Range		-55 to +150	°C	

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	45	C/VV

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86202	FDMS86202	Power 56	13 "	12 mm	3000 units

### **Electrical Characteristics** $T_J = 25$ °C unless otherwise noted

**Parameter** 

Off Characteristics								
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	120			V		
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 μA, referenced to 25 °C		103		mV/°C		
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 96 V, V <sub>GS</sub> = 0 V			1	μΑ		
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±100	nA		

**Test Conditions** 

Min

Тур

Max

Units

#### On Characteristics

Symbol

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2.0	3.1	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		-10		mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 13.5 \text{ A}$		6.0	7.2	
		$V_{GS} = 6 \text{ V}, I_D = 11.5 \text{ A}$		8.1	10.3	mΩ
		$V_{GS}$ = 10 V, $I_D$ = 13.5 A, $T_J$ = 125 °C		10.9	13.2	
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_{D} = 13.5 \text{ A}$		44		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, f = 1 MHz		3195	4250	pF
Coss	Output Capacitance			449	600	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			17	30	pF
R <sub>g</sub>	Gate Resistance		0.1	0.9	2.7	Ω

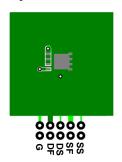
#### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time			21	33	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 60 V, I <sub>D</sub> = 13.5	5 A,	6	13	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	V <sub>GS</sub> = 10 V, R <sub>GEN</sub> =	6 Ω	27	44	ns
t <sub>f</sub>	Fall Time			5	11	ns
$Q_q$	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V		45	64	nC
Qq	Total Gate Charge	V <sub>GS</sub> = 0 V to 6 V	V <sub>DD</sub> = 60 V,	29	41	nC
$Q_{gs}$	Gate to Source Charge		<sub>D</sub> = 13.5 A	14.3		nC
$Q_{qd}$	Gate to Drain "Miller" Charge			8.7		nC

#### **Drain-Source Diode Characteristics**

V <sub>SD</sub>	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2.1 \text{ A}$ (Note 2)	0.69	1.2	V
		$V_{GS} = 0 \text{ V}, I_S = 13.5 \text{ A}$ (Note 2)	0.76	1.3	
t <sub>rr</sub>	Reverse Recovery Time	I <sub>E</sub> = 13.5 A, di/dt = 100 A/μs	73	118	ns
Q <sub>rr</sub>	Reverse Recovery Charge	1F - 15.5 A, αναί - 100 Ανμδ	117	187	nC

<sup>1.</sup>  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{in}^2$  pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 45 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b) 115 °C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test: Pulse Width < 300  $\mu$ s, Duty cycle < 2.0%.
- 3. E<sub>AS</sub> of 600 mJ is based on starting T<sub>J</sub> = 25 °C, L = 3 mH, I<sub>AS</sub> = 20 A, V<sub>DD</sub> = 120 V, V<sub>GS</sub> = 10 V. 100% test at L = 0.1 mH, I<sub>AS</sub> = 65 A.
- 4. Pulse Id limited by junction temperature, td  $\leq$  100  $\mu$ s, please refer to SOA curve for more details.

#### Typical Characteristics T<sub>.1</sub> = 25 °C unless otherwise noted

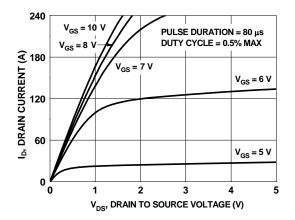


Figure 1. On Region Characteristics

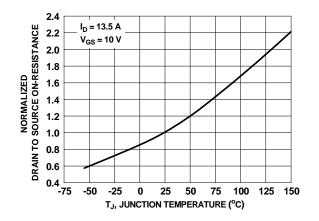


Figure 3. Normalized On Resistance vs Junction Temperature

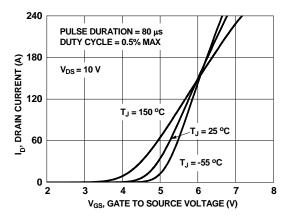


Figure 5. Transfer Characteristics

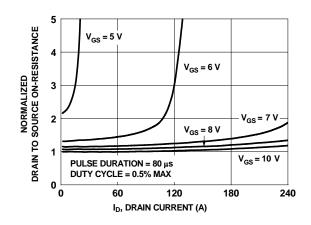


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

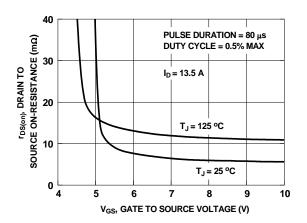


Figure 4. On-Resistance vs Gate to Source Voltage

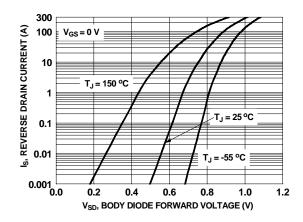


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

### Typical Characteristics $T_J$ = 25 $^{\circ}$ C unless otherwise noted

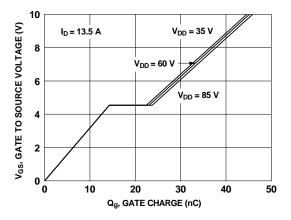


Figure 7. Gate Charge Characteristics

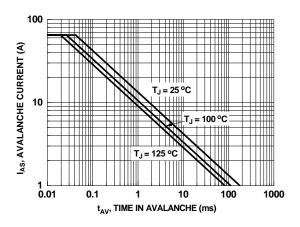


Figure 9. Unclamped Inductive Switching Capability

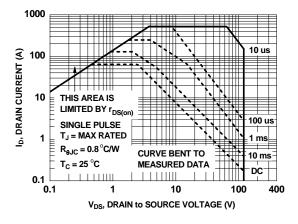


Figure 11. Forward Bias Safe Operating Area

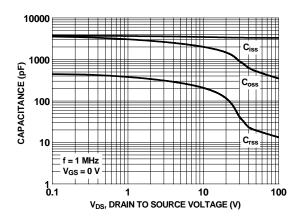


Figure 8. Capacitance vs Drain to Source Voltage

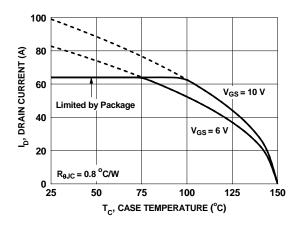


Figure 10. Maximum Continuous Drain Current vs Case Temperature

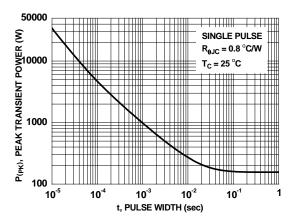


Figure 12. Single Pulse Maximum Power Dissipation

#### Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

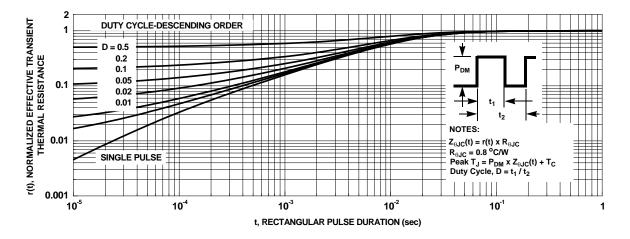
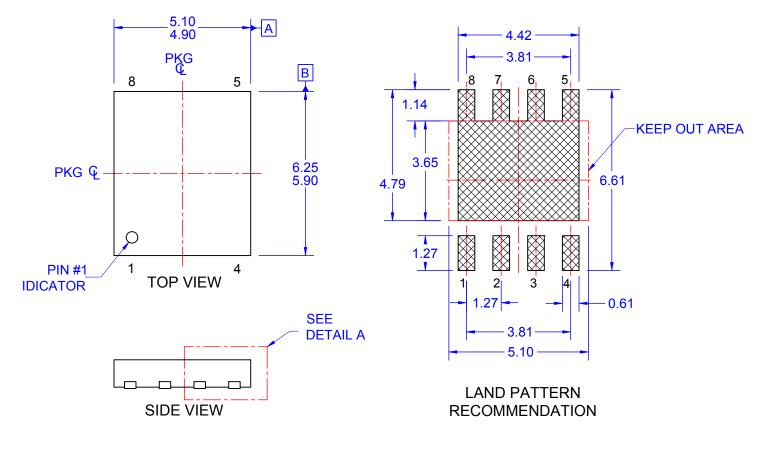
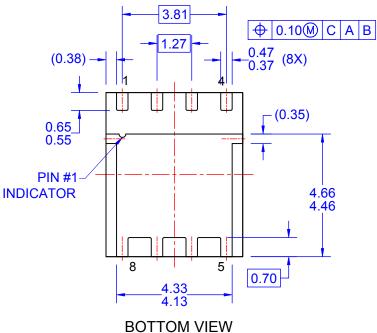
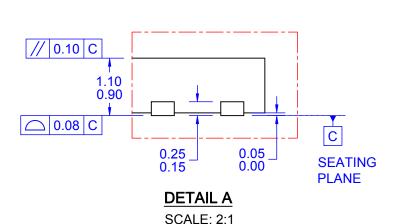


Figure 13. Junction-to-Case Transient Thermal Response Curve







NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
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