

## Automotive-grade N-channel 100 V, 5 mΩ typ., 107 A, STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

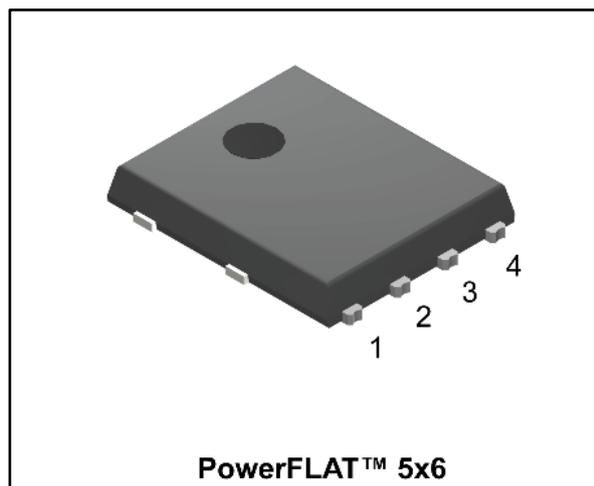
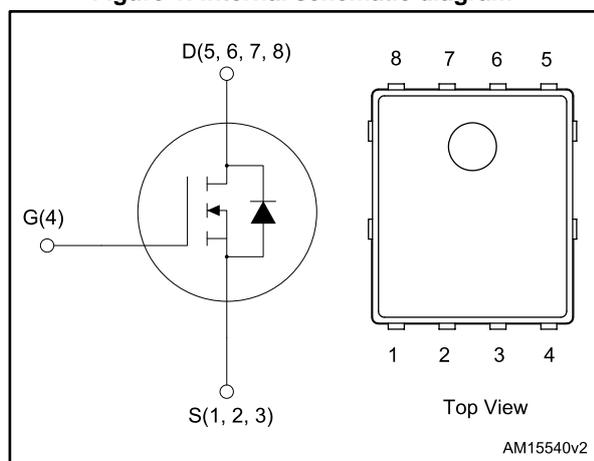


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>	P <sub>TOT</sub>
STL115N10F7AG	100 V	6 mΩ	107 A	136 W



- AEC-Q101 qualified
- Among the lowest R<sub>DS(on)</sub> on the market
- Excellent FoM (figure of merit)
- Low C<sub>rss</sub>/C<sub>iss</sub> ratio for EMI immunity
- High avalanche ruggedness

### Applications

- Switching applications

### Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL115N10F7AG	115N10F7	PowerFLAT™ 5x6	Tape and reel

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	100	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	107	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	75	A
$I_{DM}^{(1)}$	Drain current (pulsed)	428	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	136	W
$E_{AS}^{(2)}$	Single pulse avalanche energy	490	mJ
$T_J$	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		

**Notes:**

<sup>(1)</sup>Pulse width limited by safe operating area

<sup>(2)</sup>Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $I_D = 18\text{ A}$ ,  $V_{DD} = 50\text{ V}$

**Table 3: Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.1	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	$^\circ\text{C/W}$

**Notes:**

<sup>(1)</sup>When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ s}$

## 2 Electrical characteristics

(T<sub>CASE</sub> = 25 °C unless otherwise specified)

**Table 4: On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	100			V
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V			1	μA
		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V, T <sub>C</sub> = 125 °C <sup>(1)</sup>			10	
I <sub>GSS</sub>	Gate body leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.5		4.5	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 53 A		5	6	mΩ

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test.

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 50 V, f = 1 MHz, V <sub>GS</sub> = 0 V	-	5600	-	pF
C <sub>oss</sub>	Output capacitance		-	1200	-	pF
C <sub>rss</sub>	Reverse transfer capacitance		-	50	-	pF
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 107 A, V <sub>GS</sub> = 10 V (see <a href="#">Figure 14: "Test circuit for gate charge behavior"</a> )	-	72.5	-	nC
Q <sub>gs</sub>	Gate-source charge		-	35.5	-	nC
Q <sub>gd</sub>	Gate-drain charge		-	15	-	nC

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 53 A, R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V (see <a href="#">Figure 13: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 18: "Switching time waveform"</a> )	-	33	-	ns
t <sub>r</sub>	Rise time		-	38	-	ns
t <sub>d(off)</sub>	Turn-off delay time		-	48	-	ns
t <sub>f</sub>	Fall time		-	20	-	ns

Table 7: Source drain diode

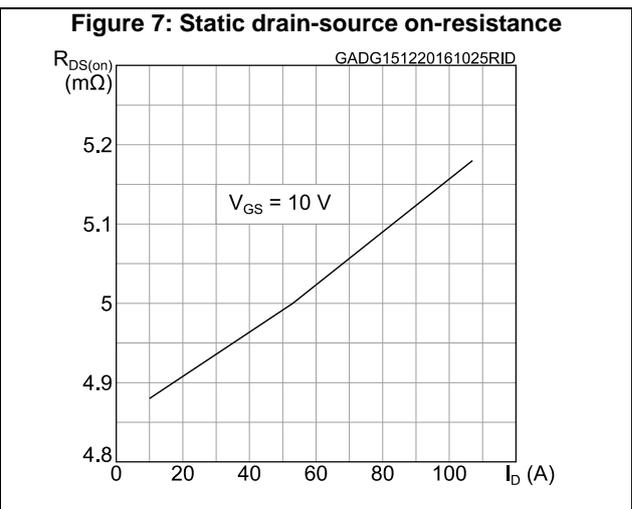
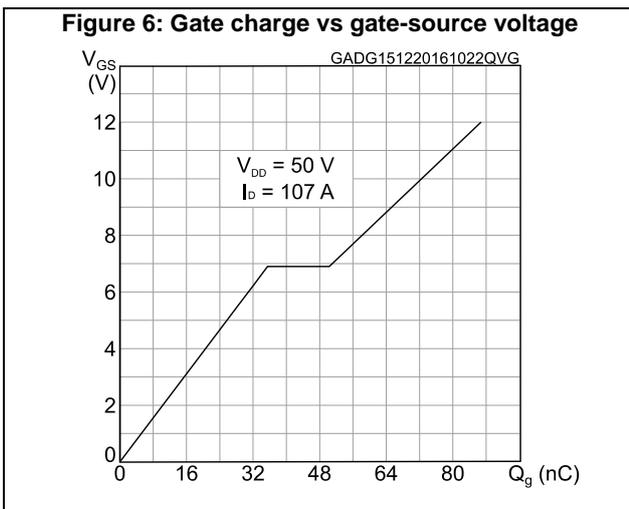
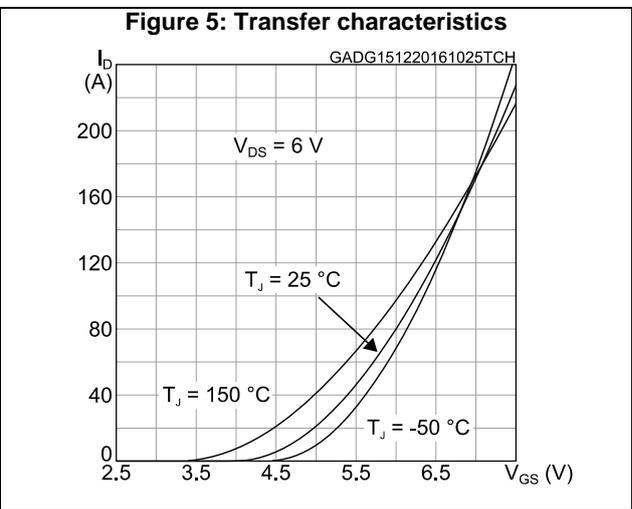
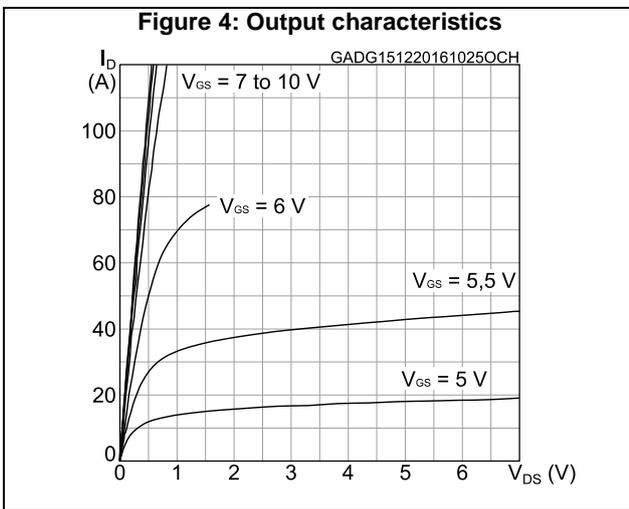
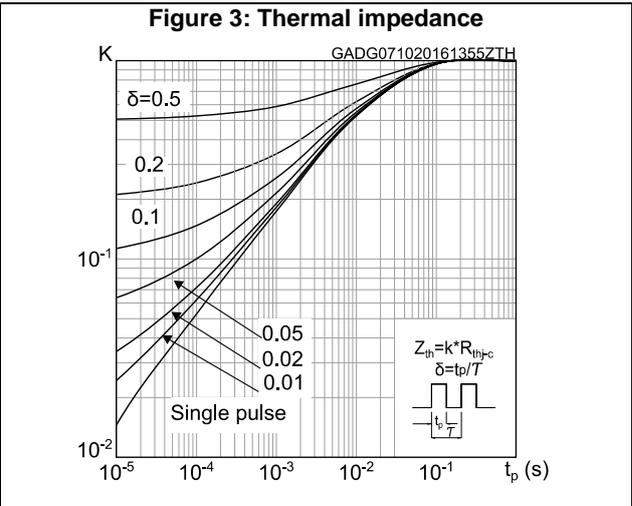
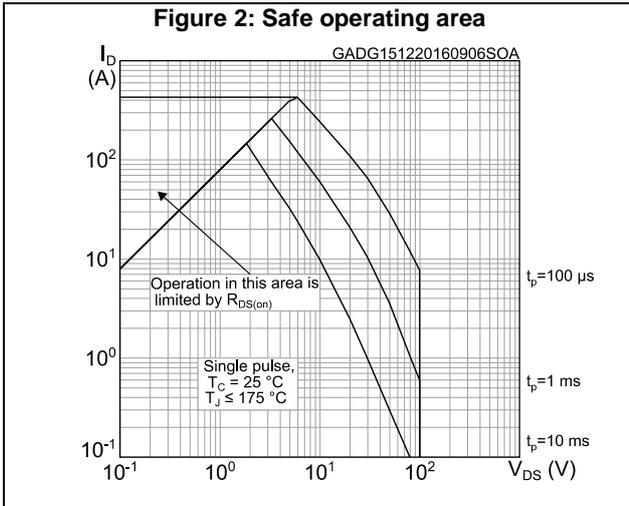
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		107	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		428	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 53 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-		1.2	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 107 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 80 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 15: "Test circuit for inductive load switching and diode recovery times"</a> )	-	60		ns
$Q_{rr}$	Reverse recovery charge		-	96		nC
$I_{RRM}$	Reverse recovery current		-	3.2		A

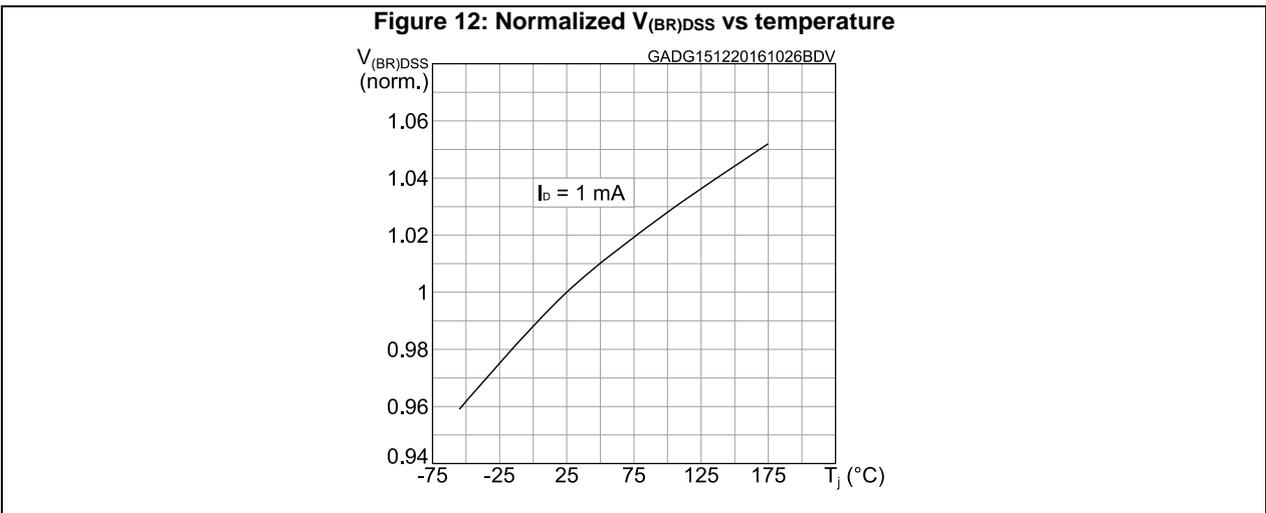
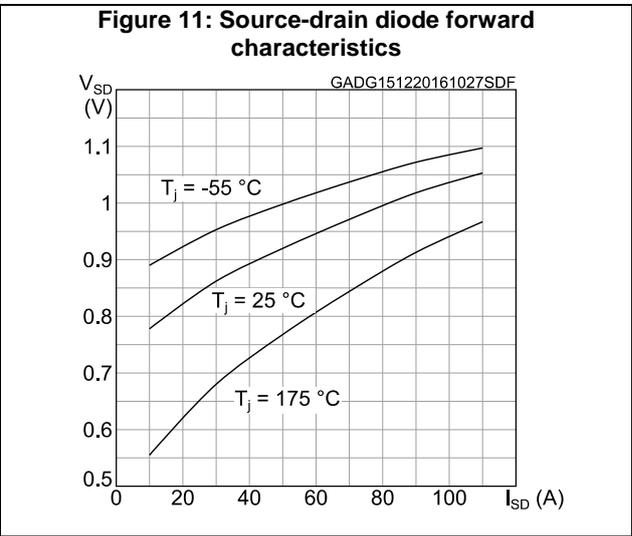
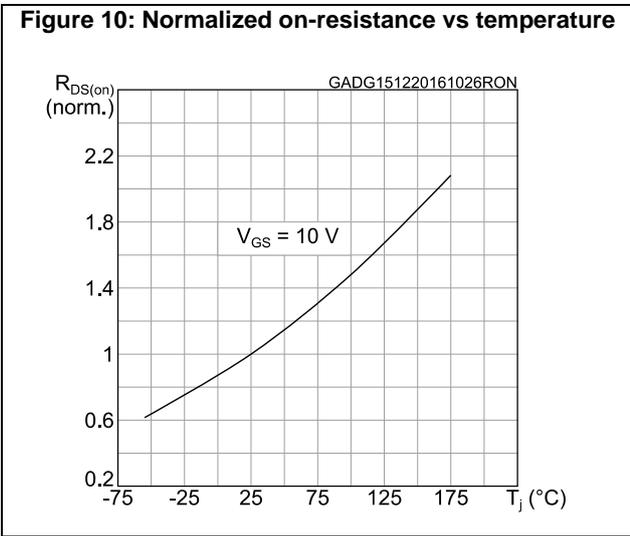
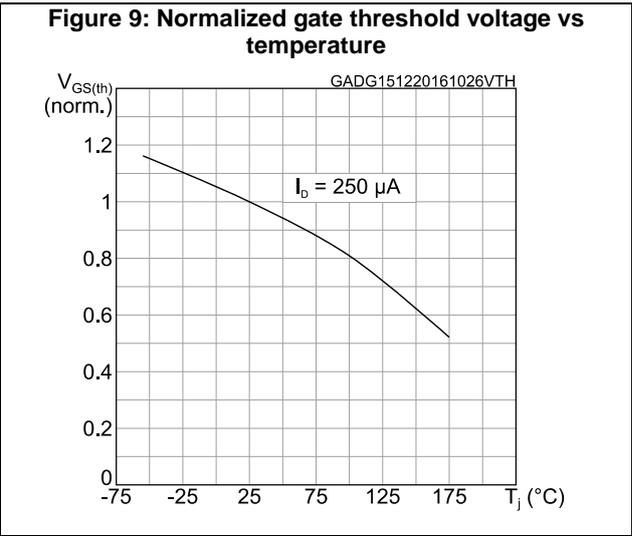
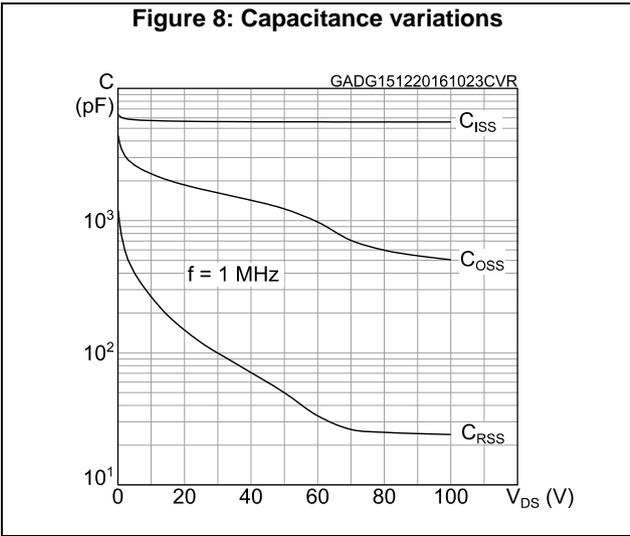
**Notes:**

<sup>(1)</sup>Pulse width limited by safe operating area

<sup>(2)</sup>Pulsed: pulse duration=300  $\mu\text{s}$ , duty cycle 1.5%

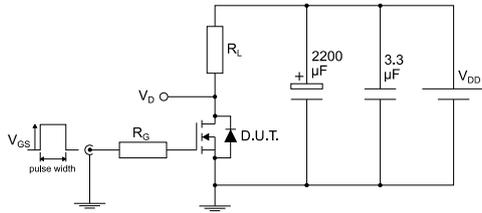
## 2.1 Electrical characteristics (curves)





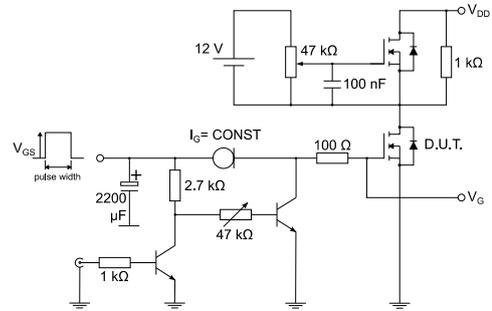
### 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**



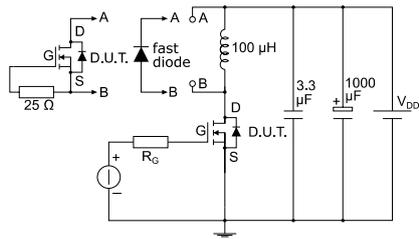
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**Figure 14: Test circuit for gate charge behavior**



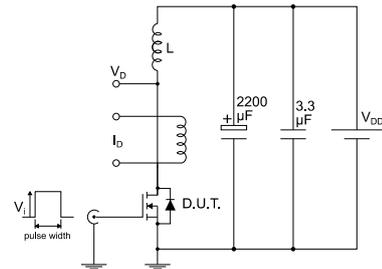
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**Figure 15: Test circuit for inductive load switching and diode recovery times**



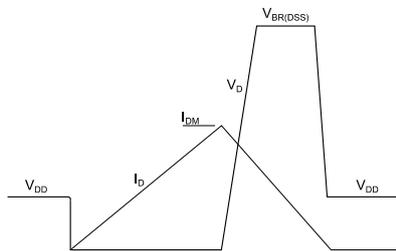
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**Figure 16: Unclamped inductive load test circuit**



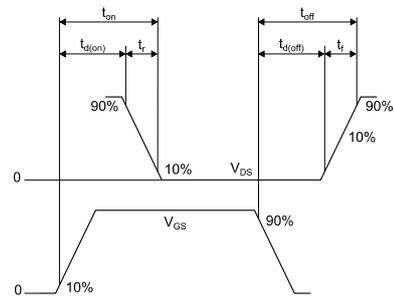
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**Figure 17: Unclamped inductive waveform**



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**Figure 18: Switching time waveform**



AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 PowerFLAT™ 5x6 WF type C package information

Figure 19: PowerFLAT™ 5x6 WF type C package outline

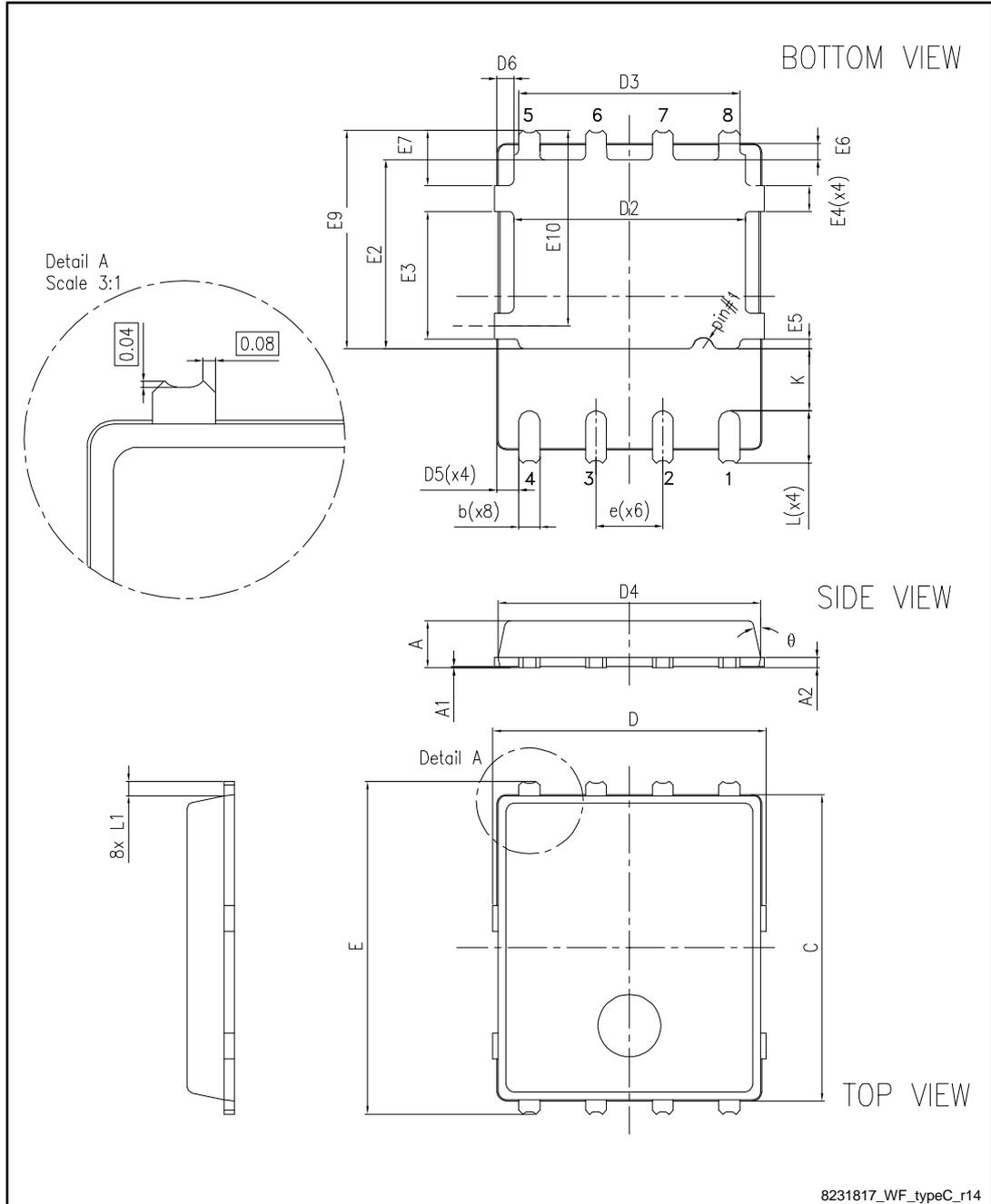
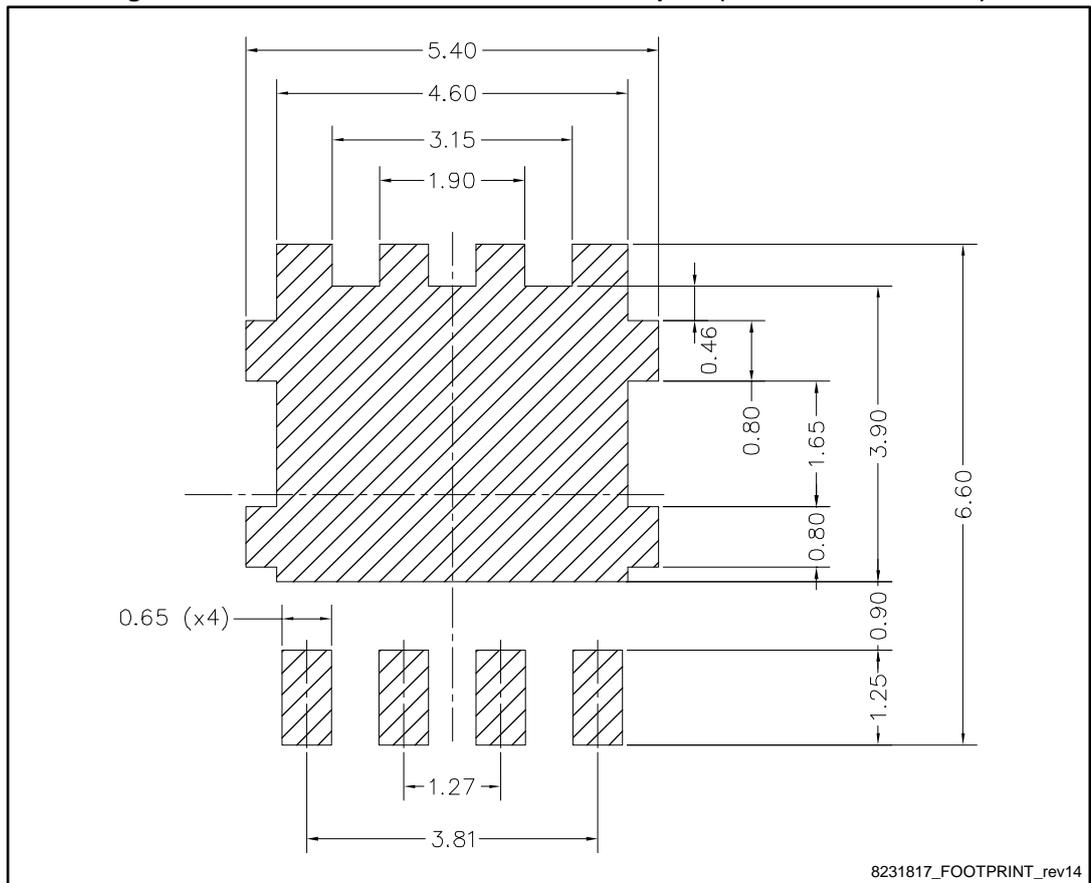


Table 8: PowerFLAT™ 5x6 WF type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.05		1.35
L	0.90	1.00	1.10
L1	0.175	0.275	0.375
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



8231817\_FOOTPRINT\_rev14

### 4.2 PowerFLAT™ 5x6 packing information

Figure 21: PowerFLAT™ 5x6 WF tape (dimensions are in mm)

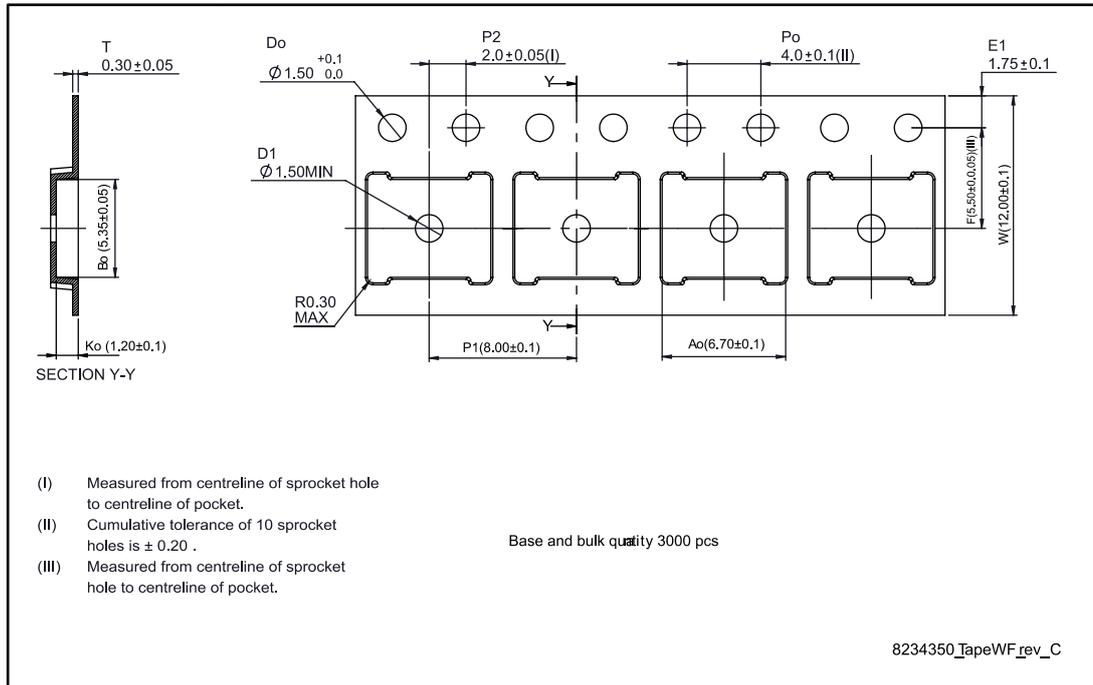


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

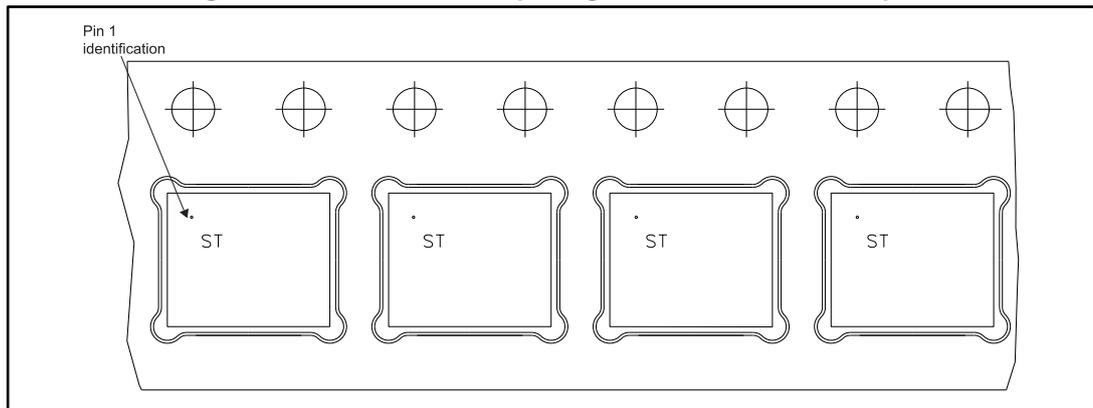
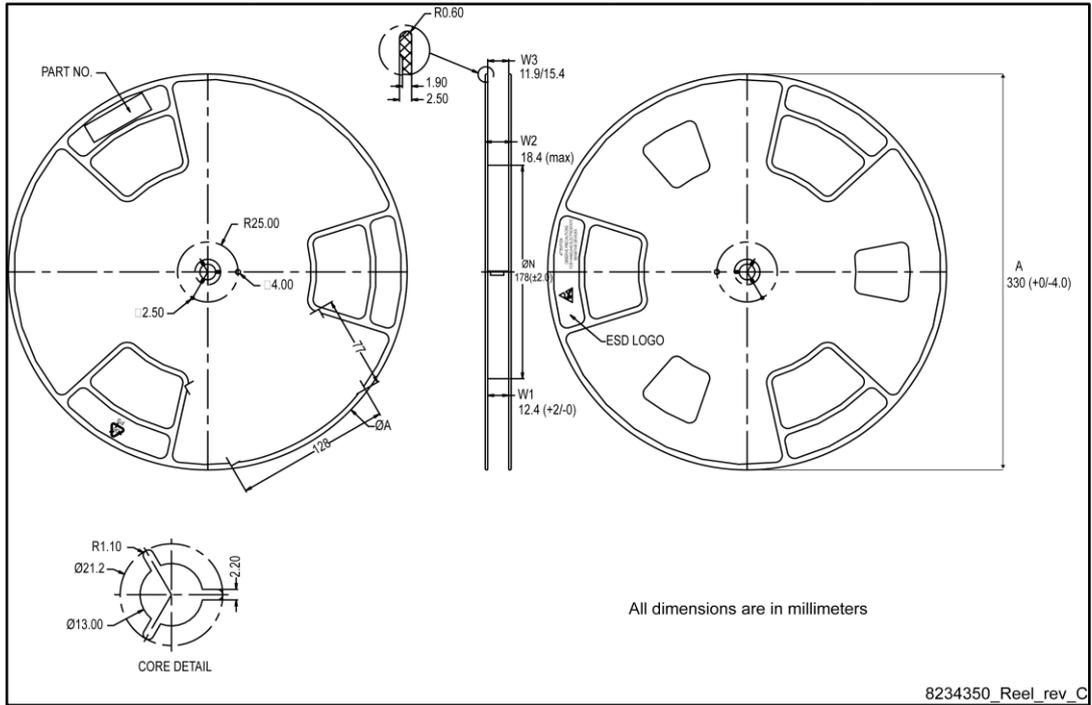


Figure 23: PowerFLAT™ 5x6 reel (dimensions are in mm)



## 5 Revision history

**Table 9: Document revision history**

Date	Revision	Changes
07-Oct-2016	1	First release.
15-Dec-2016	2	Datasheet status promoted from preliminary to production data. Updated features list on cover page. Updated <a href="#">Section 2: "Electrical characteristics"</a> .

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