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FDMS6681Z

June 2015

P-Channel PowerTrench® MOSFET

-30 V, -122 A, 3.2 m Ω

Features

- Max $r_{DS(on)} = 3.2 \text{ m}\Omega$ at $V_{GS} = -10 \text{ V}$, $I_D = -21.1 \text{ A}$
- Max $r_{DS(on)} = 5.0 \text{ m}\Omega$ at $V_{GS} = -4.5 \text{ V}$, $I_D = -15.7 \text{ A}$
- Advanced Package and Silicon combination for low r_{DS(on)}
- HBM ESD Protection Level of 8kV Typical(Note 3)
- MSL1 Robust Package Design
- RoHS Compliant

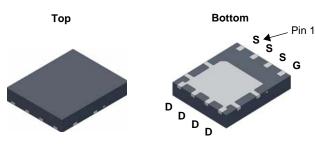


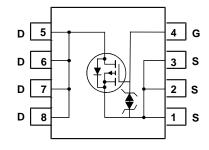
General Description

The FDMS6681Z has been designed to minimize losses in load switch applications. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ and ESD protection.

Applications

- Load Switch in Notebook and Server
- Notebook Battery Pack Power Management





Power 56

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted.

Symbol	Parame	ter		Ratings	Units
V _{DS}	Drain to Source Voltage			-30	V
V _{GS}	Gate to Source Voltage			±25	V
	Drain Current -Continuous	T _C = 25 °C	(Note5)	-122	
	-Continuous	T _C = 100 °C	(Note5)	-77	۸
I _D	-Continuous	T _A = 25 °C	(Note 1a)	-21.1	A
	-Pulsed		(Note4)	-600	
D	Power Dissipation	T _C = 25 °C		73	w
P_{D}	Power Dissipation	T _A = 25 °C	(Note 1a)	2.5	VV
T _J , T _{STG}	Operating and Storage Junction Temperat	ture Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.7	°C/W
R_{\thetaJA}	Thermal Resistance, Junction to Ambient (Note 1a)	50	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS6681Z	FDMS6681Z	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25$ °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Chara	acteristics					
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		20		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -24 V, V _{GS} = 0 V			-1	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$			±10	μΑ

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250 \mu A$	-1	-1.7	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25 °C		-7		mV/°C
		$V_{GS} = -10 \text{ V}, I_D = -22.1 \text{ A}$		2.7	3.2	
r _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = -4.5 \text{ V}, I_D = -15.7 \text{ A}$		4.0	5.0	mΩ
, ,		$V_{GS} = -10 \text{ V}, I_D = -22.1 \text{ A}, T_J = 125 \text{ °C}$		3.9	5.0	
9 _{FS}	Forward Transconductance	$V_{DD} = -10 \text{ V}, I_D = -22.1 \text{ A}$		143		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 45.V.V 0.V	7803	10380	pF
Coss	Output Capacitance	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz	1540	2050	pF
C _{rss}	Reverse Transfer Capacitance	1 = 1 1/11/12	1345	2020	pF

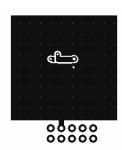
Switching Characteristics

t _{d(on)}	Turn-On Delay Time			15	24	ns
t _r	Rise Time	V _{DD} = -15 V, I _D = -22.1 A,		38	61	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = -10 \text{ V}, R_{GEN}$	$V_{GS} = -10 \text{ V}, R_{GEN} = 6 \Omega$		416	ns
t _f	Fall Time			197	316	ns
Q_g	Total Gate Charge	V _{GS} = 0 V to -10 V		172	241	nC
Q_q	Total Gate Charge	$V_{GS} = 0 \text{ V to -5 V}$	V _{DD} = -15 V,	97	136	nC
Q_{gs}	Gate to Source Charge		I _D = -22.1 A	22		nC
Q_{ad}	Gate to Drain "Miller" Charge			46		nC

Drain-Source Diode Characteristics

V	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = -2.1 \text{ A}$ (Note 2)		0.68	1.2	V
V _{SD}	Source to Drain Diode Forward voltage	V _{GS} = 0 V, I _S = -22.1 A (Note 2)		0.79	1.25	V
t _{rr}	Reverse Recovery Time	I _F = -22.1 A, di/dt = 100 A/μs		44	71	ns
Q _{rr}	Reverse Recovery Charge			39	63	nC

^{1.} R_{0JA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0JC} is guaranteed by design while R_{0CA} is determined by the user's board design.



a. 50 °C/W when mounted on a 1 in² pad of 2 oz copper.



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%.
- The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
 Pulsed Id please refer to Fig 12 SOA graph for more details.
 Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal electro-mechanical application board design.

Typical Characteristics $T_J = 25$ °C unless otherwise noted.

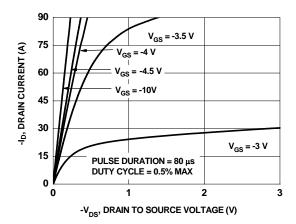


Figure 1. On Region Characteristics

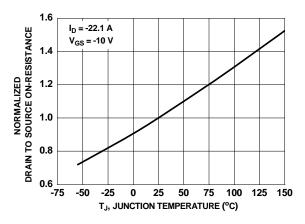


Figure 3. Normalized On Resistance vs Junction Temperature

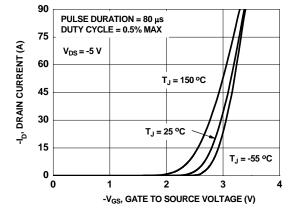


Figure 5. Transfer Characteristics

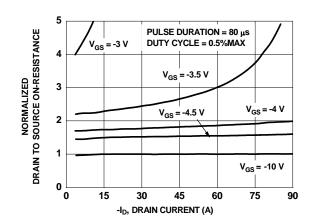


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

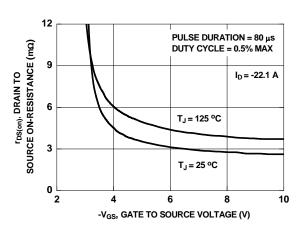


Figure 4. On-Resistance vs Gate to Source Voltage

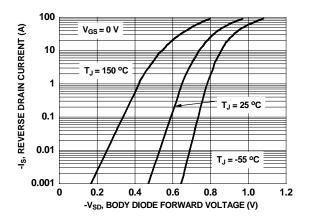


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted.

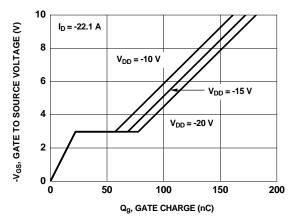


Figure 7. Gate Charge Characteristics

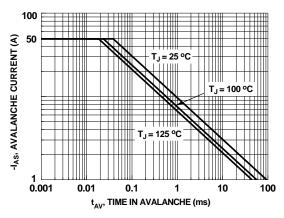


Figure 9. Unclamped Inductive Switching Capability

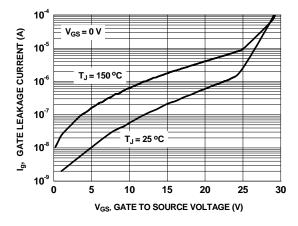


Figure 11. I_{gss} vs V_{gss}

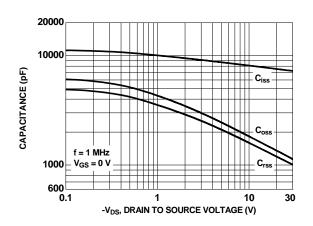


Figure 8. Capacitance vs Drain to Source Voltage

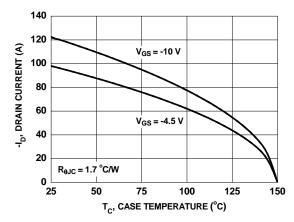


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

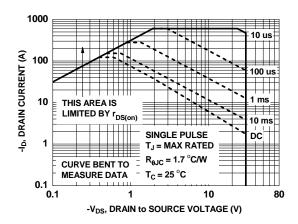


Figure 12. Forward Bias Safe Operating Area

Typical Characteristics $T_J = 25$ °C unless otherwise noted.

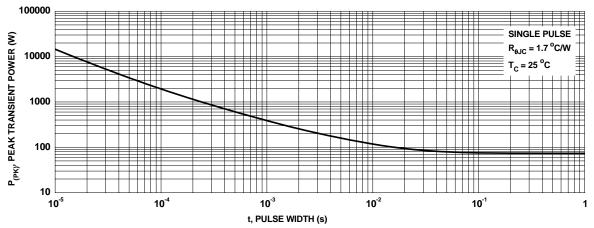


Figure 13. Single Pulse Maximum Power Dissipation

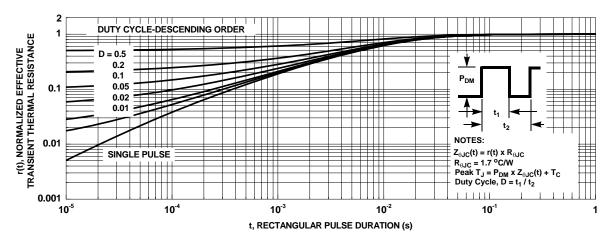
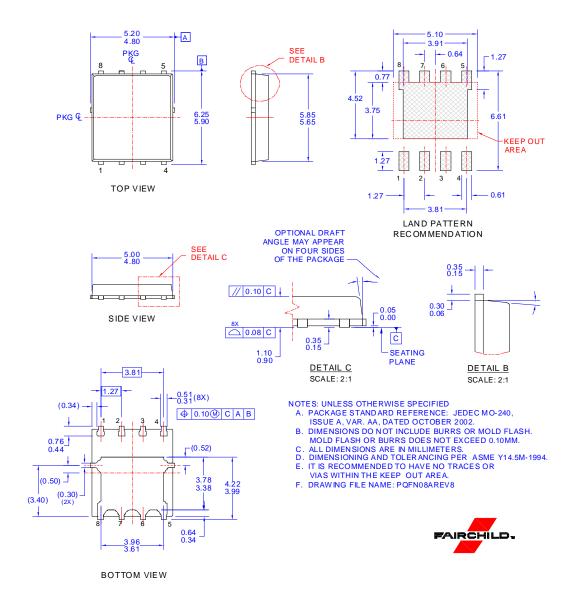


Figure 14. Transient Thermal Response Curve

Dimensional Outline and Pad Layout



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