TJA1024

Quad LIN 2.2A/SAE J2602 transceiver

Rev. 1 — 12 February 2015 Product data sheet

1. General description

The TJA1024 is a quad LIN transceiver that provides the interface between a Local Interconnect Network (LIN) master/slave protocol controller and the physical bus in a LIN network. It comprises two independent and separated dual LIN transceiver blocks on a single die (only the ground pins GND1 and GND2 are connected internally) with dedicated supply pins (V_{BAT1} for LIN 1/LIN2 and V_{BAT2} for LIN3/LIN4).

The TJA1024 is primarily intended for in-vehicle subnetworks using baud rates up to 20 kBd and is compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and SAE J2602. The TJA1024 is software compatible with the TJA1022, TJA1027 and TJA1029.

The transmit data streams generated by the protocol controller are converted by the TJA1024 into optimized bus signals shaped to minimize ElectroMagnetic Emissions (EME). The LIN bus output pins are pulled HIGH via internal termination resistors. For a master application, an external resistor in series with a diode should be connected between pin V_{BATx} and the respective LIN pins. The receivers detect receive data streams on the LIN bus input pins and transfer them via pins RXDx to the microcontroller.

Power consumption is very low when all four transceivers are in Sleep mode. However, the TJA1024 can still be woken up via pins LINx and SLPx_N.

2. Features and benefits

2.1 General

- Four LIN transceivers in a single package
- LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and SAE J2602 compliant
- Baud rate up to 20 kBd
- Very low EME
- Very low current consumption in Sleep mode with remote LIN wake-up
- Input levels compatible with 3.3 V and 5 V devices
- Integrated termination resistors for LIN slave applications
- Passive behavior in unpowered state
- Operational during cranking pulse: full operation from 5 V upwards
- Undervoltage detection
- K-line compatible
- Leadless DHVQFN24 package (3.5 mm × 5.5 mm) with improved Automated Optical Inspection (AOI)
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)
- Software-compatible with the TJA1022, TJA1027 and TJA1029

2.2 Protection

- Very high ElectroMagnetic Immunity (EMI)
- Very high ESD robustness: ±8 kV according to IEC 61000-4-2 for pins LINx and V_{BATx}
- Bus terminal and battery pins protected against transients in the automotive environment (ISO 7637)
- Bus terminal short-circuit proof to battery and ground
- Thermally protected
- Initial TXD dominant check when switching to Normal mode
- TXD dominant time-out function

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	pins V_{BAT1} and V_{BAT2}; limiting values	–0.3	-	+42	V
		operating range	5	-	18	V
I_{BAT}	battery supply current	per pin (V_{BAT1} or V_{BAT2}):				
		Sleep mode (both channels); bus recessive (both channels); $V_{LINx} = V_{BATx}$; $V_{SLPx\_N} = 0$ V	2.5	7	10	µA
		Standby mode (both channels); bus recessive (both channels); $V_{LINx} = V_{BATx}$; $V_{SLPx\_N} = 0$ V	2.5	7	10	µA
		Normal mode (both channels); bus recessive (both channels); $V_{TXDx} = 5$ V; $V_{LINx} = V_{BATx}$; $V_{SLPx\_N} = 5$ V	300	1600	3200	µA
V_{LIN}	voltage on pin LIN	pins LIN1, LIN2, LIN3 and LIN4; limiting value; with respect to GND and V_{BAT}	–42	-	+42	V
V_{ESD}	electrostatic discharge voltage	on pins LIN1, LIN2, LIN3, LIN4, V_{BAT1} and V_{BAT2}; according to IEC 61000-4-2	–8	-	+8	kV
T_{vj}	virtual junction temperature		–40	-	+150	°C

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TJA1024HG	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1

5. Block diagram

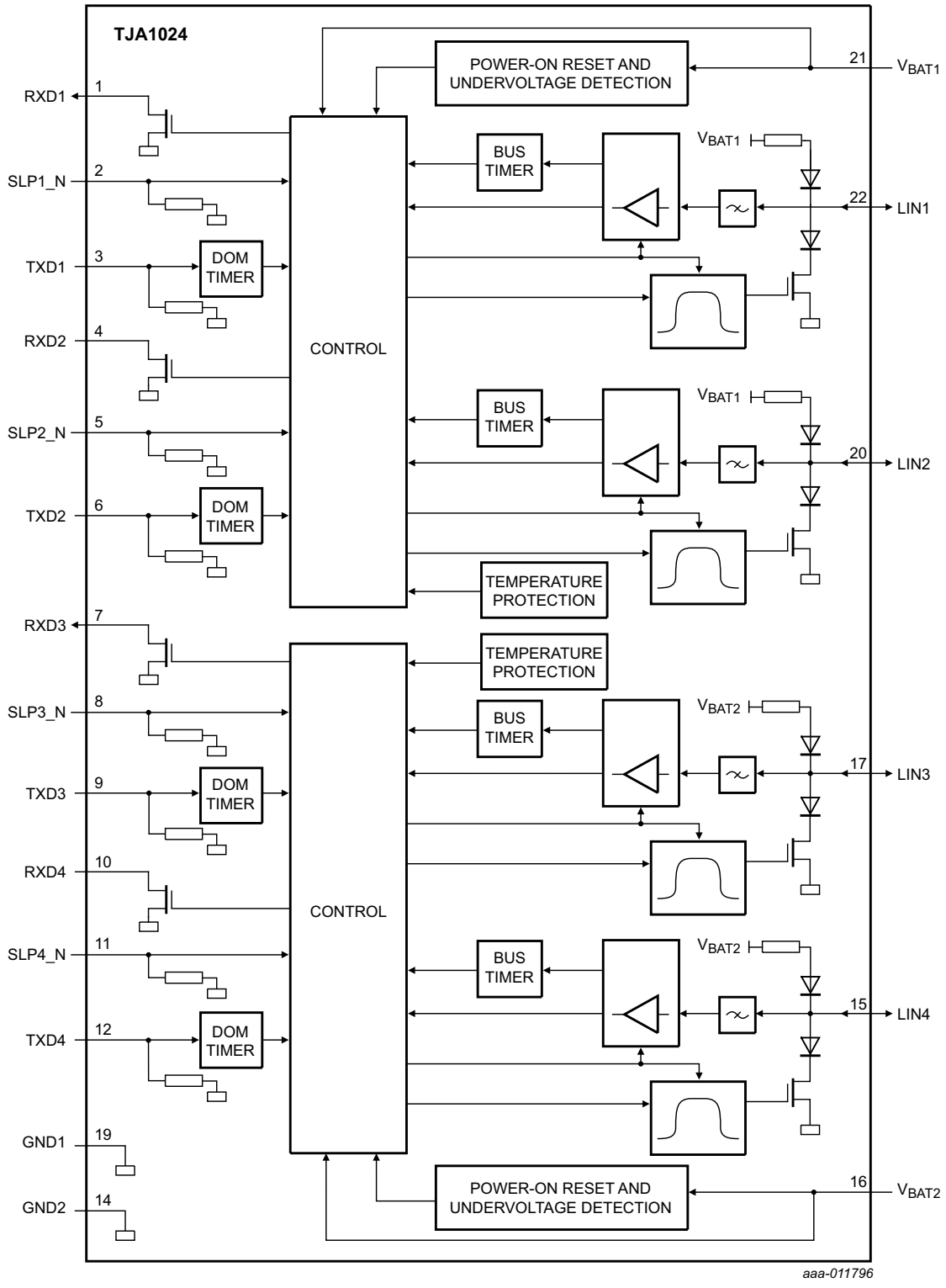


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

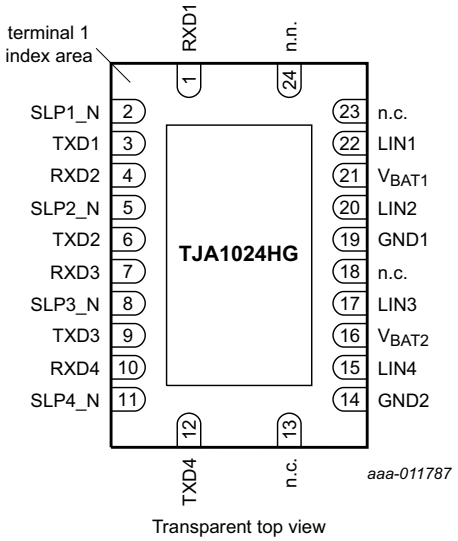


Fig 2. Pin configuration diagram

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
RXD1	1	receive data output 1 (open-drain); active LOW after a wake-up event
SLP1_N	2	sleep control input 1 (active LOW); resets wake-up request on RXD1
TXD1	3	transmit data input 1
RXD2	4	receive data output 2 (open-drain); active LOW after a wake-up event
SLP2_N	5	sleep control input 2 (active LOW); resets wake-up request on RXD2
TXD2	6	transmit data input 2
RXD3	7	receive data output 3 (open-drain); active LOW after a wake-up event
SLP3_N	8	sleep control input 3 (active LOW); resets wake-up request on RXD2
TXD3	9	transmit data input 3
RXD4	10	receive data output 4 (open-drain); active LOW after a wake-up event
SLP4_N	11	sleep control input 4 (active LOW); resets wake-up request on RXD2
TXD4	12	transmit data input 4
n.c.	13	not connected
GND2[1]	14	ground connection for LIN3 and LIN4
LIN4	15	LIN bus line 4 input/output
V_{BAT2}	16	battery supply for LIN3 and LIN4
LIN3	17	LIN bus line 3 input/output
n.c.	18	not connected

Table 3. Pin description *...continued*

Symbol	Pin	Description
GND1[1]	19	ground connection for LIN1 and LIN2
LIN2	20	LIN bus line 2 input/output
V_{BAT1}	21	battery supply for LIN1 and LIN2
LIN1	22	LIN bus line 1 input/output
n.c.	23	not connected
n.c.	24	not connected

[1] For enhanced thermal and electrical performance, the exposed center pad of the DHVQFN24 package should be soldered to board ground (and not to any other voltage level).

7. Functional description

The TJA1024 is the interface between the LIN master/slave protocol controller and the physical bus in a LIN network. According to the Open System Interconnect (OSI) model, this interface is the LIN physical layer.

The LIN transceivers are optimized for, but not limited to, automotive applications with excellent ElectroMagnetic Compatibility (EMC) performance.

7.1 LIN 2.x/SAE J2602 compliant

The TJA1024 is fully LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and SAE J2602 compliant. The LIN physical layer is independent of higher OSI model layers (e.g. the LIN protocol). Consequently, nodes containing a LIN 2.2A-compliant physical layer can be combined, without restriction, with LIN physical layer nodes that comply with earlier revisions (LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3, LIN 2.0, LIN 2.1 and LIN 2.2).

7.2 Operating modes

The transceivers are fully operational in Normal mode. A low-power Sleep mode is also supported, as well as a Reset mode. Standby mode facilitates the transition between Sleep and Normal modes.

The transceivers operate independently (except in Reset mode; see Section 7.2.4), so one transceiver can be in Normal mode while another is in Sleep or Standby etc. Power consumption is at a minimum when all four transceivers are in Sleep mode.

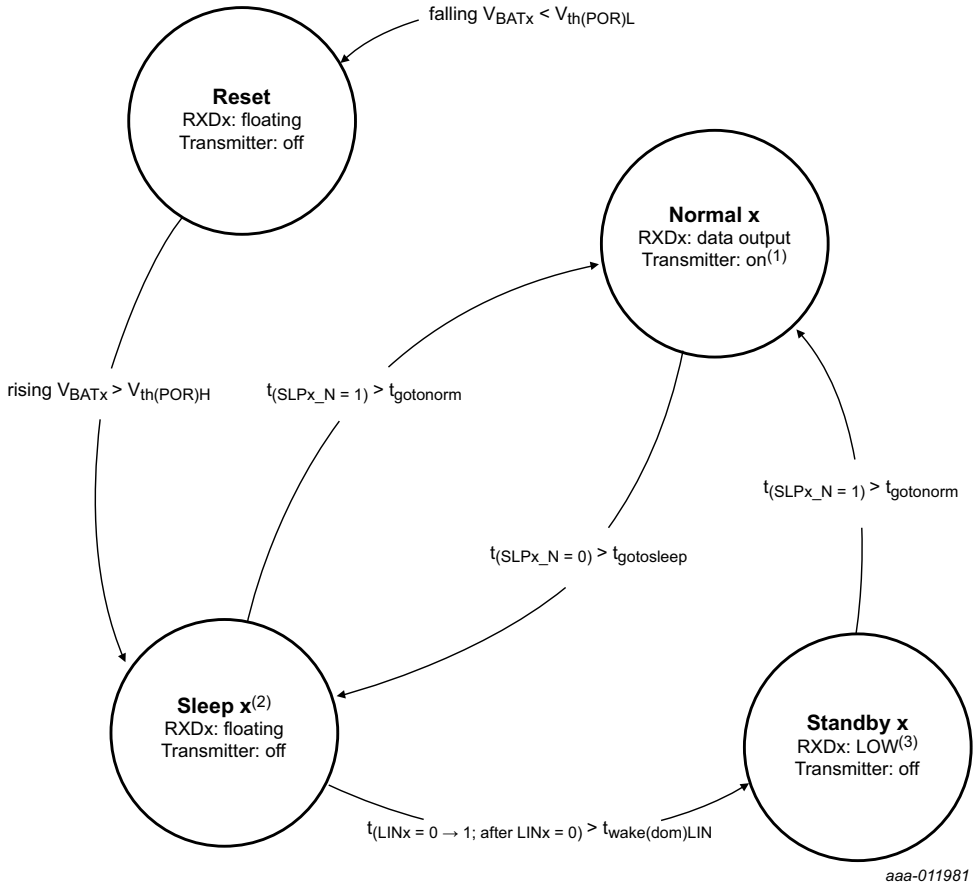
7.2.1 Normal mode

In Normal mode, the TJA1024 can transmit and receive data via the LIN bus lines. The transceivers operate independently, so one can be active while the others are off.

A transceiver switches from Sleep or Standby mode to Normal mode if SLPx_N is held HIGH for $t_{gotonorm}$. If SLPx_N is held LOW for $t_{gotosleep}$, the transceiver switches from Normal to Sleep mode.

The receivers detect data streams on the LIN bus lines (via pins LINx) and transfer the input via pins RXDx to the microcontroller (see Figure 6): HIGH for a recessive level and LOW for a dominant level on the bus. The receivers have supply-voltage related thresholds with hysteresis and integrated filters to suppress bus line noise.

Transmit data streams from the protocol controller are detected on the TXDx pins and are converted by the transmitters into optimized bus signals shaped to minimize EME. The LIN bus output pins are pulled HIGH via internal slave termination resistors. For a master application, an external resistor in series with a diode should be connected between pin V_{BATx} and the appropriate LINx pin (see Figure 6).



(1) A positive edge on SLPx_N triggers a transition to Normal mode in the corresponding LIN transceiver; the LIN transmitter is enabled once TXDx goes HIGH. In the event of thermal shutdown, the transceivers in the affected dual transceiver block are shut down (each block has its own temperature detection so the other two transceivers are not affected).

(2) Power dissipation is at a minimum when all four transceivers are in Sleep mode.

(3) When a transceiver switches to Standby mode in response to a LIN bus wake-up event, the associated RXDx pin will be LOW to indicate which LIN channel was the source of the wake-up request.

Fig 3. State diagram

7.2.2 Sleep mode

A transceiver will switch to Sleep mode from Normal mode if SLPx_N is held LOW for $t_{gotosleep}$. The relevant LIN transmit path is disabled as soon as SLPx_N goes LOW. Power consumption is very low when all four transceivers are in Sleep mode.

The voltage levels on LINx and TXDx have no effect on a transition to Sleep mode. So the transceiver switches to Sleep mode even if TXDx is held LOW or there is a continuous dominant level on LINx (e.g. due to a short circuit to ground).

Although current consumption is extremely low when all four transceivers are in Sleep mode, the TJA1024 can still be woken up remotely via the LIN bus pins or by the microcontroller via pins SLPx_N. Filters on the receiver inputs (LIN1 to LIN4) and on pins SLPx_N prevent unwanted wake-up events occurring due to automotive transients or

radio frequency interference. To be valid, all wake-up events must be maintained for a specific length of time ($t_{wake(dom)LIN}$ for a remote wake-up and $t_{gotonorm}$ for a wake-up via SLPx_N). Pin RXDx is floating when a transceiver is in Sleep mode.

If a remote wake-up event (see Figure 4) is detected on one of the LIN bus lines, the associated transceiver switches to Standby mode. A wake-up initiated by the microcontroller (SLPx_N HIGH for $t_{gotonorm}$) will cause the relevant transceiver to switch to Normal mode while the other transceivers remains in their current state.

7.2.3 Standby mode

Standby mode is an intermediate mode between Sleep and Normal modes. A transceiver switches from Sleep mode to Standby mode in response to a LIN bus wake-up event. Pin RXDx goes low to indicate the source of the remote wake-up to the microcontroller (LIN1, LIN2, LIN3 or LIN4). A transceiver switches from Standby to Normal mode if the microcontroller holds SLPx_N HIGH for $t_{gotonorm}$.

7.2.4 Reset mode

When the voltage on V_{BATx} drops below the LOW-level power-on reset threshold, $V_{th(POR)L}$, the associated dual transceiver block (LIN1/LIN2 and/or LIN3/LIN4) switches to Reset mode. All input signals are ignored and all output drivers are off for the affected transceivers. When the voltage on V_{BATx} rises again above the HIGH-level power-on reset threshold, $V_{th(POR)H}$, the transceivers switch to Sleep mode.

Table 4. Operating modes

Mode	SLPx_N	RXDx	Transmitter x	Description
Reset	x	floating	off	all inputs ignored; all output drivers off
Sleep x[1]	0	floating	off	no wake-up request detected
Standby x[2]	0	LOW[3]	off	remote wake-up request detected
Normal x	1	HIGH: recessive LOW: dominant	on/off[4]	bus signal shaping enabled

[1] Both transceivers in the associated dual transceiver block enter Sleep mode after a power-on reset (e.g. after switching on V_{BATx}).

[2] The appropriate transceiver switches automatically to Standby x mode if a remote LINx wake-up event is detected in Sleep x mode.

[3] RXDx is LOW to indicate the source of the remote wake-up request; RXDx goes HIGH in response to a positive edge on pin SLPx_N.

[4] A positive edge on SLPx_N triggers a transition to Normal mode; the transmitter will be off if TXDx is LOW and will be enabled as soon as TXDx goes HIGH.

7.3 Transceiver wake-up

7.3.1 Remote wake-up via the LIN bus

A falling edge on pin LINx followed by a LOW level maintained for $t_{wake(dom)LIN}$ followed by a rising edge on pin LINx triggers a remote wake-up (see Figure 4). It should be noted that the time period $t_{wake(dom)LIN}$ is measured either in Normal mode while TXDx is HIGH, or in Sleep mode irrespective of the status of pin TXDx.

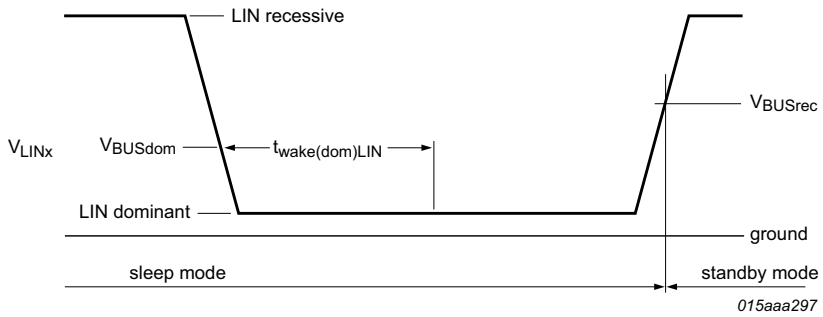


Fig 4. Remote wake-up behavior

7.3.2 Wake-up via SLPx_N

If SLPx_N is held HIGH for $t_{gotonorm}$, the transceiver switches from Sleep mode to Normal mode.

7.4 Operation during automotive cranking pulses

TJA1024 remains fully operational during automotive cranking pulses because the LIN transceivers are fully specified down to V_{BATx} = 5 V.

7.5 Operation when supply voltage is outside specified operating range

If V_{BAT1} and/or V_{BAT2} > 18 V or < 5 V, the respective dual transceiver block may remain operational, but parameter values cannot be guaranteed to remain within the operating ranges specified in Table 7 and Table 8 for the relevant transceiver block (LIN1/LIN2 or LIN3/LIN4).

In Normal mode:

- If the input level on pin TXDx is HIGH, the LIN transmitter output on pin LINx will be recessive.
- If the input level on pin LINx is recessive, the receiver output on pin RXDx will be HIGH.
- If the voltage on pin V_{BATx} rises to 27 V (e.g. during an automotive jump-start), the total LIN network pull-up resistance should be greater than 680 Ω and the total LIN network capacitance should be less than 6.8 nF to ensure reliable LIN data transfer.
- If the voltage on pin V_{BATx} drops below the LOW-level V_{BAT} LOW threshold, $V_{th(VBATL)L}$, the active LIN transmit path(s) is interrupted and both associated LIN outputs will be recessive. The previously active LIN transmit path(s) is switched on again when V_{BATx} rises above $V_{th(VBATL)H}$ and pin TXDx is HIGH.

If the voltage on pin V_{BATx} drops below the LOW-level power-on reset threshold, $V_{th(POR)L}$, the associated transceivers switch to Reset mode (i.e. the output drivers are disabled and the inputs are ignored). When the voltage on V_{BATx} rises again above $V_{th(POR)H}$, the transceivers will switch to Sleep mode.

7.6 Fail-safe features

Pin TXDx is pulled down to ground in order to force a predefined level on the transmit data input if the pin is disconnected.

Pin SLPx_N is pulled down to ground to ensure that the transceiver is forced to Sleep x mode if SLPx_N is disconnected.

Pins RXD1 and RXD2 are set floating if V_{BAT1} is disconnected. Pins RXD3 and RXD4 are set floating if V_{BAT2} is disconnected.

The current in the transmitter output stage is limited to protect the transmitter against short circuits to pins V_{BATx} or GNDx.

A loss of power (pins V_{BATx} and GNDx) has no impact on the bus lines or on the microcontroller. No reverse currents flow from the bus lines into the LINx pins. The current path from V_{BATx} to LINx via the integrated LIN slave termination resistors remains. The TJA1024 can be disconnected from the power supply without influencing the LIN buses.

The output drivers on pins LIN1, LIN2, LIN3 and LIN4 are protected against overtemperature conditions. If the junction temperature at one of the transceiver blocks exceeds the shutdown junction temperature, $T_{j(sd)}$, the thermal protection circuit disables the relevant output drivers (LIN1/LIN2 or LIN3/LIN4). The drivers are enabled again when the junction temperature falls below $T_{j(sd)}$ and pin TXDx is HIGH.

The initial TXD dominant check prevents the bus being driven to a permanent dominant state (blocking all network communications) if pin TXDx is forced permanently LOW by a hardware and/or software application failure. The input level on TXDx is checked after a transition to Normal mode. If TXDx is LOW, the transmit path remains disabled and is only enabled when TXDx goes HIGH.

Once the transmitter has been enabled, a TXD dominant time-out timer is started every time pin TXDx goes LOW. If the LOW state on pin TXDx persists for longer than the TXD dominant time-out time ($t_{to(dom)TXD}$), the transmitter is disabled, releasing the bus line to recessive state. The TXD dominant time-out timer is reset when pin TXDx goes HIGH.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to pin GND, unless otherwise specified. Positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{BAT}	battery supply voltage	pins V_{BAT1} and V_{BAT2}	–0.3	+42	V
V_{TXD}	voltage on pin TXD	pins TXD1 to TXD4	–0.3	+7	V
V_{RXD}	voltage on pin RXD	pins RXD1 to RXD4	–0.3	+7	V
V_{SLP_N}	voltage on pin SLP_N	pins SLP1_N to SLP4_N	–0.3	+7	V
V_{LIN}	voltage on pin LIN	pins LIN1 to LIN4; with respect to GND and V_{BAT}	–42	+42	V
$\lvert\Delta V_{(LIN1-LIN2)}\rvert$	voltage difference between pin LIN1 and pin LIN2 (absolute value)		-	42	V
$\lvert\Delta V_{(LIN3-LIN4)}\rvert$	voltage difference between pin LIN3 and pin LIN4 (absolute value)		-	42	V
V_{ESD}	electrostatic discharge voltage				
	according to IEC 61000-4-2	on pins LINx, V_{BATx} [1]	–8	+8	kV
	human body model	on pins LINx, V_{BATx} [2]	–8	+8	kV
		on pins TXDx, RXDx and SLPx_N [2]	–2	+2	kV
	charge device model	all pins	–750	+750	V
	machine model	all pins [3]	–200	+200	V
T_{vj}	virtual junction temperature	[4]	–40	+150	°C
T_{stg}	storage temperature		–55	+150	°C

[1] Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor.

[2] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.

[3] Equivalent to discharging a 200 pF capacitor through a 10 Ω resistor and a 0.75 μH coil.

[4] Junction temperature in accordance with IEC 60747-1. An alternative definition is: $T_j = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	dual-layer board [1]	68	K/W
		four-layer board [2]	39	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-3 at natural convection on 1s board with thermal via array under the exposed pad connected to the second copper layer.

[2] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 μm) and thermal via array under the exposed pad connected to the first inner copper layer.

10. Static characteristics

Table 7. Static characteristics

V_{BAT} = 5 V to 18 V; T_{vj} = −40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500 Ω; all voltages are referenced to pin GND; positive currents flow into the IC; typical values are given at V_{BAT} = 12 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{BAT}	battery supply voltage	pins V_{BAT1} and V_{BAT2}	5	-	18	V
I_{BAT}	battery supply current	per pin (V_{BAT1} or V_{BAT2}):				
		Sleep mode (both channels); bus recessive (both channels); V_{LINx} = V_{BATx}; V_{SLPx_N} = 0 V	2.5	7	10	µA
		Sleep mode (both channels); bus dominant (both channels); V_{LINx} = 0 V; V_{SLPx_N} = 0 V; V_{BATx} = 12 V	300	800	3200	µA
		Standby mode (both channels); bus recessive (both channels); V_{LINx} = V_{BATx}; V_{SLPx_N} = 0 V	2.5	7	10	µA
		Standby mode (both channels); bus dominant (both channels); V_{LINx} = 0 V; V_{SLPx_N} = 0 V; V_{BATx} = 12 V	200	600	2000	µA
		Normal mode (both channels); bus recessive (both channels); V_{TXDx} = 5 V; V_{LINx} = V_{BATx}; V_{SLPx_N} = 5 V	300	1600	3200	µA
		Normal mode (both channels); bus dominant (both channels); V_{TXDx} = 0 V; V_{SLPx_N} = 5 V; V_{BATx} = 12 V	1	4	10	mA
Undervoltage reset						
$V_{th(POR)L}$	LOW-level power-on reset threshold voltage	power-on reset	1.6	3.1	3.9	V
$V_{th(POR)H}$	HIGH-level power-on reset threshold voltage		2.3	3.4	4.3	V
$V_{hys(POR)}$	power-on reset hysteresis voltage	[2]	0.05	0.3	1	V
$V_{th(VBATL)L}$	LOW-level V_{BAT} LOW threshold voltage		3.9	4.4	4.7	V
$V_{th(VBATL)H}$	HIGH-level V_{BAT} LOW threshold voltage		4.2	4.7	4.9	V
$V_{hys(VBATL)}$	V_{BAT} LOW hysteresis voltage	[2]	0.15	0.3	0.6	V
Pins TXDx and SLPx_N						
V_{IH}	HIGH-level input voltage		2	-	7	V
V_{IL}	LOW-level input voltage		−0.3	-	+0.8	V
V_{hys}	hysteresis voltage	[2]	50	200	400	mV

Table 7. Static characteristics *...continued*

V_{BAT} = 5 V to 18 V; T_{vj} = −40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500 Ω; all voltages are referenced to pin GND; positive currents flow into the IC; typical values are given at V_{BAT} = 12 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{pd}	pull-down resistance	on TXDx	50	125	325	kΩ
		on SLPx_N	100	250	650	kΩ
I_{IL}	LOW-level input current	V_{TXDx} = 0 V or V_{SLPx_N} = 0 V	−5	-	+5	µA
Pin RXDx (open-drain)						
I_{OL}	LOW-level output current	V_{RXDx} = 0.4 V	2	-	-	mA
I_{LH}	HIGH-level leakage current	[2]	−5	-	+5	µA
Pin LINx						
I_{BUS_LIM}	current limitation for driver dominant state	V_{BAT} = 18 V; V_{LINx} = 18 V; V_{TXDx} = 0 V	40	-	100	mA
$I_{BUS\_PAS\_dom}$	receiver dominant input leakage current including pull-up resistor	[2] V_{BAT} = 12 V; V_{LINx} = 0 V; V_{TXDx} = 5 V	−600	-	-	µA
$I_{BUS\_PAS\_rec}$	receiver recessive input leakage current	[2] V_{BAT} = 5 V; V_{LINx} = 18 V; V_{TXDx} = 5 V	-	0	1	µA
$I_{BUS\_NO\_GND}$	loss-of-ground bus current	[2] V_{BAT} = 18 V; V_{LINx} = 0 V	−750	-	+10	µA
$I_{BUS\_NO\_BAT}$	loss-of-battery bus current	[2] V_{BAT} = 0 V; V_{LINx} = 18 V	-	-	1	µA
V_{BUSdom}	receiver dominant state		-	-	$0.4V_{BAT}$	V
V_{BUSrec}	receiver recessive state		$0.6V_{BAT}$	-	-	V
V_{BUS_CNT}	receiver center voltage	V_{BUS_CNT} = (V_{BUSdom} + V_{BUSrec}) / 2	$0.475V_{BAT}$	$0.5V_{BAT}$	$0.525V_{BAT}$	V
V_{HYS}	receiver hysteresis voltage	V_{HYS} = V_{BUSrec} − V_{BUSdom}	-	-	$0.175V_{BAT}$	V
$V_{SerDiode}$	voltage drop at the serial diode	[2] in pull-up path with R_{slave}; $I_{SerDiode}$ = 0.9 mA	0.4	-	1.0	V
$V_{O(dom)}$	dominant output voltage	[2] Normal mode; V_{TXDx} = 0 V; V_{BAT} = 7.0 V	-	-	1.4	V
		[2] Normal mode; V_{TXDx} = 0 V; V_{BAT} = 18 V	-	-	2.0	V
R_{slave}	slave resistance		20	30	60	kΩ
C_{LIN}	capacitance on pin LIN	[2] pins LIN1 and LIN2; with respect to GND	-	-	20	pF
Thermal shutdown						
$T_{j(sd)}$	shutdown junction temperature	[2]	150	-	200	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] Not tested in production; guaranteed by design.

11. Dynamic characteristics

Table 8. Dynamic characteristics

V_{BAT} = 5 V to 18 V; T_{vj} = −40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500 Ω; all voltages are referenced to pin GND; positive currents flow into the IC; typical values are given at V_{BAT} = 12 V, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Duty cycles						
δ1	duty cycle 1	$V_{th(rec)(max)}$ = 0.744 × V_{BAT}; $V_{th(dom)(max)}$ = 0.581 × V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 7 V to 18 V [2][4][5]	0.396	-	-	
		$V_{th(rec)(max)}$ = 0.768 × V_{BAT}; $V_{th(dom)(max)}$ = 0.6 × V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 5 V to 7 V [2][4][5]	0.396	-	-	
δ2	duty cycle 2	$V_{th(rec)(min)}$ = 0.422 × V_{BAT}; $V_{th(dom)(min)}$ = 0.284 × V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 7.6 V to 18 V [3][4][5]	-	-	0.581	
		$V_{th(rec)(min)}$ = 0.405 × V_{BAT}; $V_{th(dom)(min)}$ = 0.271 × V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 5.6 V to 7.6 V [3][4][5]	-	-	0.581	
δ3	duty cycle 3	$V_{th(rec)(max)}$ = 0.778 × V_{BAT}; $V_{th(dom)(max)}$ = 0.616 × V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 7 V to 18 V [2][4][5]	0.417	-	-	
		$V_{th(rec)(max)}$ = 0.805 × V_{BAT}; $V_{th(dom)(max)}$ = 0.637 × V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 5 V to 7 V [2][4][5]	0.417	-	-	
δ4	duty cycle 4	$V_{th(rec)(min)}$ = 0.389 × V_{BAT}; $V_{th(dom)(min)}$ = 0.251 × V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 7.6 V to 18 V [3][4][5]	-	-	0.590	
		$V_{th(rec)(min)}$ = 0.372 × V_{BAT} $V_{th(dom)(min)}$ = 0.238 × V_{BAT} t_{bit} = 96 µs; V_{BAT} = 5.6 V to 7.6 V [3][4][5]	-	-	0.590	
Timing characteristics						
t_{rx_pd}	receiver propagation delay	rising and falling; C_{RXDx} = 20 pF; R_{RXDx} = 2.4 kΩ [5]	-	-	6	µs
t_{rx_sym}	receiver propagation delay symmetry	C_{RXDx} = 20 pF; R_{RXDx} = 2.4 kΩ; rising edge with respect to falling edge [5]	−2	-	+2	µs
$t_{wake(dom)LIN}$	LIN dominant wake-up time	Sleep mode	30	80	150	µs
$t_{gotonorm}$	go to normal time	time period for mode change from Sleep or Standby mode to Normal mode	2	6	10	µs
$t_{init(norm)}$	normal mode initialization time		7	-	20	µs
$t_{gotosleep}$	go to sleep time	time period for mode change from Normal to Sleep mode	2	6	10	µs
$t_{to(dom)TXD}$	TXD dominant time-out time	timer started at falling edge on TXDx	6	12	50	ms

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.

[2] $\delta 1, \delta 3 = \frac{t_{bus(rec)(min)}}{2 \times t_{bit}}$. Variable $t_{bus(rec)(min)}$ is illustrated in the LIN timing diagram in Figure 5.

[3] $\delta 2, \delta 4 = \frac{t_{bus(rec)(max)}}{2 \times t_{bit}}$. Variable $t_{bus(rec)(max)}$ is illustrated in the LIN timing diagram in Figure 5.

[4] Bus load conditions: C_{BUS} = 1 nF and R_{BUS} = 1 kΩ; C_{BUS} = 6.8 nF and R_{BUS} = 660 Ω; C_{BUS} = 10 nF and R_{BUS} = 500 Ω.

[5] See timing diagram in Figure 5.

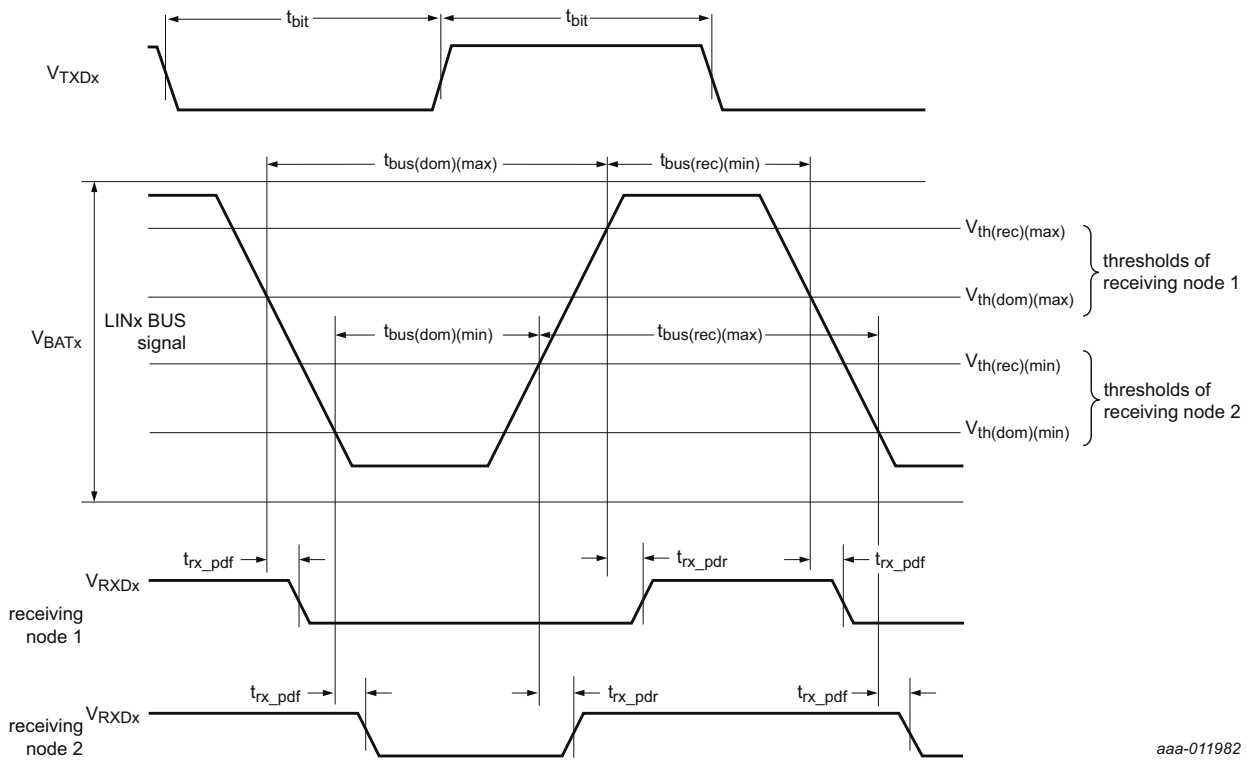
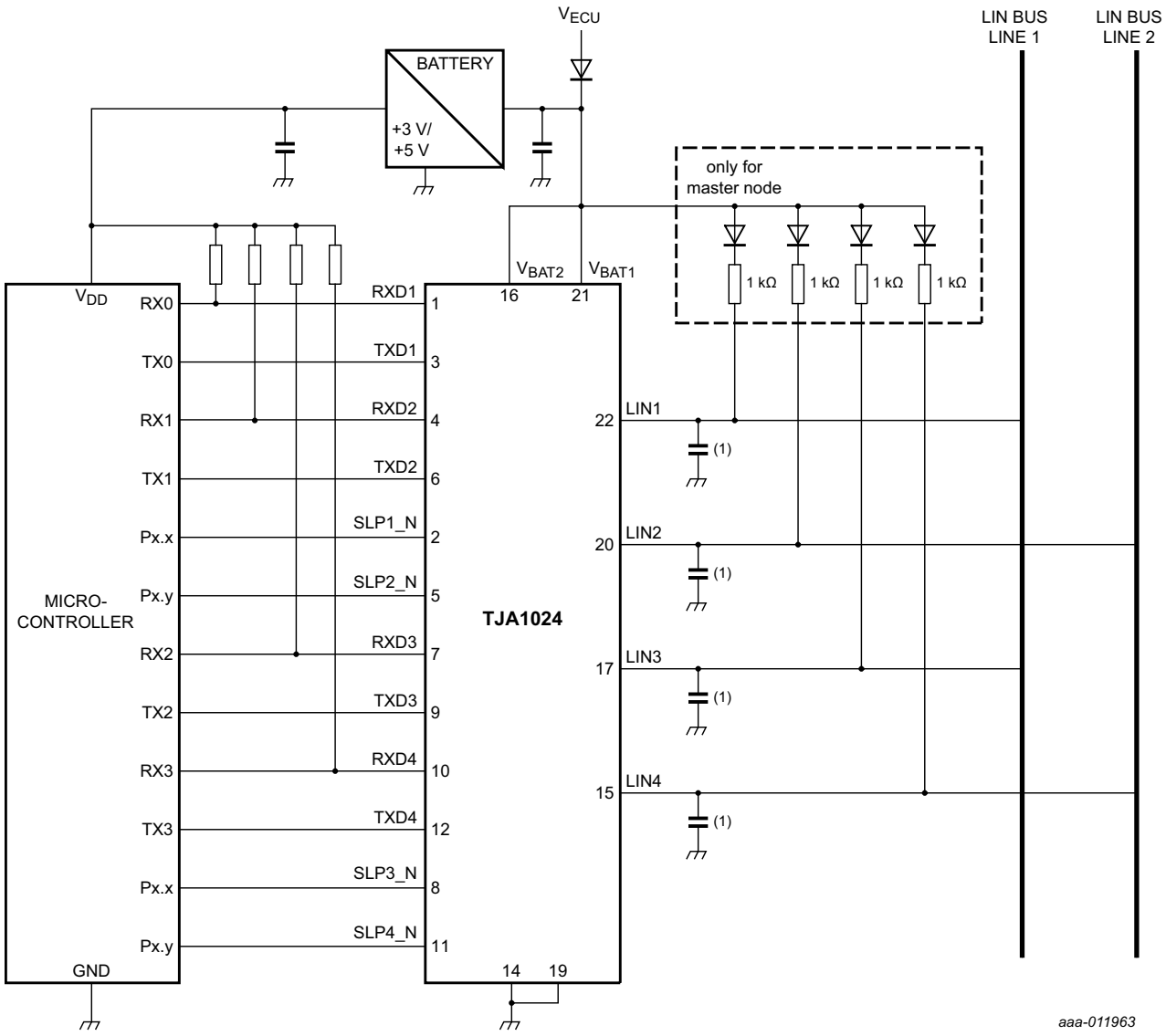


Fig 5. Timing diagram of LIN transceiver duty cycle

12. Application information

12.1 Application diagram



(1) Master: C = 1 nF; slave: C = 220 pF

Fig 6. Application diagram

12.2 ESD robustness according to LIN EMC test specification

ESD robustness (IEC 61000-4-2) has been tested by an external test house according to the LIN EMC test specification (part of Conformance Test Specification Package for LIN 2.1, October 10th, 2008). The test report is available on request.

Table 9. ESD robustness (IEC 61000-4-2) according to LIN EMC test specification

Pin	Test configuration	Value	Unit
LINx	no capacitor connected to LINx pin	±11	kV
	220 pF capacitor connected to LINx pin	±12	kV
V_{BATx}	100 nF capacitor connected to V_{BATx} pin	> |15|	kV

12.3 Hardware requirements for LIN interfaces in automotive applications

The TJA1024 satisfies the "Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications", Version 1.3, May 2012.

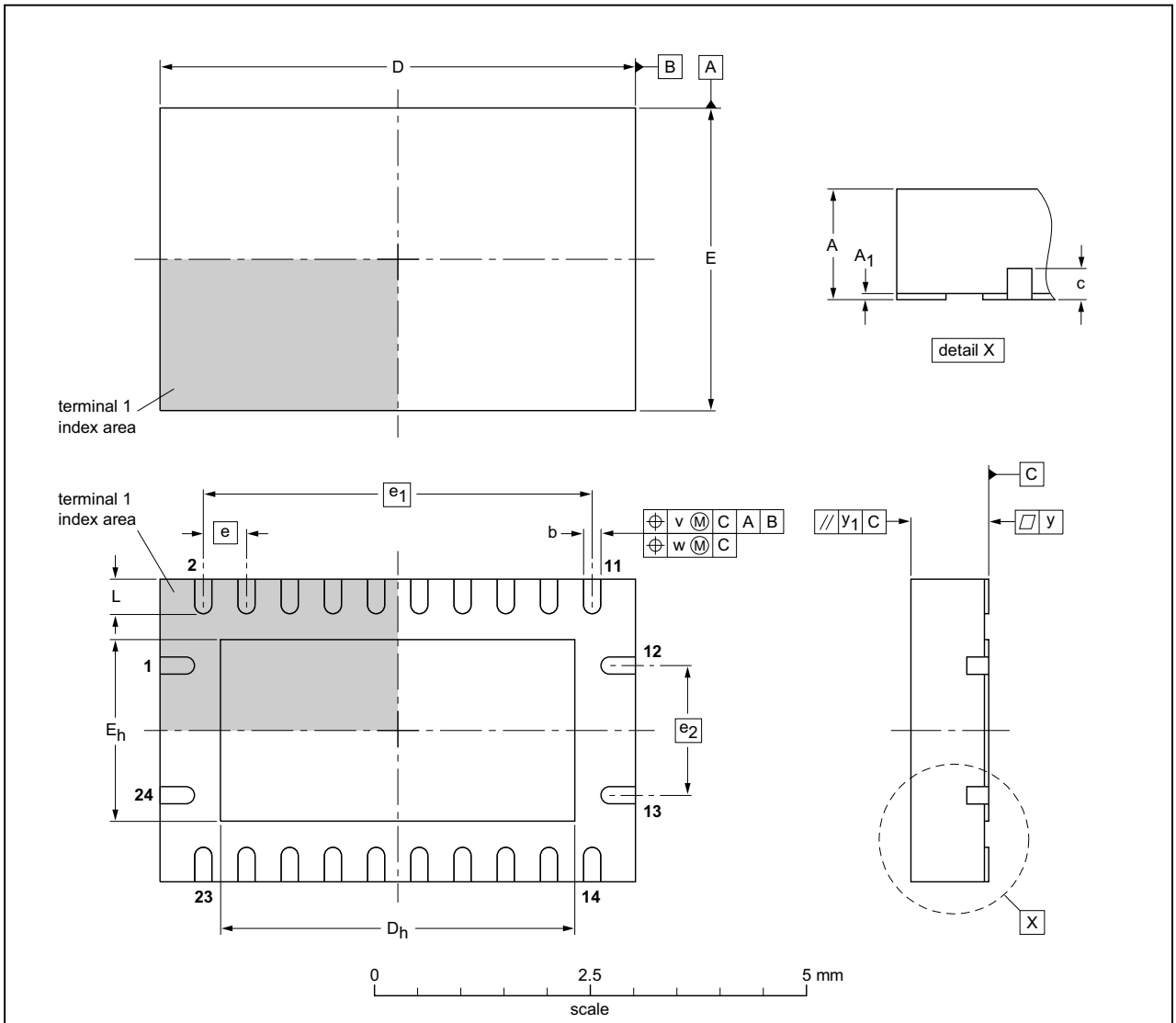
13. Test information

13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-G - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

14. Package outline

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm **SOT815-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.6 5.4	4.25 3.95	3.6 3.4	2.25 1.95	0.5	4.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT815-1	- - -	- - -	- - -			03-04-29

Fig 7. Package outline SOT815-1 (DHVQFN24)

15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 8) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and 11

Table 10. SnPb eutectic process (from J-STD-020D)

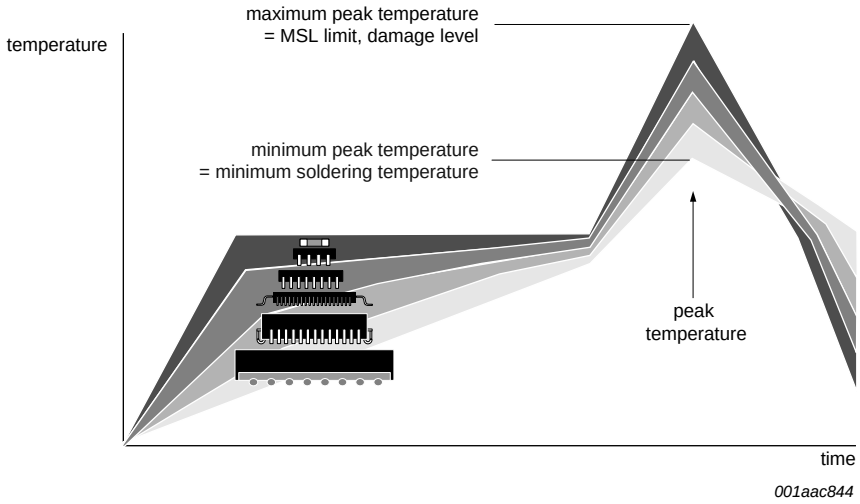
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 11. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 8.



MSL: Moisture Sensitivity Level

Fig 8. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Soldering of DHVQFN packages

Section 16 contains a brief introduction to the techniques most commonly used to solder Surface Mounted Devices (SMD). A more detailed discussion on soldering DHVQFN leadless package ICs can be found in the following application notes:

- *AN10365 "Surface mount reflow soldering description"*
- *AN10366 "HVQFN application information"*

18. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1024 v.1	20150212	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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