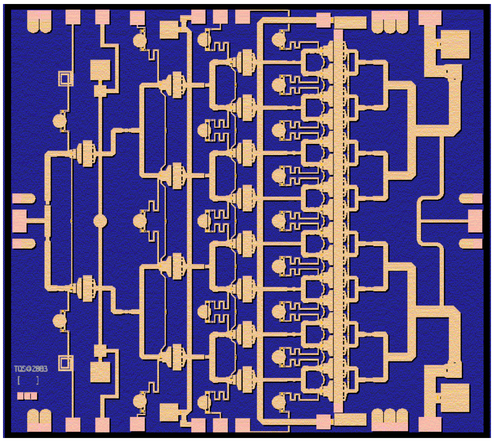
Ka Band Power Amplifier



Key Features

- Frequency Range: 31 - 37 GHz
- 35 dBm Nominal Psat @ Mid-band
- 20 dB Nominal Gain @ Mid-band
- 12 dB Nominal Return Loss
- Bias 5-6 V, 2 A Quiescent
- 0.15 um 3MI pHEMT Technology
- Chip Dimensions 4.35 x 3.90 x 0.05 mm
  (0.171 x 0.154 x 0.002) in

Primary Applications

- Point-to-Point Radio
- Military Radar Systems
- Ka-Band Sat-Com

Product Description

The TriQuint TGA4517 is a compact High Power Amplifier MMIC for Ka-band applications. The part is designed using TriQuint's 0.15um gate power pHEMT process.

The TGA4517 nominally provides 35dBm of Saturated Output Power, and 20dB small signal gain @ mid-band of 31 - 37GHz. The MMIC also provides 12dB Return Loss.

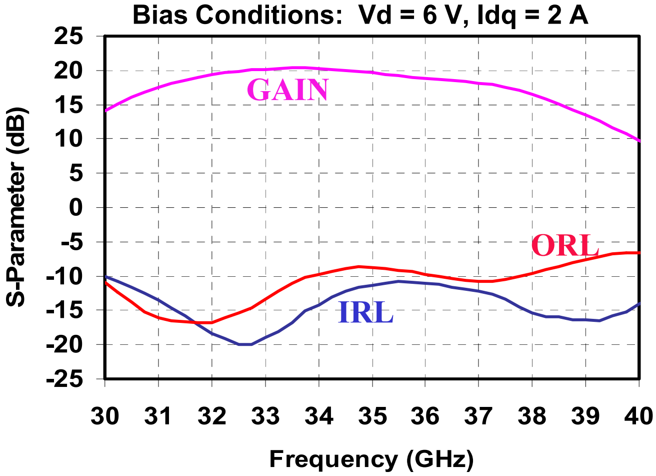
The part is ideally suited for markets such as Point-to-Point Radio, Military Radar Systems, and Ka-Band Satellite Communications both commercial and military.

The TGA4517 is 100% DC and RF tested on-wafer to ensure performance compliance.

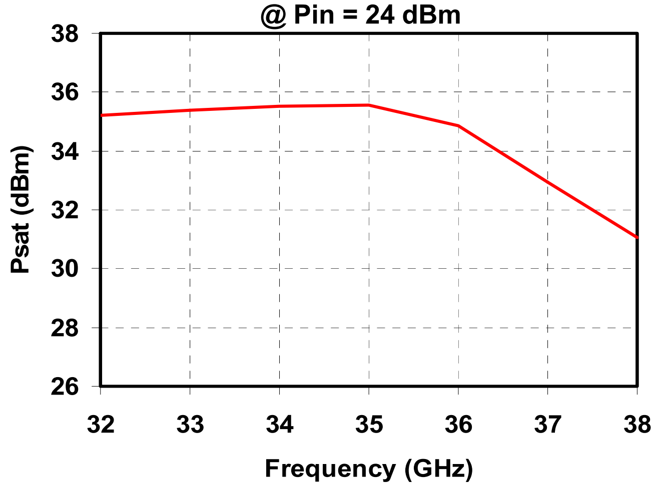
Lead-Free & RoHS compliant.

Measured Fixtured Data

Bias Conditions: Vd = 6 V, Idq = 2 A



Bias Conditions: Vd = 6 V, Idq = 2 A, Duty = 20% @ Pin = 24 dBm



Datasheet subject to change without notice

TABLE I
ABSOLUTE MAXIMUM RATINGS 1/

SYMBOL	PARAMETER	VALUE	NOTES
Vd	Drain Voltage	6.5 V	2/
Vg	Gate Voltage Range	-3 TO 0 V	
Id	Drain Current (Under RF Drive)	4 A	2/ 3/
$\lvert Ig \rvert$	Gate Current	141 mA	3/
P_{IN}	Input Continuous Wave Power	TBD	
P_D	Power Dissipation	26 W	2/ 4/
T_{CH}	Operating Channel Temperature	200 °C	5/ 6/
	Mounting Temperature (30 Seconds)	320 °C	
T_{STG}	Storage Temperature	-65 to 150 °C	

1/ These ratings represent the maximum operable values for this device.

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.

3/ Total current for the entire MMIC.

4/ When operated at this bias condition (with RF applied) at a base plate temperature of 70 °C, the median life is 3.5E+4 hrs.

5/ Junction operating temperature will directly affect the device median time to failure (Tm). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

6/ These ratings apply to each individual FET.

TABLE II
DC PROBE TESTS
(Ta = 25 °C, Nominal)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
$V_{BVGD,Q1-Q2}$	Breakdown Voltage Gate-Drain	-30	-14	-11	V
$V_{BVGD,Q15-Q30}$	Breakdown Voltage Gate-Drain	-30	-14	-11	V
$V_{P,Q15-Q30}$	Pinch-Off Voltage	-1.5	-1	-0.5	V

Each FET Cell is 750um

TABLE III
ELECTRICAL CHARACTERISTICS
(Ta = 25 ^{0}C, Nominal)

PARAMETER	TYPICAL	UNITS
Frequency Range	31 - 37	GHz
Drain Voltage, Vd	6	V
Drain Current (Quiescent), Idq	2	A
Gate Voltage, Vg	-0.5	V
Small Signal Gain, S21 @ Mid-band	20	dB
Input Return Loss, S11	14	dB
Output Return Loss, S22	12	dB
Output Power, Psat	35	dBm

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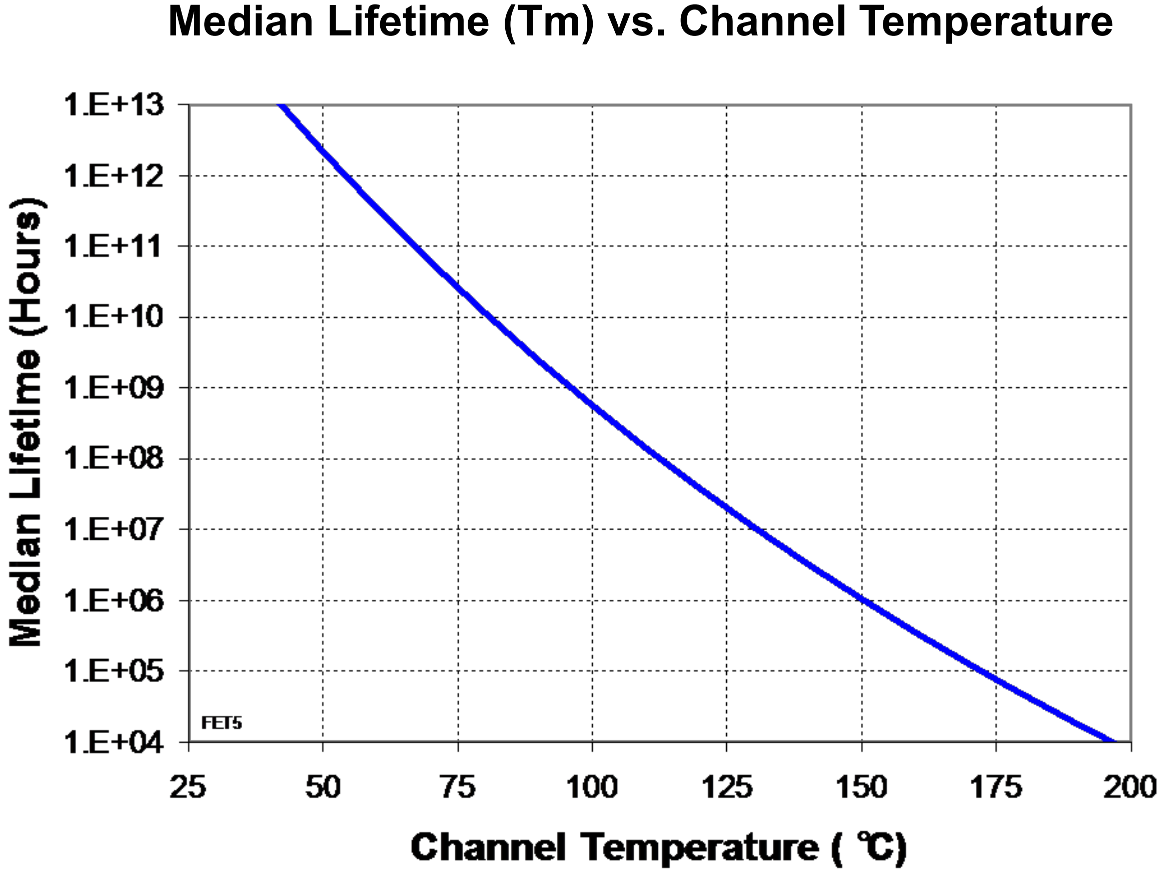
TABLE IV
THERMAL INFORMATION

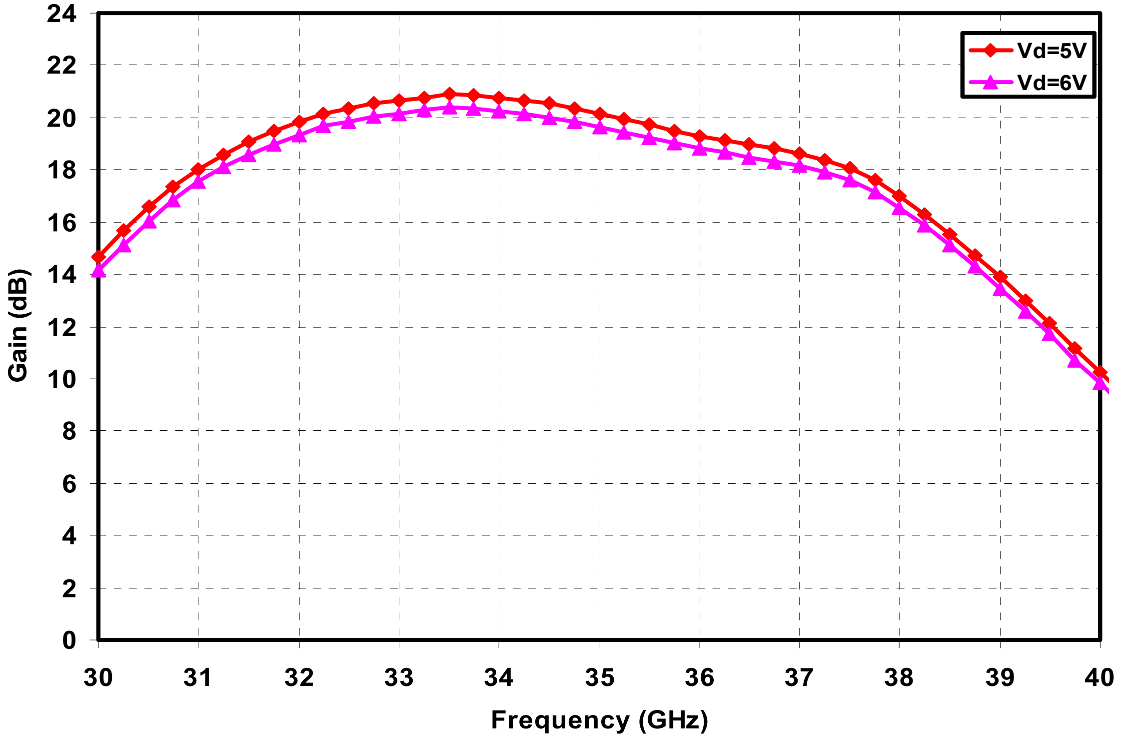
PARAMETER	TEST CONDITIONS	T_{CH} (°C)	θ_{JC} (°C/W)	Tm (HRS)
θ_{JC} Thermal Resistance (channel to backside of carrier)	Vd = 6 V Idq = 2 A Pdiss = 12 W	122.3	4.36	1.2E+7

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

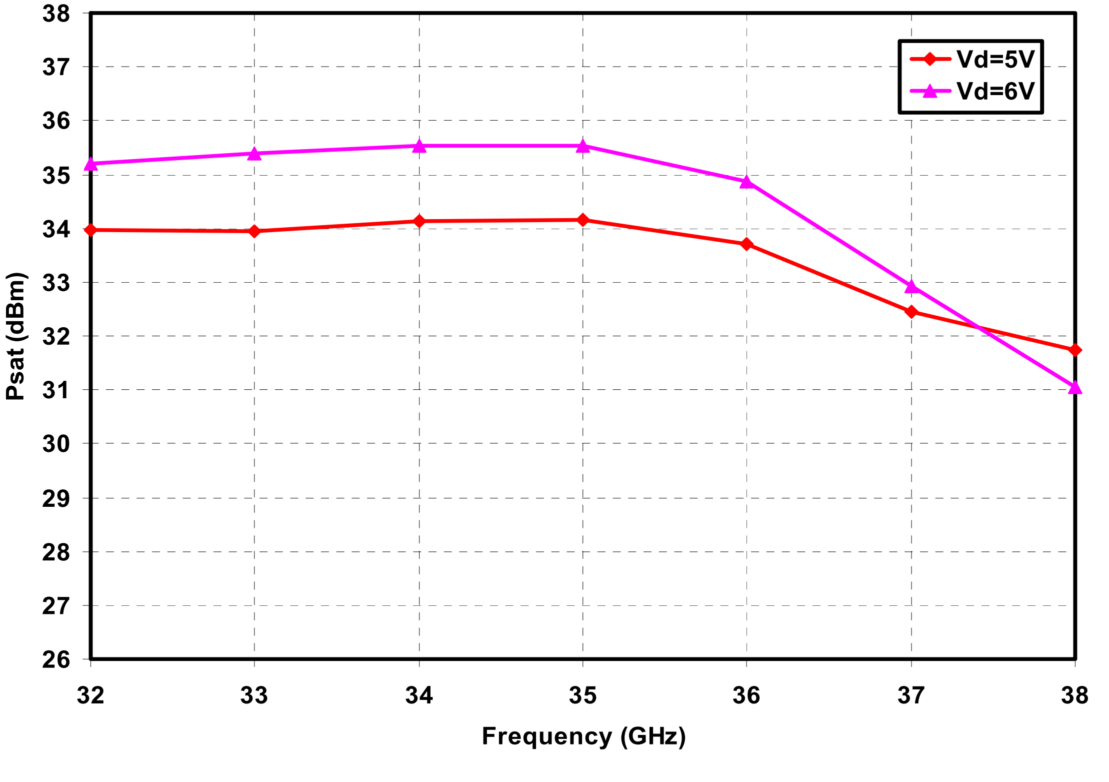


Measured Data

Bias Conditions: Vd =5-6 V, Idq = 2 A, Room Temp.



Bias Conditions: Vd =5-6 V, Idq = 2 A, Duty = 20%, Room Temp.



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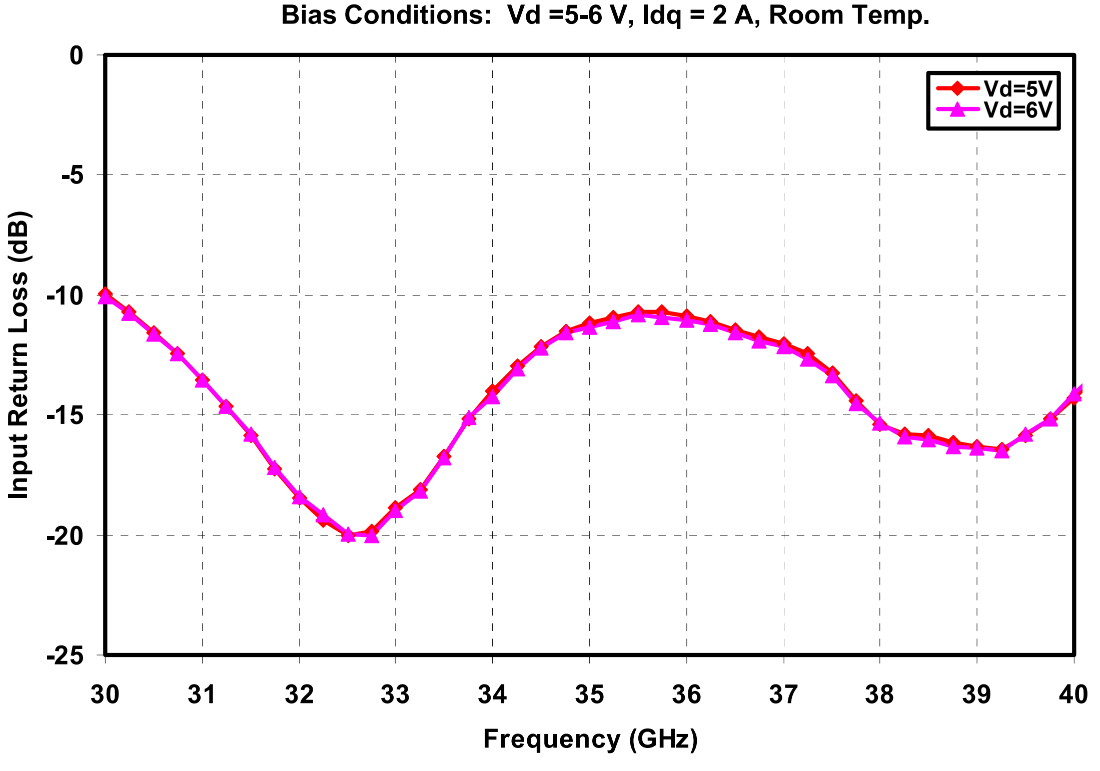
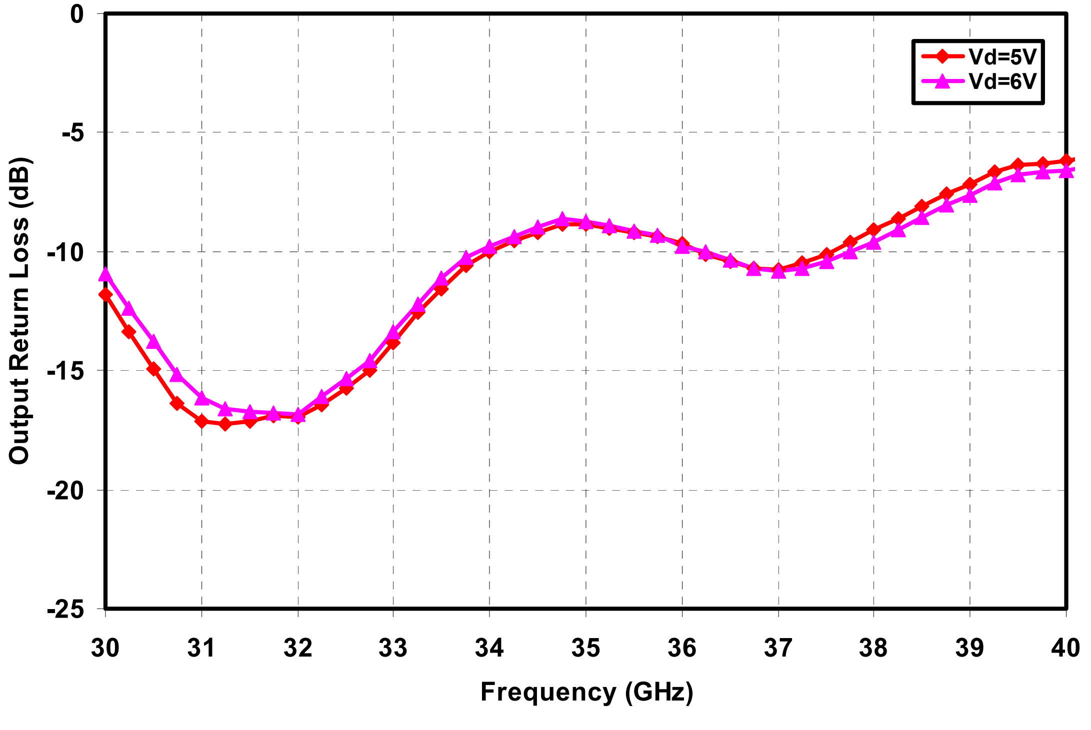
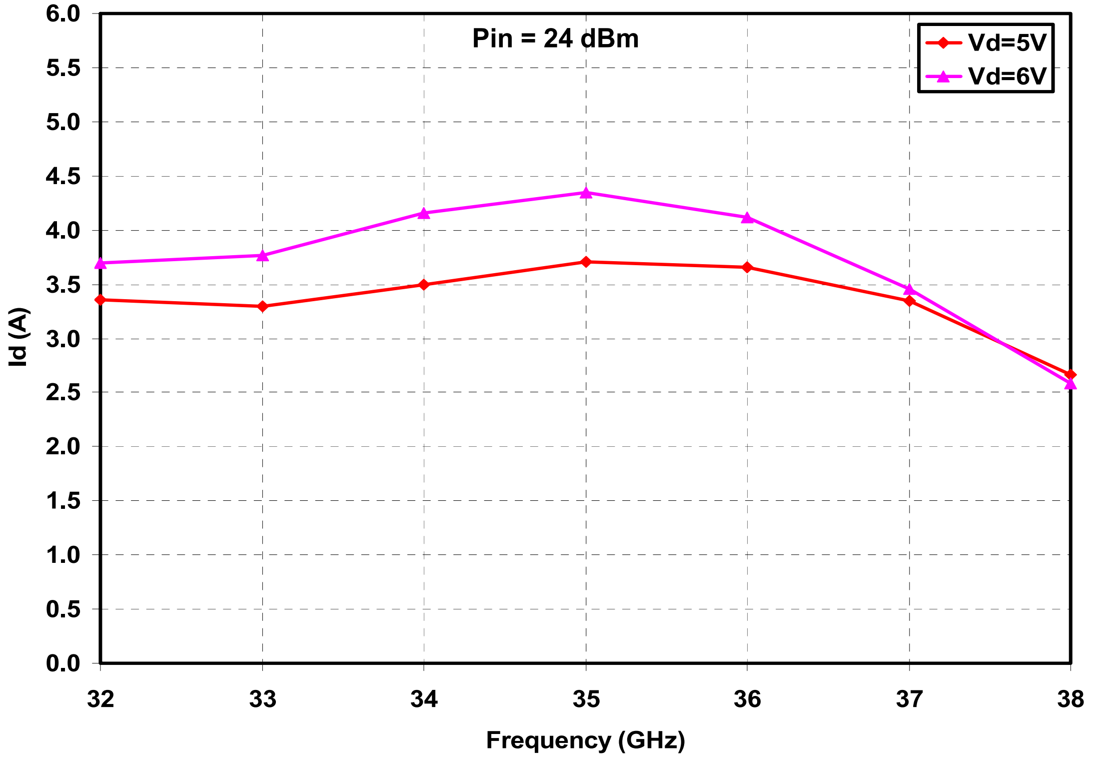
Measured Data

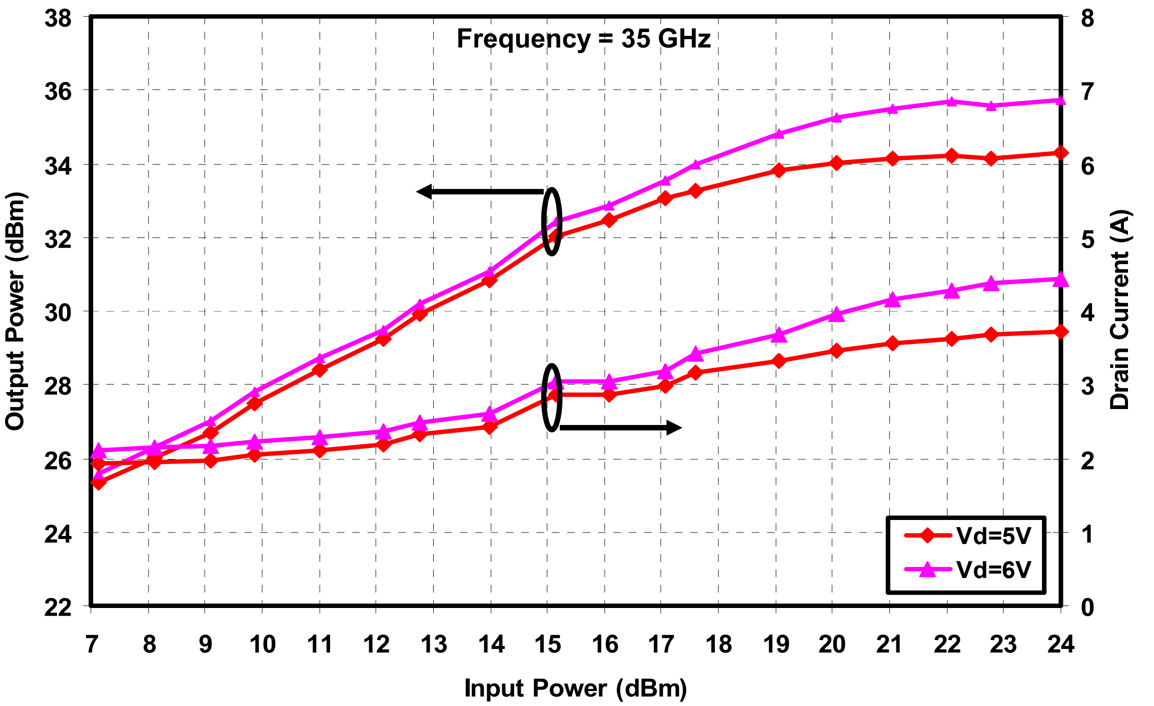




Measured Data

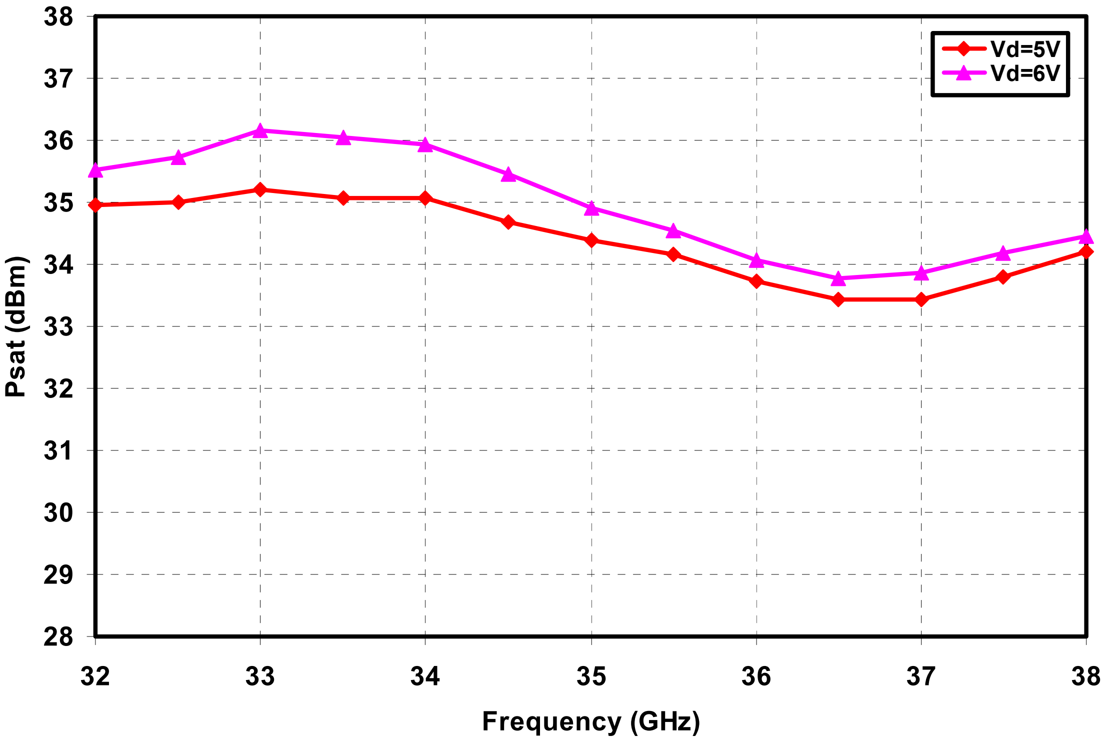
Drain Current vs. Drain Voltage, Duty = 20%, Room Temp.



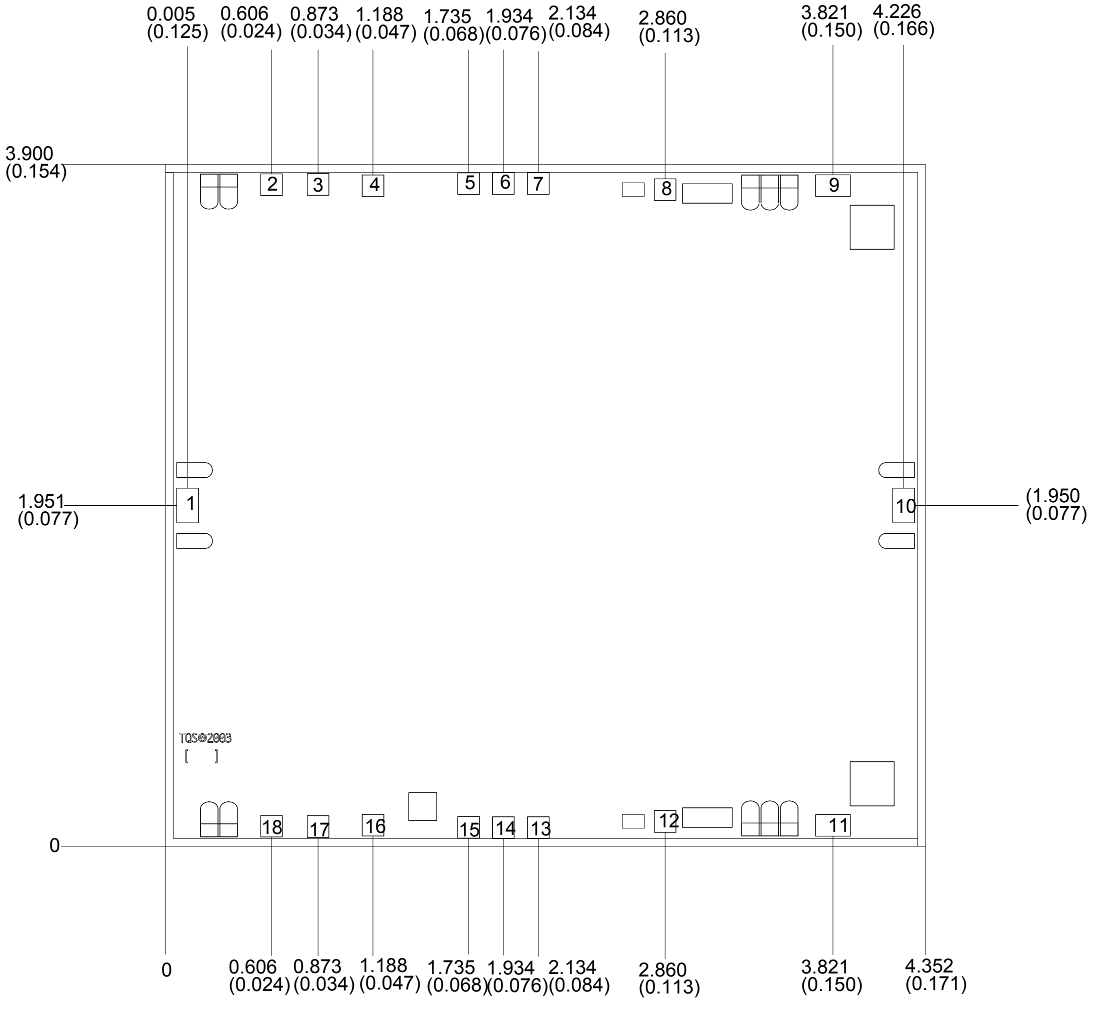


Measured Data

Bias Conditions: Vd =5-6 V, Idq = 2 A, CW Power @ Pin = 22dBm, Room Temp.



Mechanical Drawing

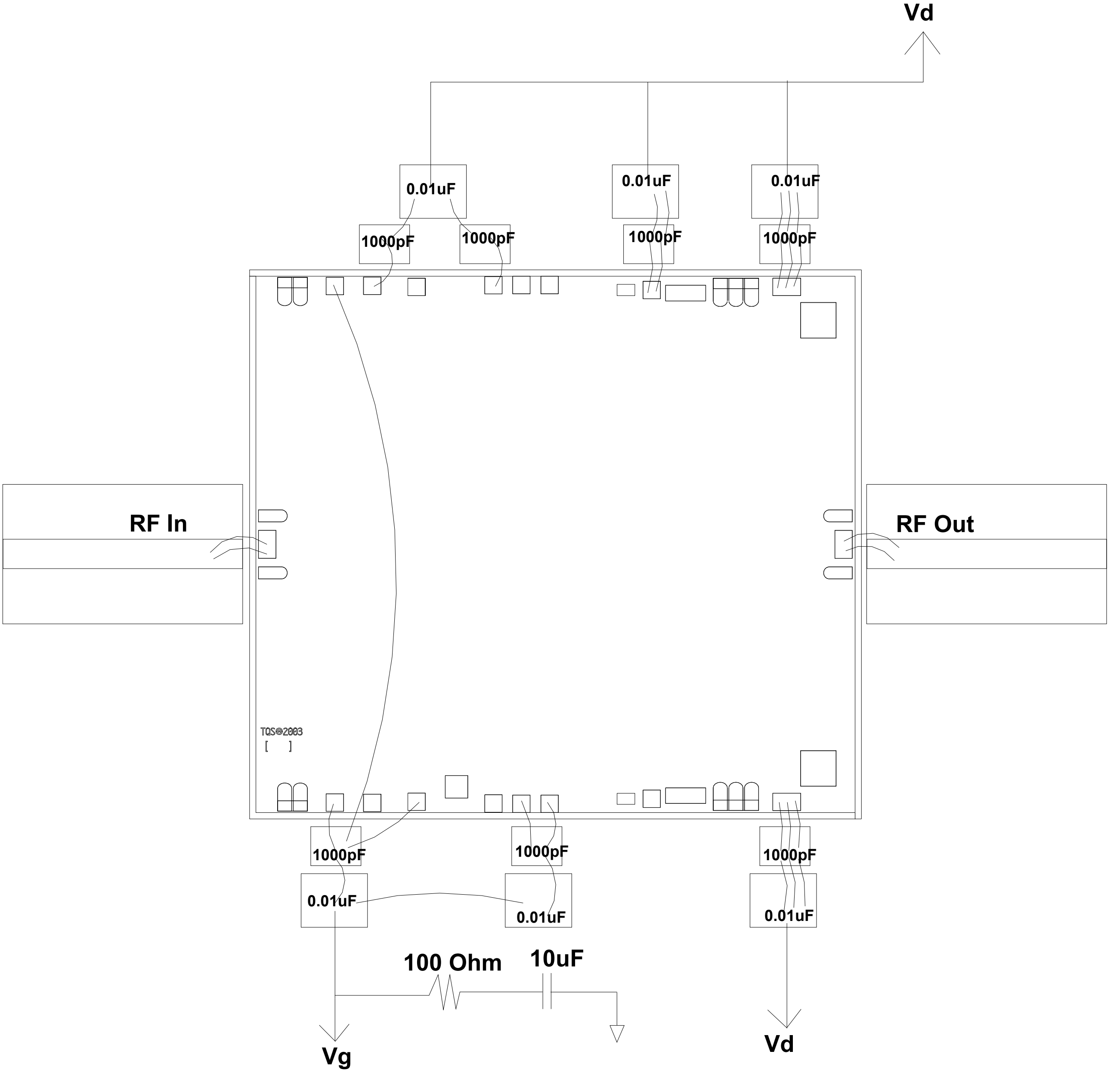


Units: Millimeters (inches)
Thickness: 0.050 (0.002) (reference only)
Chip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance: +/- 0.051 (0.002)
RF Ground is backside of MMIC

Bond pad # 1:	(RF In)	0.125 x 0.200	(0.005 x 0.008)
Bond pad # 2, 18:	(Vg1)	0.125 x 0.125	(0.005 x 0.005)
Bond pad # 3, 17:	(Vd1)	0.125 x 0.125	(0.005 x 0.005)
Bond pad # 4, 16:	(Vg2)	0.125 x 0.125	(0.005 x 0.005)
Bond pad # 5, 15:	(Vd2)	0.125 x 0.125	(0.005 x 0.005)
Bond pad # 6, 14:	(Vg3)	0.125 x 0.125	(0.005 x 0.005)
Bond pad # 7, 13:	(Vg4)	0.125 x 0.125	(0.005 x 0.005)
Bond pad # 8, 12:	(Vd3)	0.125 x 0.125	(0.005 x 0.005)
Bond pad # 9, 11:	(Vd4)	0.125 x 0.125	(0.005 x 0.005)
Bond pad # 10:	(RF Out)	0.125 x 0.200	(0.005 x 0.008)

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Chip Assembly Diagram



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Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300^{0}C (30 seconds max).
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Maximum stage temperature is 200^{0}C.

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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