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Panasonic Global Part Number AN41908A-VB

Vendor Issue Number 1203027

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Product Standards

Part No.	AN41908A
Package Code No.	∗QFN044-P-0606D

Semiconductor Company
Panasonic Corporation

Established by	Applied by	Checked by	Prepared by
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Contents

AN41908A

Lens Driver IC for camcorder and security-camera incorporating Iris control

■ Overview

AN41908A is a lens motor driver IC for camcorder and security-camera featuring the functions of Iris control. Voltage drive system and several torque ripple correction techniques enable super- low noise microstep drive.

■ Features

- Voltage drive system 256-step microstep drivers (2 systems)
- Built-in Iris controller
- Motor control by 4-line serial data communication
- 2 systems of open-drain for driving LED

■ Applications

- Camcorder, Security-camera

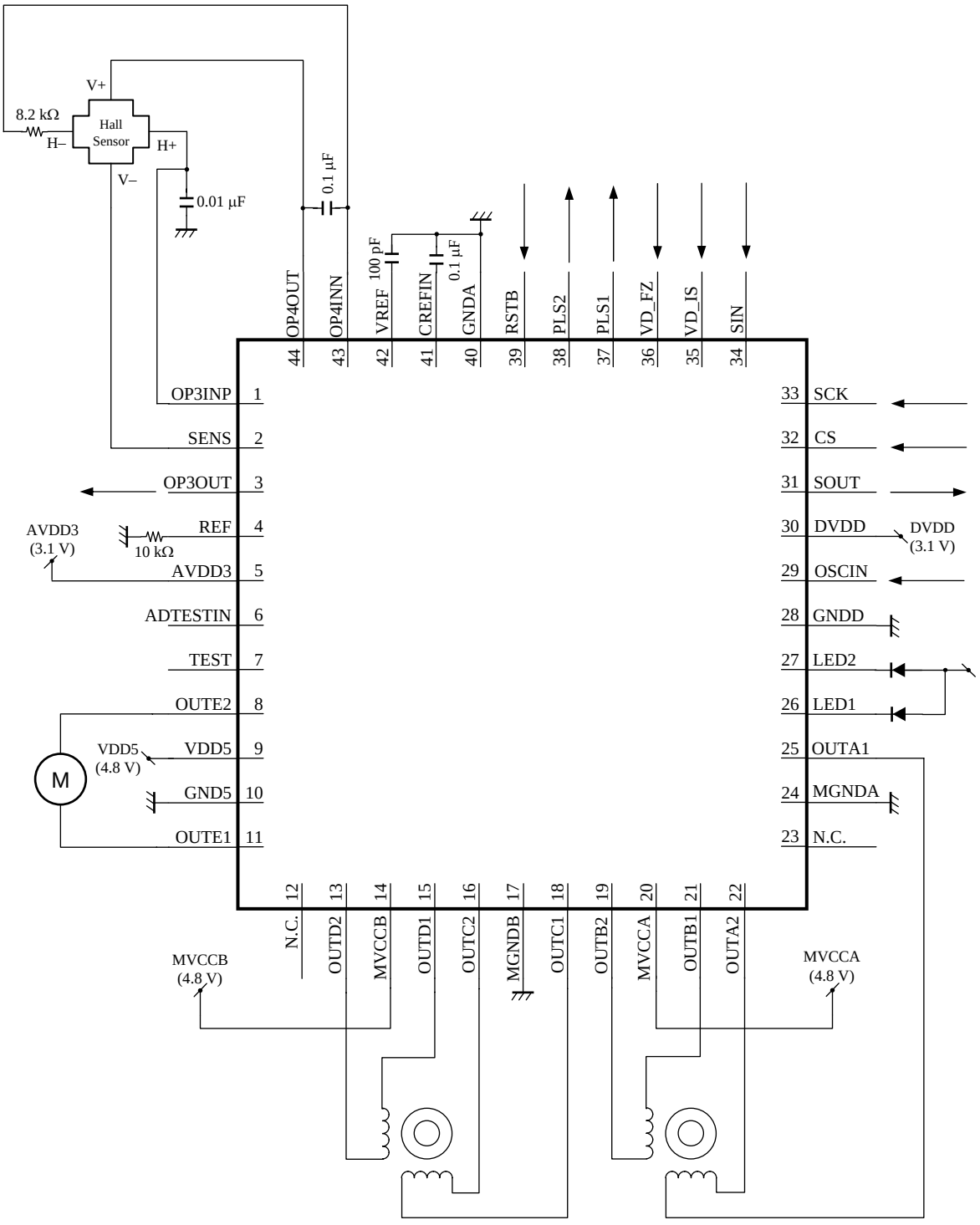
■ Package

- 44 pin Plastic Quad Flat Non-leaded Package (QFN Type)

■ Type

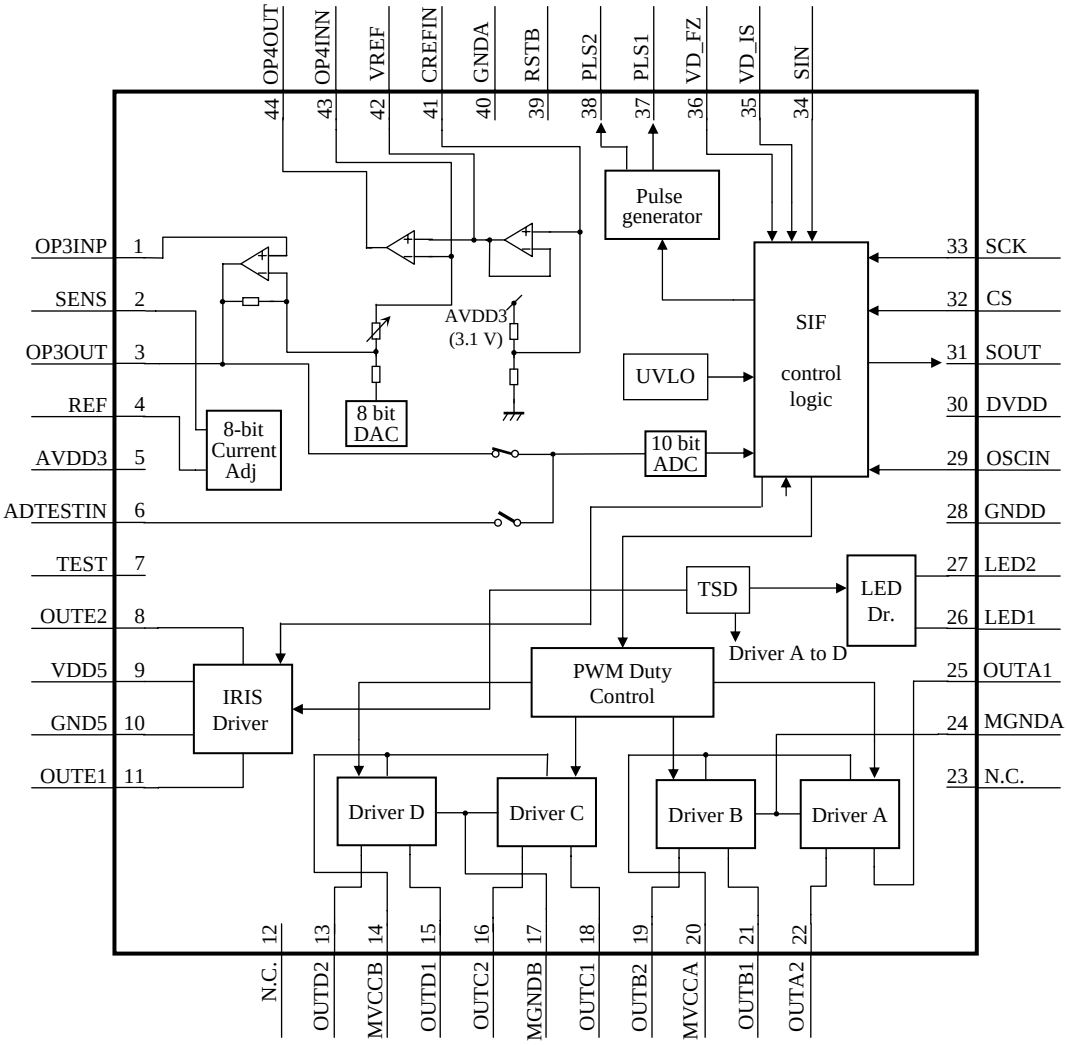
- Bi-COMS IC

■ Application Circuit Example



Note) This application circuit is shown as an example but does not guarantee the design for mass production set.

■ Block Diagram



Note) This block diagram is for explaining functions. The part of the block diagram may be omitted, or it may be simplified.

■ Pin Descriptions

Pin No.	Pin name	Type	Description
1	OP3INP	Input	Hall signal amplifier non-inverting input
2	SENS	Output	Hall current bias output
3	OP3OUT	Output	Hall signal amplifier output
4	REF	—	Resistor connection for Hall current bias setting
5	AVDD3	Power supply	3 V analog power supply
6	ADTESTIN	Input	ADC test input
7	TEST	Input	Test mode input
8	OUTE2	Output	Motor output E2
9	VDD5	Power supply	Power supply for Iris
10	GND5	Ground	GND for Iris
11	OUTE1	Output	Motor output E1
12	N. C.	—	N. C.
13	OUTD2	Output	Motor output D2
14	MVCCB	Power supply	Power supply for motor B
15	OUTD1	Output	Motor output D1
16	OUTC2	Output	Motor output C2
17	MGNDB	Ground	GND for motor B
18	OUTC1	Output	Motor output C1
19	OUTB2	Output	Motor output B2
20	MVCCA	Power supply	Power supply for motor A
21	OUTB1	Output	Motor output B1
22	OUTA2	Output	Motor output A2
23	N. C.	—	N. C.
24	MGNDA	Ground	GND for motor A
25	OUTA1	Output	Motor output A1
26	LED1	Input	Open-drain 1 for driving LED
27	LED2	Input	Open-drain 2 for driving LED
28	GNDD	Ground	Digital GND
29	OSCIN	Input	OSCIN input
30	DVDD	Power supply	3 V digital power supply
31	SOUT	Output	Serial data output
32	CS	Input	Chip select signal input
33	SCK	Input	Serial clock input
34	SIN	Input	Serial data input
35	VD_IS	Input	Iris video sync. signal input

■ Pin Descriptions (continued)

Pin No.	Pin name	Type	Description
36	VD_FZ	Input	Focus zoom sync. signal input
37	PLS1	Output	Pulse 1 output
38	PLS2	Output	Pulse 2 output
39	RSTB	Input	Reset signal input
40	GNDA	Ground	3 V analog GND
41	CREFIN	—	(AVDD3)/2 capacitor connection pin
42	VREF	Output	Reference voltage for Hall sensor
43	OP4INN	Input	Midpoint bias amplifier inverting input
44	OP4OUT	Output	Midpoint bias amplifier output

■ Absolute Maximum Ratings

Note) Absolute maximum ratings are limit values which do not result in damages to this IC, and IC operation is not guaranteed at these limit values.

A No.	Parameter	Symbol	Rating	Unit	Notes
1	Controller supply voltage	AVDD3	–0.3 to + 4.0	V	*1
		DVDD	–0.3 to + 4.0		
2	Supply voltage for motor controller 1	MVCCx	–0.3 to + 6.0	V	*1
3	Supply voltage for motor controller 2	VDD5	–0.3 to + 6.0	V	*1
4	Power dissipation	P_D	141.4	mW	*2
5	Operating ambient temperature	T_{opr}	–20 to + 85	°C	*3
6	Storage temperature	T_{stg}	–55 to + 125	°C	*3
7	Motor driver 1 (focus, zoom) H bridge drive current	$I_{M1(CD)}$	±0.25	A/ch	—
8	Motor driver 2 (iris) H bridge drive current	$I_{M2(CD)}$	±0.15	A/ch	—
9	Instantaneous H bridge drive current	$I_{M(pulse)}$	±0.4	A/ch	—
10	Digital input voltage	V_{in}	–0.3 to (DVDD + 0.3)	V	*4

Notes) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2 : The power dissipation shown is the value at T_a = 85°C for the independent (unmounted) IC package without a heat sink. When using this IC, refer to the P_D-T_a diagram of the package standard and design the heat radiation with sufficient margin so that the allowable value might not be exceeded based on the conditions of power supply voltage, load, and ambient temperature.

*3 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

*4 : (DVDD + 0.3) V must not be exceeded 4.0 V.

■ Operating Supply Voltage Range

Parameter	Symbol	Range			Unit	Notes
		Min	Typ	Max		
Supply voltage range	AVDD3	2.7	3.1	3.6	V	*1
	DVDD	2.7	3.1	3.6		
	MVCCx	3.0	4.8	5.5		
	VDD5	3.0	4.8	5.5		

Note) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

■ Allowable Current and Voltage Range

Notes)
- Allowable current and voltage ranges are limit ranges which do not result in damages to this IC, and IC operation is not guaranteed within these limit ranges.
- Voltage values, unless otherwise specified, are with respect to GND.
  GND is voltage for GNDA, GNDD, GND5, MGNDA, and MGNDB. GND = GNDA = GNDD = GND5 = MGNDA = MGNDB
- VCC3V is voltage for AVDD3 and DVDD. AVDD3 = DVDD
- Do not apply external currents or voltages to any pin not specifically mentioned.
- For the circuit currents, "+" denotes current flowing into the IC, and "–" denotes current flowing out of the IC.

Pin No.	Pin name	Rating	Unit	Notes
1	OP3INP	–0.3 to (AVDD3 + 0.3)	V	*1
6	ADTESTIN	–0.3 to (AVDD3 + 0.3)	V	*1
7	TEST	–0.3 to (DVDD + 0.3)	V	*1
29	OSCIN	–0.3 to (DVDD + 0.3)	V	*1
32	CS	–0.3 to (DVDD + 0.3)	V	*1
33	SCK	–0.3 to (DVDD + 0.3)	V	*1
34	SIN	–0.3 to (DVDD + 0.3)	V	*1
35	VD_IS	–0.3 to (DVDD + 0.3)	V	*1
36	VD_FZ	–0.3 to (DVDD + 0.3)	V	*1
39	RSTB	–0.3 to (DVDD + 0.3)	V	*1
43	OP4INN	–0.3 to (AVDD3 + 0.3)	V	*1

Pin No.	Pin name	Rating	Unit	Notes
8	OUTE2	±0.15	A	—
11	OUTE1	±0.15	A	—
13	OUTD2	±0.25	A	—
15	OUTD1	±0.25	A	—
16	OUTC2	±0.25	A	—
18	OUTC1	±0.25	A	—
19	OUTB2	±0.25	A	—
21	OUTB1	±0.25	A	—
22	OUTA2	±0.25	A	—
25	OUTA1	±0.25	A	—
26	LED1	30	mA	—
27	LED2	30	mA	—

Note) *1 : (AVDD3 + 0.3) V must not be exceeded 4.0 V, and (DVDD + 0.3) V must not be exceeded 4.0 V.

■ Electrical Characteristics at VDD5 = MVCCx = 4.8 V, DVDD = AVDD3 = 3.1 V

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Test circuits	Conditions	Limits			Unit	Notes
					Min	Typ	Max		
Current circuit, Common circuit									
P1	MVCC supply current on Reset	$I_{Omdisable}$	1	No load, no 27 MHz input	—	0	3.0	μA	—
P2	MVCC supply current on Enable	$I_{menable}$	1	Output open	—	0.5	1.5	mA	—
P3	3 V supply current on Reset	$Icc3_{reset}$	1	No 27 MHz input	—	0	10.0	μA	—
P4	3 V supply current on Enable	$Icc3_{enable}$	1	Output open	—	7.0	20.0	mA	—
P5	VDD5 supply current on Reset	$Icc5_{reset}$	1	No 27 MHz input	—	0	3.0	μA	—
P6	VDD5 supply current on Enable	$Icc5_{enable}$	1	Output open	—	0.3	1.0	mA	—
P7	Supply current on Standby	$Icc_{standby}$	1	RSTB = High, output open, 27 MHz input, Total current	—	5.0	10.0	mA	—
P8	Supply current when FZ is Enable and Iris is in power save mode	Icc_{ps}	1	RSTB = High, output open, 27 MHz input, FZ = Enable, Total current	—	6.0	12.0	mA	—
Digital input / output									
D1	High-level input	$V_{in(H)}$	2	RSTB	0.54 × DVDD	—	DVDD + 0.3	V	—
D2	Low-level input	$V_{in(L)}$	2	RSTB	–0.3	—	0.2 × DVDD	V	—
D3	SOUT High-level output	$V_{out(H):SDATA}$	2	[SOUT] 1 mA Source	DVDD – 0.5	—	—	V	—
D4	SOUT Low-level output	$V_{out(L):SDATA}$	2	[SOUT] 1 mA Sink	—	—	0.5	V	—
D5	PLS1 to 2 High-level output	$V_{out(H):MUX}$	2	—	0.9 × DVDD	—	—	V	—
D6	PLS1 to 2 Low-level output	$V_{out(L):MUX}$	2	—	—	—	0.1 × DVDD	V	—
D7	Input pull-down resistance	$R_{pullret}$	3	RSTB	50	100	200	kΩ	—
Motor driver 1 (focus, zoom)									
H1	H bridge ON resistance	R_{onFZ}	4	IM = 100 mA	—	—	2.5	Ω	—
H2	H bridge leak current	I_{leakFZ}	6	—	—	—	0.8	μA	—
Motor driver 2 (iris)									
H3	H bridge ON resistance	R_{onIR}	5	IM = 50 mA	—	—	5	Ω	—
H4	H bridge leak current	I_{leakIR}	6	—	—	—	0.8	μA	—
LED driver									
L1	Output ON resistance	R_{onLED}	7	I = 20 mA, 5 V cell	—	—	8	Ω	—
L2	Output leak current	$I_{leakLED}$	6	—	—	—	0.8	μA	—

■ Electrical Characteristics (continued) at VDD5 = MVCCx = 4.8 V, DVDD = AVDD3 = 3.1 V

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Test circuits	Conditions	Limits			Unit	Notes
					Min	Typ	Max		
OPAMP3 (HALL Sensor Amp. for output amplifier)									
O1	Input voltage range	V_{IN}	8	—	½ AVDD3 – 0.5	½ AVDD3	½ AVDD3 + 0.5	V	—
O2	Input offset voltage	V_{OF}	8	—	–15	—	15	mV	—
O3	Output voltage (Low)	V_{OL}	9	ILOAD = –100 µA	—	0.1	0.2	V	—
O4	Output voltage (High)	V_{OH}	9	ILOAD = 100 µA	AVDD3 – 0.2	AVDD3 – 0.1	—	V	—
O5	Gain	V_{OG}	8	Gain setting value : 0h	19.7	21.9	24.1	V/V	—
OPAMP4 (HALL Sensor Amp. for eliminating common-mode voltage)									
O6	Input voltage range	V_{IN}	10	—	½ AVDD3 – 0.1	—	½ AVDD3 + 0.1	V	—
O7	Input offset voltage	V_{OF}	10	—	–10	—	10	mV	—
O8	Output voltage (Low)	V_{OL}	10	ILOAD = –10 µA	—	0.1	0.2	V	—
O9	Output voltage (High)	V_{OH}	10	ILOAD = 3 mA	AVDD3 – 0.5	AVDD3 – 0.2	—	V	—
Reference voltage output block									
O10	Output voltage 1	VREF	10	ILOAD = 0 A, CVREF = 100 pF	½ AVDD3 – 0.1	½ AVDD3	½ AVDD3 + 0.1	V	—
O11	Output voltage 2	VREFL	10	ILOAD = ±100 µA, CVREF = 100 pF	VREF – 0.1	VREF	VREF + 0.1	V	—
Hall bias controller (SENS pin output)									
O12	Min. output current	IBL	10	REF = 10 kΩ, SENS = 0.7 V Setting value : 00 h	—	0	0.1	mA	—
O13	Output current accuracy 1	IB40H	10	REF = 10 kΩ, SENS = 0.7 V Setting value : 40 h	0.9	1.02	1.14	mA	—
O14	Output current accuracy 2	IBBFH	10	REF = 10 kΩ, SENS = 0.7 V Setting value : BE h	2.66	3.02	3.38	mA	—

■ Electrical Characteristics (Reference values for design) at VDD5 = MVCCx = 4.8 V, DVDD = AVDD3 = 3.1 V

Notes) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Test circuits	Conditions	Reference values			Unit	Notes
					Min	Typ	Max		
Serial port input									
S1	Serial clock	Sclock	—	—	1	—	5	MHz	—
S2	SCK low time	T1	—	—	100	—	—	ns	—
S3	SCK high time	T2	—	—	100	—	—	ns	—
S4	CS setup time	T3	—	—	60	—	—	ns	—
S5	CS hold time	T4	—	—	60	—	—	ns	—
S6	CS disable high time	T5	—	—	100	—	—	ns	—
S7	SIN setup time	T6	—	—	50	—	—	ns	—
S8	SIN hold time	T7	—	—	50	—	—	ns	—
S9	SOUT delay time	T8	—	—	—	—	60	ns	—
S10	SOUT hold time	T9	—	—	60	—	—	ns	—
S11	SOUT Enable-Hi-Z time	T10	—	—	—	—	60	ns	—
S12	SOUT Hi-Z-Enable time	T11	—	—	—	—	60	ns	—
S13	SOUT C load	T_{SC}	—	—	—	—	40	pF	—
Digital input / output									
D8	High-level input threshold voltage	$V_{in(H)}$	—	SCK, SIN, CS, OSCIN, VD_IS, VD_FZ, TEST	—	1.36	—	V	—
D9	Low-level input threshold voltage	$V_{in(L)}$	—	SCK, SIN, CS, OSCIN, VD_IS, VD_FZ, TEST	—	1.02	—	V	—
D10	RSTB signal pulse width	Trst	—	—	100	—	—	µs	—
D11	Input hysteresis width	V_{hysin}	—	SCK, SIN, CS, OSCIN, VD_IS, VD_FZ, TEST	—	0.34	—	V	—
D12	Video sync. signal width	VD_W	—	—	80	—	—	µs	—
D13	CS signal wait time 1	$T_{(VD-CS)}$	—	—	400	—	—	ns	—
D14	CS signal wait time 2	$T_{(CS-DT1)}$	—	—	5	—	—	µs	—

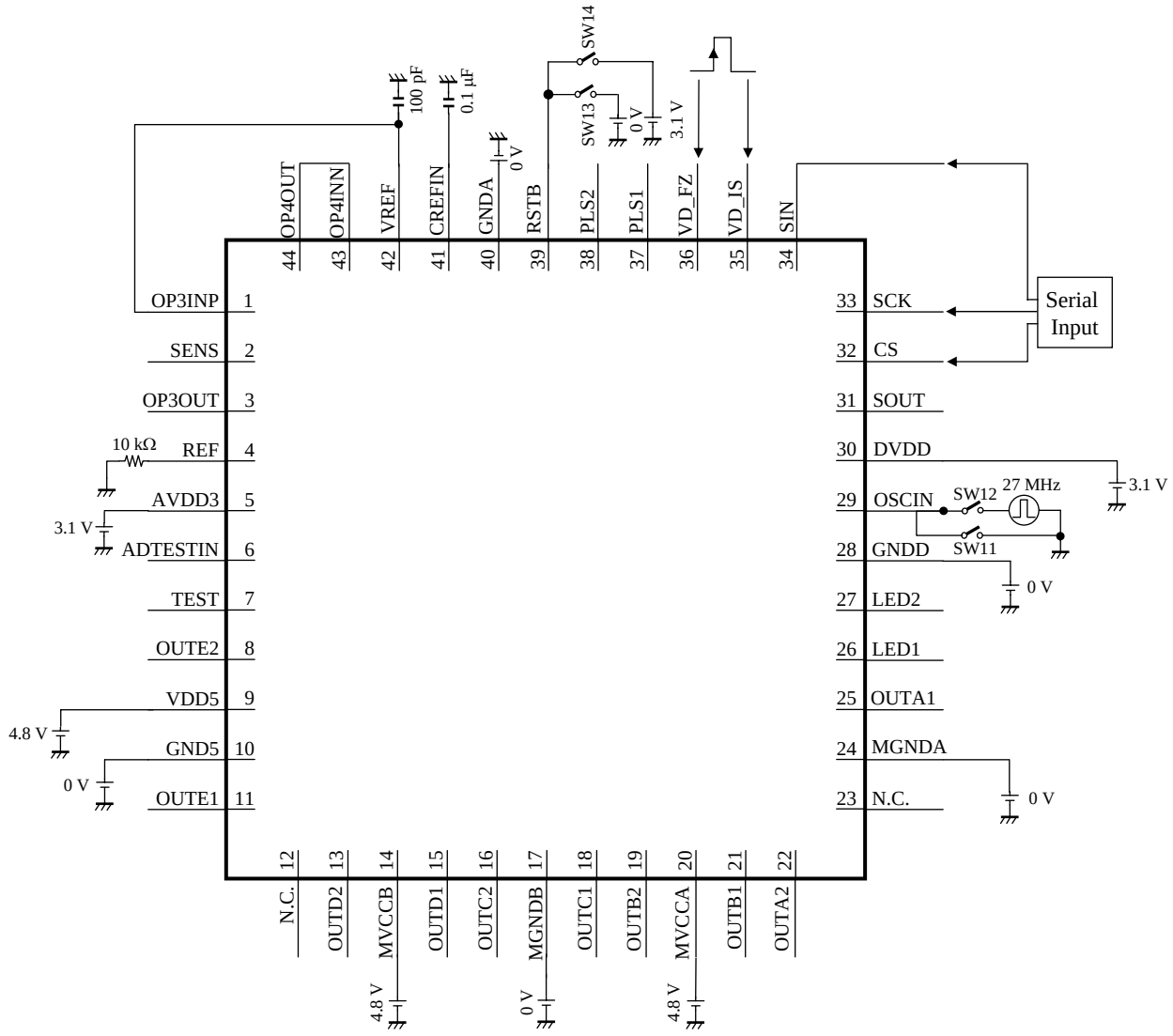
■ Electrical Characteristics (Reference values for design) (continued) at
VDD5 = MVCCx = 4.8 V, DVDD = AVDD3 = 3.1 V

Notes) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Test circuits	Conditions	Reference values			Unit	Notes
					Min	Typ	Max		
Pulse generator									
PL1	Pulse start resolution for pulse 1	PL1wait	—	OSCIN = 27 MHz	—	20.1	—	µs	—
PL2	Pulse resolution for pulse 1	PL1width	—	OSCIN = 27 MHz	—	1.2	—	µs	—
PL3	Pulse start resolution for pulse 2	PL2wait	—	OSCIN = 27 MHz	—	20.1	—	µs	—
Iris control									
IR1	AD sampling frequency	$IRIS_{Sample}$	—	OSCIN = 27 MHz	—	500	—	kHz	—
Thermal shutdown									
T1	Thermal shutdown operation temperature	Ttsd	—	—	—	150	—	°C	—
T2	Thermal shutdown hysteresis width	ΔTtsd	—	—	—	40	—	°C	—
Supply voltage monitor circuit									
R1	3.3 V Reset operation	Vrston	—	—	—	2.27	—	V	—
R2	3.3 V Reset hysteresis width	Vrsthys	—	—	—	0.2	—	V	—
R3	MVCCx Reset operation	$V_{rstFZon}$	—	—	—	2.2	—	V	—
R4	MVCCx Reset hysteresis width	$V_{rstFZhys}$	—	—	—	0.2	—	V	—
R5	VDD5 Reset operation	$V_{rstISon}$	—	—	—	2.2	—	V	—
R6	VDD5 Reset hysteresis width	$V_{rstIShys}$	—	—	—	0.2	—	V	—
8 bit DAC for Hall Offset adjustment									
DA1	Adjustment range (High)	DAOTHof	—	—	—	AVDD3	—	V	—
DA2	Adjustment range (Low)	DAOTLof	—	—	—	0	—	V	—
10 bit ADC									
AD1	Input Range (High)	$V_{in(H)}$	—	—	—	—	AVDD3 – 0.2	V	—
AD2	Input Range (Low)	$V_{in(L)}$	—	—	0.2	—	—	V	—
AD3	DNLE (Differential linearity error)	DNL10A	—	—	—	1.0	—	LSB	—
AD4	INLE (Integral linearity error)	INL10A	—	—	—	2.0	—	LSB	—

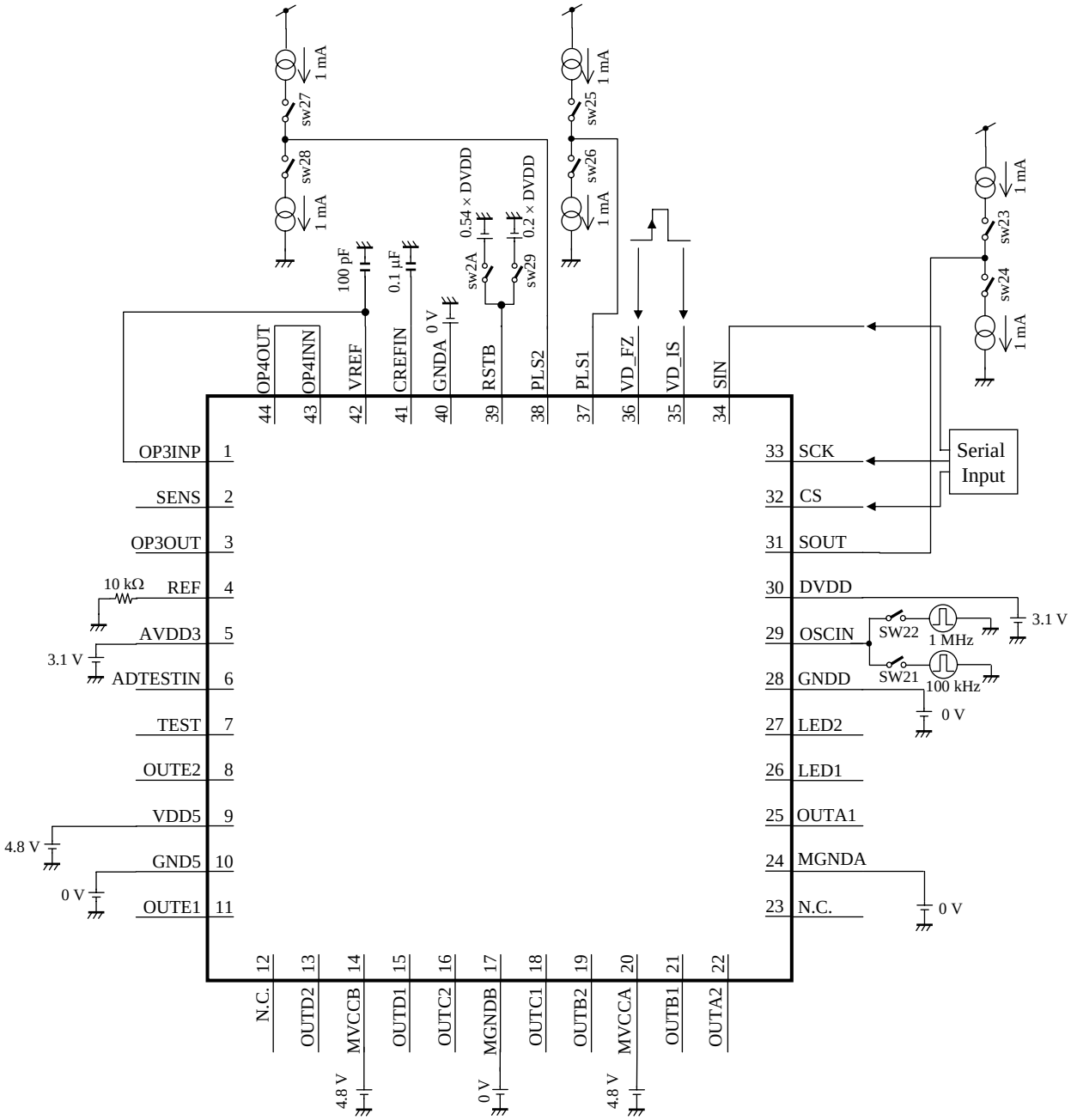
■ Test Circuit Diagram

1. Test Circuit 1 (Circuit current, Common circuit)



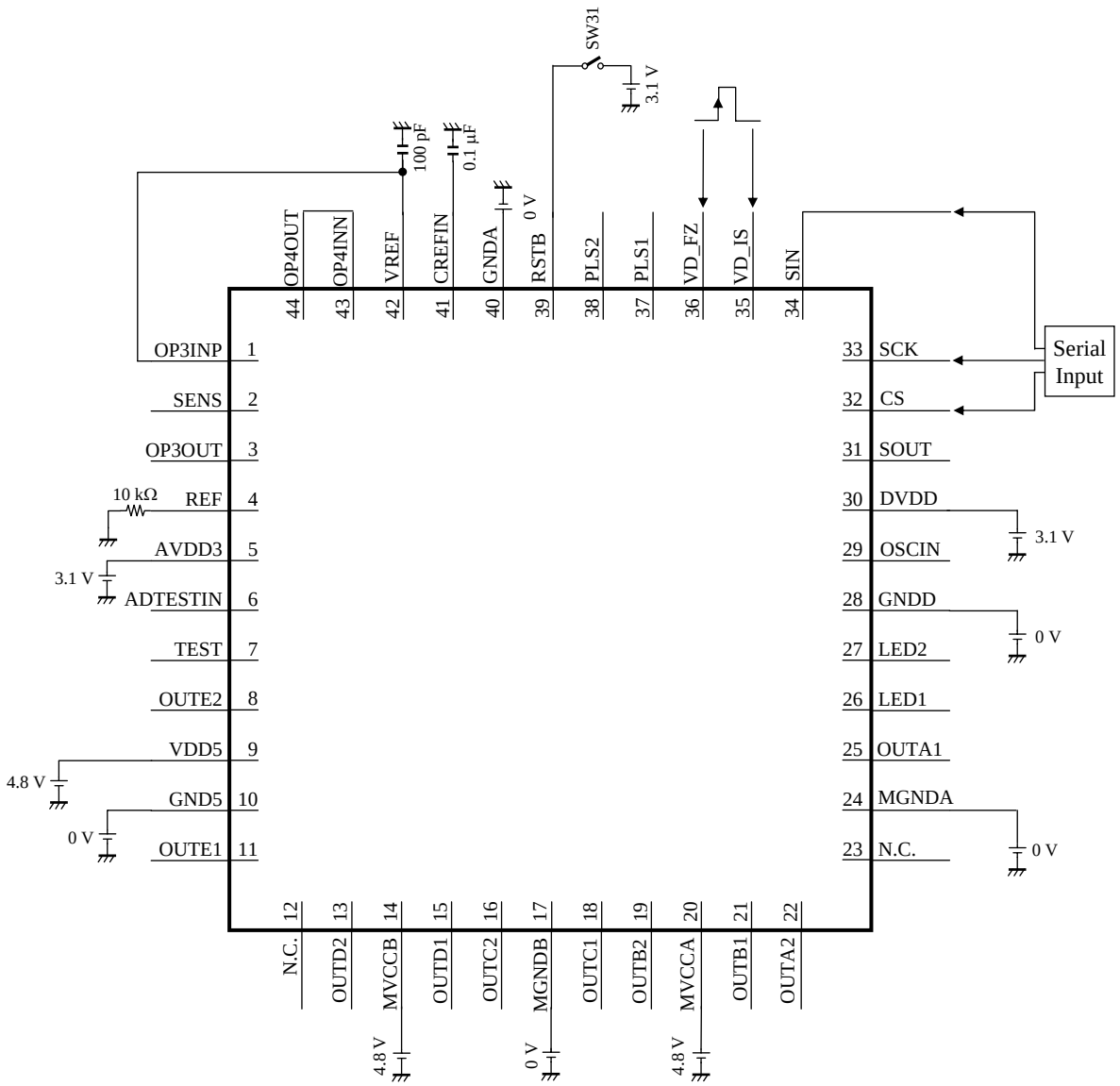
■ Test Circuit Diagram (continued)

2. Test Circuit 2 (Digital input / output)



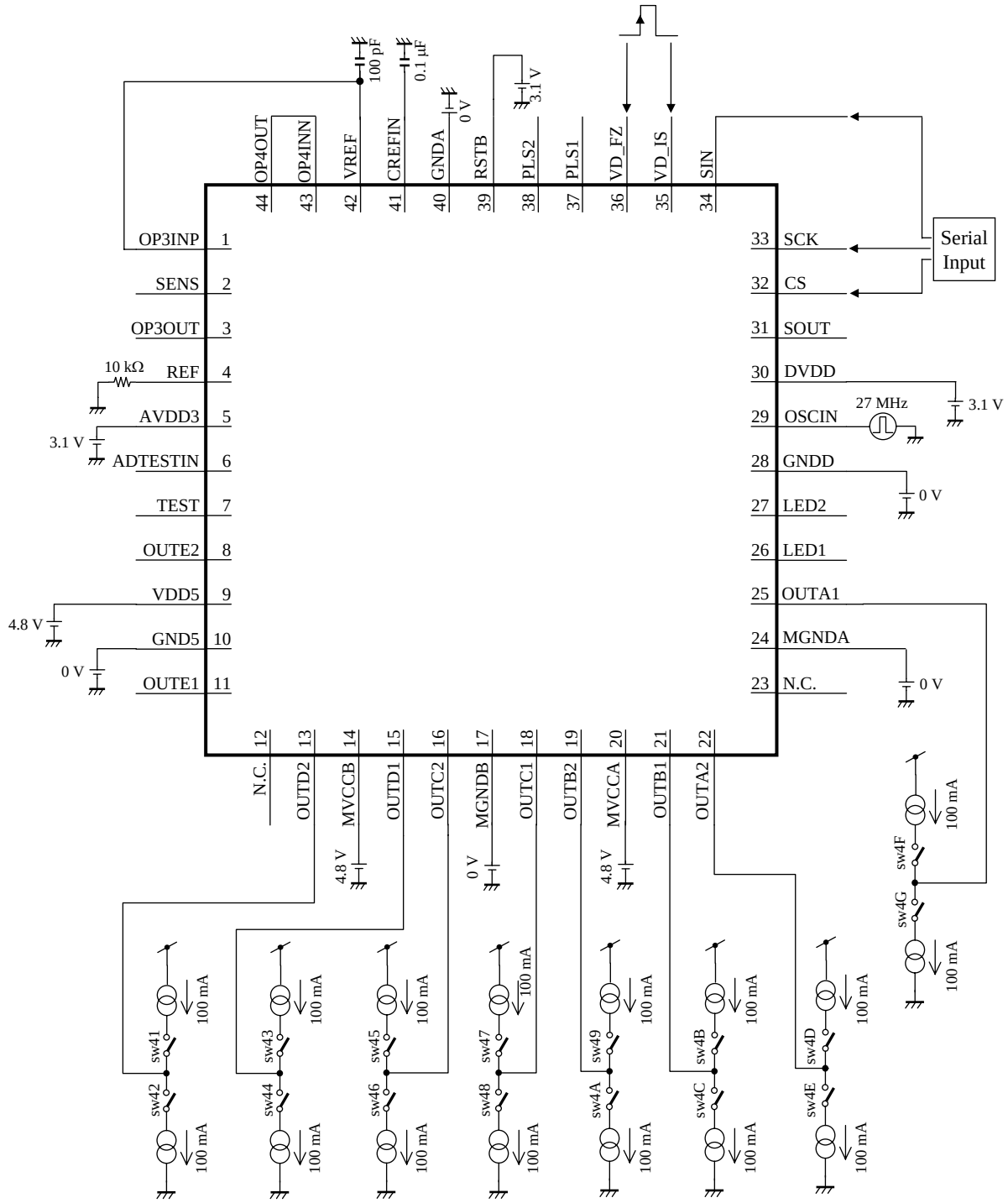
■ Test Circuit Diagram (continued)

3. Test Circuit 3 (Digital input / output : Input pull-down resistance)



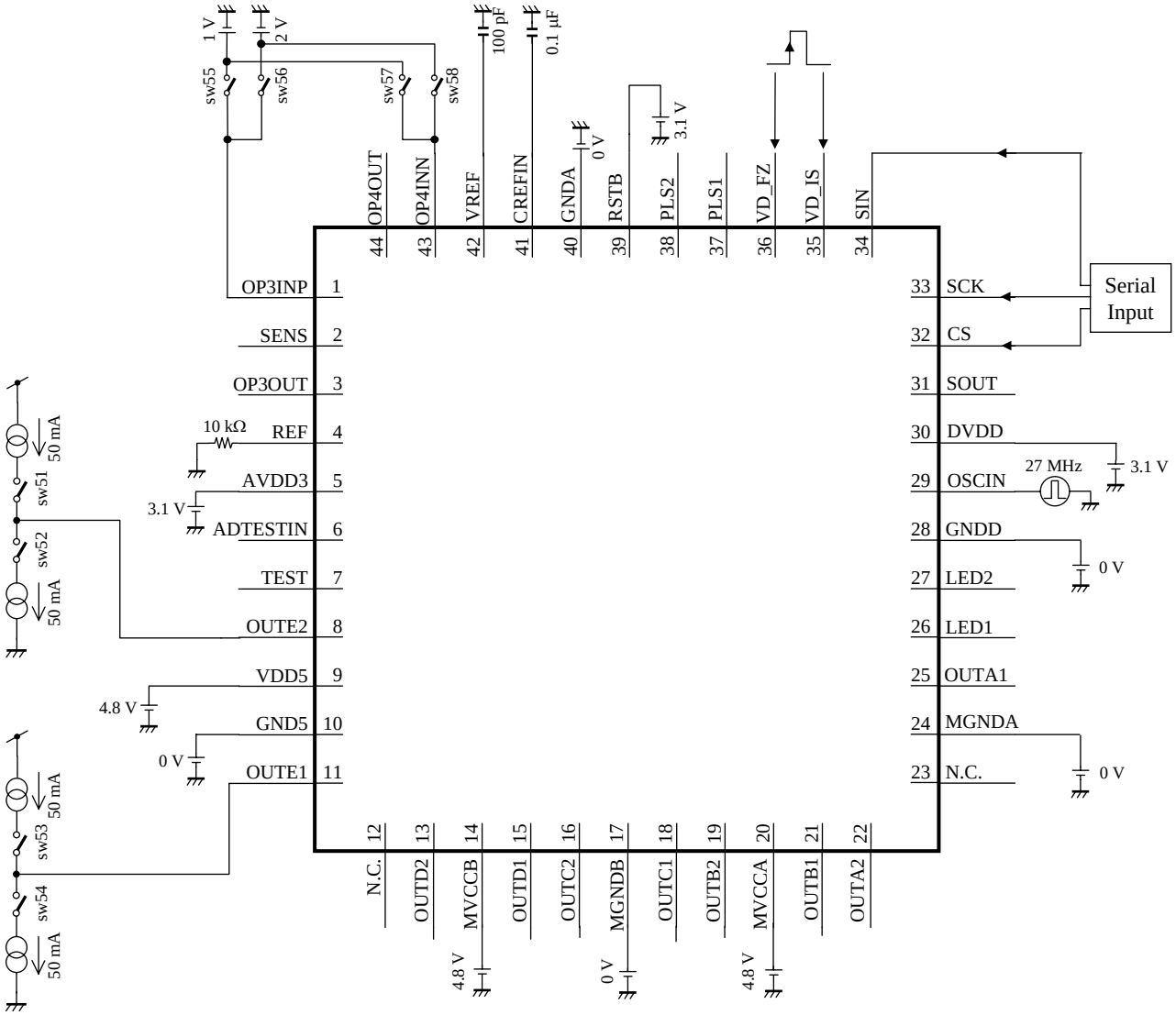
■ Test Circuit Diagram (continued)

4. Test Circuit 4 (Motor driver : focus, zoom H bridge ON resistance)



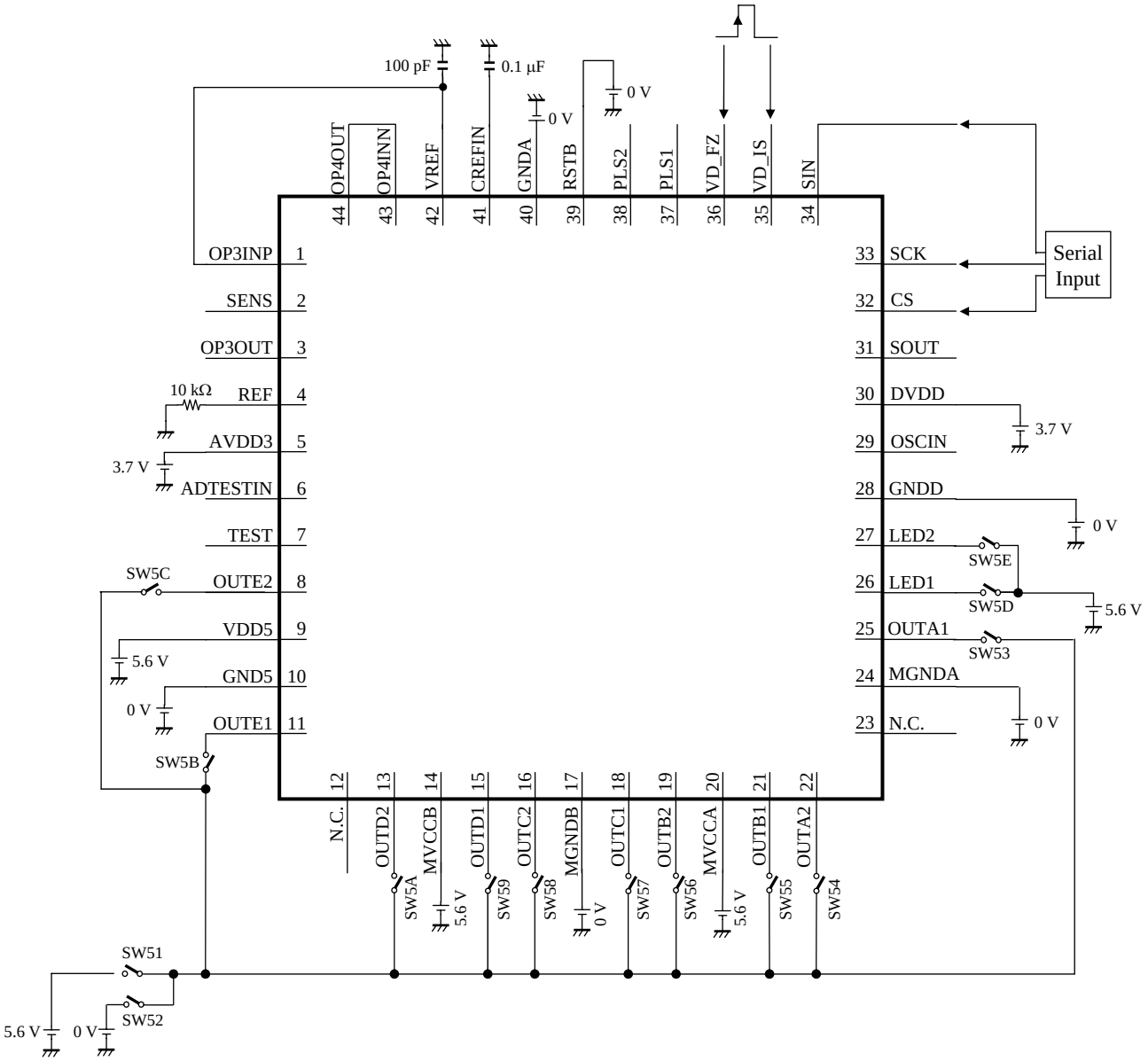
■ Test Circuit Diagram (continued)

5. Test Circuit 5 (Motor driver : Iris H bridge ON resistance)



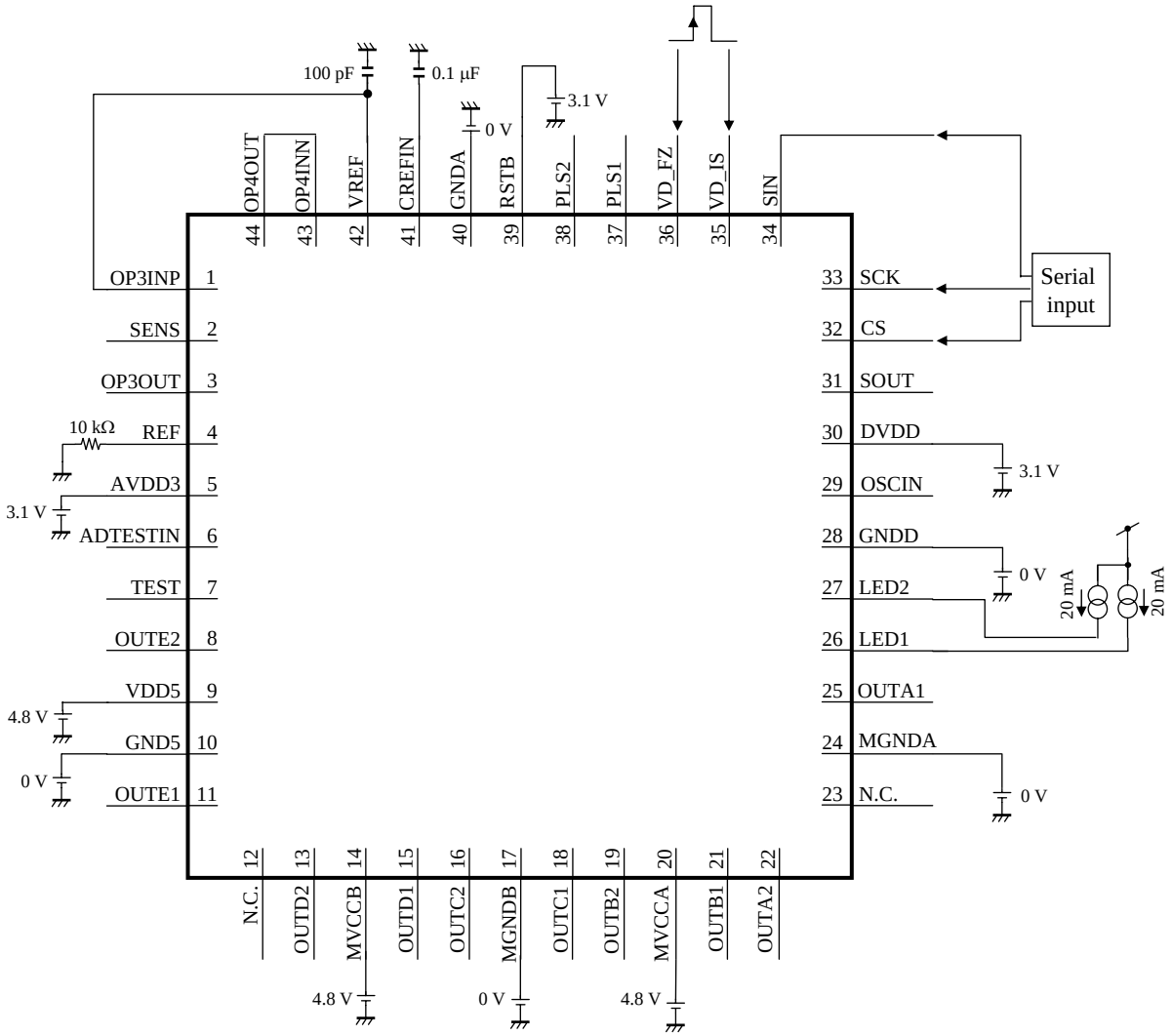
■ Test Circuit Diagram (continued)

6. Test Circuit 6 (Motor driver : H bridge leak current, LED driver : Output leak current)



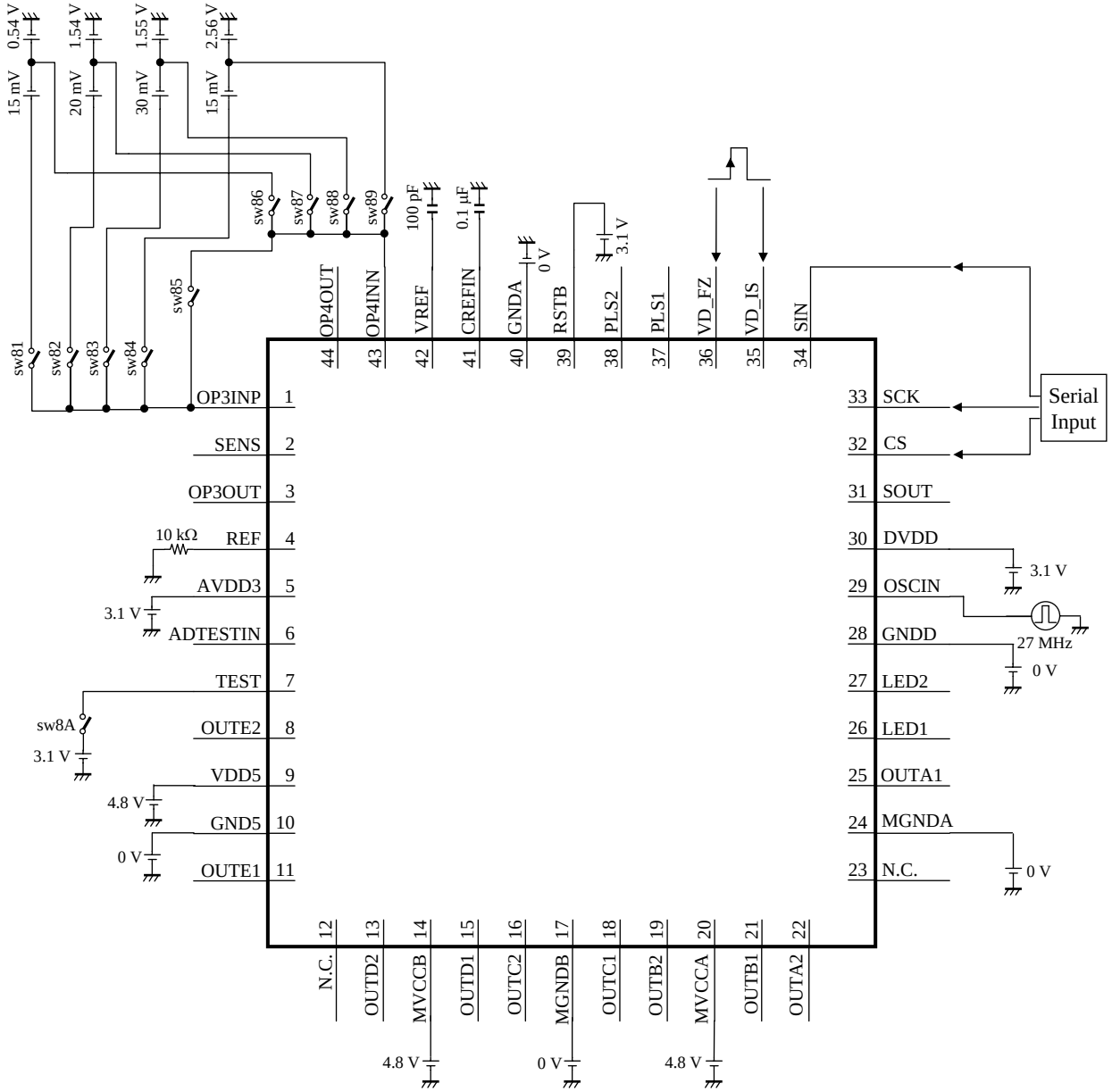
■ Test Circuit Diagram (continued)

7. Test Circuit 7 (LED driver : Output ON resistance)



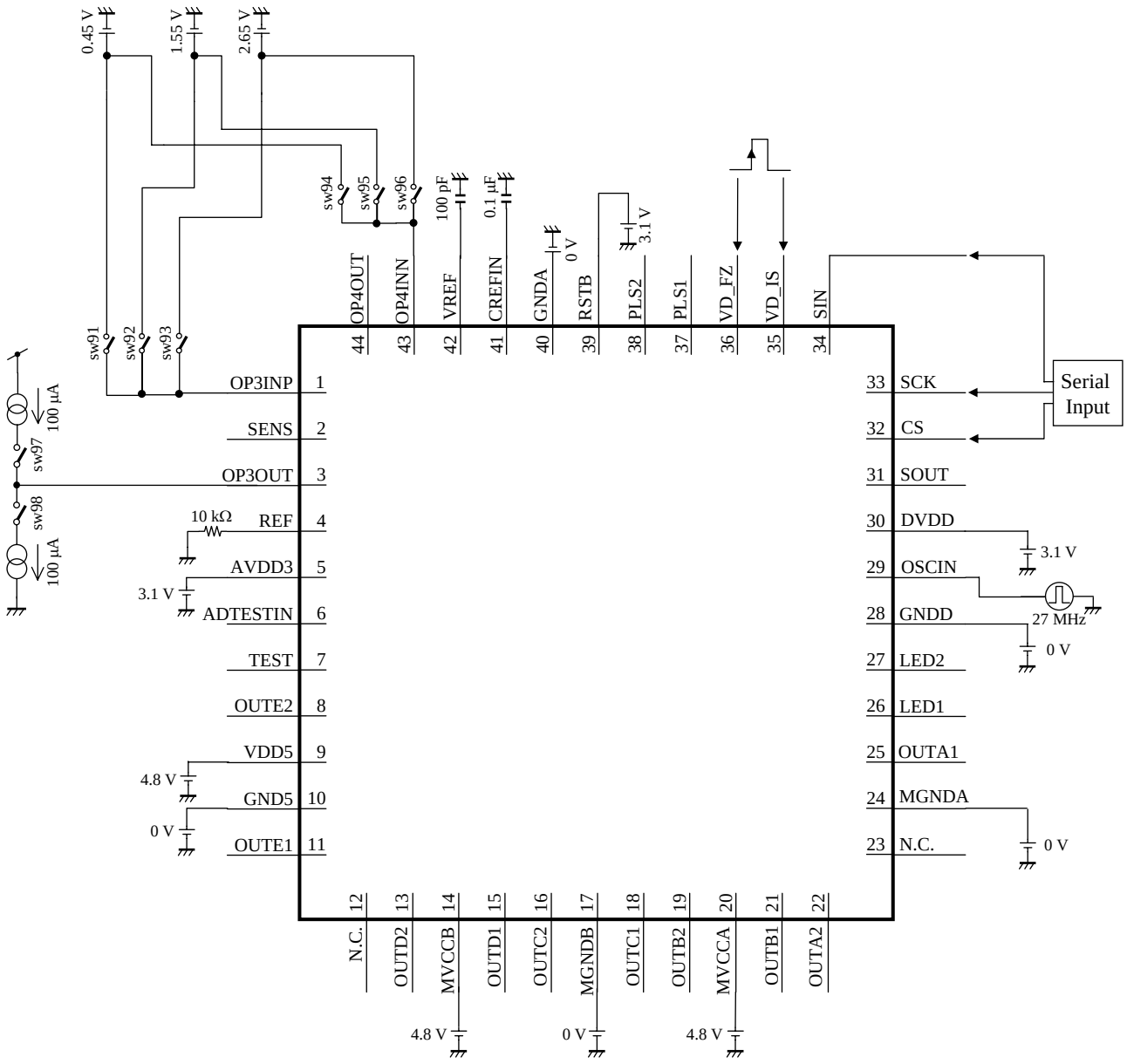
■ Test Circuit Diagram (continued)

8. Test Circuit 8 (OPAMP3)



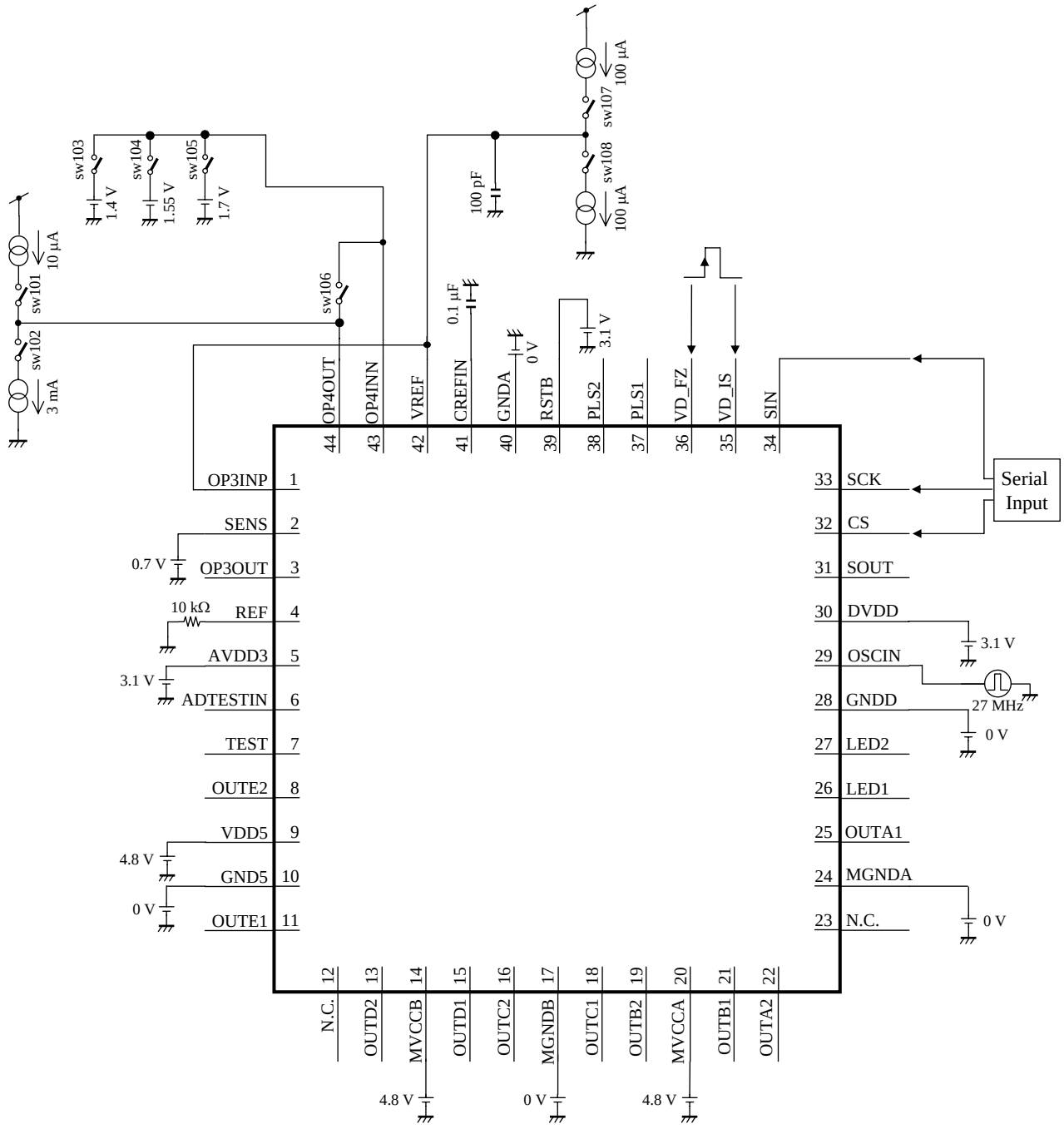
■ Test Circuit Diagram (continued)

9. Test Circuit 9 (OPAMP3)



■ Test Circuit Diagram (continued)

10. Test Circuit 10 (OPAMP4, Reference voltage output block, Hall bias controller)



■ Electrical Characteristics Test Procedures

C No.	Parameter	Input		Output		Pin settings			
		Pin No.	Conditions	Pin No.	Conditions	SW11	SW12	SW13	SW14
Circuit current, Common circuit									
P1	MVCC supply current on Reset	9 14 20	4.8 V	14 20	Measure the current	ON	OFF	ON	OFF
		5 30	3.1 V						
		7	0 V						
		39	0 V						
P2	MVCC supply current on Enable	9 14 20	4.8 V	14 20	Measure the current	OFF	ON	OFF	ON
		5 30	3.1 V						
		7	0 V						
		39	3.1 V						
		34	*11						
P3	3 V supply current on Reset	9 14 20	4.8 V	5 30	Measure the current	ON	OFF	ON	OFF
		5 30	3.1 V						
		7	0 V						
		39	0 V						
P4	3 V supply current on Enable	9 14 20	4.8 V	5 30	Measure the current	OFF	ON	OFF	ON
		5 30	3.1 V						
		7	0 V						
		39	3.1 V						
		34	*12						

*11 : Serial setting ENDISAB = 1, LEDA = 1, ENDISCD = 1, LEDB = 1
*12 : Serial setting ENDISAB = 1, LEDA = 1, ENDISCD = 1, LEDB = 1, PDWNB=1, HALL_OFFSET_DAC[7:0] = 0Fh

Note） Serial settings are reflected on the rising edge of VD_IS or VD_FZ.

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings			
		Pin No.	Conditions	Pin No.	Conditions	SW11	SW12	SW13	SW14
Circuit current, Common circuit (continued)									
P5	VDD5 supply current on Reset	9 14 20	4.8 V	9	Measure the current	ON	OFF	ON	OFF
		5 30	3.1 V						
		7	0 V						
		39	0 V						
P6	VDD5 supply current on Enable	9 14 20	4.8 V	9	Measure the current	OFF	ON	OFF	ON
		5 30	3.1 V						
		7	0 V						
		39	3.1 V						
		34	*12						
P7	Supply current on Standby	9 14 20	4.8 V	5 9 14 20 30	Measure the current	OFF	ON	OFF	ON
		5 30	3.1 V						
		7	0 V						
		39	3.1 V						
		34	*13						
P8	Supply current when FZ is Enable and Iris is in Power Save mode	9 14 20	4.8 V	5 9 14 20 30	Measure the current	OFF	ON	OFF	ON
		5 30	3.1 V						
		7	0 V						
		39	3.1 V						
		34	*14						

*12 : Serial setting ENDISAB = 1, LEDA = 1, ENDISCD = 1, LEDB = 1, PDWNB = 1, HALL_OFFSET_DAC[7:0] = 0Fh
*13 : Serial setting ENDISAB = 0, LEDA = 0, ENDISCD = 0, LEDB = 0, PDWNB = 0
*14 : Serial setting ENDISAB = 1, ENDISCD = 1

Note) Serial settings are reflected on the rising edge of VD_IS or VD_FZ.

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings							
		Pin No.	Conditions	Pin No.	Conditions	SW21	SW22	SW23	SW24	SW25 SW27	SW26 SW28	SW29	SW2A
Digital input / output													
D1	High-level input	5 30	3.1 V	41	Measure the voltage (Confirm 1/2 × AVDD3)	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON
		9 14 20	4.8 V										
		39	0.54 × DVDD										
		29	100 kHz, 0 V / 3.1 V										
		34	*21										
D2	Low-level input	5 30	3.1 V	41	Measure the voltage (Confirm AVDD3)	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF
		9 14 20	4.8 V										
		39	0.2 × DVDD										
		29	100 kHz, 0 V / 3.1 V										
D3	SOUT High-level output	5 30	3.1 V	31	Measure the voltage	ON	OFF	OFF	ON	OFF	OFF	OFF	ON
		9 14 20	4.8 V										
		39	3.1 V										
		31	–1 mA										
		29	100 kHz, 0 V / 3.1 V										
		34	*22										
D4	SOUT Low-level output	5 30	3.1 V	31	Measure the voltage	ON	OFF	ON	OFF	OFF	OFF	OFF	ON
		9 14 20	4.8 V										
		39	3.1 V										
		31	1 mA										
		29	100 kHz, 0 V / 3.1 V										
		34	*23										

*21 : Serial setting PDWNB = 1
*22 : Serial setting PPWA[7:0] = FFh, PPWB[7:0] = FFh
*23 : Serial setting PPWA[7:0] = 00h, PPWB[7:0] = 00h

Note） Serial settings are reflected on the rising edge of VD_IS or VD_FZ.

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings					
		Pin No.	Conditions	Pin No.	Conditions	SW21	SW22	SW23	SW24	SW25 SW27	SW26 SW28
Digital input / output (continued)											
D5	PLS1 to 2 High-level output	5 30	3.1 V	38 39	Measure the voltage	OFF	ON	OFF	OFF	OFF	ON
		9 14 20	4.8 V								
		39	3.1 V								
		38	–1 mA								
		39	–1 mA								
		29	1 MHz, 0 V / 3.1 V								
		34	*24								
D6	PLS1 to 2 Low-level output	5 30	3.1 V	38 39	Measure the voltage	OFF	ON	OFF	OFF	ON	OFF
		9 14 20	4.8 V								
		39	3.1 V								
		38	1 mA								
		39	1 mA								
		29	1 MHz, 0 V / 3.1 V								
		34	*25								

*24 : Serial setting TESTEN1 = TESTEN2 = 1, FZTEST[4:0] = 03h, ENDISAB = ENDISCD = 1
*25 : Serial setting TESTEN1 = TESTEN2 = 1, FZTEST[4:0] = 03h, ENDISAB = ENDISCD = 0

Note） Serial settings are reflected on the rising edge of VD_IS or VD_FZ.

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings
		Pin No.	Conditions	Pin No.	Conditions	SW31
Digital input / output (continued)						
D7	Input pull-down resistance	5	3.1 V	39	Measure the current	ON (Pin 39 measurement only)
		9	4.8 V			
		14	4.8 V			
		20	4.8 V			
		30	3.1 V			

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings							
		Pin No.	Conditions	Pin No.	Conditions	SW41 SW44	SW42 SW43	SW45 SW48	SW46 SW47	SW49 SW4C	SW4A SW4B	SW4D SW4G	SW4E SW4F
Motor driver													
H1	H bridge ON resistance OUTB (OUTB1_UP + OUTB2_DOWN)	5 30	3.1 V	19 20 21 24	Measure the voltage Ron = {(Pin 20 – Pin 21) + (Pin 19 – Pin 24)} / 100 mA	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
		9 14 20	4.8 V										
		39	3.1 V										
		29	27 MHz, 0 V / 3.1 V										
		34	*31										
		19	100 mA										
		21	–100 mA										
H1	H bridge ON resistance OUTD (OUTD1_UP + OUTD2_DOWN)	5 30	3.1 V	13 14 15 17	Measure the voltage Ron = {(Pin 14 – Pin 15) + (Pin 13 – Pin 17)} / 100 mA	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
		9 14 20	4.8 V										
		39	3.1 V										
		29	27 MHz, 0 V / 3.1 V										
		13	100 mA										
		15	–100 mA										

*31 : Serial setting

PDWNB = 1
TESTEN1 = TESTEN2 = 1,
DT1[7:0] = DT2A[7:0] = DT2B[7:0] = 01h,
ENDISAB = ENDISCD = 1,
SKIPDT1 = SKIPDT2 = 1,
PWMMODE = [11111], PWMRES = 2h,
PPWA[7:0] = PPWB[7:0] = PPWC[7:0] = PPWD[7:0] = FFh,
INTCTAB[15:0] = INTCTCD[15:0] = 0001h

Note） Serial settings are reflected on the rising edge of VD_IS or VD_FZ.

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings							
		Pin No.	Conditions	Pin No.	Conditions	SW41 SW44	SW42 SW43	SW45 SW48	SW46 SW47	SW49 SW4C	SW4A SW4B	SW4D SW4G	SW4E SW4F
Motor driver													
H1	H bridge ON resistance OUTA (OUTA1_UP + OUTA2_DOWN)	5 30	3.1 V	20 22 24 25	Measure the voltage Ron = {(Pin 20 – Pin 25) + (Pin 22 – Pin 24)} / 100 mA	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
		9 14 20	4.8 V										
		39	3.1 V										
		29	27 MHz, 0 V / 3.1 V										
		34	*32										
		22	100 mA										
		25	–100 mA										
H1	H bridge ON resistance OUTC (OUTC1_UP + OUTC2_DOWN)	5 30	3.1 V	14 16 17 18	Measure the voltage Ron = {(Pin 14 – Pin 18) + (Pin 16 – Pin 17)} / 100 mA	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
		9 14 20	4.8 V										
		39	3.1 V										
		29	27 MHz, 0 V / 3.1 V										
		16	100 mA										
		18	–100 mA										

*32 : Serial setting PSUMAB[7:0] = PSUMCD[7:0] = 08h

Note） Serial settings are reflected on the rising edge of VD_IS or VD_FZ.

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings							
		Pin No.	Conditions	Pin No.	Conditions	SW41 SW44	SW42 SW43	SW45 SW48	SW46 SW47	SW49 SW4C	SW4A SW4B	SW4D SW4G	SW4E SW4F
Motor driver													
H1	H bridge ON resistance OUTB (OUTB2_UP + OUTB1_DOWN)	5 30	3.1 V	19 20 21 24	Measure the voltage Ron = {(Pin 20 – Pin 19) + (Pin 21 – Pin 24)} / 100 mA	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
		9 14 20	4.8 V										
		39	3.1 V										
		29	27 MHz, 0 V / 3.1 V										
		36	*33										
		19	–100 mA										
		21	100 mA										
H1	H bridge ON resistance OUTD (OUTD2_UP + OUTD1_DOWN)	5 30	3.1 V	13 14 15 17	Measure the voltage Ron = {(Pin 14 – Pin 13) + (Pin 15 – Pin 17)} / 100 mA	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
		9 14 20	4.8 V										
		39	3.1 V										
		29	27 MHz, 0 V / 3.1 V										
		13	–100 mA										
		15	100 mA										

*33 : Impulse input to VD_FZ

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings							
		Pin No.	Conditions	Pin No.	Conditions	SW41 SW44	SW42 SW43	SW45 SW48	SW46 SW47	SW49 SW4C	SW4A SW4B	SW4D SW4G	SW4E SW4F
Motor driver													
H1	H bridge ON resistance OUTA (OUTA2_UP + OUTA1_DOWN)	5 30	3.1 V	20 22 24 25	Measure the voltage Ron = {(Pin 20 – Pin 22) + (Pin 25 – Pin 24)} / 100 mA	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
		9 14 20	4.8 V										
		39	3.1 V										
		29	27 MHz, 0 V / 3.1 V										
		36	*34										
		22	–100 mA										
		25	100 mA										
H1	H bridge ON resistance OUTC (OUTC2_UP + OUTC1_DOWN)	5 30	3.1 V	14 16 17 18	Measure the voltage Ron = {(Pin 14 – Pin 16) + (Pin 18 – Pin 17)} / 100 mA	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
		9 14 20	4.8 V										
		39	3.1 V										
		29	27 MHz, 0 V / 3.1 V										
		16	–100 mA										
		18	100 mA										

*34 : Impulse input to VD_FZ

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings							
		Pin No.	Conditions	Pin No.	Conditions	SW51	SW52	SW53	SW54	SW55	SW56	SW57	SW58
Motor driver													
H3	H bridge ON resistance OUTE (OUTE1_UP + OUTE2_DOWN)	5 30	3.1 V	8 9 10 11	Measure the voltage Ron = {(Pin 9 – Pin 11) + (Pin 8 – Pin 10)} / 50 mA	ON	OFF	OFF	ON	OFF	ON	ON	OFF
		9 14 20	4.8 V										
		39	3.1 V										
		29	27 MHz, 0 V / 3.1 V										
		34	*41										
		1	2 V										
		43	1 V										
		8	50 mA										
		11	–50 mA										
H3	H bridge ON resistance OUTE (OUTE2_UP + OUTE1_DOWN)	5 30	3.1 V	8 9 10 11	Measure the voltage Ron = {(Pin 9 – Pin 8) + (Pin 11 – Pin 10)} / 50 mA	OFF	ON	ON	OFF	ON	OFF	OFF	ON
		9 14 20	4.8 V										
		39	3.1 V										
		29	27 MHz, 0 V / 3.1 V										
		1	1 V										
		43	2 V										
		8	–50 mA										
		11	50 mA										

*41 : Serial setting PDWNB = 1,
IRS_TGT[9:0] = 200h, DGAIN[6:0] = 40h,
PWM_IRIS[2:0] = 7h, HGAIN[3:0] = Fh

Note) Serial settings are reflected on the rising edge of VD_IS or VD_FZ.

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings											
		Pin No.	Conditions	Pin No.	Conditions	SW 51	SW 52	SW 53	SW 54	SW 55	SW 56	SW 57	SW 58	SW 59	SW 5A	SW 5B	SW 5C
Motor driver (continued)																	
H2	H bridge leak current upper	5	3.7 V	8	Measure the current	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
				11												ON	OFF
		9	5.6 V	13											ON	OFF	
				15										ON	OFF		
		14 20	5.6 V	16									ON	OFF			
				18								ON	OFF				
		30	3.7 V	19							ON	OFF					
				21						ON	OFF						
		39	0 V	22					ON	OFF							
				25				ON	OFF								
H2	H bridge leak current lower	5	3.7 V	8	Measure the current	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
				11												ON	OFF
		9	5.6 V	13											ON	OFF	
				15										ON	OFF		
		14 20	5.6 V	16									ON	OFF			
				18								ON	OFF				
		30	3.7 V	19							ON	OFF					
				21						ON	OFF						
		39	0 V	22					ON	OFF							
				25				ON	OFF								

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings	
		Pin No.	Conditions	Pin No.	Conditions	SW5D	SW5E
LED driver							
L2	LED output leak current	26 27	5.6 V	26	Measure the current	ON	OFF
				27		OFF	ON
L1	Output ON resistance	26 27	20 mA	26 27	After measuring the voltage of each pin, calculate the below ; LED1 : (Pin 26 – Pin 24) / 20 mA LED2 : (Pin 27 – Pin 24) / 20 mA	—	—
		34	LEDA = 1 LEDB = 1				

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings									
		Pin No.	Conditions	Pin No.	Conditions	SW 81	SW 82	SW 83	SW 84	SW 85	SW 86	SW 87	SW 88	SW 89	SW 8A
OPAMP3 (Hall Sensor Amp. for output amplifier)															
O1	Input voltage range Low	5 30 39	3.1 V	3	Measure the voltage ; Vo1 : Output voltage when inputting 0.54 V to Pin 1 and Pin 43 Vo2 : Output voltage when inputting 0.555 V to Pin 1, 0.54 V to Pin 43 Calculation (Vo1 – 0.54) × 0.015 / (Vo2 – Vo1) Confirm that the calculational result is within input offset rating.	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	ON
		9 14 20	4.8 V												
		7	3.1 V												
		34	*51												
		1 43	0.54 V												
		1	0.555 V			ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON
O1	Input voltage range High	5 30 39	3.1 V	3	Measure the voltage ; Vo1 : Output voltage when inputting 2.56 V to Pin 1 and Pin 43 Vo2 : Output voltage when inputting 2.575 V to Pin 1, 2.56 V to Pin 43 Calculation (Vo1 – 2.56) × 0.015 / (Vo2 – Vo1) Confirm that the calculational result is within input offset rating.	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON
		9 14 20	4.8 V												
		7	3.1 V												
		34	*51												
		1 43	2.56 V												
		1	2.575 V			OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON
O2	Input offset voltage	5 30 39	3.1 V	3	Measure the voltage Vo1 : Output voltage when inputting 1.55 V to Pin 1 and Pin 43 Vo2 : Output voltage when inputting 1.58 V to Pin 1, 1.55 V to Pin 43 Calculation (Vo1 – 1.55) × 0.03 / (Vo2 – Vo1)	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	ON
		9 14 20	4.8 V												
		7	3.1 V												
		34	*51												
		1 43	1.55 V												
		1	1.58 V			OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	ON

*51 : Serial setting PDWNB = 1, HALL_GAIN[3:0] = 0

Note） Serial settings are reflected on the rising edge of VD_IS or VD_FZ.

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings							
		Pin No.	Conditions	Pin No.	Conditions	SW91	SW92	SW93	SW94	SW95	SW96	SW97	SW98
OPAMP3 (Hall Sensor Amp. for output amplifier) (continued)													
O3	Output voltage Low	5 30 39	3.1 V	3	Measure the voltage	OFF	ON	OFF	OFF	OFF	ON	ON	OFF
		9 14 20	4.8 V										
		1	1.55 V										
		43	2.65 V										
		34	*52										
		3	100 μA										
O3	Output voltage Low	5 30 39	3.1 V	3	Measure the voltage	ON	OFF	OFF	OFF	ON	OFF	ON	OFF
		9 14 20	4.8 V										
		1	0.45 V										
		43	1.55 V										
		34	*52										
		3	100 μA										
O4	Output voltage High	5 30 39	3.1 V	3	Measure the voltage	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
		9 14 20	4.8 V										
		1	2.65 V										
		43	1.55 V										
		34	*52										
		3	–100 μA										
O4	Output voltage High	5 30 39	3.1 V	3	Measure the voltage	OFF	ON	OFF	ON	OFF	OFF	OFF	ON
		9 14 20	4.8 V										
		1	1.55 V										
		43	0.45 V										
		34	*52										
		3	–100 μA										

*52 : Serial setting PDWNB = 1, HALL_GAIN[3:0] = 0, HALL_OFFSET_DAC[7:0] = 0Fh

Note) Serial settings are reflected on the rising edge of VD_IS or VD_FZ.

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings									
		Pin No.	Conditions	Pin No.	Conditions	SW 81	SW 82	SW 83	SW 84	SW 85	SW 86	SW 87	SW 88	SW 89	SW 8A
OPAMP3 (Hall Sensor Amp. for output amplifier) (continued)															
O5	Gain	5 30 39	3.1 V	3	Measure the voltage Vo1 : Output voltage when inputting 1.54 V to Pin 1 and Pin 43 Vo2 : Output voltage when inputting 1.56 V to Pin 1, 1.54 V to Pin 43 Calculation (Vo2 – Vo1)/0.02	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF
		9 14 20	4.8 V												
		34	*53												
		1 43	1.54 V												
		1	1.56 V			OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

*53 : Serial setting PDWNB = 1, HALL_GAIN[3:0] = 0h, HALL_OFFSET_DAC[7:0] = 0Fh

Note）Serial settings are reflected on the rising edge of VD_IS or VD_FZ.

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings							
		Pin No.	Conditions	Pin No.	Conditions	SW 101	SW 102	SW 103	SW 104	SW 105	SW 106	SW 107	SW 108
OPAMP4 (Hall Sensor Amp. for eliminating common-mode voltage)													
O6 O8	Input voltage range Output voltage Low OP4INN = High	5 30 39	3.1 V	44	Measure the voltage	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF
		9 14 20	4.8 V										
		43	1.7 V										
		44	10 μA										
		34	*61										
O6 O9	Input voltage range Output voltage High OP4INN = Low	5 30 39	3.1 V	44	Measure the voltage	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF
		9 14 20	4.8 V										
		43	1.40 V										
		44	–3 mA										
		34	*61										
O7	Input offset voltage	5 30 39	3.1 V	42 44	Measure the voltage OP4OUT, VREF Calculation OP4OUT – VREF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
		9 14 20	4.8 V										
		34	*61										

*61 : Serial setting PDWNB = 1

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings							
		Pin No.	Conditions	Pin No.	Conditions	SW 101	SW 102	SW 103	SW 104	SW 105	SW 106	SW 107	SW 108
Reference voltage output block													
O10	Output voltage 1	5 30 39	3.1 V	42	Measure the voltage	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
		9 14 20	4.8 V										
		34	*61										
O11	Output voltage 2 (–100 μA)	5 30 39	3.1 V	42	Measure the voltage	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
		9 14 20	4.8 V										
		34	*61										
		42	–100 μA										
O11	Output voltage 2 (100 μA)	5 30 39	3.1 V	42	Measure the voltage	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
		9 14 20	4.8 V										
		34	*61										
		42	100 μA										

*61 : Serial setting PDWNB = 1

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings							
		Pin No.	Conditions	Pin No.	Conditions	SW 101	SW 102	SW 103	SW 104	SW 105	SW 106	SW 107	SW 108
Hall bias controller (SENS pin output)													
O12	Min. output current	5 30 39	3.1 V	2	Measure the current	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
		9 14 20	4.8 V										
		34	*71										
		2	0.7 V										
O13	Output current accuracy 1	5 30 39	3.1 V	2	Measure the current	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
		9 14 20	4.8 V										
		34	*72										
		2	0.7 V										
O14	Output current accuracy 2	5 30 39	3.1 V	2	Measure the current	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
		9 14 20	4.8 V										
		34	*73										
		2	0.7 V										

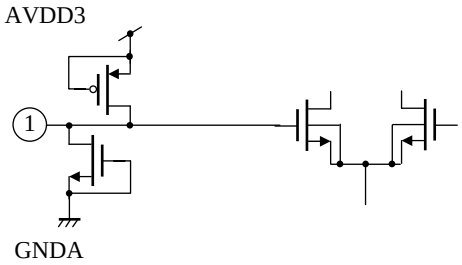
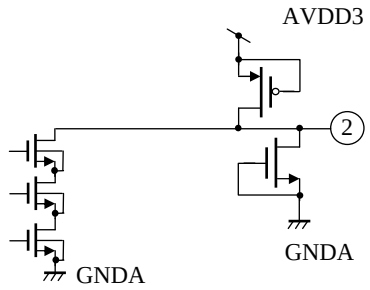
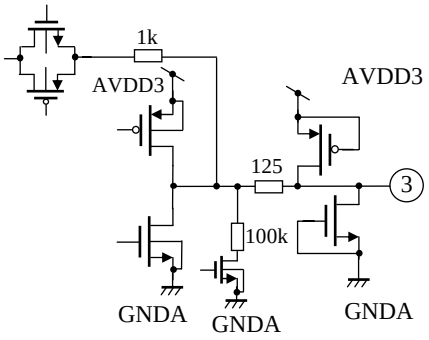
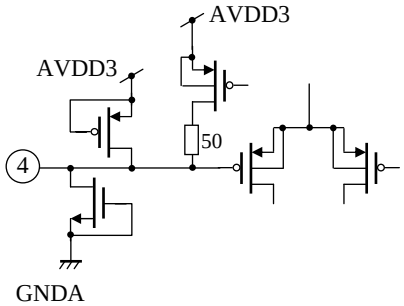
*71 : Serial setting PDWNB = 1, HALL_BIAS_DAC[7:0] = 00h
*72 : Serial setting PDWNB = 1, HALL_BIAS_DAC[7:0] = 40h
*73 : Serial setting PDWNB = 1, HALL_BIAS_DAC[7:0] = BEh

Note) Serial settings are reflected on the rising edge of VD_IS or VD_FZ.

■ Technical Data

- I/O block circuit diagrams and pin function descriptions

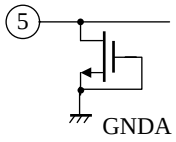
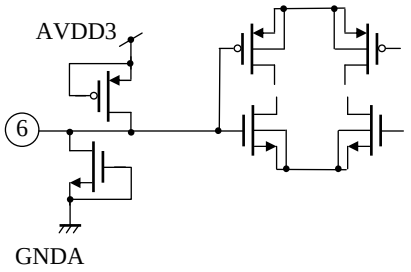
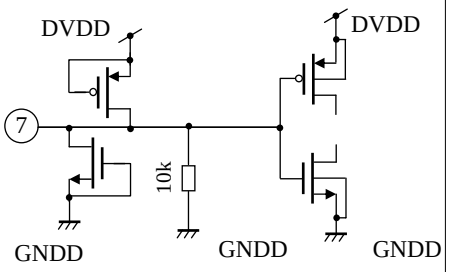
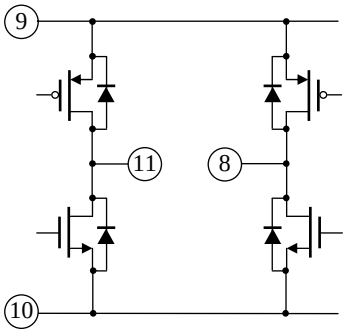
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
1	—		—	OP3INP Hall signal amplifier non-inverting input pin
2	—		—	SENS Hall current bias output pin
3	Hall signal amplifier output		—	OP3OUT Hall amp. output pin
4	—		—	REF Resistor pin for Hall bias

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

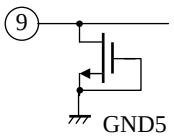
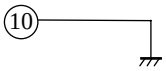
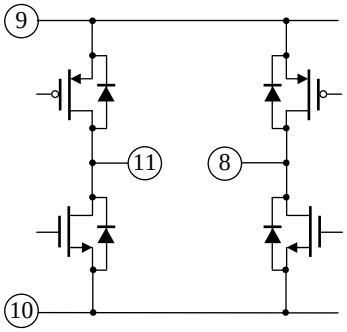
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
5	AVDD3		—	AVDD3 3 V analog power supply pin
6	—		—	ADTESTIN ADC test input pin
7	GNDD to DVDD Logic signal input		10 kΩ	TEST Test mode input pin TEST
8	—		—	OUTE2 Iris output pin 0

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

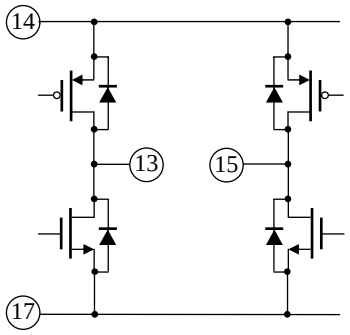
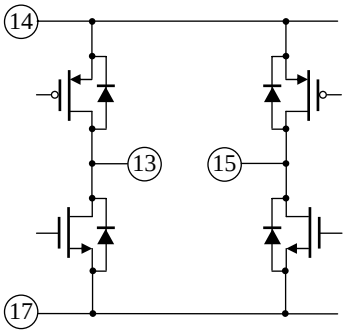
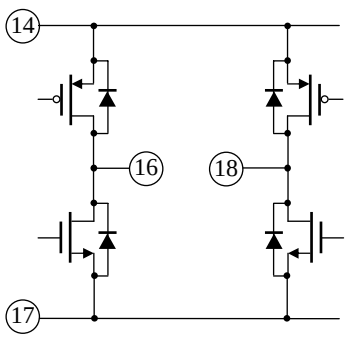
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
9	VDD5		—	VDD5 5 V power supply pin
10	GND5		—	GND5 5V GND pin
11	—		—	OUTE1 Iris output pin 1
12	—	—	—	N.C.

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

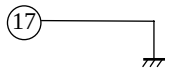
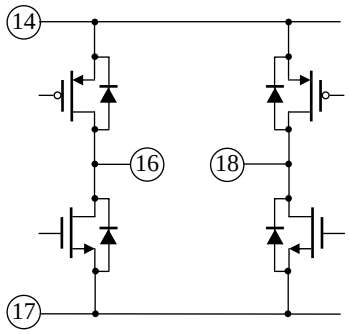
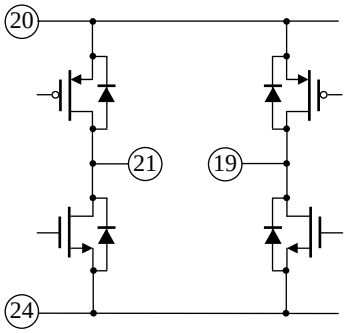
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
13	—		—	OUTD2 Motor output pin D2
14	MVCCB	—	—	MVCCB Power supply pin for motor B
15	—		—	OUTD1 Motor output pin D1
16	—		—	OUTC2 Motor output pin C2

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

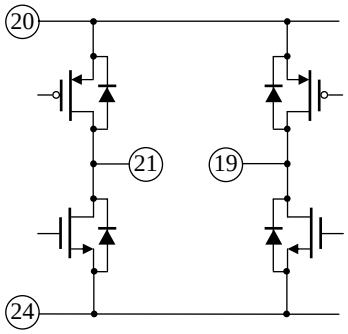
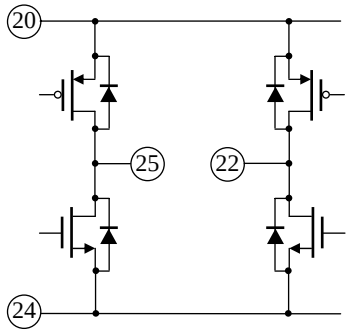
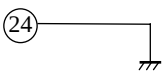
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
17	MGNDB		—	MGNDB GND pin for motor B
18	—		—	OUTC1 Motor output pin C1
19	—		—	OUTB2 Motor output pin B2
20	—	—	—	MVCCA Power supply pin for motor A

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

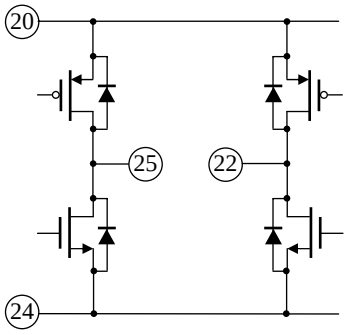
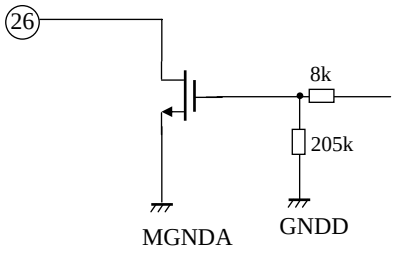
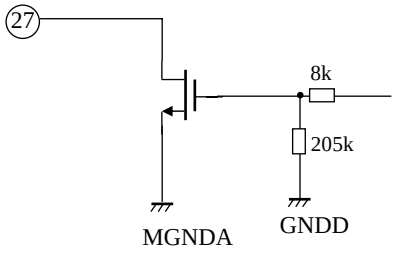
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
21	—		—	OUTB1 Motor output pin B1
22	—		—	OUTA2 Motor output pin A2
23	—	—	—	N.C.
24	MGNDA		—	MGNDA GND pin for motor A

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

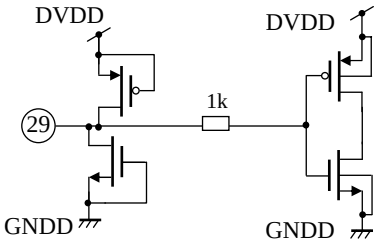
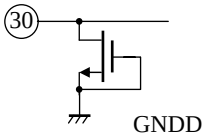
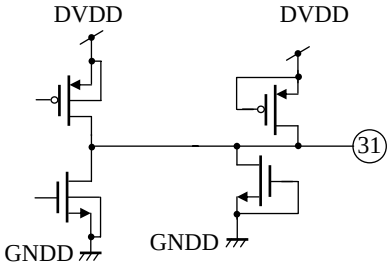
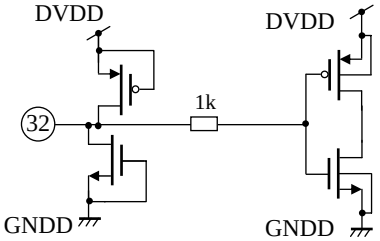
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
25	—		—	OUTA1 Motor output pin A1
26	Hi-Z or open-drain output		Serial selection Hi-Z Max. 8 Ω	LED1 Open-drain 1 for driving LED
27	Hi-Z or open-drain output		Serial selection Hi-Z Max. 8 Ω	LED2 Open-drain 2 for driving LED
28	GNDD		—	GNDD Digital GND pin

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

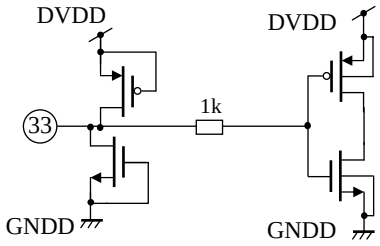
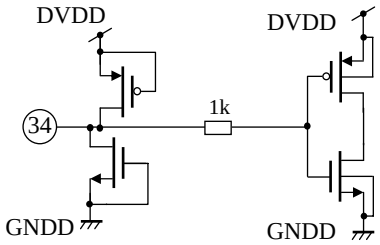
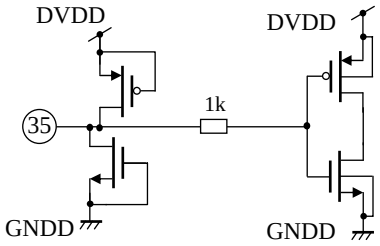
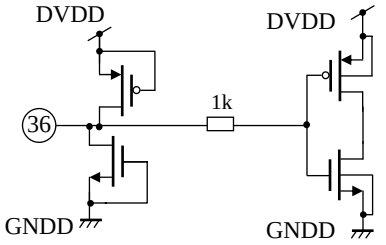
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
29	GNDD to DVDD logic signal input		Hi-Z	OSCIN OSCIN input pin (Schmidt)
30	DVDD		—	DVDD 3 V digital power supply pin
31	GNDD to DVDD logic signal output / Hi-Z		—	SOUT Serial data output pin
32	GNDD to DVDD logic signal input		Hi-Z	CS Chip select signal input pin (Schmidt)

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

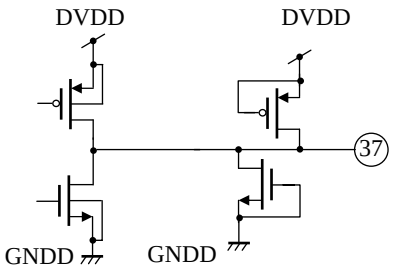
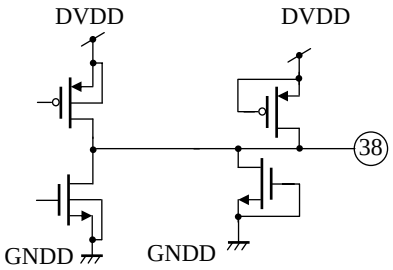
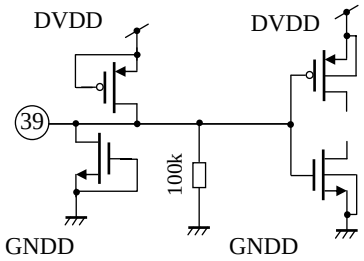
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
33	GNDD to DVDD logic signal input		Hi-Z	SCK Serial clock input pin (Schmidt)
34	GNDD to DVDD logic signal input		Hi-Z	SIN Serial data input pin (Schmidt)
35	GNDD to DVDD logic signal input		Hi-Z	VD_IS VD_IS input pin (Schmidt)
36	GNDD to DVDD logic signal input		Hi-Z	VD_FZ VD_FZ input pin (Schmidt)

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

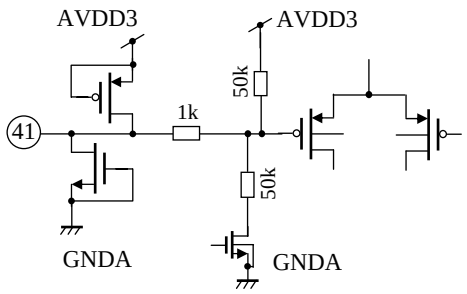
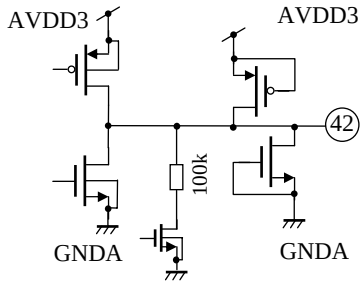
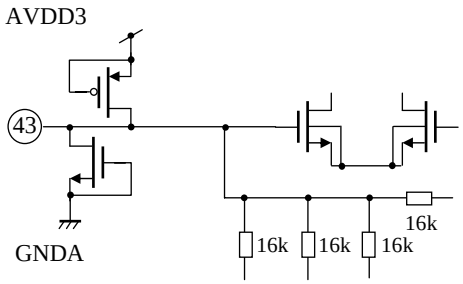
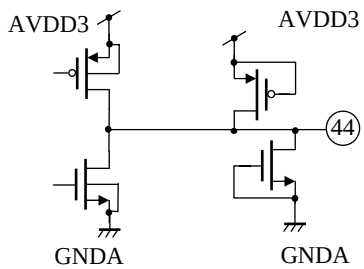
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
37	GNDD to DVDD logic signal output		—	PLS1 Pulse 1 output pin
38	GNDD to DVDD logic signal output		—	PLS2 Pulse 2 output pin
39	Logic signal input		100 kΩ	RSTB Reset signal input pin
40	GNDA		—	GNDA 3 V analog GND

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
41	—		25 kΩ	CREFIN (AVDD3)/2 capacitor connection pin
42	—		—	VREF Reference voltage for Hall sensor
43	—		—	OP4INN Midpoint bias amplifier non-inverting input pin
44	—		—	OP4OUT Midpoint bias amplifier output pin

■ Usage Notes

• Special attention and precaution in using

1. This IC is intended to be used for general electronic equipment [camcorder].
   Consult our sales staff in advance for information on the following applications:
   - Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   - Any applications other than the standard applications intended.
     (1) Space appliance (such as artificial satellite, and rocket)
     (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
     (3) Medical equipment for life support
     (4) Submarine transponder
     (5) Control equipment for power plant
     (6) Disaster prevention and security device
     (7) Weapon
     (8) Others : Applications of which reliability equivalent to (1) to (7) is required

2. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.

3. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.

4. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.

5. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-V_{CC} short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) .
   And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.

6. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
   Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

7. When using the LSI for new models, verify the safety including the long-term reliability for each product.

8. When the application system is designed by using this LSI, be sure to confirm notes in this book.
   Be sure to read the notes to descriptions and the usage notes in the book.

9. Take time to check the characteristics on use. When changing an external circuit constant for use, consider not only static characteristics, but also transient characteristics and external parts with respect to the characteristics difference among ICs so that you can get enough margin. Moreover, consider the influence of electric charge remaining in an external capacitor on rising/falling of power supply.

■ Usage Notes (continued)

- Notes of Power LSI

1. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
   Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to V_{CC} short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.

2. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.

3. The product which has specified ASO (Area of Safe Operation) should be operated in ASO.

4. Verify the risks which might be caused by the malfunctions of external components.

5. Apply voltage from a low-impedance to power supply pins and connect a bypass capacitor to the LSI as near as possible.

Package Standards

Package Code	∗QFN044-P-0606D

Semiconductor Company
Panasonic Corporation

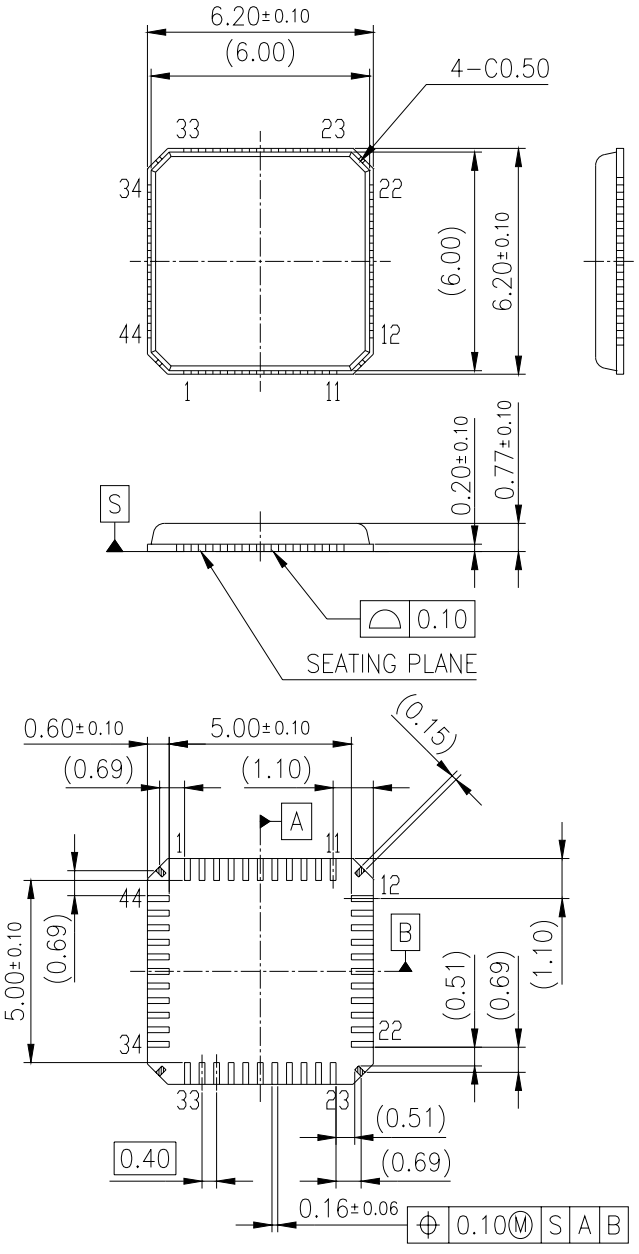
Established by	Applied by	Checked by	Prepared by
H.Shidooka	H.Yoshida	M.Okajima	M.Itoh

Established: 2009-06-01
Revised : 2009-06-17

1. Outline Drawing

Unit:mm

Package Code : ∗QFN044-P-0606D



Body Material	:	Br / Sb Free Epoxy Resin
Lead Material	:	Cu Alloy
Lead Finish Method	:	Pd Plating

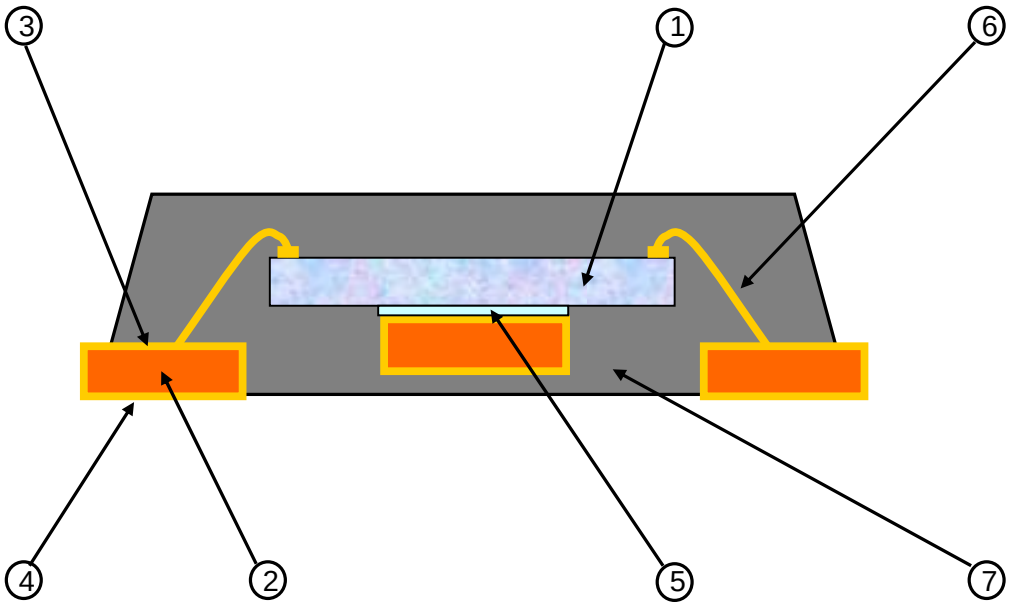
Established	Revised
-	-

Established: 2009-06-01
Revised : 2009-06-17

2. Package Structure (Technical Report : Reference Value)

Package Code : ∗QFN044-P-0606D

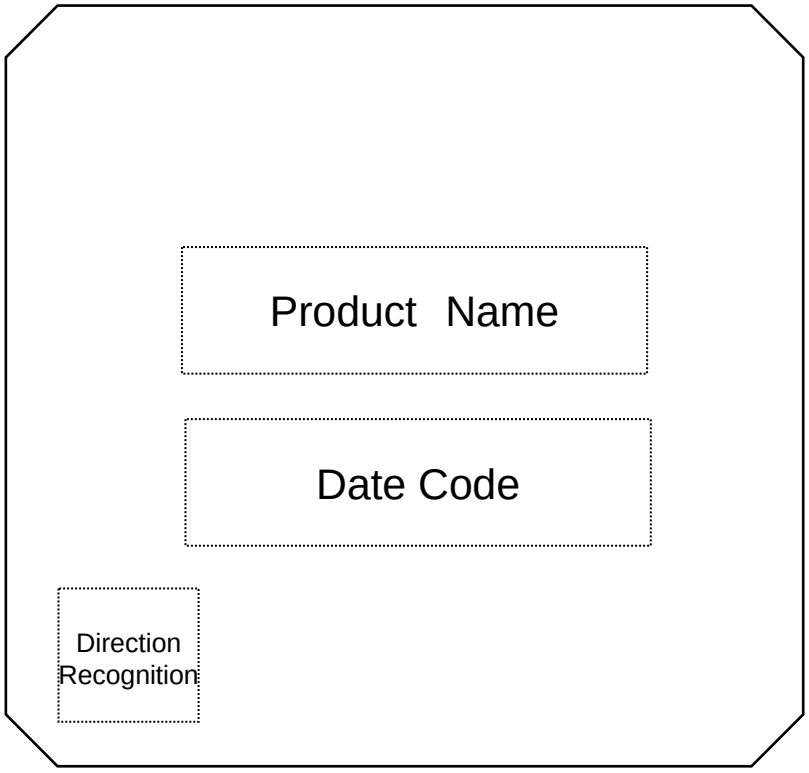
Chip Material		Si	①
Leadframe material		Cu alloy	②
Inner lead surface		Pd plating	③
Outer lead surface		Pd plating	④
Die attach	Method	Resin adhesive method	⑤
	Material	Adhesive material	
Wirebond	Method	Thermo-compression bonding	⑥
	Material	Au	
Molding	Method	Transfer molding	⑦
	Material	Br/Sb Free Epoxy resin	
Mass		67 mg	



Established: 2009-06-01
Revised : 2009-06-17

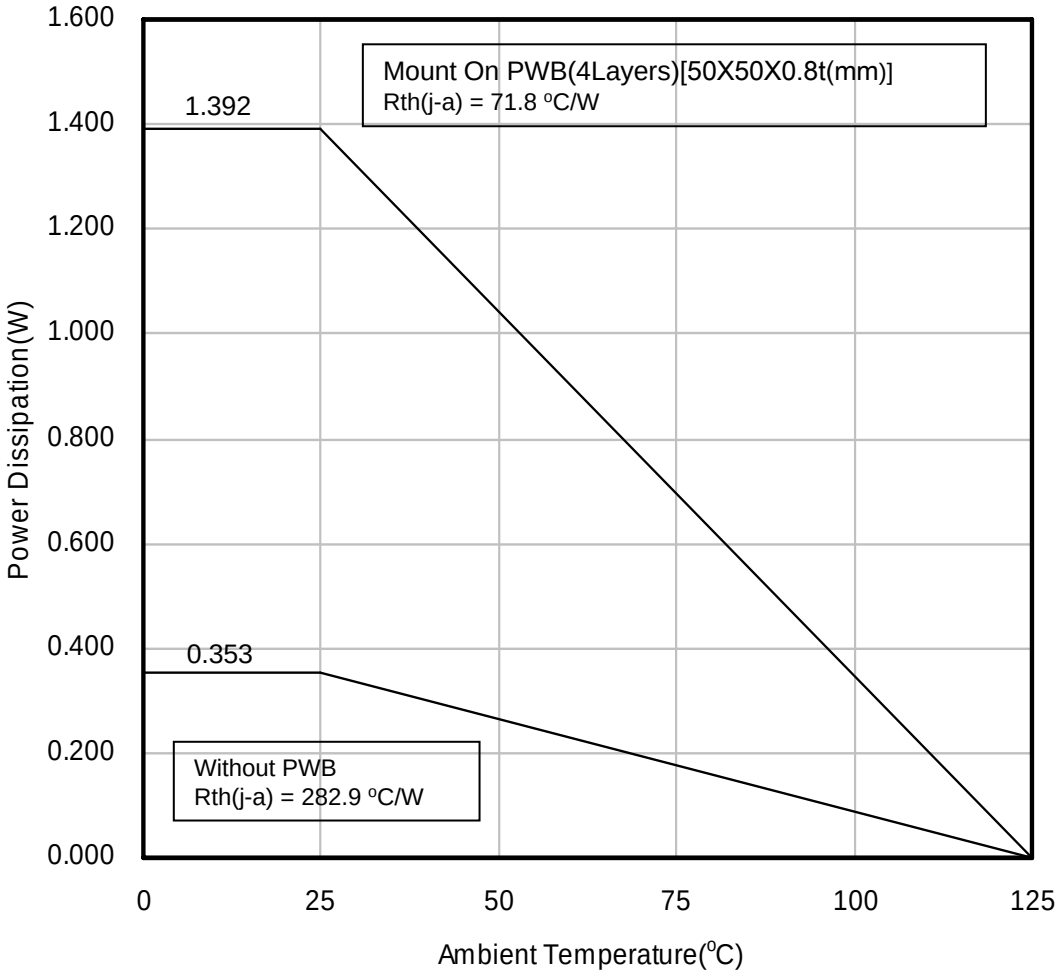
3. Mark Layout

Package Code : ∗QFN044-P-0606D



4. Power Dissipation (Technical Report)

Package Code : ∗QFN044-P-0606D



Established: 2009-06-01
Revised : 2009-06-17

5. Power Dissipation (Supplementary Explanation)

[Experiment environment]

Power Dissipation（Technical Report）is a result in the experiment environment of SEMI standard conformity. （Ambient air temperature (Ta) is 25 degrees C）

[Supplementary information of PWB to be used for measurement]

The supplement of PWB information for Power Dissipation data (Technical Report）are shown below.

Indication	Total Layer	Resin Material
Glass-Epoxy	1-layer	FR-4
4-layer	4-layer	FR-4

[Notes about Power Dissipation（Thermal Resistance）]

Power Dissipation values（Thermal Resistance）depend on the conditions of the surroundings, such as specification of PWB and a mounting condition , and a ambient temperature. (Power Dissipation (Thermal Resistance) is not a fixed value.)

The Power Dissipation value（Technical Report）is the experiment result in specific conditions (evaluation environment of SEMI standard conformity) ,and keep in mind that Power Dissipation values (Thermal resistance) depend on circumference conditions and also change.

[Definition of each temperature and thermal resistance]

Ta ：Ambient air temperature

※The temperature of the air is defined at the position where the convection, radiation, etc. don't affect the temperature value, and it's separated from the heating elements.

Tc ：It's the temperature near the center of a package surface. The package surface is defined at the opposite side if the PWB.

Tj ：Semiconductor element surface temperature (Junction temperature.)

Rth(j-c)：The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the package surface

Rth(c-a)：The thermal resistance (difference of temperature of per 1 Watts) between the package surface and the ambient air

Rth(j-a)：The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the ambient air

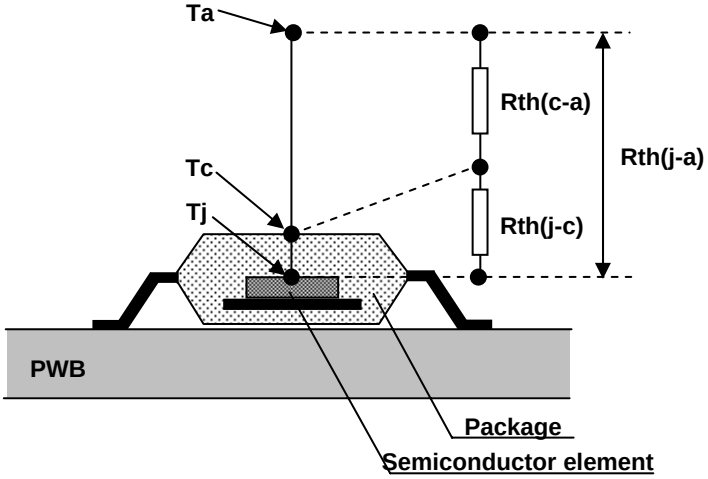


Fig1. Definition image

[Definition formula]

$$Tj=\{Rth(j\text{-}c)+Rth(c\text{-}a)\}\times P+Ta$$

$$=Rth(j\text{-}a)\times P+Ta$$

$$Rth(j\text{-}c)=\frac{Tj-Tc}{P}\ (℃/W)$$

$$Rth(c\text{-}a)=\frac{Tc-Ta}{P}\ (℃/W)$$

$$Rth(j\text{-}a)=\frac{Tj-Ta}{P}\ (℃/W)$$

$$=Rth(j\text{-}c)+Rth(c\text{-}a)$$

P:power(W)

Established: 2009-06-01
Revised : 2009-06-17

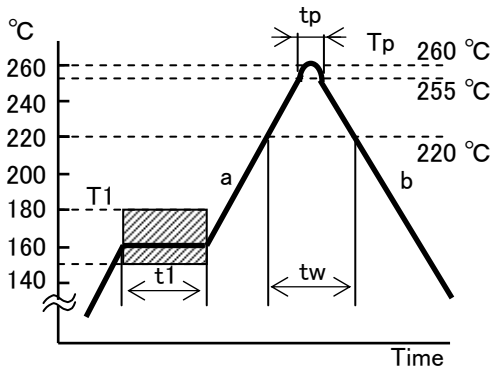
Product name : AN41908A-VB
Package : *QFN044-P-0606D

1. Recommended Soldering Conditions

In case that the semiconductor packages are mounted on the PCB, the soldering should be performed under the following conditions.

① Reflow soldering

Reflow peak temp. :	max. 260 ℃

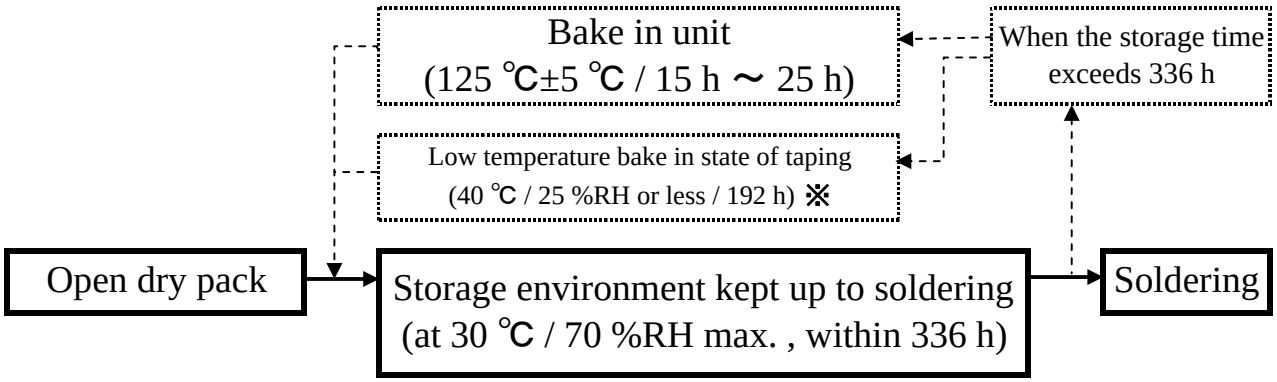


No.	mark	contents	value
1	T1	Pre-heating temp.	150 ℃～180 ℃
2	t1	Pre-heating temp. hold time	60 s～120 s
3	a	Rising rate	2 ℃/s～5 ℃/s
4	Tp	Peak temp.	255 ℃+5 ℃、-0 ℃
5	tp	Peak temp. hold time	10 s±3 s
6	tw	High temp. region hold time	within 60 s (≧220 ℃)
7	b	Down rate	2 ℃/s～5 ℃/s
8	-	Number of reflow	within 2 times

＊Peak temperature : less than 260 ℃

＊Temperature is measured at package surface point

2. Storage environment after dry pack opening



※ Because the taping and the magazine materials are not the heat-resistant materials, the bake at 125℃ cannot be done.
Therefore, please solder everything or control everything in the rule time.
Please keep them in an equal environment with the moisture-proof packaging or dry box.
(Temperature: room temperature, relative humidity: 30% or less.)
To control storage time, when bake in the taping and the magazine is necessary, it is necessary for each type to set a bake condition. Please inquire of our company.

☆ **AN41908A-VB limitation, low temperature bake condition : 40 ℃ / 25 %RH or less / 192 h**

3. Note

① Storage environment conditions: keep the following conditions Ta=5 ℃～30 ℃、RH=30 %～70 %.
② Storage period before opening dry pack shall be 1year from a shipping day under Ta=5 ℃～30 ℃、RH=30 %～70 %.
③ Baking cycle should be only one time. Please be cautious of solderability at baking.
④ Reflow soldering : max. two times. (1st reflow must be finished within 336 hours.)
⑤ Remove flux sufficiently from product in the washing process.
(Flux : Chlorineless rosin flux is recommended.)
⑥ In case that use ultrasonic for product washing,
There is the possibility that the resonance may occur due to the frequency and shape of PCB.
It may be affected to the strength of lead. Please be cautious of this matter.

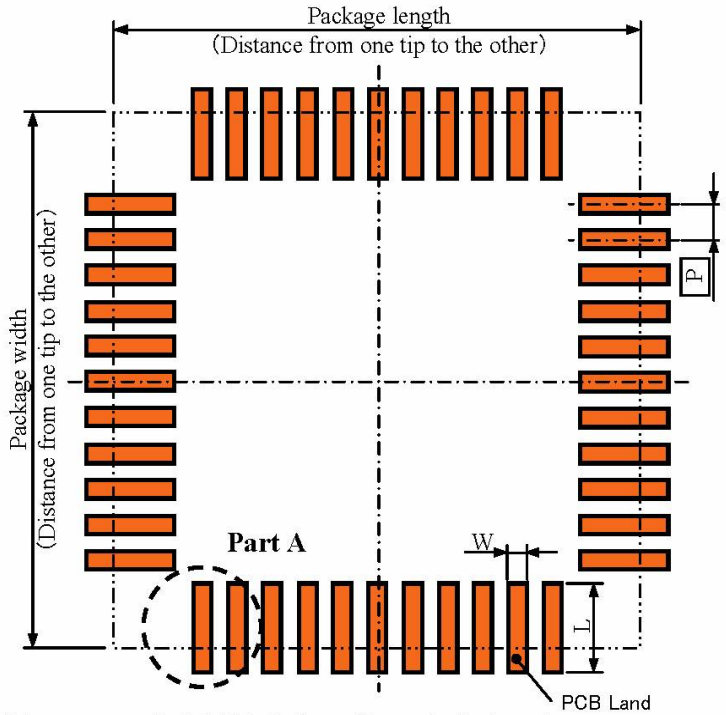
Referential PCB & Mask spec. for QFN

Application Specific Standard Products BU
Semiconductor Company
Panasonic Corporation

Reference

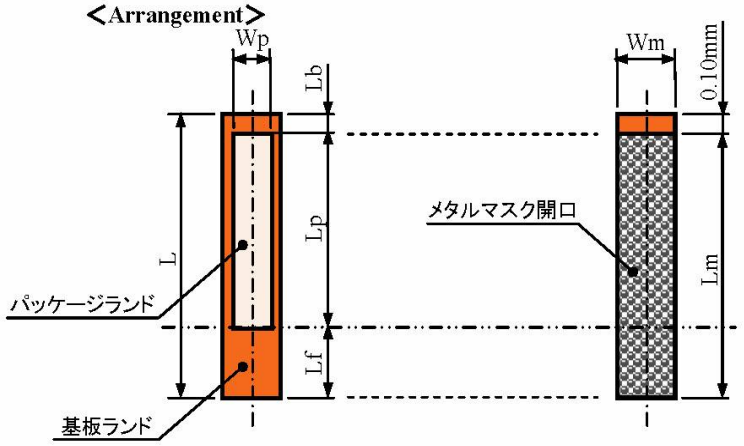
【Whole PCB land figure】

(Reference figure)Package Code：QFN044-P-0606（0.40mmP/44pin、6.2mm□）



【Expansion of part A】

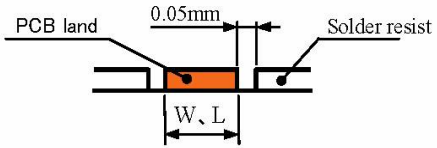
<Arrangement>



PCB land and package land

PCB land and mask opening

【Cross-sectional figure of PCB land】



Solder resist：Normal resist structure（NSMD）
（PCB land size＋0.10mm（One side＋0.05mm））

*Stencil mask thickness
：0.11～0.13mmt

■Recommended PCB & Stencil mask design size

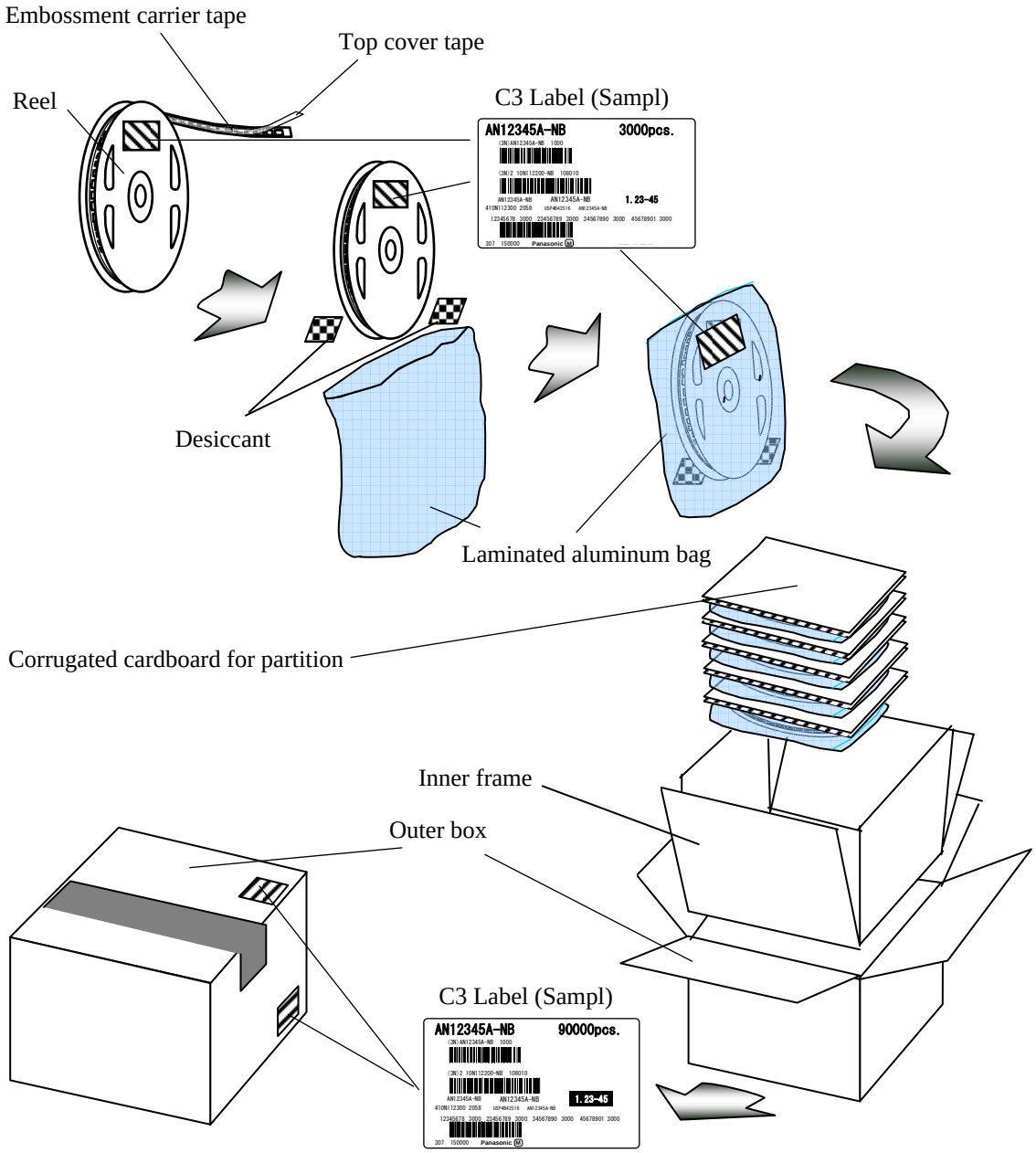
（Unit：mm）

Terminal pitch P	Package land		PCB Land				Metal Mask Opening	
	Width Wp	Length Lp	Width W	Length L	Front fillet Lf	Back fillet Lb	Width Wm	Length Lm
0.40mmP	0.16	0.60	0.20	1.00	0.30	0.10	0.20	0.90
0.50mmP	0.20	0.60	0.25	1.00	0.30	0.10	0.25	0.90

*The above size is calculated based on the experiment results by Panasonic Corporation and is not intended as a guarantee of mounting reliability. Mounting reliability can vary depending on factors such as the equipment specifications and conditions, material specifications and properties, and environmental conditions. To ensure satisfactory results, your company should evaluate and confirm actual mounting performance.

Specifications of packing by the embossment tape

(Specifications for dampproof packing of the reel without the inner carton)



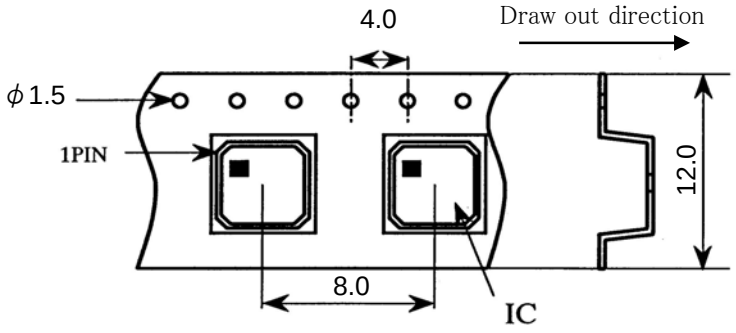
Package : *QFN044-P-0606D

Unit : mm

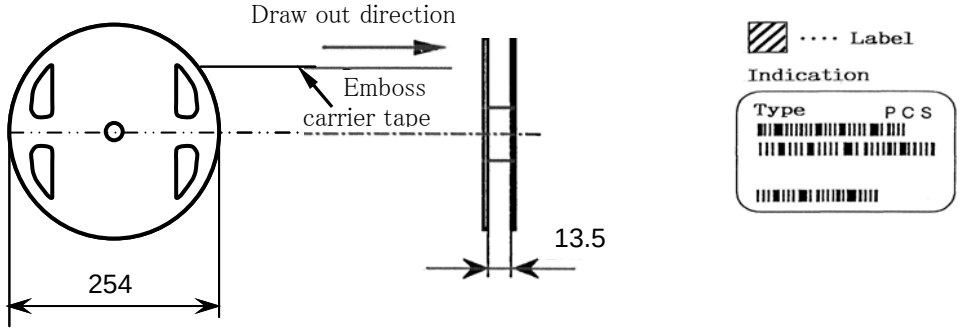
1 Packing

1) Tape

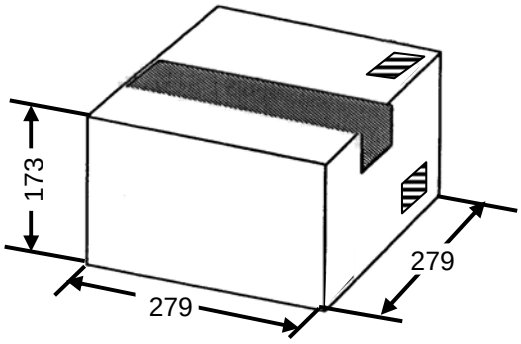
V B



2) Reel



3) Packing case

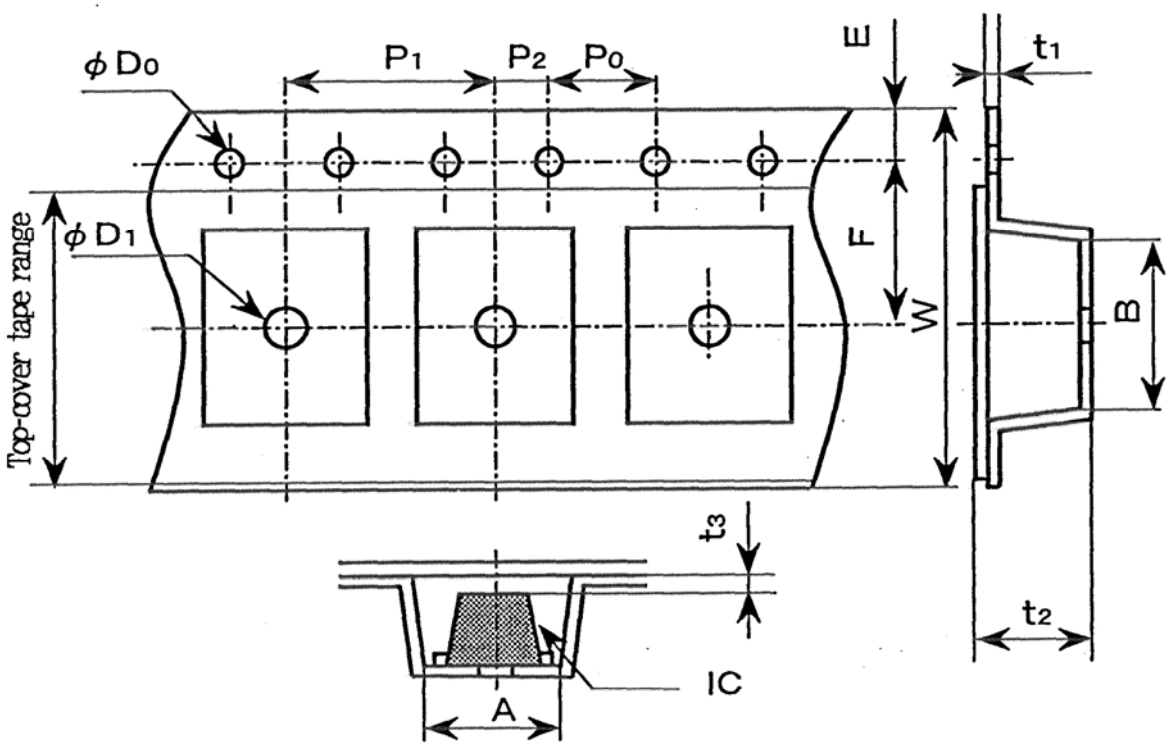


2 Packing quantity

Form	IC quantity	Contents
Reel	2000 Pcs	Reel × 1Pcs
Packing case	10000 Pcs	Reel × 5Pcs

Package : *QFN044-P-0606D

Unit : mm



Unit:mm

Dimension & Tolerance					
W	A	B	E	F	P_1
12.0±0.2	6.5±0.1	6.5±0.1	1.75±0.1	5.5±0.05	8.0±0.1
P_2	P_o	ϕD_1	ϕD_o	t_1	t_2
2.0±0.05	4.0±0.1	$1.5^{+0.3}_{-0}$	1.55±0.05	0.3±0.05	1.8max
t_3					
(0.4)					

Panasonic

Industrial Devices Company, Panasonic Corporation

1 Kotari-yakemachi, Nagaokakyo City, Kyoto 617-8520, Japan
Tel:075-951-8151

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